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EVALUATION KIT AVAILABLE

2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

General Description

The MAX2839AS direct conversion, zero-IF, RF transceiver is designed specifically for 2.3GHz to 2.7GHz 802.16e MIMO mobile WiMAX™ systems. The device incorporates one transmitter and two receivers, with > 40dB isolation between each receiver. The MAX2839AS completely integrates all circuitry required to implement the RF transceiver function, providing RF to baseband receive path, and baseband to RF transmit path, VCO, frequency synthesizer, crystal oscillator, and baseband/control interface. The device includes a fast-settling sigma-delta RF synthesizer with smaller than 40Hz frequency steps and a crystal oscillator that allows the use of a low-cost crystal in place of a TCXO. The transceiver IC also integrates circuits for on-chip DC-offset cancellation, I/Q error, and carrier leakage detection circuits. An internal transmit to receive loopback mode allows for receiver I/Q imbalance calibration. The local oscillator I/Q quadrature phase error can be digitally corrected in approximately 0.125° steps. Only an RF bandpass filter (BPF), crystal, RF switch, PA, and a small number of passive components are needed to form a complete wireless broadband RF radio solution.

The MAX2839AS completely eliminates the need for an external SAW filter by implementing on-chip programmable monolithic filters for both the receiver and transmitter, for all 2GHz and 802.16e profiles and WiBro. The baseband filters along with the Rx and Tx signal paths are optimized to meet the stringent noise figure and linearity specifications. The device supports up to 2048 FFT OFDM and implements programmable channel filters for 3.5MHz to 20MHz RF channel bandwidths. The transceiver requires only 2µs Tx-Rx switching time. The IC is available in a small wafer-level package (WLP) measuring 5.16mm x 3.66mm x 0.5mm.

Applications

802.16e Mobile WiMAX Systems

Korean WiBro Systems

Proprietary Wireless Broadband Systems

802.11g or n WLAN with MRC or MIMO Down Link

WiMAX is a trademark of the WiMAX Forum.

SPI is a trademark of Motorola, Inc.

Features

- **2.3GHz to 2.7GHz Wideband Operation**
- **Dual Receivers for MIMO, Single Transmitter**
- **Complete RF Transceiver, PA Driver, and Crystal Oscillator**
  - **3.5dB Rx Noise Figure on Each Receiver with Balun**
  - **-35dB Rx EVM for 64QAM Signal**
  - **0dBm Linear OFDM Transmit Power (64QAM)**
  - **-70dBr Tx Spectral Emission Mask**
  - **-35dBc LO Leakage**
  - **Automatic Rx DC Offset Correction**
  - **Monolithic Low-Noise VCO with -39dBc Integrated Phase Noise**
  - **Programmable Rx I/Q Lowpass Channel Filters**
  - **Programmable Tx I/Q Lowpass Anti-Aliasing Filters**
  - **Sigma-Delta Fractional-N PLL with 28.61Hz Minimum Step Size**
  - **62dB Tx Gain Control Range with 1dB Step Size, Digitally Controlled**
  - **95dB Rx Gain Control Range with 1dB Step Size, Digitally Controlled**
  - **60dB Analog RSSI Instantaneous Dynamic Range**
  - **4-Wire SPI™ Digital Interface**
  - **I/Q Analog Baseband Interface**
  - **Digital Tx/Rx Mode Control**
  - **Digitally Tuned Crystal Oscillator**
  - **On-Chip Digital Temperature Sensor Readout**
- **+2.7V to +3.6V Transceiver Supply**
- **Low-Power Shutdown Current**
- **Small WLP Package (5.16mm x 3.66mm x 0.5mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2839ASEWO+T	-40°C to +85°C	73 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Bump Configuration and Typical Operating Circuit appear at end of data sheet.

2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ Pins to GND....................-0.3V to +3.9V
RF Inputs: RXINA+, RXINA-, RXINB+,
RXINB- to GND ....AC-Coupled Only
RF Outputs: TXOUT+, TXOUT- to GND..............-0.3V to +3.9V
Analog Inputs: TXBBI+, TXBBI-, TXBBQ+,
TXBBQ- to GND....................-0.3V to +3.9V
Analog Input: REFCLK, XTAL1 ....-0.3V to +3.9V_{P-P}
Analog Outputs: RXBBIA+, RXBBIA-, RXBBQA+, RXBBQA-,
RXBBIB+, RXBBIB-, RXBBQB+, RXBBQB-, CPOUT+,
CPOUT-, PABIAS, RSSI to GND....................-0.3V to +3.9V
Digital Inputs: TXRX, $\overline{CS}$, SCLK, DIN, B7:B0,
CLKOUT_DIV, RXHP, ENABLE to GND ....-0.3V to +3.9V
Digital Outputs: DOUT, CLKOUT ....-0.3V to +3.9V
Bias Voltages: VCOBYP ....-0.3V to +3.9V
Short-Circuit Duration on All Output Pins 10s
RF Input Power: All RXIN_ ....+10dBm
RF Output Differential Load VSWR: All TXOUT 6:1
Continuous Power Dissipation (T_A = +70°C)
73-Bump WLP (derate 31.3mW/°C above +70°C).....2500mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Soldering Temperature (reflow) ....(Note 1) +260°C

Note 1: Refer to Application Note 1891: *Understanding the Basics of the Wafer-Level Chip-Scale Package (WL-CSP)* available at **www.maxim-ic.com**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. ENABLE and TXRX set according to operating mode. $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω. 90mV_{RMS} differential I and Q signals (1MHz) applied to I, Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$		2.7		3.6	V
Supply Current	Shutdown mode, T_A = +25°C; all logic inputs equal 0 or V_{CC}			2		µA
	Clock-out only mode			2.7	3.8	mA
	Standby mode			33	50	mA
	Rx mode	One receiver on		79	101	mA
		Both receivers on		120	148	mA
	Tx mode	16 QAM		116	148	mA
		64 QAM (Note 3)		145	183	mA
	Rx calibration mode, both receivers on			153	200	mA
	Tx calibration mode			102	145	mA
Rx I/Q Output Common-Mode Voltage	D[9:8] = 00 in A[4:0] = 00100		0.8	1.05	1.35	V
	D[9:8] = 01 in A[4:0] = 00100			1.15		V
	D[9:8] = 10 in A[4:0] = 00100			1.25		V
	D[9:8] = 11 in A[4:0] = 00100			1.45		V
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled		0.5		1.2	V
Tx Baseband Input Bias Current	Source current			10	20	µA
LOGIC INPUTS: TXRX, ENABLE, SCLK, DIN, $\overline{CS}$, B7:B0, CLKOUT_DIV, RXHP						
Digital Input-Voltage High, V_{IH}			V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}					0.4	V
Digital Input-Current High, I_{IH}			-1		+1	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. ENABLE and TXRX set according to operating mode. $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω. $90mV_{RMS}$ differential I and Q signals (1MHz) applied to I, Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input-Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: DOUT, CLKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC ELECTRICAL CHARACTERISTICS—Rx MODE

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit* and registers set to default settings. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF INPUT TO I, Q BASEBAND-LOADED OUTPUT						
RF Input Frequency Range			2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Input Frequency Range	Tested at band edges and band center			1.5		dB
RF Input Return Loss	All LNA settings			12		dB
Total Voltage Gain	T_A = -40°C to +85°C	Maximum gain, B7:B0 = 0000000	92	99		dB
		Minimum gain, B7:B0 = 1111111		4	10	
RF Gain Steps	From max RF gain (B7:B6 = 00) to max RF gain - 8dB (B7:B6 = 01)			8		dB
	From max RF gain to max RF gain - 16dB (B7:B6 = 10)			16		
	From max RF gain to max RF gain - 32dB (B7:B6 = 11)			32		
Gain Change Settling Time	Any RF or baseband gain change; gain settling to within ±1dB of steady state; RXHP = 1			200		ns
	Any RF or baseband gain change; gain settling to within ±0.1dB of steady state; RXHP = 1			2000		
Baseband Gain Range	From maximum baseband gain (B5:B0 = 000000) to minimum gain (B5:B0 = 111111), T_A = -40°C to +85°C		60.5	63	65.5	dB
Baseband Gain Step Size				1		dB
DSB Noise Figure (Including Balun Loss)	Voltage gain = 65dB with max RF gain (B7:B6 = 00)			3.5		dB
	Voltage gain = 50dB with max RF gain - 8dB (B7:B6 = 01)			8.5		
	Voltage gain = 45dB with max RF gain - 16dB (B7:B6 = 10)			14.5		
	Voltage gain = 15dB with max RF gain - 32dB (B7:B6 = 11)			32		

AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit* and registers set to default settings. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Out-of-Band Input IP3 (Note 4)	AGC set for -65dBm wanted signal, max RF gain (B7:B6 = 00)		-13		dBm
	AGC set for -55dBm wanted signal, max RF gain - 8dB (B7:B6 = 01)		-9		
	AGC set for -40dBm wanted signal, max RF gain - 16dB (B7:B6 = 10)		-7		
	AGC set for -30dBm wanted signal, max RF gain - 32dB (B7:B6 = 11)		+16		
Inband Input P-1dB	Max RF gain (B7:B6 = 00)		-37		dBm
	Max RF gain - 8dB (B7:B6 = 01)		-29		
	Max RF gain - 16dB (B7:B6 = 01)		-21		
	Max RF gain - 32dB (B7:B6 = 11)		-4		
Maximum Output Signal Level	Over passband frequency range at VGA gain between max and max - 54dB; 1dB compression point		1.15		V_{P-P}
I/Q Gain Imbalance	100kHz IQ baseband output; 1 σ variation		0.05		dB
I/Q Phase Error	100kHz IQ baseband output; 1 σ variation		0.25		Degrees
Rx I/Q Output Load Impedance (R ll C)	Minimum differential resistance	10			kΩ
	Maximum differential capacitance			5	pF
Loopback Gain (for Receiver I/Q Calibration)	Transmitter I/Q input to receiver I/Q output; transmitter B6:B1 = 000011, receiver B5:B0 = 101010 programmed through SPI	-6	-1	+4.5	dB
I/Q Output DC Droop	After switching RXHP to 0; average over 1µs after any gain change, or 2µs after receive enabled with 100Hz AC-coupling		1		V/s
I/Q Static DC Offset	No RF input signal; measure at 3µs after receive enable; RXHP = 1 for 0 to 2µs and set to 0 after 2µs, 1 σ variation		1		mV
Isolation Between Rx Channels A and B	Any RF gain settings		40		dB
RECEIVER BASEBAND FILTERS					
Baseband Filter Rejection	At 15MHz		57		dB
	At 20MHz		75		
	At > 40MHz		75		
Baseband Highpass Filter Corner Frequency	RXHP = 1 (used before AGC completion)		650		kHz
	RXHP = 0 (used after AGC completion) address A[4:0] = 01110; D[5:4] = 00		0.1		
	RXHP = 0 (used after AGC completion) address A[4:0] = 01110; D[5:4] = 01		1		
	RXHP = 0 (used after AGC completion) address A[4:0] = 01110; D[5:4] = 10		30		
	RXHP = 0 (used after AGC completion) address A[4:0] = 01110; D[5:4] = 11		100		

AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.4999GHz, f_{LO} = 2.5GHz; baseband output signal frequency = 100kHz, f_{REF} = 40MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit* and registers set to default settings. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Channel BW Supported by Baseband Filter	A[4:0] = 00100 serial bits D[9:6] = 0000			1.75		MHz
	A[4:0] = 00100 serial bits D[9:6] = 0001			2.25		
	A[4:0] = 00100 serial bits D[9:6] = 0010			3.5		
	A[4:0] = 00100 serial bits D[9:6] = 0011			5.0		
	A[4:0] = 00100 serial bits D[9:6] = 0100			5.5		
	A[4:0] = 00100 serial bits D[9:6] = 0101			6.0		
	A[4:0] = 00100 serial bits D[9:6] = 0110			7.0		
	A[4:0] = 00100 serial bits D[9:6] = 0111			8.0		
	A[4:0] = 00100 serial bits D[9:6] = 1000			9.0		
	A[4:0] = 00100 serial bits D[9:6] = 1001			10.0		
	A[4:0] = 00100 serial bits D[9:6] = 1010			12.0		
	A[4:0] = 00100 serial bits D[9:6] = 1011			14.0		
	A[4:0] = 00100 serial bits D[9:6] = 1100			15.0		
	A[4:0] = 00100 serial bits D[9:6] = 1101			20.0		
	A[4:0] = 00100 serial bits D[9:6] = 1110			24.0		
	A[4:0] = 00100 serial bits D[9:6] = 1111			28.0		
Baseband Gain Ripple	0 to 2.3MHz for RF BW = 5MHz			1.3		dB_{P-P}
	0 to 4.6MHz for RF BW = 10MHz			1.3		
Baseband Group Delay Ripple	0 to 2.3MHz for RF BW = 5MHz			90		ns_{P-P}
	0 to 4.6MHz for RF BW = 10MHz			50		
Baseband Filter Rejection for 5MHz RF Channel BW	At 2.3MHz			1.8		dB
	At > 8.75MHz			75		
Baseband Filter Rejection for 10MHz RF Channel BW	At 4.6MHz			1.6		dB
	At > 17.5MHz			75		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} ≥ 10kΩ			0.6		V
RSSI Maximum Output Voltage	R_{LOAD} ≥ 10kΩ			2.1		V
RSSI Slope				29		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		800		

2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

AC ELECTRICAL CHARACTERISTICS—Tx MODE

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.501GHz, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, TXRX = SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit* and registers set to default settings. Lowpass filter is set to 10MHz RF channel BW. 1MHz 90mV$_{RMS}$ cosine and sine signals applied to I/Q baseband inputs of transmitter (differential DC-coupled)). (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx BASEBAND I/Q INPUTS TO RF OUTPUTS					
RF Output Frequency Range		2.3		2.7	GHz
Peak-to-Peak Peak Gain Variation over RF Band			1	2	dB
Total Voltage Gain	Max gain - 3dB; at unbalanced 50Ω matched output	3.5	8		dB
Max Output Power over Frequency	64 QAM OFDM signal conforming to spectral emission mask and -36dB EVM after I/Q imbalance calibration by modem (Note 5)		0		dBm
RF Output Return Loss			8		dB
RF Gain Control Range	B6:B1 = 000000 to 111111		62		dB
Unwanted Sideband Suppression	Without calibration by modem, and excludes modem I/Q imbalance; P_{OUT} = 0dBm		40		dB
RF Gain Control Binary Weights	B1		1		dB
	B2		2		
	B3		4		
	B4		8		
	B5		16		
	B6		32		
Carrier Leakage	Relative to 0dBm output power; without calibration by modem		-30		dBc
Tx I/Q Input Impedance (RllC)	Differential resistance		100		kΩ
	Differential capacitance		0.5		pF
Baseband Frequency Response for 5MHz RF Channel BW	0 to 3.333MHz		0.9		dB
	At > 9.45MHz		43		
Baseband Frequency Response for 10MHz RF Channel BW	0 to 6.667MHz		0.9		dB
	At > 18.9MHz		43		
Baseband Group Delay Ripple	0 to 3.333MHz (RF BW = 5MHz)		20		ns
	0 to 6.667MHz (RF BW = 10MHz)		12		

AC ELECTRICAL CHARACTERISTICS—FREQUENCY SYNTHESIS

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL closed-loop unity gain bandwidth = 120kHz. VCO and RF synthesis enabled.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Channel Center Frequency Range		2.3		2.7	GHz
Channel Center Frequency Programming Minimum Step Size			28.61		Hz
Charge-Pump Comparison Frequency			40		MHz
Reference Frequency Range		15	40	80	MHz
Reference Frequency Input Levels	AC-coupled to REFCLK pin	0.6			V_{P-P}
Reference Frequency Input Impedance (RllC)	Resistance (REFCLK pin)		10		kΩ
	Capacitance (REFCLK pin)		1		pF
Programmable Reference Divider Values		1	2	4	
Closed-Loop Integrated Phase Noise	Integrate phase noise from 200Hz to 5MHz; charge-pump comparison frequency = 40MHz		-39		dBc
Charge-Pump Output Current	On each differential side		0.8		mA
Close-In Spur Level	f_{OFFSET} = 0 to 1.8MHz		-40		dBc
	f_{OFFSET} = 1.8MHz to 7MHz		-70		
	f_{OFFSET} > 7MHz		-80		
Reference Spur Level			-85		dBc
Turnaround LO Frequency Error	Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes		±50		Hz
Temperature Range Over Which VCO Maintains Lock	Relative to the ambient temperature T_A at initial lock		T_A ±40		°C
Reference Output Clock Divider Values	CLKOUT_DIV pin = 0		1		
	CLKOUT_DIV pin = 1		2		
Output Clock Drive Level	20MHz output, A[4:0] = 10100, D5 = 0		2.4		V_{P-P}
Output Clock Load Impedance (RllC)	Resistance		10		kΩ
	Capacitance		2		pF

AC ELECTRICAL CHARACTERISTICS—MISCELLANEOUS BLOCKS

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, and T_A = +25°C.) (Note

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA BIAS DAC: VOLTAGE MODE						
Output High level	10mA source current			V_{CC} - 0.1		V
Output Low level	100µA sink current			0.1		V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs			200		ns
CRYSTAL OSCILLATOR						
On-Chip Tuning Capacitance Range	Maximum capacitance, A[4:0] = 11000, D[6:0] = 1111111			15.5		pF
	Minimum capacitance, A[4:0] = 11000, D[6:0] = 0000000			0.5		
On-Chip Tuning Capacitance Step Size				0.12		pF
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Readout at DOUT pin through SPI A[4:0] = 01011, D[4:0]	T_A = +25°C		01111		
		T_A = +85°C		11101		
		T_A = -40°C		00001		

AC ELECTRICAL CHARACTERISTICS—TIMING

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL closed-loop unity gain bandwidth = 120kHz, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING							
Turnaround Time		Measured from Tx or Rx enable edge; signal settling to within 2dB of steady state	Rx to Tx		2		µs
			Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)		Measured from Tx-enable edge; signal settling to within 2dB of steady state			2		µs
Tx Turn-Off Time (to Standby Mode)		From Tx-disable edge			0.1		µs
Rx Turn-On Time (from Standby Mode)		Measured from Rx-enable edge; signal settling to within 2dB of steady state			2		µs
Rx Turn-Off Time (to Standby Mode)		From Rx-disable edge			0.1		µs

AC ELECTRICAL CHARACTERISTICS—TIMING (continued)

(MAX2839AS Evaluation Kit. Unless otherwise noted, $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL closed-loop unity gain bandwidth = 120kHz, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
4-WIRE SERIAL PARALLEL INTERFACE TIMING (see Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}			6		ns
Clock Frequency	f_{CLK}			40		MHz
Rise Time	t_R			$0.1/f_{CLK}$		ns
Fall Time	t_F			$0.1/f_{CLK}$		ns
SCLK Falling Edge to Valid DOUT	t_D			12.5		ns

Note 2: Min/max limits are production tested at T_A = +85°C. Min/max limits at T_A = -40°C and T_A = +25°C are guaranteed by design and characterization. The power-on default register settings are not production tested. Load register setting 10µs after V_{CC} is applied.

Note 3: Tx mode supply current is specified for 64 QAM while achieving the Tx output spectrum mask shown in the *Typical Operating Characteristics*. The supply current can be reduced for 16 QAM signal by adjusting the Tx bias settings through the SPI.

Note 4: Two tones at +20MHz and +39MHz offset with -35dBm/tone. Measure IM3 at 1MHz.

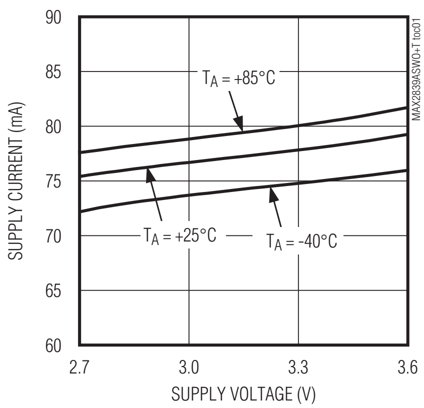
Note 5: Gain adjusted over max gain and max gain -3dB.

2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

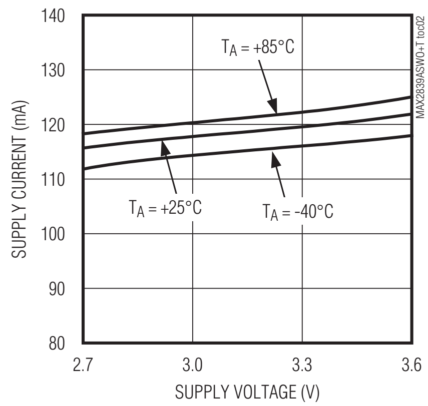
Typical Operating Characteristics

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

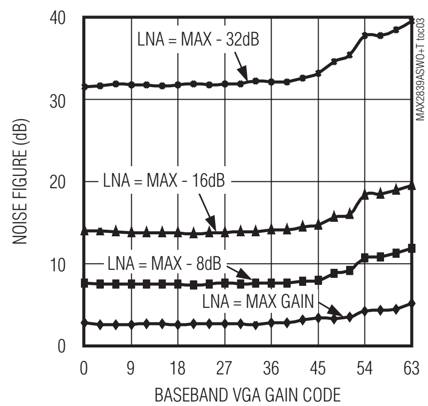
SINGLE Rx SUPPLY CURRENT vs. SUPPLY VOLTAGE



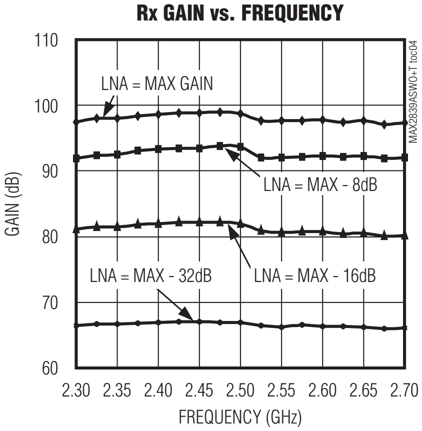
DUAL Rx SUPPLY CURRENT vs. SUPPLY VOLTAGE



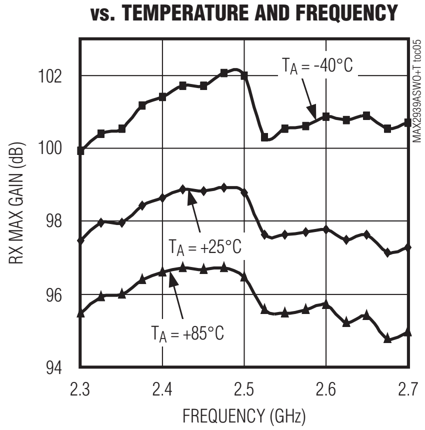
Rx NOISE FIGURE vs. BASEBAND GAIN SETTING



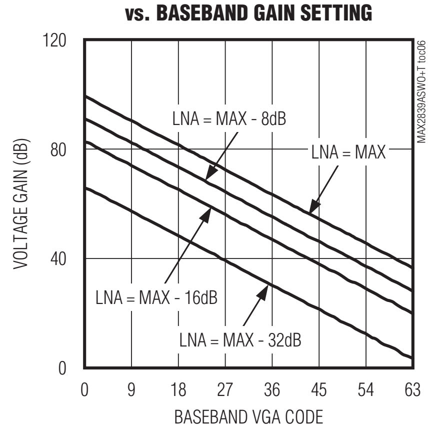
Rx GAIN vs. FREQUENCY



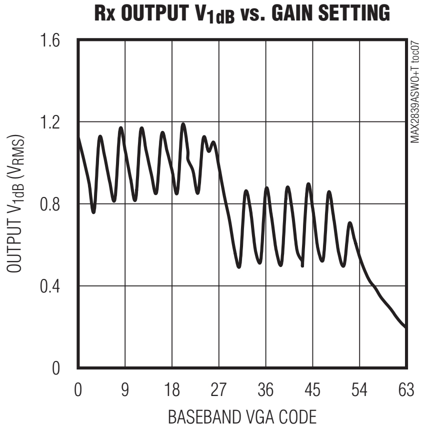
Rx MAX GAIN vs. TEMPERATURE AND FREQUENCY



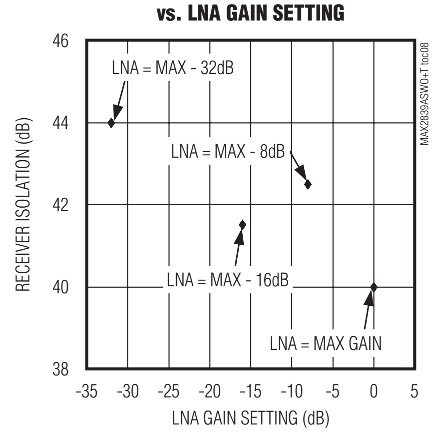
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



Rx OUTPUT V_{1dB} vs. GAIN SETTING



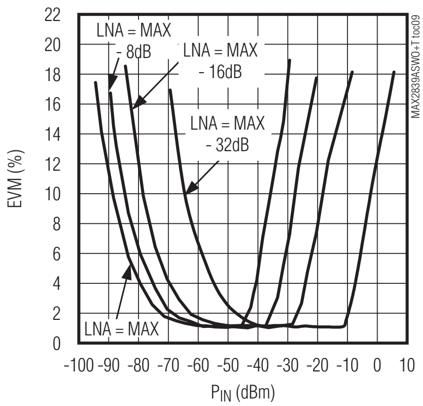
RX_B TO RX_A ISOLATION vs. LNA GAIN SETTING



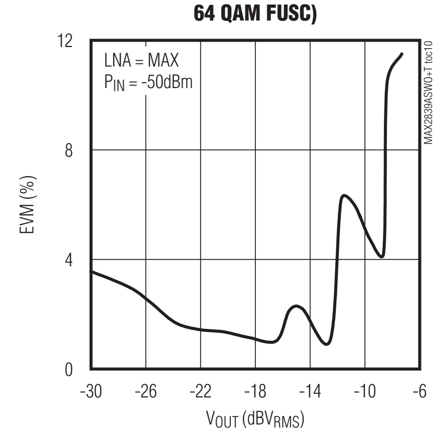
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

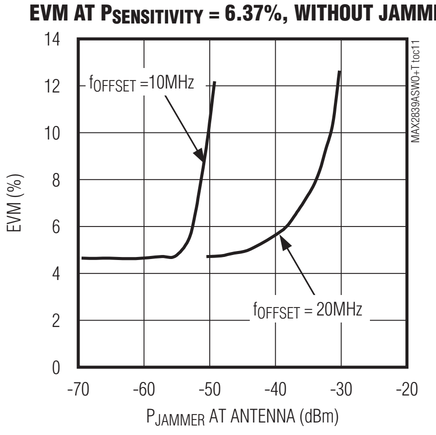
Rx EVM vs. P_{IN} (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)



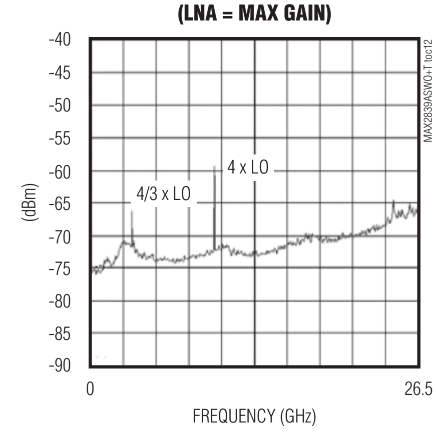
Rx EVM vs. V_{OUT} (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)



WiMAX EVM vs. OFDM JAMMER (10MHz CHANNEL BANDWIDTH, 64 QAM FUSC) P_{WANTED} = $P_{SENSITIVITY}$ + 3dB = -70.3dBm AT ANTENNA (INCLUDING 4dB FRONT-END LOSS), EVM AT $P_{SENSITIVITY}$ = 6.37%, WITHOUT JAMMER



Rx EMISSION SPECTRUM AT LNA INPUT (LNA = MAX GAIN)

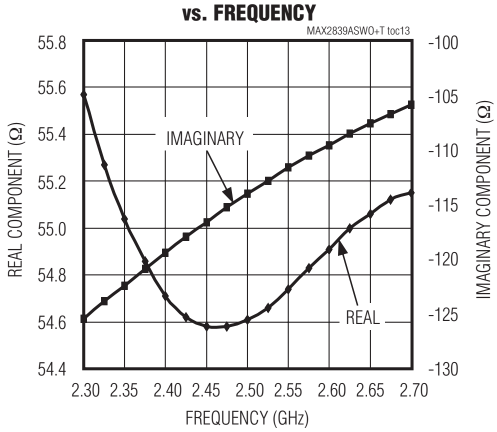


2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

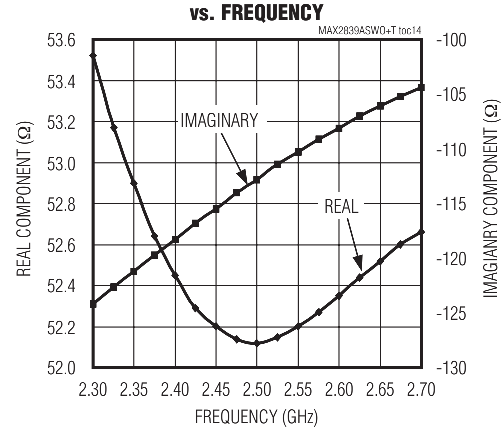
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

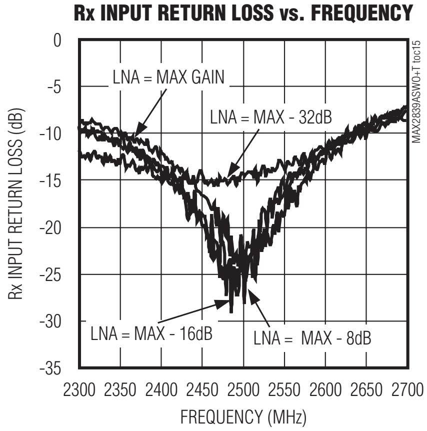
RXINA± DIFFERENTIAL IMPEDANCE vs. FREQUENCY



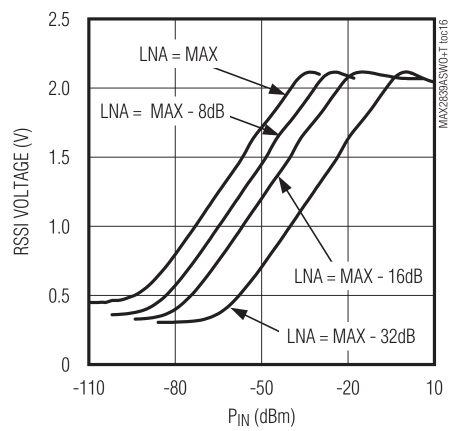
RXINB± DIFFERENTIAL IMPEDANCE vs. FREQUENCY



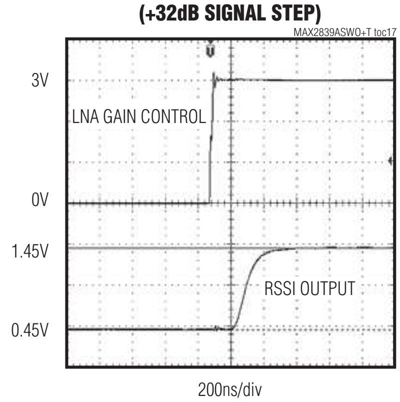
Rx INPUT RETURN LOSS vs. FREQUENCY



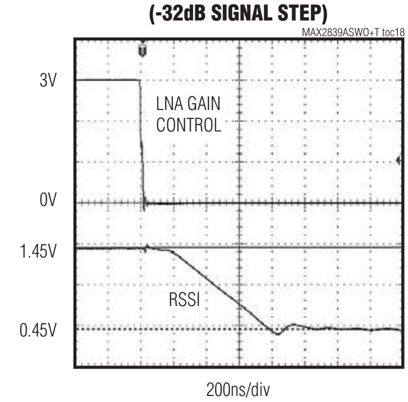
RSSI VOLTAGE vs. INPUT POWER



Rx RSSI STEP RESPONSE (+32dB SIGNAL STEP)



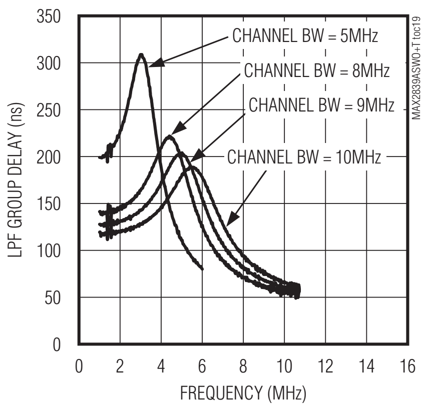
Rx RSSI STEP RESPONSE (-32dB SIGNAL STEP)



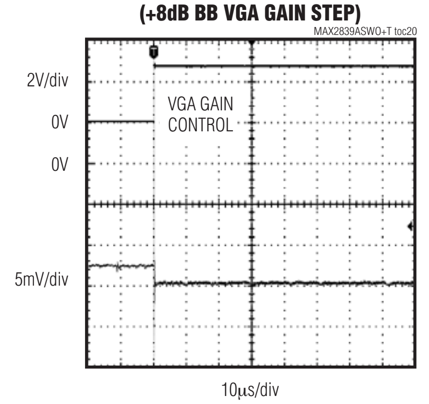
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

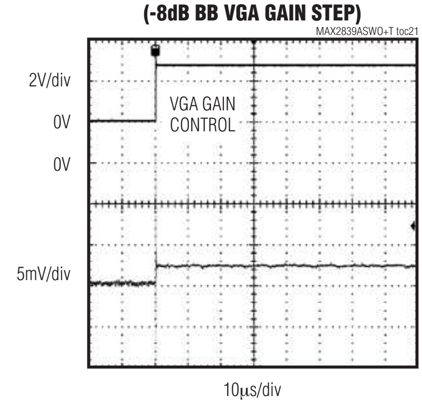
Rx LPF GROUP DELAY vs. FREQUENCY



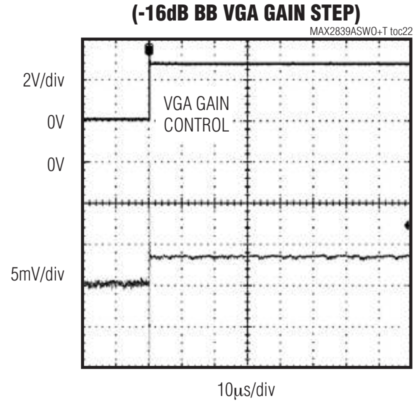
Rx DC OFFSET SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



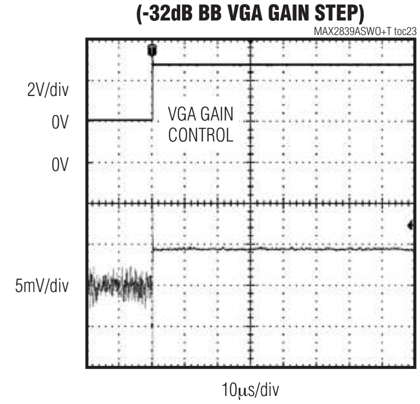
Rx DC OFFSET SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



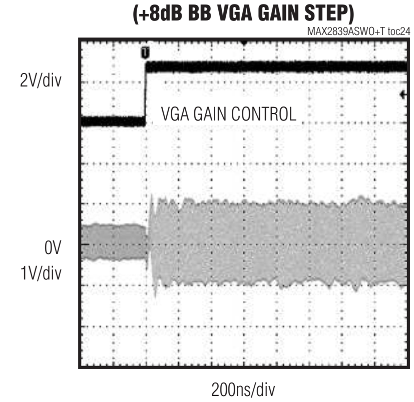
Rx DC OFFSET SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



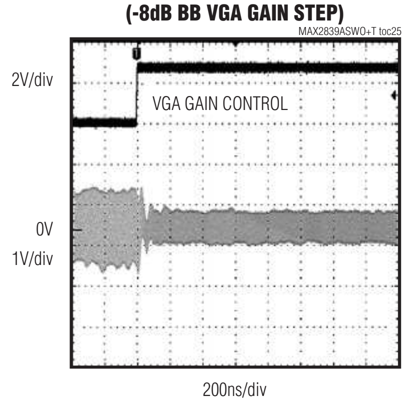
Rx DC OFFSET SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



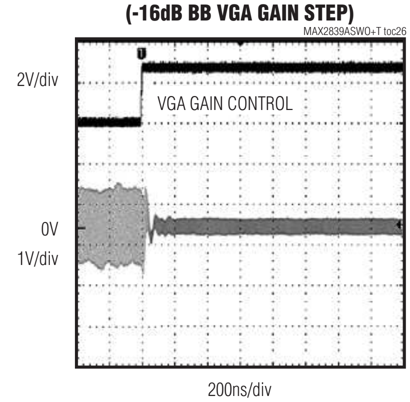
Rx BB VGA SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



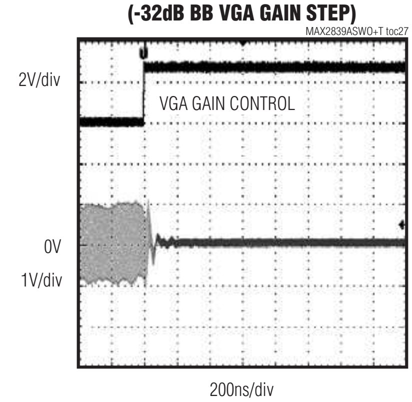
Rx BB VGA SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



Rx BB VGA SETTLING RESPONSE (-16dB BB VGA GAIN STEP)

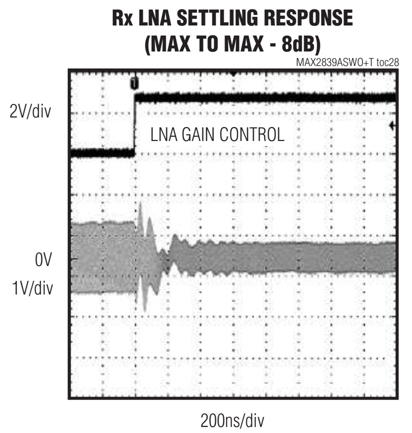


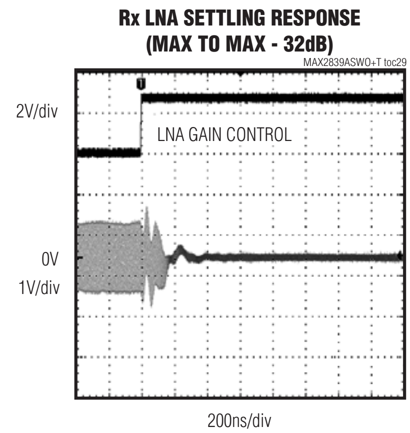
Rx BB VGA SETTLING RESPONSE (-32dB BB VGA GAIN STEP)

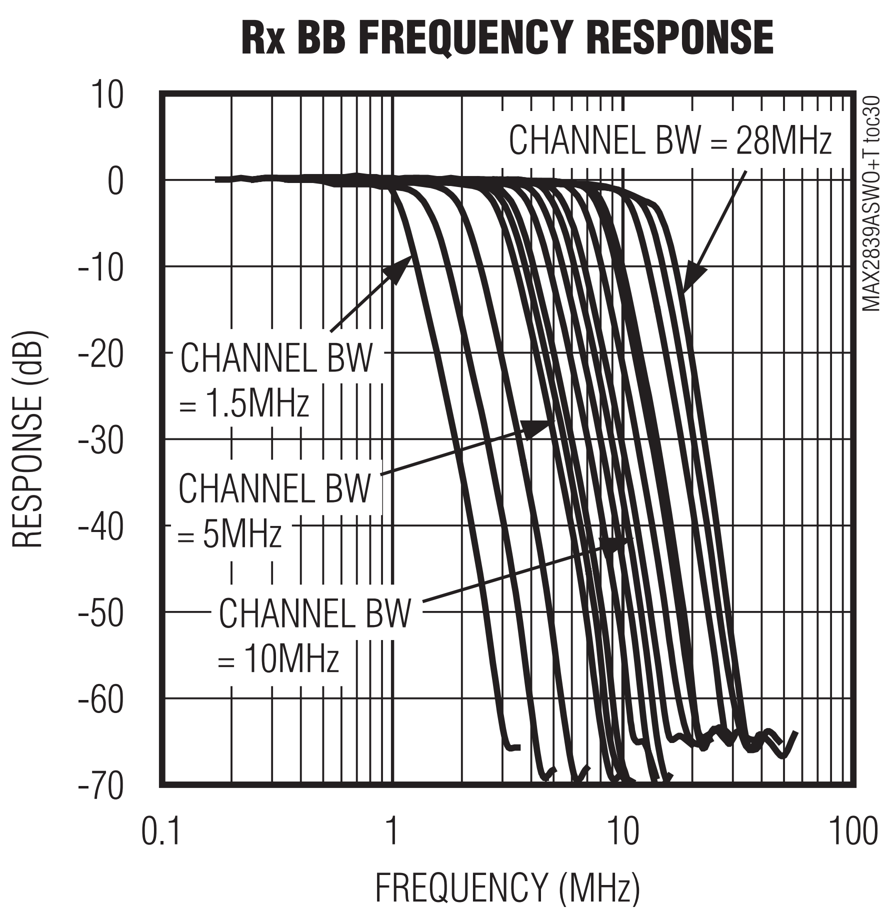


Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)



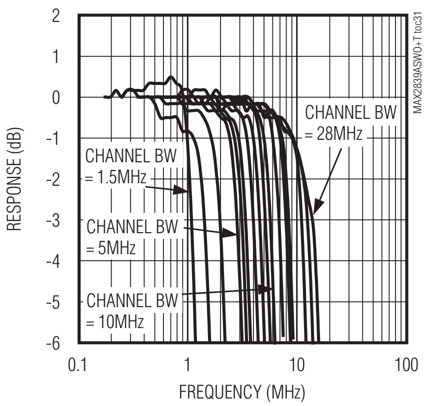




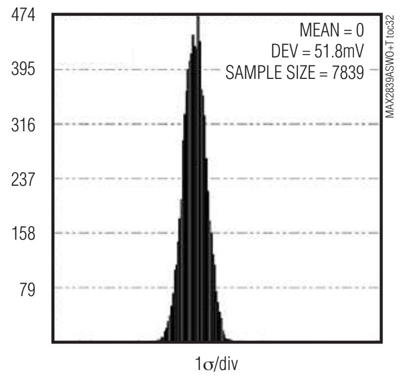
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

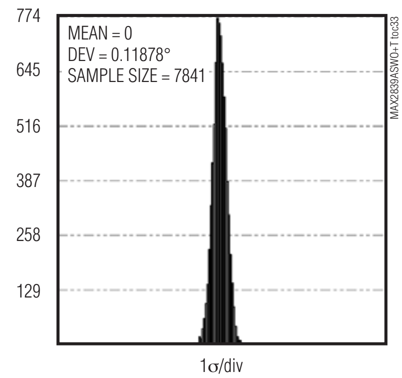
Rx BB FREQUENCY RESPONSE



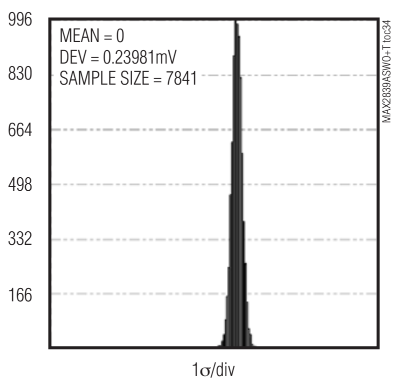
HISTOGRAM: IQ GAIN IMBALANCE



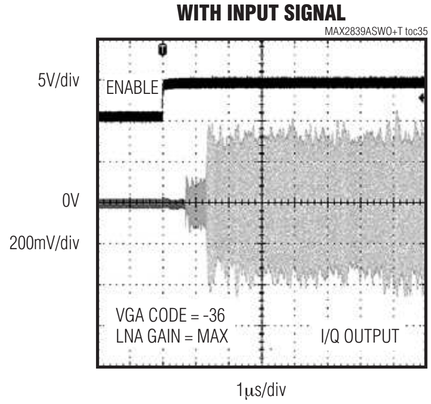
HISTOGRAM: Rx PHASE IMBALANCE



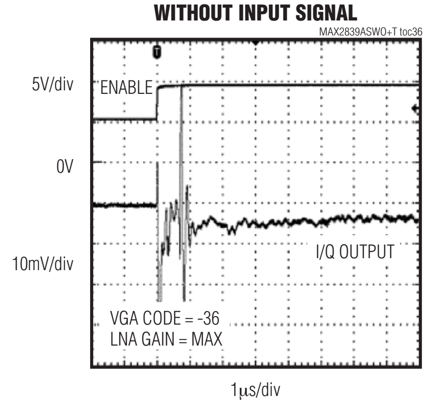
HISTOGRAM: Rx STATIC DC OFFSET



POWER-ON DC OFFSET CANCELLATION WITH INPUT SIGNAL



POWER-ON DC OFFSET CANCELLATION WITHOUT INPUT SIGNAL

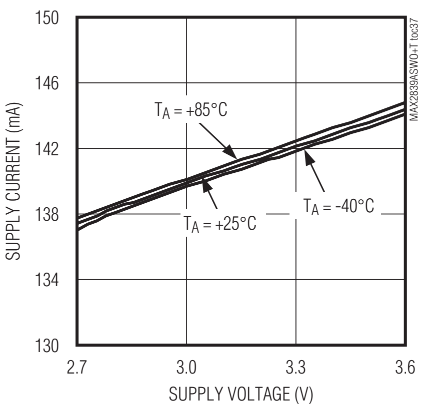


2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

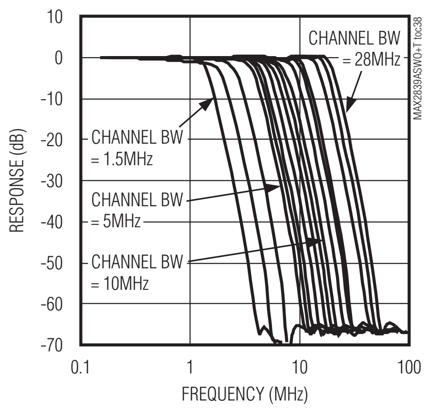
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

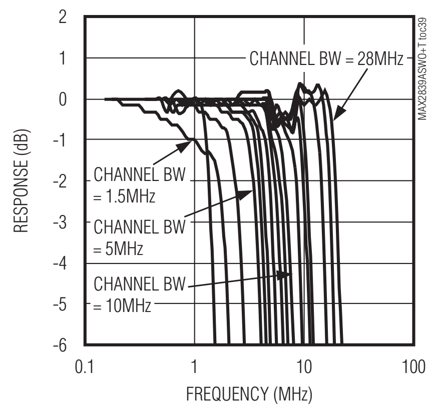
Tx SUPPLY CURRENT vs. SUPPLY VOLTAGE



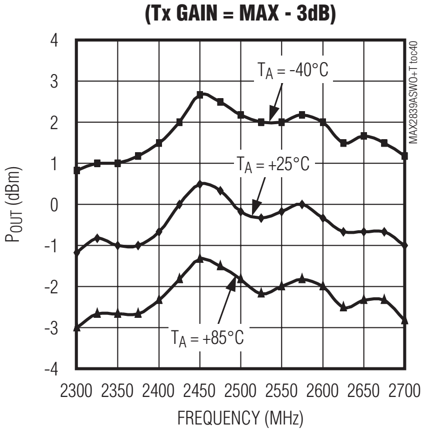
Tx BASEBAND FREQUENCY RESPONSE



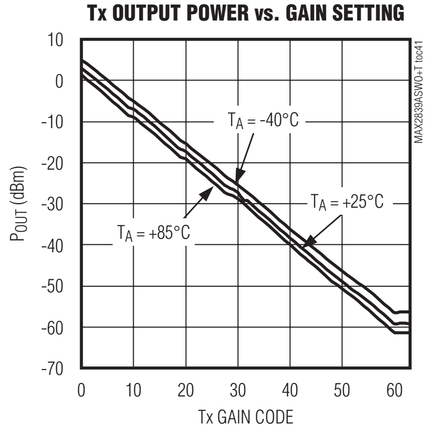
Tx BASEBAND FREQUENCY RESPONSE



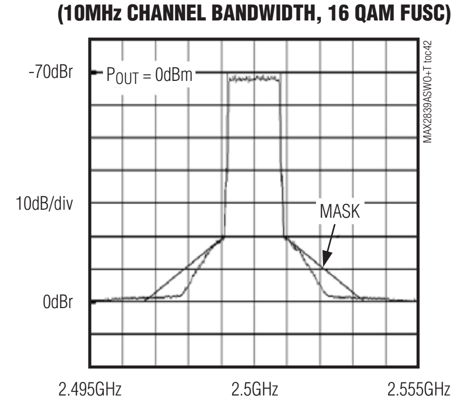
Tx OUTPUT POWER vs. FREQUENCY (Tx GAIN = MAX - 3dB)



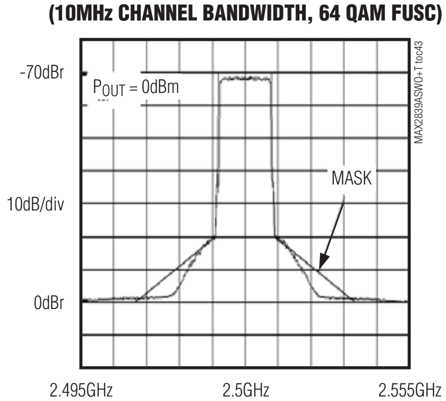
Tx OUTPUT POWER vs. GAIN SETTING



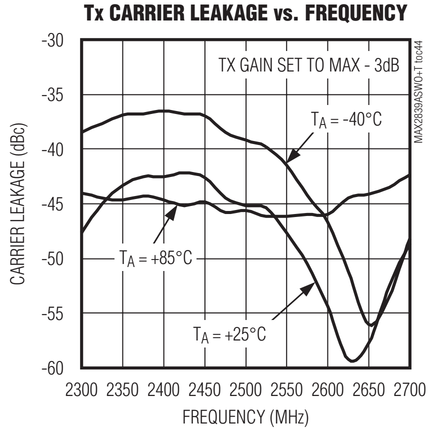
Tx OUTPUT SPECTRUM (10MHz CHANNEL BANDWIDTH, 16 QAM FUSC)



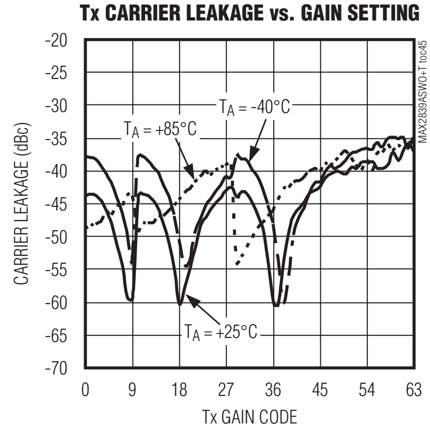
Tx OUTPUT SPECTRUM (10MHz CHANNEL BANDWIDTH, 64 QAM FUSC)



Tx CARRIER LEAKAGE vs. FREQUENCY



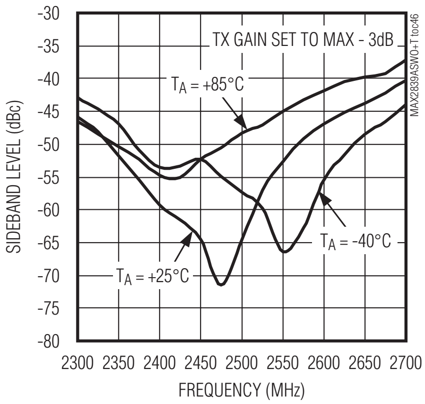
Tx CARRIER LEAKAGE vs. GAIN SETTING



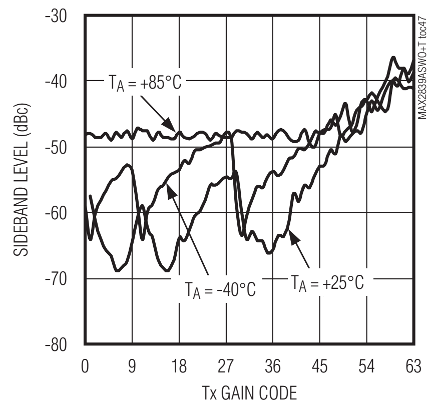
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

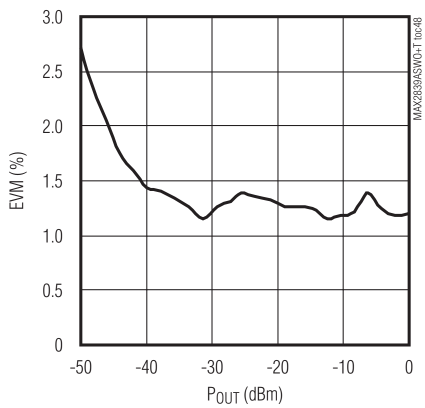
Tx SIDEBAND LEVEL vs. FREQUENCY



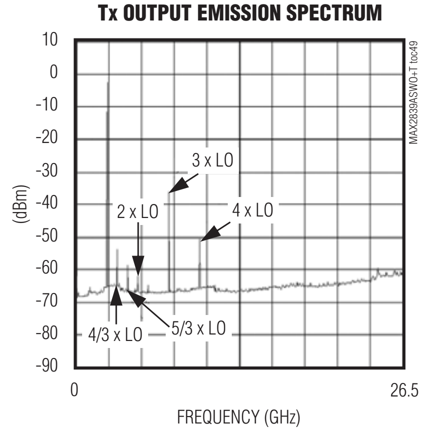
Tx SIDEBAND LEVEL vs. GAIN SETTING



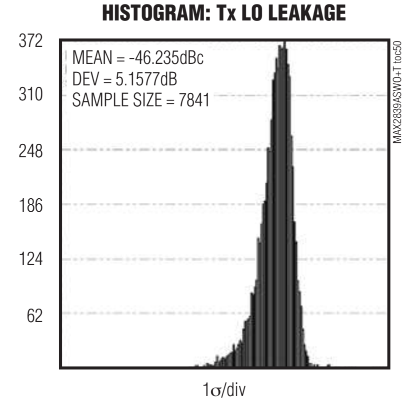
EVM vs. Tx OUTPUT POWER (64 QAM FUSC, 10MHz CHANNEL BANDWIDTH)



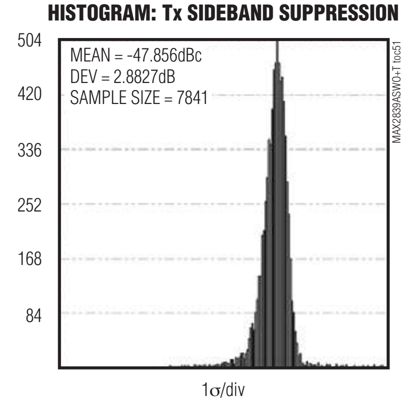
Tx OUTPUT EMISSION SPECTRUM



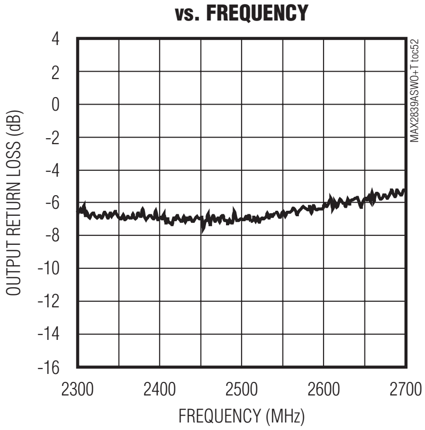
HISTOGRAM: Tx LO LEAKAGE



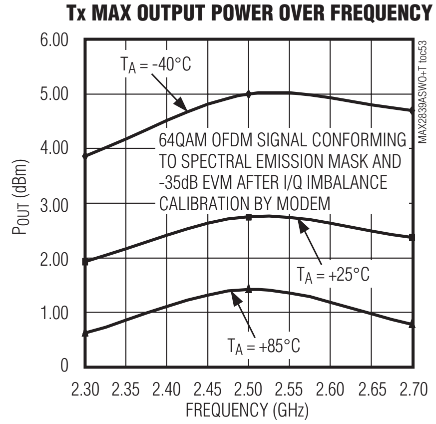
HISTOGRAM: Tx SIDEBAND SUPPRESSION



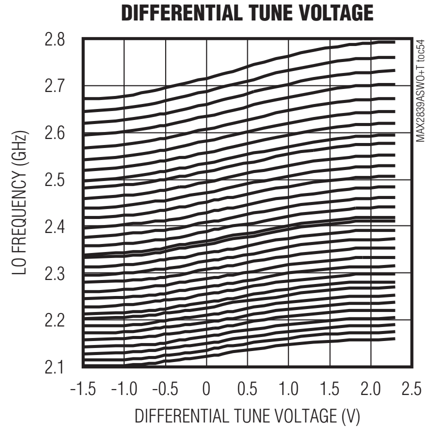
Tx OUTPUT RETURN LOSS vs. FREQUENCY



Tx MAX OUTPUT POWER OVER FREQUENCY



LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE

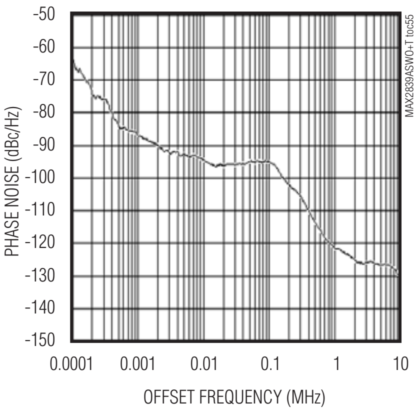


2.3GHz to 2.7GHz MIMO Wireless Broadband RF Transceiver

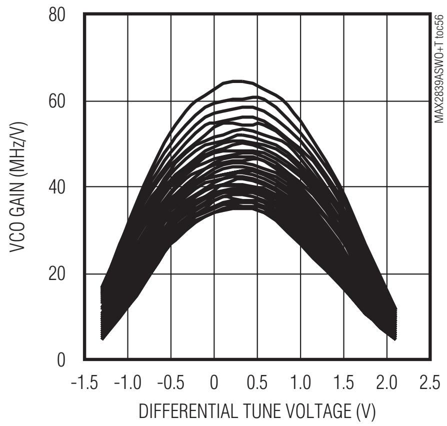
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 2.5GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2839AS Evaluation Kit.)

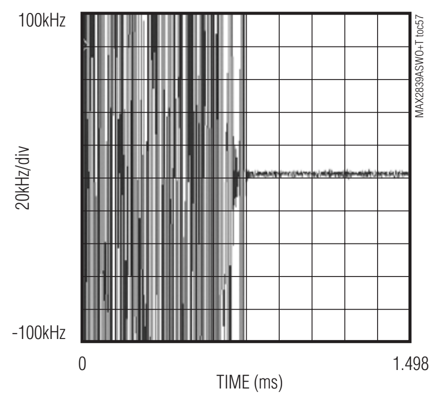
PHASE NOISE vs. OFFSET FREQUENCY



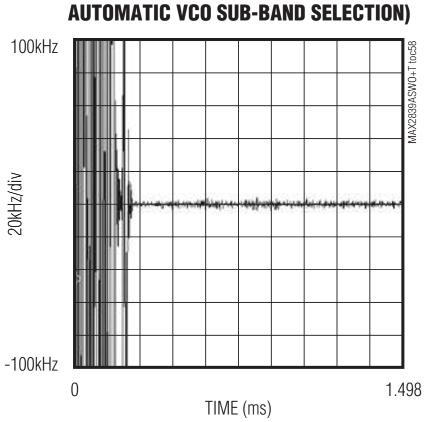
VCO GAIN vs. DIFFERENTIAL TUNE VOLTAGE



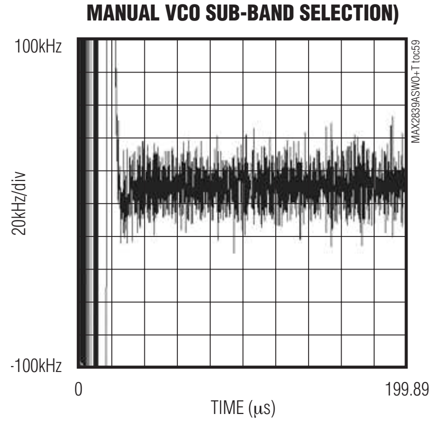
CHANNEL-SWITCHING FREQUENCY SETTLING (2.3GHz TO 2.7GHz, AUTOMATIC VCO SUB-BAND SELECTION)



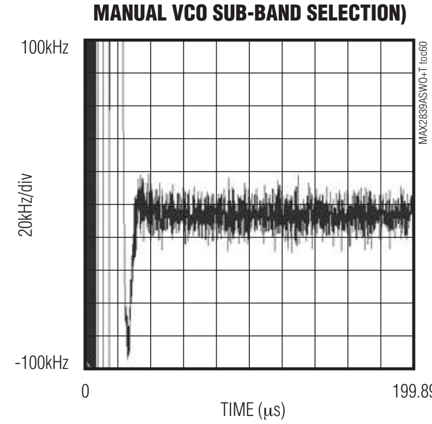
CHANNEL-SWITCHING FREQUENCY SETTLING (2.7GHz TO 2.3GHz, AUTOMATIC VCO SUB-BAND SELECTION)



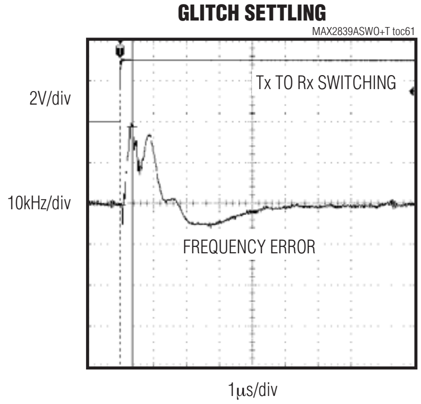
CHANNEL-SWITCHING FREQUENCY SETTLING (2.3GHz TO 2.7GHz, MANUAL VCO SUB-BAND SELECTION)



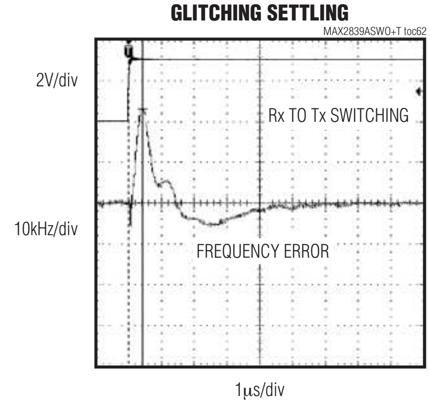
CHANNEL-SWITCHING FREQUENCY SETTLING (2.7GHz TO 2.3GHz, MANUAL VCO SUB-BAND SELECTION)



Tx-TO-Rx TURNAROUND FREQUENCY GLITCH SETTLING



Rx-TO-Tx TURNAROUND FREQUENCY GLITCHING SETTLING



Bump Description

BUMP	NAME	FUNCTION
1	GNDRXLNA_A	Receiver A LNA Ground
2	$V_{CCRXLNA\_A}$	Receiver A LNA Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
3	$V_{CCRXLNA\_B}$	Receiver B LNA Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
4	GND_LNA_B	Receiver B LNA Ground
5	RXINB+	Receiver B LNA Differential Input Plus. Input is internally DC-coupled.
6	GND_MXR_B	Receiver B Mixer Ground
7	B2	Receiver and Transmitter Gain-Control Logic Input Bit 2
8	B3	Receiver and Transmitter Gain-Control Logic Input Bit 3
9	B4	Receiver and Transmitter Gain-Control Logic Input Bit 4
10	$V_{CCTXPAD}$	Supply Voltage for Transmitter Power Amplifier Driver. Bypass with a 22pF capacitor as close as possible to the pin.
11	GND1_PAD_RF	Transmit Power Amplifier Driver Ground
12	GND2_PAD_RF	Transmit Power Amplifier Driver Ground
13	PABIAS	Transmit External Power Amplifier Bias DAC Output
14	GND_TXMX	Transmit Upconverter Ground
15	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface
16	REFCLK	Reference Clock Input. AC-couple a reference clock to this analog input.
17	V_{CCXTAL}	Crystal Oscillator Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
18	V_{CCCP}	PLL Charge-Pump Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
19	GNDCP	Charge-Pump Ground
20	CPOUT+	Differential Charge-Pump Output Plus. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*).
21	GNDVCO	VCO Ground
22	VCOBYP	On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this point.
23	V_{CCVCO}	VCO Supply Voltage. Bypass with a 22nF capacitor as close as possible to the pin.
24	GND_LO	Local Oscillator Generation Ground
25	$\overline{CS}$	Active-Low Chip-Select Logic Input of 4-Wire Serial Interface
26	GND_RXBB_B	Receiver B Baseband Ground
27	RXBBIB+	Receiver B Baseband I-Channel Differential Output Plus
28	RXBBQB+	Receiver B Baseband Q-Channel Differential Output Plus
29	B6	Receiver and Transmitter Gain-Control Logic Input Bit 6
30	RXBBQA-	Receiver A Baseband Q-Channel Differential Output Minus
31	RXBBQA+	Receiver A Baseband Q-Channel Differential Output Plus
32	$V_{CCRXVGA}$	Receiver VGA Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
33	GND_RXBB_A	Receiver A Baseband Ground
34	GND_RXLOGEN	Receiver Divide-by-2 Ground
35	GND_MXR_A	Receiver A Mixer Ground
36	GND_LNA_A	Receiver A LNA Ground
37	TXBBQ-	Transmitter Baseband Q-Channel Differential Input Minus
38	CLKOUT_DIV	Clockout Divide Ratio Select Logic Input

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Bump Description (continued)

BUMP	NAME	FUNCTION
39	GNDRXLNA_B	Receiver B LNA Ground
40	RXINB-	Receiver B LNA Differential Input Minus. Input is internally DC-coupled.
41	TXRX	Transmit/Receive Mode Enable Logic Input
42	B5	Receiver and Transmitter Gain-Control Logic Input Bit 5
43	TXOUT+	Power Amplifier Driver Differential Output Plus. The pin is biased at $V_{CC}/2$ internally.
44	B1	Receiver and Transmitter Gain-Control Logic Input Bit 1
45	TXOUT-	Power Amplifier Driver Differential Output Minus. The pin is biased at $V_{CC}/2$ internally.
46	V_{CCTXMX}	Transmitter Upconverter Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
47	CLKOUT	Reference Clock Buffer Output
48	GND_XTAL	Crystal Oscillator Ground
49	GND_DIG	PLL Digital Ground
50	V_{CC_DIG}	PLL Digital Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
51	CPOUT-	Differential Charge-Pump Output Minus. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*).
52, 67	GND	Ground. Connect to the PCB ground plane.
53	DIN	Data Logic Input of 4-Wire Serial Interface
54	GND_PAD_BIAS	Transmit Bias Ground
55	XTAL1	XTAL Input. AC-couple crystal to this analog pin.
56	RXHP	Receiver I- and Q-Channel AC-Coupling Highpass Corner Frequency Selection Logic Input
57	RXBBIA-	Receiver A Baseband I-Channel Differential Output Minus
58	RXBBIA+	Receiver A Baseband I-Channel Differential Output Plus
59	TXBBI+	Transmitter Baseband I-Channel Differential Input Plus
60	TXBBQ+	Transmitter Baseband Q-Channel Differential Input Plus
61	V_{CCRXMX}	Receiver Downconverters Supply Voltage. Bypass with a 22pF capacitor as close as possible to the pin.
62	RXINA-	Receiver A LNA Differential Input Minus. Input is internally DC-coupled.
63	RXINA+	Receiver A LNA Differential Input Plus. Input is internally DC-coupled.
64	B0	Receiver and Transmitter Gain-Control Logic Input Bit 0
65	ENABLE	Transceiver Enable Logic Input
66	DOUT	Data Logic Output of 4-Wire Serial Interface
68	RXBBIB-	Receiver B Baseband I-Channel Differential Output Minus
69	RXBBQB-	Receiver B Baseband Q-Channel Differential Output Minus
70	RSSI	Receiver Signal Strength Output
71	B7	Receiver Gain-Control Logic Input Bit 7
72	V_{CCRXFL}	Receiver Baseband Filter Supply Voltage. Bypass with a 100nF capacitor as close as possible to the pin.
73	TXBBI-	Transmitter Baseband I-Channel Differential Input Minus

Table 1. Operating Mode

MODE	MODE CONTROL LOGIC INPUTS				CIRCUIT BLOCK STATES				
	ENABLE PIN	TXRX PIN	SPI REG1 D<3>	SPI REG16 D<1:0>	Rx PATH	Tx PATH	PLL, VCO, LO GEN	CALIBRATION SECTIONS ON	CLOCK OUTPUT
Shutdown	0	0	X	XX	Off	Off	Off	None	Off
Clock-Out Only	1	X	X	X0	Off	Off	Off	None	On
Clock-Out Only	X	1	X	X0	Off	Off	Off	None	On
Standby	0	1	X	01	Off	Off	On or Off	None	On
Rx (1x2 MIMO)	1	1	1	01	On	Off	On	None	On
Rx (1x1 SISO)	1	1	0	01	On (RX_A)	Off	On	None	On
Tx	1	0	X	01	Off	On	On	None	On
Tx Calibration	1	0	X	11	Off	On (except PA driver)	On SPI REG7D<7> = 1	AM detector + Rx I, Q buffers	On
RX_A Calibration (Loopback)	1	1	0	11	On (except LNA)	On (except PA driver)	On SPI REG26D<3> = 1	Loopback	On
RX_B Calibration (Loopback)	1	1	1	11	On (except LNA)	On (except PA driver)	On SPI REG26D<3> = 1	Loopback	On

Detailed Description

Modes of Operation

The modes of operation for the MAX2839AS are shutdown, clock-out only, standby, receive, transmit, transmitter calibration, and receiver calibration. See Table 1 for a summary of the modes of operation. When the parts are active, various blocks can be shutdown individually by programming different SPI registers.

Shutdown Mode

The MAX2839AS features a low-power shutdown mode. In shutdown mode, all circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers.

Clock-Out Only

In clock-out mode, the entire transceiver is off except the divided reference clock output on the CLKOUT pin and the clock divider, which remain on.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, the PLL, VCO, and LO generator are on so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks can be selectively enabled in this mode by programming different SPI registers.

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx BB I and Q outputs. Either receiver A or both receivers can be enabled. Receiver B cannot be enabled by itself.

Transmit (Tx) Mode

In transmit mode, all Tx circuit blocks are powered on. The external PA is powered on after a programmable delay using the on-chip PA bias DAC.

Transmitter (Tx) Calibration Mode

All Tx circuit blocks except PA driver and external PA are powered on and active. The AM detector and receiver I/Q channel buffers are also on, along with multiplexers in the receiver side to route this AM detector's signal to each I and Q differential outputs. When required, the I/Q lowpass filter can be bypassed.

Receiver (Rx) Calibration or Loopback

Part of the Rx and Tx circuit blocks except LNA and PA driver are powered on and active. The transmitter I/Q input signals are upconverted to RF, and the output of the Tx gain control block (VGA) is fed to the receiver at the input of the downconverter. Either receiver A or both receivers can be connected to the transmitter and powered on. The I/Q lowpass filters are not present in the transmitter signal path (they are bypassed).

Programmable Registers and 4-Wire SPI Interface

The MAX2839AS includes 32 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit. The next 5 bits are register address. The 10 least significant bits (LSBs) are register data. Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. Data at DIN is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock. During the read mode, register data selected by address bits is shifted out to DOUT at the falling edges of the clock. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. After power-up, the user must program all register values.

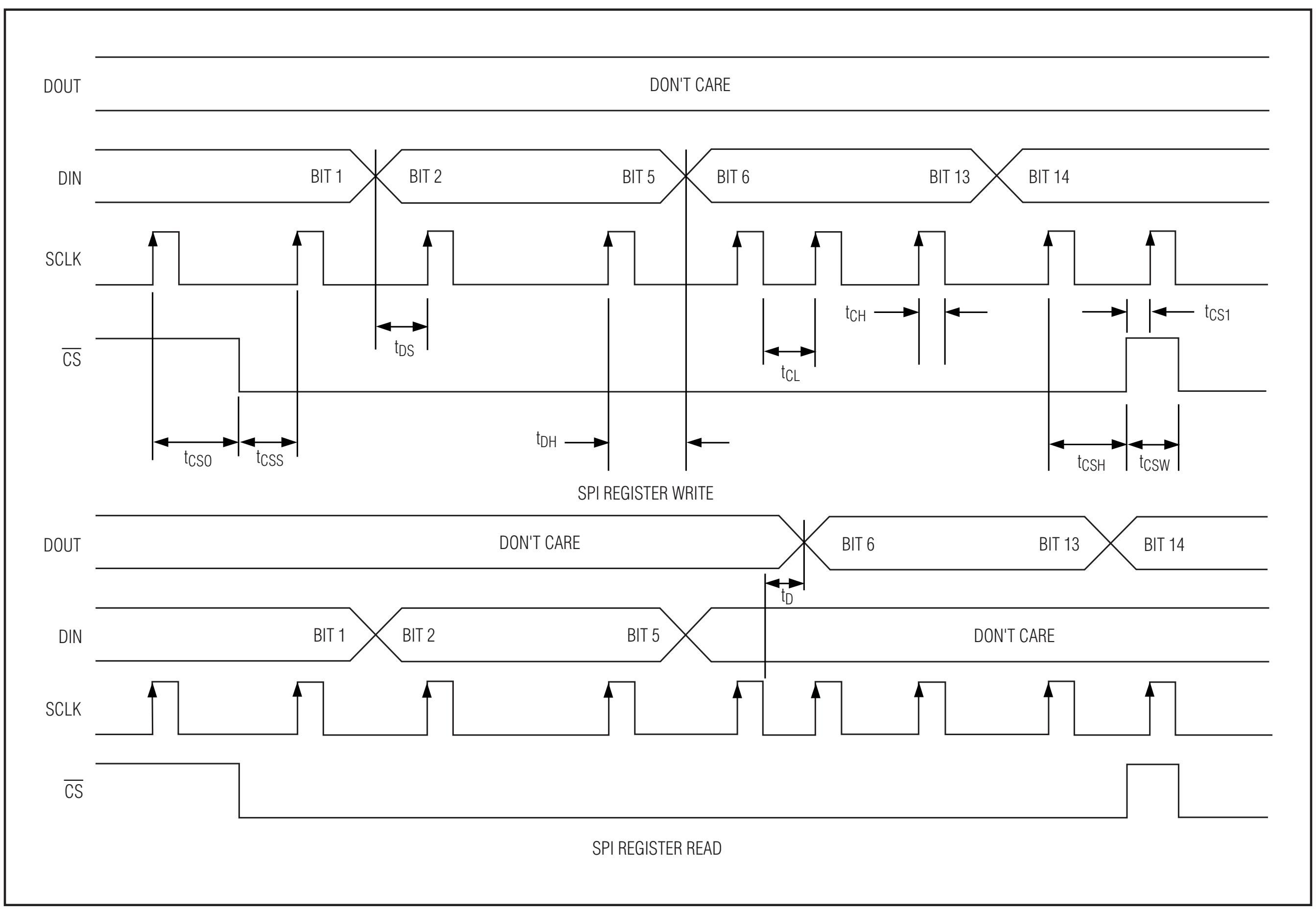

Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

MICROWIRE is a trademark of National Semiconductor Corp.

SPI Register Definitions

(All values in the register definition table are typical numbers. The MAX2839AS SPI does not have a power-on-default feature; the user must program all SPI addresses for normal operation. Prior to use of any untested settings, contact the factory.)

Table 2. MAX2839AS Register Summary

REGISTER NO.	REGISTER NAME	DEFAULT	FUNCTIONS
0	RX_ENABLE	000	Reserved for internal use
1	RX_RF_1	00C	• LNA band select, MIMO mode select • Rx I/Q phase error correction
2	RX_RF_2	081	• LNA gain SPI control enable • Rx I/Q phase error SPI control enable
3	RX_RF/LPF	1B9	Reserved for internal use
4	LPF	3E6	• RF channel bandwidth select
5	LPF/VGA_1	100	• RX_A LNA and VGA gain controls • LPF operating mode select
6	LPF/VGA_2	000	• RX_B LNA and VGA gain controls • Rx VGA common-mode select
7	RSSI/VGA	208	• RSSI pin output select, operating mode as a function of RXHP, and receiver select • Rx baseband outputs routing select
8	RX_TOP_SPI_1	222	• Rx VGA gain SPI control enable • LPF operating mode select enable
9	RX_TOP_SPI_2	018	• Temperature sensor enable, and ADC readout trigger • DOUT output selection, drive select, three-state output select
10	TX_TOP_ SPI	00C	• Tx AM detector gain and filter bandwidth controls
11	TEMP_SEN	004	• Temperature sensor ADC readout
12	HPFSM 1	24F	• 10MHz HPC duration select when triggered by RXEN or LNA gain • 600kHz HPC duration select when triggered by RXEN or LNA gain
13	HPFSM 2	150	• 100kHz HPC duration select when triggered by RXEN or LNA gain • 30kHz HPC duration select when triggered by RXEN or LNA gain • 1kHz HPC duration select when triggered by RXEN
14	HPFSM 3	3C5	• 1kHz HPC duration select when triggered by LNA gain • HPC rising edge delay and final highpass corner select • HPC on-hold corner select as a function of RXHP • HPC state machine retriggered by LNA gain enable
15	HPFSM 4	201	• HPC state machine clock divider, sequence bypass, and RXHP dependent select
16	BLK_SPI_EN	01C	• Block enabled by SPI
17	FRAC_DIV_1	155	• Last 10 of 20 fractional divider bits
18	FRAC_DIV_2	155	• First 10 of 20 fractional divider bits
19	INT_DIV	153	• Integer divider bits • LO generation band select
20	SYNTH_CONFIG_1	249	• Reference divider ratio • CLKOUT buffer drive select
21	SYNTH_CONFIG_2	02D	Reserved for internal use

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Table 2. MAX2839AS Register Summary (continued)

REGISTER NO.	REGISTER NAME	DEFAULT	FUNCTIONS
22	VAS_CONFIG	1A9	• VAS operating mode select, relock location, clock divide ratio, delay counter ratio, and triggering
23	LO_MISC_CONFIG	24F	• VAS sub-band SPI overwrite • Crystal oscillator bias select
24	XTAL_CONFIG	180	• Crystal oscillator core enable, and frequency tuning
25	VCO_CONFIG	000	Reserved for internal use
26	LOGEN_CONFIG	3C0	• VAS test signal select • VTUNE test signal select • LOGEN G_m enable
27	TXLO_I/Q_CONFIG	280	• Tx LO I/Q phase adjustment by SPI enable, and phase adjustment select • Tx DC correction by SPI enable • Tx VGA gain control by SPI enable
28	PA_BIAS_ DAC	0C0	• PA DAC output current select, and turn-on delay control
29	TX_GAIN_CONFIG	03F	• Tx VGA gain control
30	TX_DC CORR_1	380	• Tx DC offset correction for I-channel • PA DAC output type select, and voltage mode output select
31	TX_DC_CORR_2	340	• Tx DC offset correction for Q-channel • PA DAC clock-divide ratio

REGISTER NAME	ADDRESS BITS					DATA BITS									
	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RX_ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RX_RF_1	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0
RX_RF_2	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1
RX_RF/LPF	0	0	0	1	1	0	1	1	0	1	1	1	0	0	1
LPF	0	0	1	0	0	1	1	1	1	1	0	0	1	1	0
LPF/VGA_1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
LPF/VGA_2	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
RSSI/VGA	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0
RX_TOP_SPI_1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
RX_TOP_SPI_2	0	1	0	0	1	0	0	0	0	0	1	1	0	0	0
TX_TOP_ SPI	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0
TEMP_SEN	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0
HPFSM 1	0	1	1	0	0	1	0	0	1	0	0	1	1	1	1
HPFSM 2	0	1	1	0	1	0	1	0	1	0	1	0	0	0	0
HPFSM 3	0	1	1	1	0	1	1	1	1	0	0	0	1	0	1
HPFSM 4	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1
BLK_SPI_EN	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
FRAC_DIV_1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1
FRAC_DIV_2	1	0	0	1	0	0	1	0	1	0	1	0	1	0	1
INT_DIV	1	0	0	1	1	0	1	0	1	0	1	0	0	1	1

Table 2. MAX2839AS Register Summary (continued)

REGISTER NAME	ADDRESS BITS					DATA BITS									
	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SYNTH_CONFIG_1	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1
SYNTH_CONFIG_2	1	0	1	0	1	0	0	0	0	1	0	1	1	0	1
VAS_CONFIG	1	0	1	1	0	0	1	1	0	1	0	1	0	0	1
LO_MISC_CONFIG	1	0	1	1	1	1	0	0	1	0	0	1	1	1	1
XTAL_CONFIG	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0
VCO_CONFIG	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
LOGEN_CONFIG	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0
TXLO_I/Q_CONFIG	1	1	0	1	1	1	0	1	0	0	0	0	0	0	0
PA_BIAS_ DAC	1	1	1	0	0	0	0	1	1	0	0	0	0	0	0
TX_GAIN_CONFIG	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1
TX_DC CORR_1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0
TX_DC_CORR_2	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Table 3. Register 0: RX_ENABLE Register (Address = 00000, Default = 000_{HEX})

BIT NAME	BIT LOCATION (0 = LSB)	DESCRIPTION
RESERVED	9:0	Reserved bits—set to default

Table 4. Register 1: RX_RF_1 Register (Address = 00001, Default = $00C_{HEX}$)

BIT NAME	BIT LOCATION (0 = LSB)	DESCRIPTION
RESERVED	9:4	Reserved bits—set to default
MIMO_MODE_SEL	3	MIMO mode selection. 0 = RX_A 1 = RX_A + RX_B (default)
RESERVED	2:1	Reserved bits—set to default
LNA_BAND	0	LNA output LC tank center frequency select. 0 = 2.3GHz to 2.5GHz (default) 1 = 2.5GHz to 2.7GHz

Table 5. Register 2: RX_RF_2 Register (Address = 00010, Default = 081_{HEX})

BIT NAME	BIT LOCATION (0 = LSB)	DESCRIPTION
RESERVED	9:1	Reserved bits—set to default
LNA_GAIN_SPI_EN	0	LNA gain control select. 0 = LNA gain controlled by external pins B7 and B6 1 = LNA gain controlled by SPI through register 6 bits 1:0 (default)