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MAX2851 5GHz, 5-Channel MIMO Receiver

General Description

The MAX2851 is a single-chip, 5-channel RF receiver IC designed for 5GHz wireless HDMI™ applications. The IC includes all circuitry required to implement the complete 5-channel MIMO RF receiver function and crystal oscillator, providing a fully integrated receive path, VCO, frequency synthesis, and baseband/control interface. It includes a fast-settling sigma-delta RF fractional synthesizer with 76Hz frequency programming step size. The IC also integrates on-chip I/Q amplitude and phase-error calibration circuits. The receiver includes both an in-channel RSSI and also an RF RSSI.

On-chip monolithic filters are included for receiver I/Q baseband signal channel selection, for supporting both 20MHz and 40MHz RF channels. The baseband filtering and Rx signal paths are optimized to meet stringent WHDI requirements. The downconverter local oscillator is coherent among all the receiver channels.

The reverse-link control channel uses an on-chip 5GHz OFDM transmitter. It shares the RF synthesizer and LO generation circuit with the MIMO receivers. Dynamic on/off control of the external PA is implemented with programmable precision voltage. An analog mux routes external PA power-detect voltage to the RSSI pin.

The MIMO receiver chip is housed in a small 68-pin TQFN leadless plastic package with exposed paddle.

Applications

- 5GHz Wireless HDMI (WHDI™)
- 5GHz FDD Backhaul and WiMAX™
- 5GHz MIMO Receiver Up to Five Spatial Streams
- 5GHz Beam Steering Receiver

HDMI is a trademark of HDMI Licensing, LLC.
WHDI is a trademark of WHDI Special Interest Group.
WiMAX is a trademark of the WiMAX Forum.

Features

- 5GHz, 5x MIMO Downlink Receivers, Single-Uplink IEEE 802.11a Transmitter
- 4900MHz to 5900MHz Frequency Range
- Coherent LO Among Receivers
- 4.5dB Rx Noise Figure
- 70dB Rx Gain Control Range with 2dB Step Size, Digitally Controlled
- 60dB Dynamic Range Receiver RSSI
- RF Wideband Receiver RSSI
- Programmable 20MHz/40MHz Rx I/Q Lowpass Channel Filters
- -5dBm Transmit Power (54Mbps OFDM)
- 31dB Tx Gain Control Range with 0.5dB Step Size, Digitally Controlled
- Tx/Rx I/Q Error and LO Leakage Detection and Adjustment
- Programmable 20MHz/40MHz Tx I/Q Lowpass Anti-Aliasing Filter
- Analog Mux for PA Power Detect
- PA On/Off Control
- Sigma-Delta Fractional-N PLL with 76Hz Resolution
- Monolithic Low-Noise VCO with -35dBc Integrated Phase Noise
- 4-Wire SPI Digital Interface
- I/Q Analog Baseband Interface
- Digital Tx/Rx Mode Control
- On-Chip Digital Temperature Sensor Readout
- Complete Baseband Interface
- Digital Tx/Rx Mode Control
- +2.7V to +3.6V Supply Voltage
- Small 68-Pin TQFN Package (10mm x 10mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2851ITK+	-25°C to +85°C	68 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

***Typical Operating Circuit* appears at end of data sheet.**

maxim integrated™

19-5121; Rev 1; 3/10

Absolute Maximum Ratings

$V_{CC\_}$ Pins to GND ....-0.3V to +3.9V
RF Inputs Max Current: RXRF1+, RXRF1-, RXRF2+, RXRF2-, RXRF3+, RXRF3-, RXRF4+, RXRF4-, RXRF5+, RXRF5- to GND................................-1mA to +1mA
RF Outputs: TXRF+, TXRF- to GND...................-0.3V to +3.9V
Analog Inputs: TXBBI+, TXBBI-, TXBBQ+, TXBBQ-, PA_DET, XTAL, XTAL_CAP to GND...............................-0.3V to +3.9V
Analog Outputs: RXBBI1+, RXBBI1-, RXBBQ1+, RXBBQ1-, RXBBI2+, RXBBI2-, RXBBQ2+, RXBBQ2-, RXBBI3+, RXBBI3-, RXBBQ3+, RXBBQ3-, RXBBI4+, RXBBI4-, RXBBQ4+, RXBBQ4-, RXBBI5+, RXBBI5-, RXBBQ5+, RXBBQ5-, RSSI, CLKOUT2, BYP_VCO, CPOUT+, CPOUT-, PA_BIAS to GND...-0.3V to +3.9V
Digital Inputs: ENABLE, $\overline{CS}$, SCLK, DIN to GND ....-0.3V to +3.9V
Digital Outputs: DOUT, CLKOUT to GND ....-0.3V to +3.9V
Short-Circuit Duration
Analog Outputs.. 10s
Digital Outputs.. 10s
RF Input Power ....+10dBm
RF Output Differential Load VSWR...6:1
Continuous Power Dissipation (T_A = +85°C)
68-Pin TQFN (derate 29.4mW/°C above +70°C)......2352mW
Operating Temperature Range.......................... -25°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range........................... -65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow)......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC Electrical Characteristics

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, ENABLE set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter in maximum gain. Power matching and termination for the differential RF output pins using the *Typical Operating Circuit*; 100mV_{RMS} differential I and Q signals applied to I and Q baseband inputs of transmitters in transmit mode. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO freq = 5.35GHz. Channel bandwidth is set to 40MHz. PA control pins open circuit, $V_{CC\_PA\_BIAS}$ is disconnected.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			2.7		3.6	V
Supply Current	Shutdown mode	T_A = +25°C		10		µA
	Clockout only mode with load = 10pF at CLKOUT pin	XTAL oscillator, CLKOUT2 is off		3.7		mA
		XTAL oscillator, CLKOUT2 is on		4.6		
		TCXO input, CLKOUT2 is off		4.8	7.0	
		TCXO input, CLKOUT2 is on		6.1		
	Standby mode			60		
	Transmit mode			183	212	
	Receive mode	One receiver is on		144	184	
		Five receivers are on		367	458	
	Receive calibration mode	One receiver is on		248		
		Five receivers are on		435	517	
	Transmit calibration mode			256		
Rx I/Q Output Common-Mode Voltage			0.88	1.1	1.34	V
Tx Baseband Input Common-Mode Voltage Operating Range			0.5		1.1	V
Tx Baseband Input Bias Current	Source current			10	20	µA

DC Electrical Characteristics (continued)

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, ENABLE set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter in maximum gain. Power matching and termination for the differential RF output pins using the *Typical Operating Circuit*; 100mV_{RMS} differential I and Q signals applied to I and Q baseband inputs of transmitters in transmit mode. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO freq = 5.35GHz. Channel bandwidth is set to 40MHz. PA control pins open circuit, $V_{CC\_PA\_BIAS}$ is disconnected.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS: ENABLE, SCLK, DIN, $\overline{CS}$					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}	(Note 2)			0.3	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: DOUT, CLKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 1mA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 1mA			0.4	V
Digital Output Voltage in Shutdown Mode	Sinking 1mA		V_{OL}		V

AC Electrical Characteristics—Rx Mode

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, RF freq = 5.351GHz, LO freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF_+ and RXRF_- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV_{RMS} loaded with 10kΩ differential load resistance and 10pF load capacitance. RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, channel bandwidths of 40MHz.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER SECTION: RF INPUT TO I/Q BASEBAND LOADED OUTPUT Includes 50Ω to 100Ω RF Balun and Matching					
RF Input Frequency Range		4.9		5.9	GHz
Peak-to-Peak Gain Variation Over RF Frequency Range at One Temperature	4.9GHz to 5.9GHz		1.8	4.2	dB
RF Input Return Loss	All LNA settings		-6		dB
Total Voltage Gain	Maximum gain, Main address 1 D[7:0] = 11111111	61.8	68		dB
	Minimum gain, Main address 1 D[7:0] = 00000000		-2	+6.9	
RF Gain Steps Relative to Maximum Gain	Main address 1 D[7:5] = 110		-8		dB
	Main address 1 D[7:5] = 101		-16		
	Main address 1 D[7:5] = 001		-32		
	Main address 1 D[7:5] = 000		-40		
Baseband Gain Range	From maximum baseband gain (Main address 1 D[3:0] = 1111) to minimum baseband gain (Main address 1 D[3:0] = 0000)	28	30	32	dB
Baseband Gain Step			2		dB
RF Gain Change Settling Time	Gain settling to within ±0.5dB of steady state, RXHP = 1		400		ns

AC Electrical Characteristics—Rx Mode (continued)

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, RF freq = 5.351GHz, LO freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF_+ and RXRF_- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV$_{RMS}$ loaded with 10kΩ differential load resistance and 10pF load capacitance. RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, channel bandwidths of 40MHz.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Gain Change Settling Time	Gain settling to within ±0.5dB of steady state, RXHP = 1			200		ns
DSB Noise Figure	Balun input referred, integrated from 10kHz to 9.5MHz at I/Q baseband output for 20MHz RF bandwidth	Maximum RF gain (Main address 1 D[7:5] = 111)		4.5		dB
		Maximum RF gain - 16dB (Main address 1 D[7:5] = 101)		15		
	Balun input referred, integrated from 10kHz to 19MHz at I/Q base-band output for 40MHz RF bandwidth	Maximum RF gain (Main address 1 D[7:5] = 111)		4.5		
		Maximum RF gain - 16dB (Main address 1 D[7:5] = 101)		15		
Out-of-Band Input IP3	20MHz RF channel, two-tone jammers at +25MHz and +48MHz frequency offset with -39dBm/tone	-65dBm wanted signal, RF gain = max (Main address 1 D[7:0] = 11101001)		-13		dBm
		-49dBm wanted signal, RF gain = max - 16dB (Main address 1 D[7:0] = 10101001)		-5		
		-45dBm wanted signal, RF gain = max - 32dB (Main address 1 D[7:0] = 00111111)		11		
	40MHz RF channel, two-tone jammers at +50MHz and +96MHz frequency offset with -39dBm/tone	-65dBm wanted signal, RF gain = max (Main address 1 D[7:0] = 11101001)		-13		
		-49dBm wanted signal, RF gain = max - 16dB (Main address 1 D[7:0] = 10101001)		-5		
		-45dBm wanted signal, RF gain = max - 32dB (Main address 1 D[7:0] = 00101001)		11		
1dB Gain Desensitization by Alternate Channel Blocker	Blocker at ±40MHz offset frequency for 20MHz RF channel			-24		dBm
	Blocker at ±80MHz offset frequency for 40MHz RF channel			-24		
Input 1dB Gain Compression	Max RF gain (Main address 1 D[7:5] = 111)			-34		dBm
	Max RF gain - 8dB (Main address 1 D[7:5] = 110)			-25		
	Max RF gain - 16dB (Main address 1 D[7:5] = 101)			-18		
	Max RF gain - 32dB (Main address 1 D[7:5] = 001)			-1		

AC Electrical Characteristics—Rx Mode (continued)

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, RF freq = 5.351GHz, LO freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF_+ and RXRF_- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV$_{RMS}$ loaded with 10kΩ differential load resistance and 10pF load capacitance. RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, channel bandwidths of 40MHz.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output 1dB Gain Compression	Over passband frequency range, at any gain setting, 1dB compression point		0.63		V_{P-P}
Baseband -3dB Lowpass Corner Frequency	Main address 0 D1 = 0		9.5		MHz
	Main address 0 D1 = 1		19		
Baseband Filter Stopband Rejection	Rejection at 30MHz offset frequency for 20MHz channel		74		dB
	Rejection at 60MHz offset frequency for 40MHz channel		69		
Baseband -3dB Highpass Corner Frequency	Main address 5 D1 = 1		600		kHz
	Main address 5 D1 = 0, Main address 4 D3 = 1		10		
	Main address 5 D1 = 0, Main address 4 D3 = 0 (Note 3)		0.1		
Steady-State I/Q Output DC Error with AC-Coupling	50µs after enabling receive mode and togging RXHP from 1 to 0, averaged over many measurements if I/Q noise voltage exceeds 1mV$_{RMS}$, at any given gain setting, no input signal, 1-sigma value		2		mV
I/Q Gain Imbalance	1MHz baseband output, 1-sigma value		0.1		dB
I/Q Phase Imbalance	1MHz baseband output, 1-sigma value		0.2		deg
Sideband Suppression	1MHz baseband output		40		dB
Receiver Spurious Signal Emissions	LO frequency		-75		dBm/MHz
	2O LO frequency		-62		
	3O LO frequency		-75		
	4O LO frequency		-54		
RF RSSI Output Voltage	-25dBm input power		1.6		V
Baseband RSSI Slope		18	26.5	37	mV/dB
Baseband RSSI Maximum Output Voltage			2.3		V
Baseband RSSI Minimum Output Voltage			0.5		V
RF Loopback Conversion Gain	Tx VGA gain at max (Main address 9 D[9:4] = 111111), Rx VGA gain at max - 24dB (Main address 1 D[3:0] = 0101)	-17.1	-10	-1.7	dB

AC Electrical Characteristics—Tx Mode

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, RF freq = 5.351GHz, LO freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at TXRF+ and TXRF- differential ports using the *Typical Operating Circuit*; 100mV$_{RMS}$ sine and cosine signal applied to I/Q baseband inputs of transmitter (differential DC-coupled). Typical values measured at V_{CC} = 2.85V, T_A = +25°C, channel bandwidths of 40MHz.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS Includes Matching and Balun Loss					
RF Output Frequency Range		4.9		5.9	GHz
Peak-to-Peak Gain Variation Over RF Band	At one temperature		0.7	1.55	dB
Maximum Output Power	20MHz OFDM signal conforming to spectral emission mask and -34dB EVM		-3		dBm
	40MHz OFDM signal confirming to spectral emission mask and -34dB EVM		-3		
Output 1dB Gain Compression	Relative to typical maximum output power at 9.5MHz input frequency		11		dBc
Input 1dB Gain Compression	At 19MHz input frequency, over input common-mode voltage between 0.5V and 1.1V		380		mV$_{RMS}$
Gain Control Range		24	31.5	34	dB
Gain Control Step			0.5		dB
RF Output Return Loss			-3		dB
Unwanted Sideband	Over RF channel, RF frequency, baseband frequency, and gain settings (Note 4)		-40		dBc
Carrier Leakage	Over RF channel, RF frequency, and gain settings (Note 4)		-29	-15	dBc
Tx I/Q Input Impedance (R || C)	Minimum differential resistance		60		kΩ
	Maximum differential capacitance		2		pF
Baseband Filter Stopband Rejection	At 30MHz frequency offset for 20MHz RF channel		86		dB
	At 60MHz frequency offset for 40MHz RF channel		67		
Tx Calibration Ftone Level	At Tx gain code (Main address 9 D[9:4]) = 100010 and -15dBc carrier leakage (Local address 27 D[2:0] = 110 and Main address 1 D[3:0] = 0000)		-24		dBV$_{RMS}$
Tx Calibration RF Gain Step Relative to Maximum Gain	Local address 27 D[1:0] = 01		-14		dB
	Local address 27 D[1:0] = 00		-28		
Tx Calibration Baseband Gain Step Relative to Maximum Gain	Local address 27 D2 = 0		-5		dB

AC Electrical Characteristics—Frequency Synthesis

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO freq = 5.35GHz.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
RF Channel Center Frequency		4.9		5.9	GHz
Channel Center Frequency Programming Step			76.294		Hz
Closed-Loop Integrated Phase Noise	Loop BW = 200kHz, integrate phase noise from 1kHz to 10MHz		-35		dBc
Charge-Pump Output Current			0.8		mA
Spur Level	f_{OFFSET} = 0 to 19MHz		-42		dBc
	f_{OFFSET} = 40MHz		-66		
Reference Frequency			40		MHz
Reference Frequency Input Levels	AC-coupled to XTAL pin	800			mV_{P-P}
Maximum Crystal Motional Resistance			50		Ω
Crystal Capacitance Tuning Range	Base-to-ground capacitance		30		pF
Crystal Capacitance Tuning Step			140		fF
CLKOUT Signal Level	10pF load capacitance	V_{CC} - 0.8	V_{CC} - 0.1		V_{P-P}
CLKOUT2 Signal Level	4pF load capacitance		0.3		V_{P-P}

AC Electrical Characteristics—Miscellaneous Blocks

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA POWER-DETECTOR MUX						
Output Voltage Drop	V_{IN} = 2.0V, load resistance = 10kΩ to ground			15	32	mV
PA ON/OFF CONTROL						
$V_{CC\_PA\_BIAS}$ Input Voltage Range			3.1		3.6	V
$V_{CC\_PA\_BIAS}$ Supply Current	With 10mA load at PA_BIAS			10.5		mA
Output High Level	10mA load current, Main address 11 D[7:5] = 011			2.8		V
Output Low Level	1mA load current, Main address 11 D[7:5] = 011			25		mV
Turn-On Time	Measured from $\overline{CS}$ rising edge			0.3		µs
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Readout at DOUT pin through Main address 3 D[4:0]	T_A = +25°C		13		
		T_A = +85°C		22		
		T_A = -25°C		2		

AC Electrical Characteristics—Timing

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO freq = 5.35GHz.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING						
Shutdown Time				2		µs
Maximum Channel Switching Time		Loop bandwidth = 200kHz, settling to within ±1kHz from steady state		2		ms
Maximum Channel Switching Time with Preselected VCO Sub-Band		Loop bandwidth = 200kHz, settling to within ±1kHz from steady state		56		µs
Rx/Tx Turnaround Time		Measured from $\overline{CS}$ rising edge: Rx to Tx mode, Tx gain settles to within 0.2dB of steady state		2		µs
		Measured from $\overline{CS}$ rising edge: Tx to Rx mode with RXHP = 1, Rx gain settles to within 0.5dB of steady state		2		
Tx Turn-On Time (from Standby Mode)		Measured from $\overline{CS}$ rising edge, Tx gain settles to within 0.2dB of steady state		2		µs
Tx Turn-Off Time (to Standby Mode)		From $\overline{CS}$ rising edge		0.1		µs
Rx Turn-On Time (from Standby Mode)		Measured from $\overline{CS}$ rising edge, Rx gain settles to within 0.5dB of steady state		2		µs
Rx Turn-Off Time (to Standby Mode)		From $\overline{CS}$ rising edge		0.1		µs

AC Electrical Characteristics—Timing (continued)

(Operating conditions unless otherwise specified: V_{CC} = 2.7V to 3.6V, T_A = -25°C to +85°C, freq = 5.35GHz. Reference freq = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO freq = 5.35GHz.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
4-WIRE SERIAL INTERFACE TIMING (Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			50		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}			6		ns
SCLK Frequency	f_{CLK}				40	MHz
Rise Time	t_R			2.5		ns
Fall Time	t_F			2.5		ns

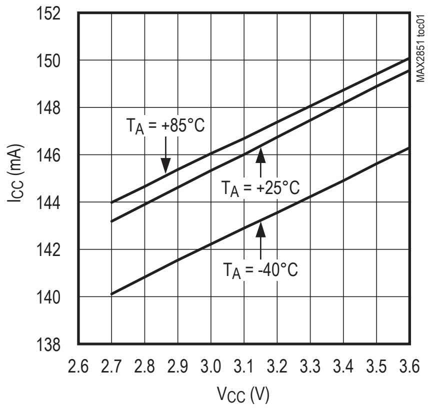
Note 1: The MAX2851 is production tested at T_A = +25°C, minimum/maximum limits at T_A = +25°C are guaranteed by test unless otherwise specified. Minimum/maximum limits at T_A = -25°C and +85°C are guaranteed by design and characterization. There is no power-on register settings self-reset; recommended register settings must be loaded after V_{CC} is applied.
Note 2: Minimum/maximum limit is guaranteed by design and characterization.
Note 3: It is currently not recommended and not tested. For test coverage support, contact manufacturer.
Note 4: For optimal Rx and Tx quadrature accuracy over temperature, the user can utilize the Rx calibration and Tx calibration circuit to assist quadrature calibration.

Typical Operating Characteristics

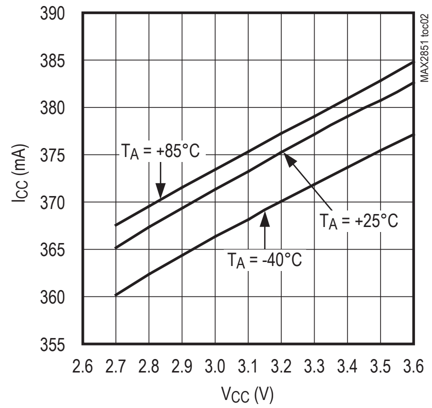
(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

RECEIVER

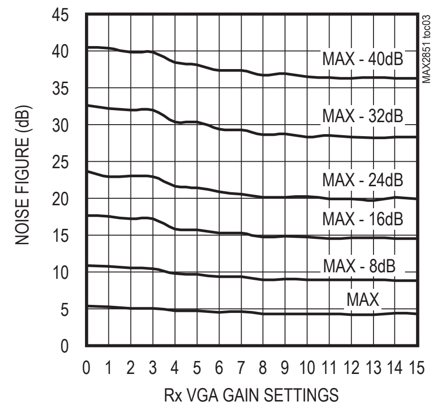
Rx MODE SINGLE-CHANNEL SUPPLY CURRENT



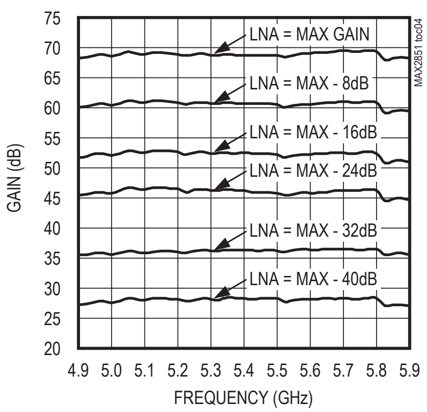
Rx MODE 5-CHANNEL SUPPLY CURRENT



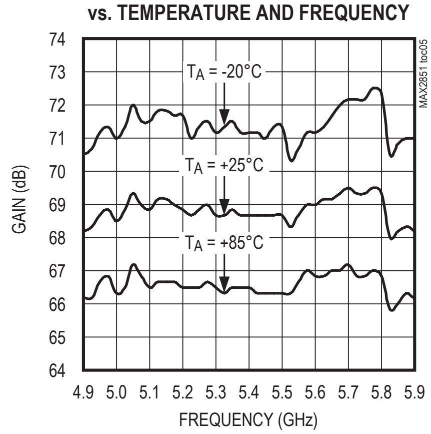
Rx NOISE FIGURE vs. VGA GAIN SETTINGS (BALUN INPUT REFERRED)



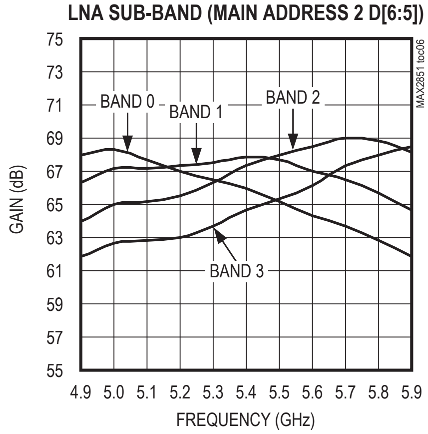
Rx3 MAXIMUM GAIN vs. FREQUENCY



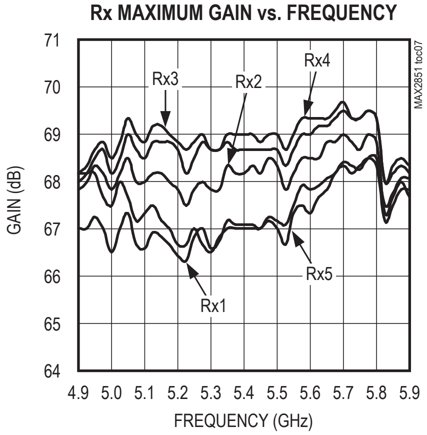
Rx3 MAXIMUM GAIN vs. TEMPERATURE AND FREQUENCY



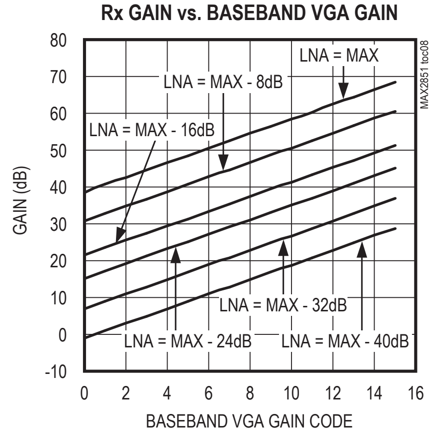
Rx2 MAXIMUM GAIN WITH FIXED LNA SUB-BAND (MAIN ADDRESS 2 D[6:5])



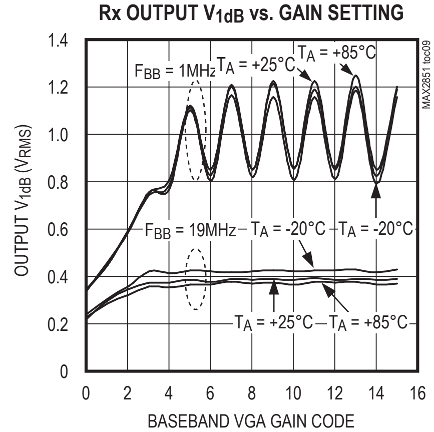
Rx MAXIMUM GAIN vs. FREQUENCY



Rx GAIN vs. BASEBAND VGA GAIN



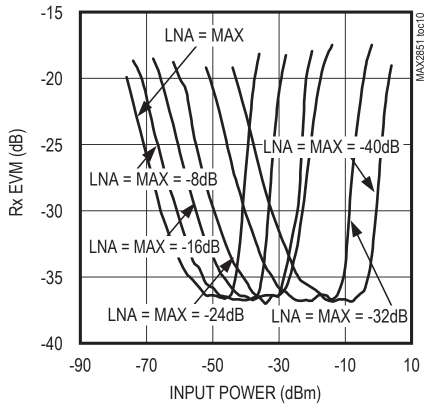
Rx OUTPUT V_{1dB} vs. GAIN SETTING



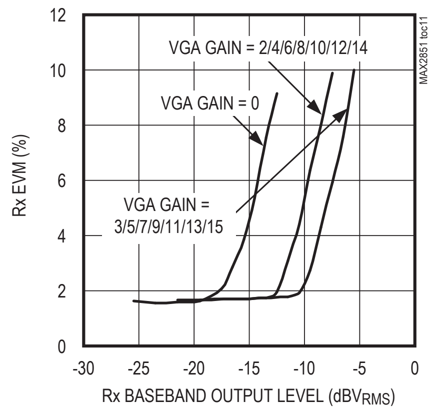
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

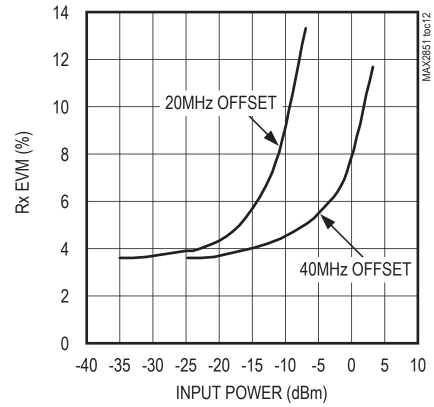
Rx EVM vs. INPUT POWER (CHANNEL BANDWIDTH = 20MHz)



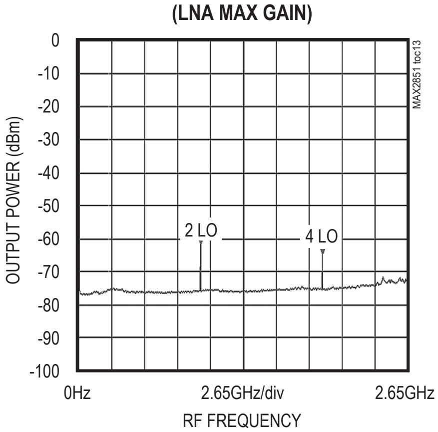
Rx EVM vs. Rx BASEBAND OUTPUT LEVEL



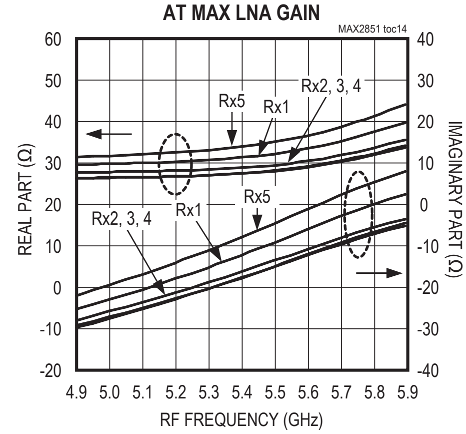
Rx EVM vs. OFDM JAMMER POWER AT 20MHz AND 40MHz OFFSET FREQUENCY WITH WANTED SIGNAL AT -66dBm



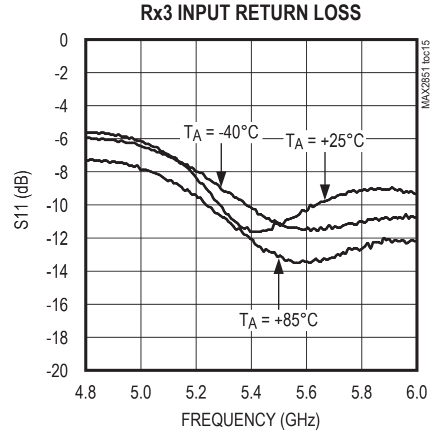
Rx4 EMISSION SPECTRUM AT LNA INPUT (LNA MAX GAIN)



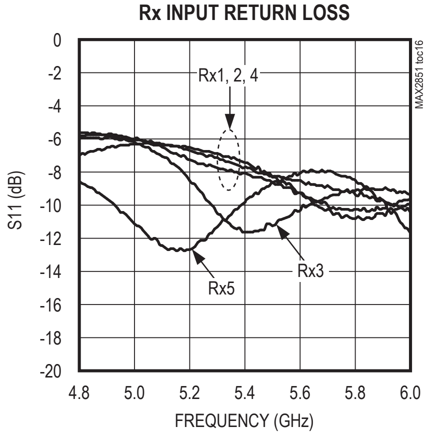
Rx INPUT IMPEDANCE AT MAX LNA GAIN



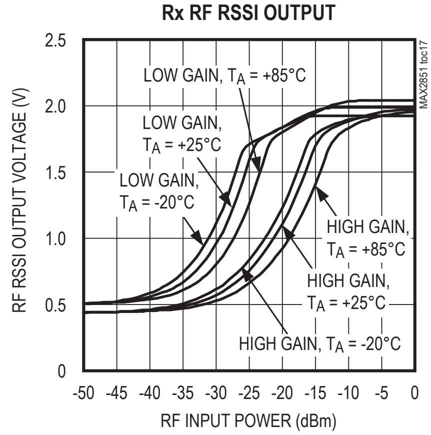
Rx3 INPUT RETURN LOSS



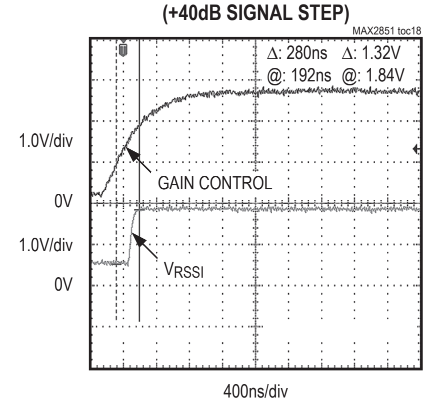
Rx INPUT RETURN LOSS



Rx RF RSSI OUTPUT



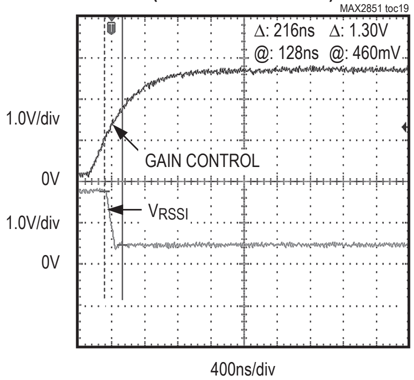
Rx RF RSSI ATTACK TIME (+40dB SIGNAL STEP)



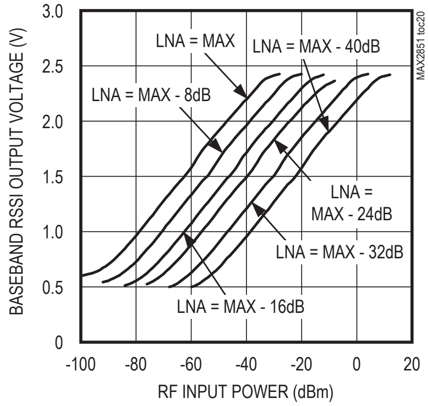
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

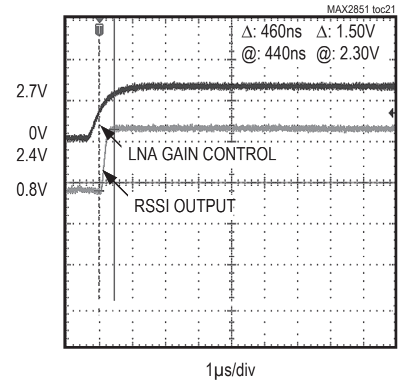
Rx RF RSSI DELAY TIME (-40dB SIGNAL STEP)



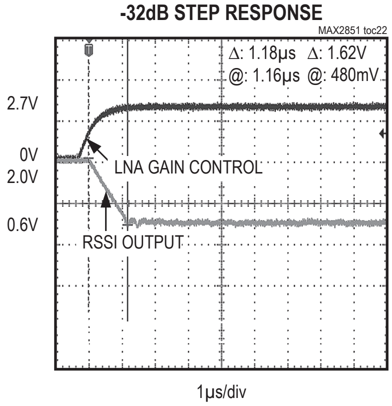
BASEBAND RSSI VOLTAGE vs. INPUT POWER



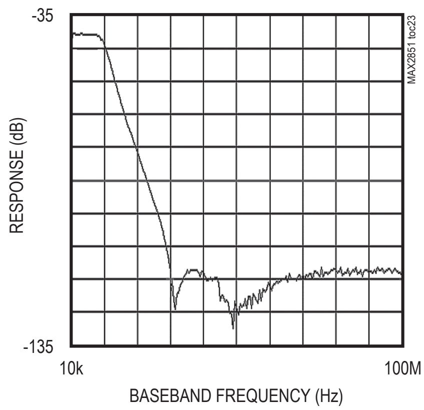
Rx BASEBAND RSSI +40dB STEP RESPONSE



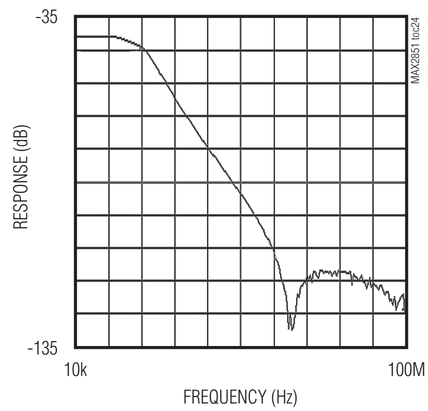
Rx BASEBAND RSSI -32dB STEP RESPONSE



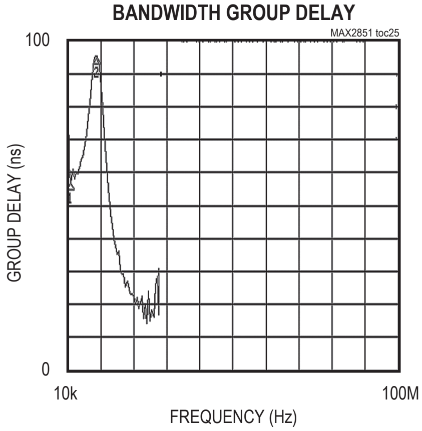
Rx LPF 20MHz CHANNEL BANDWIDTH RESPONSE



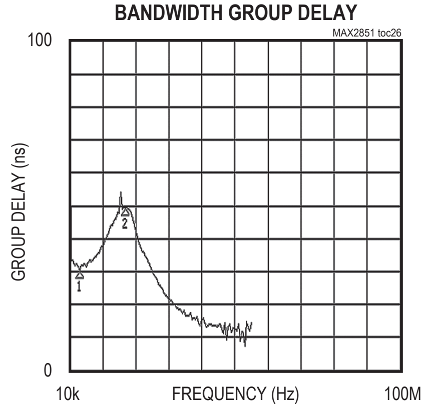
Rx LPF 40MHz CHANNEL BANDWIDTH RESPONSE



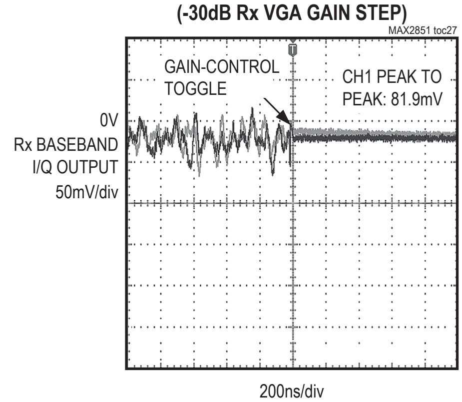
Rx LPF 20MHz CHANNEL BANDWIDTH GROUP DELAY



Rx LPF 40MHz CHANNEL BANDWIDTH GROUP DELAY



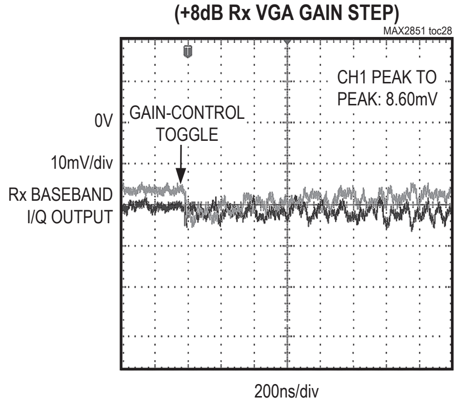
Rx DC OFFSET SETTLING RESPONSE (-30dB Rx VGA GAIN STEP)



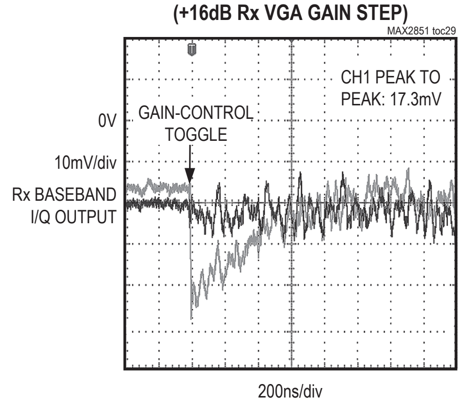
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

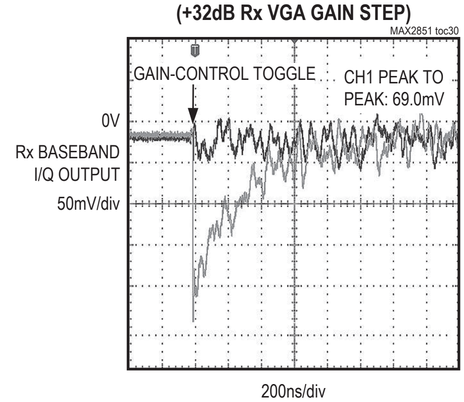
Rx DC OFFSET SETTLING RESPONSE (+8dB Rx VGA GAIN STEP)



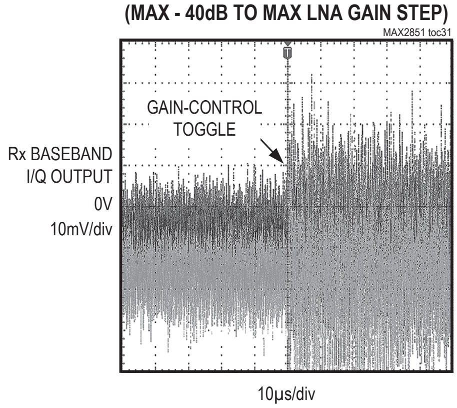
Rx DC OFFSET SETTLING RESPONSE (+16dB Rx VGA GAIN STEP)



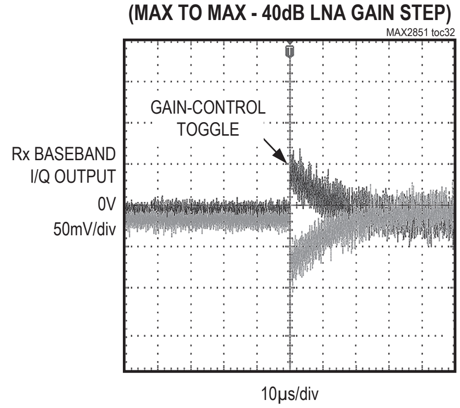
Rx DC OFFSET SETTLING RESPONSE (+32dB Rx VGA GAIN STEP)



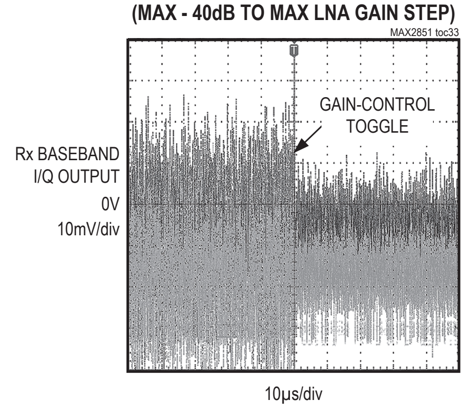
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 1 (MAX - 40dB TO MAX LNA GAIN STEP)



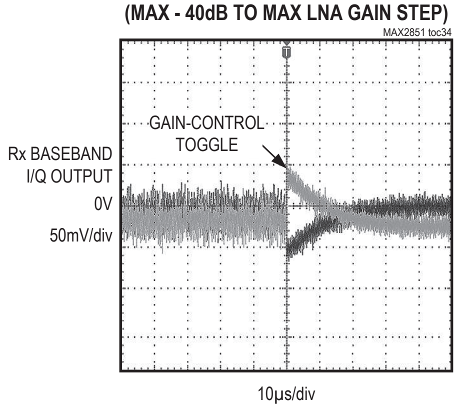
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 0 (MAX TO MAX - 40dB LNA GAIN STEP)



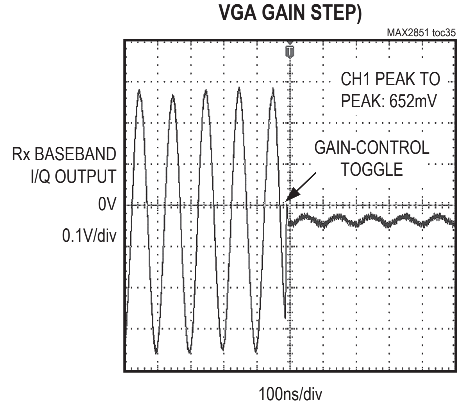
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 1 (MAX - 40dB TO MAX LNA GAIN STEP)



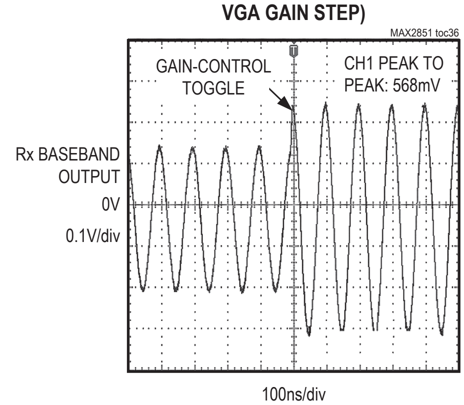
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 0 (MAX - 40dB TO MAX LNA GAIN STEP)



Rx BASEBAND VGA SETTLING RESPONSE (-30dB BASEBAND VGA GAIN STEP)



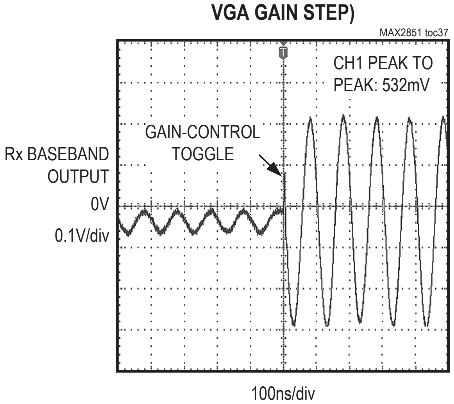
Rx BASEBAND VGA SETTLING RESPONSE (+4dB BASEBAND VGA GAIN STEP)



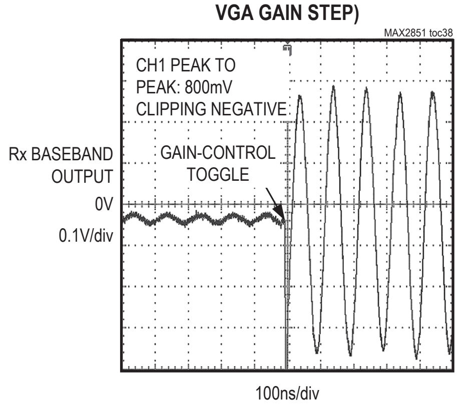
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

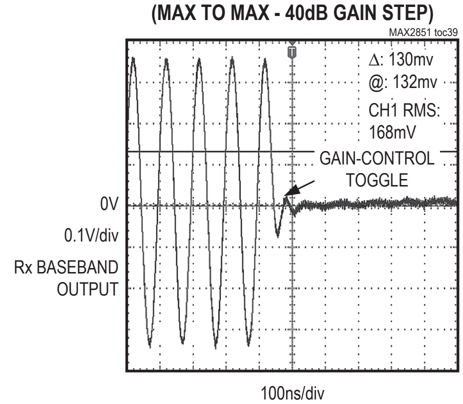
Rx BASEBAND VGA SETTLING RESPONSE (+16dB BASEBAND VGA GAIN STEP)



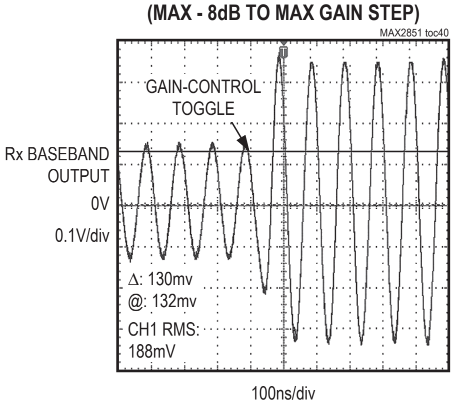
Rx BASEBAND VGA SETTLING RESPONSE (+30dB BASEBAND VGA GAIN STEP)



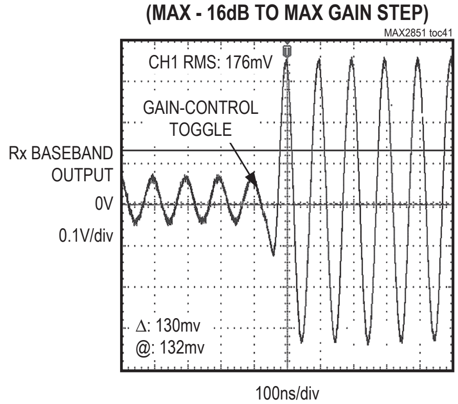
Rx LNA SETTLING RESPONSE (MAX TO MAX - 40dB GAIN STEP)



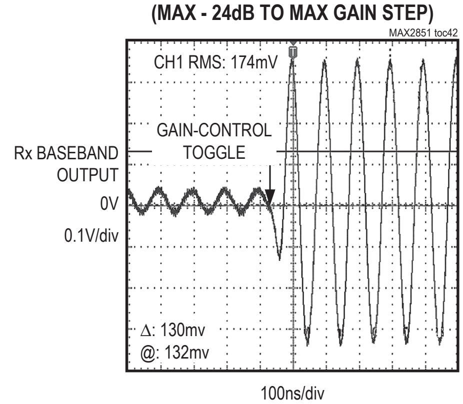
Rx LNA SETTLING RESPONSE (MAX - 8dB TO MAX GAIN STEP)



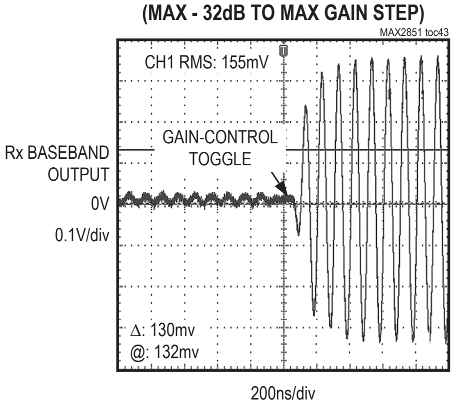
Rx LNA SETTLING RESPONSE (MAX - 16dB TO MAX GAIN STEP)



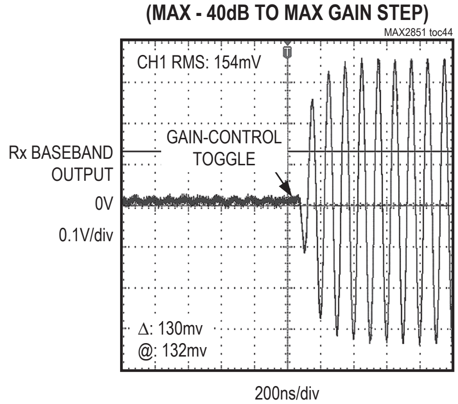
Rx LNA SETTLING RESPONSE (MAX - 24dB TO MAX GAIN STEP)



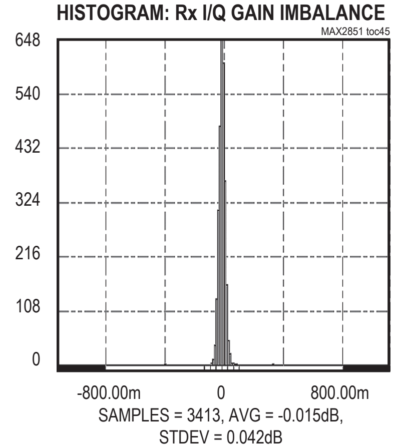
Rx LNA SETTLING RESPONSE (MAX - 32dB TO MAX GAIN STEP)



Rx LNA SETTLING RESPONSE (MAX - 40dB TO MAX GAIN STEP)

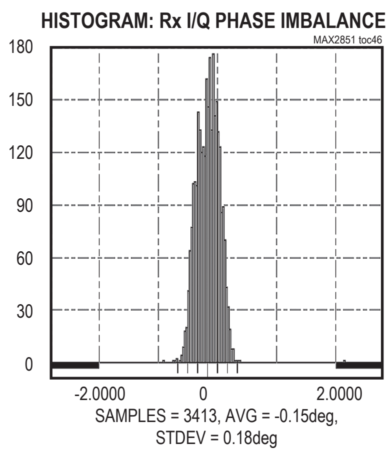


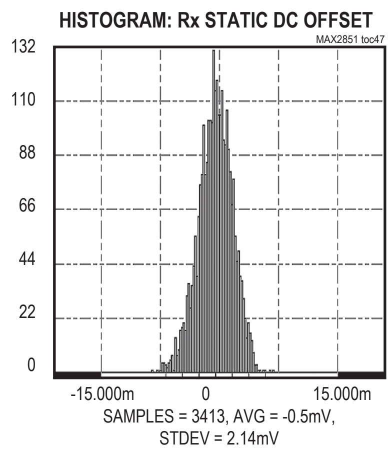
HISTOGRAM: Rx I/Q GAIN IMBALANCE

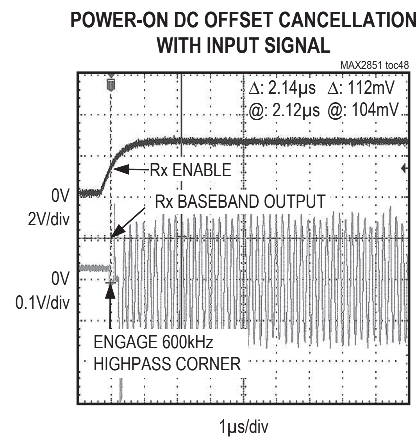


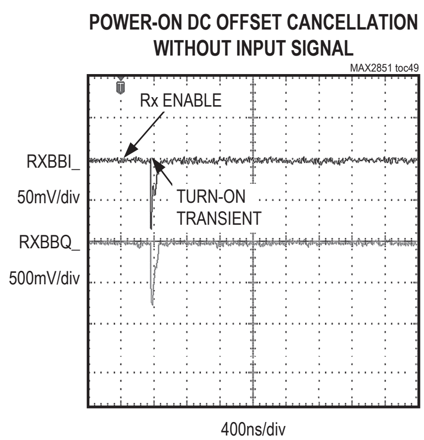
Typical Operating Characteristics (continued)

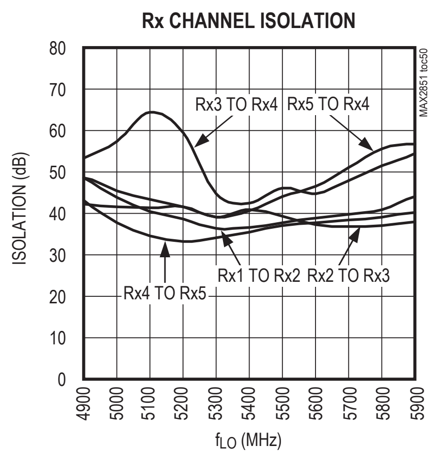
(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)









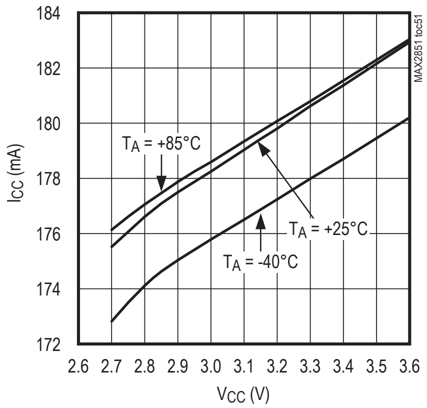


Typical Operating Characteristics (continued)

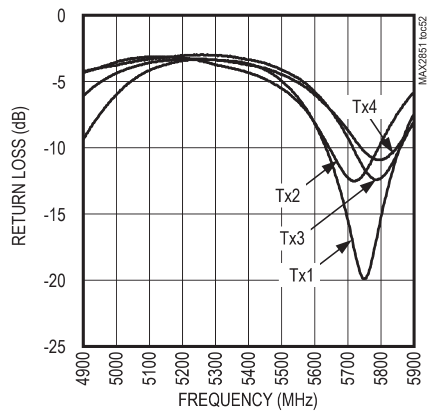
(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

TRANSMITTER

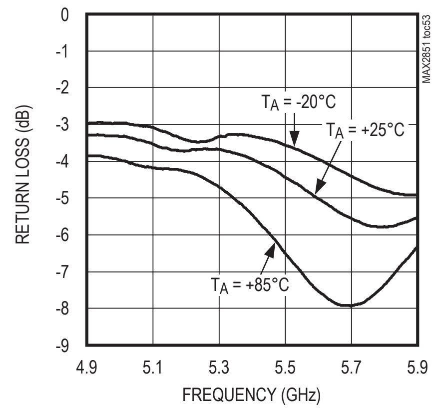
Tx MODE SUPPLY CURRENT



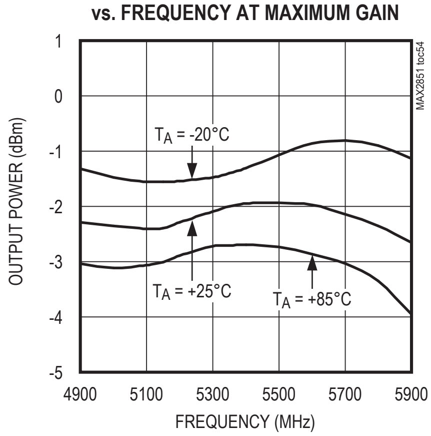
OUTPUT RETURN LOSS AT T_A = +25°C vs. Tx CHANNELS



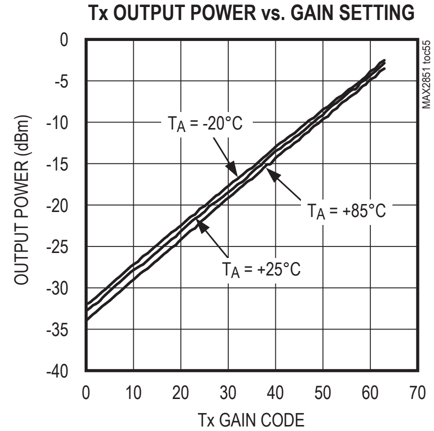
Tx OUTPUT RETURN LOSS vs. FREQUENCY



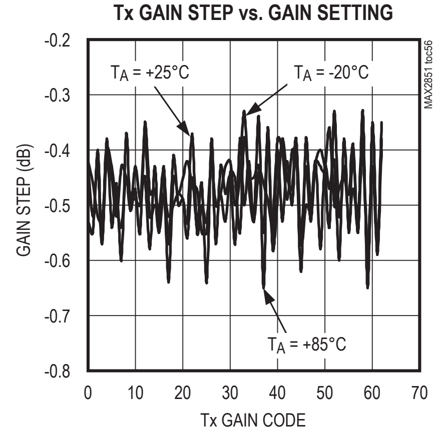
Tx OUTPUT POWER vs. FREQUENCY AT MAXIMUM GAIN



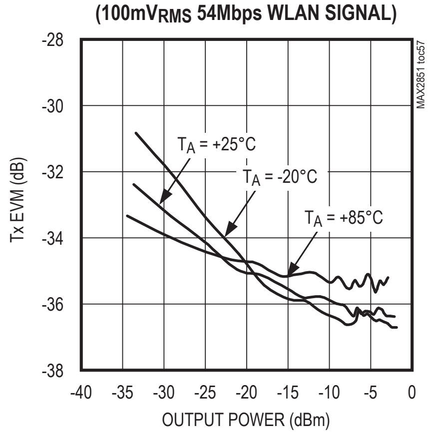
Tx OUTPUT POWER vs. GAIN SETTING



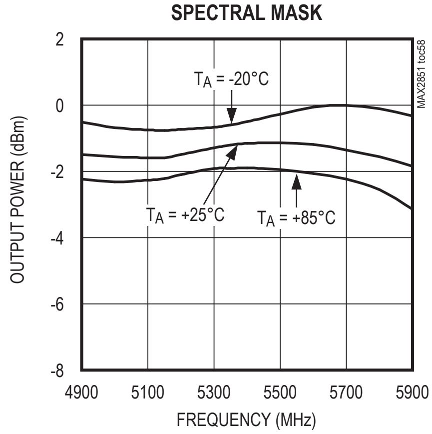
Tx GAIN STEP vs. GAIN SETTING



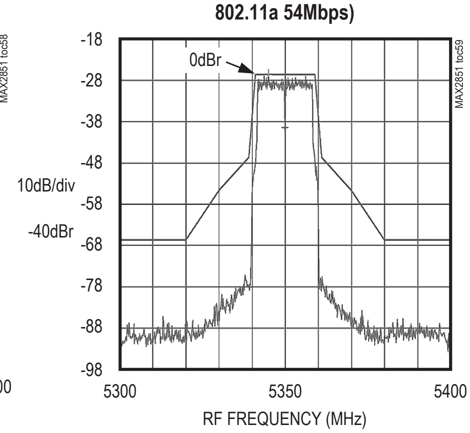
Tx EVM vs. OUTPUT POWER (100mV_{RMS} 54Mbps WLAN SIGNAL)



Tx MAX OUTPUT POWER MEETING -33dBc EVM AND 802.11a SPECTRAL MASK

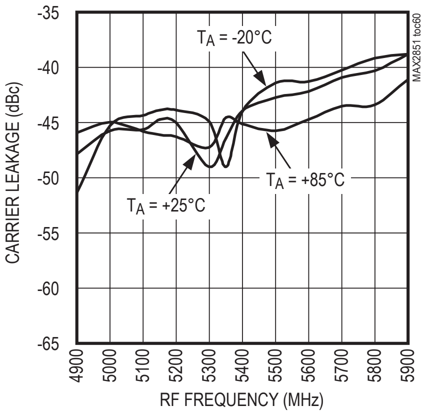


Tx2 OUTPUT SPECTRUM AT -5dBM (20MHz CHANNEL BANDWIDTH, 802.11a 54Mbps)

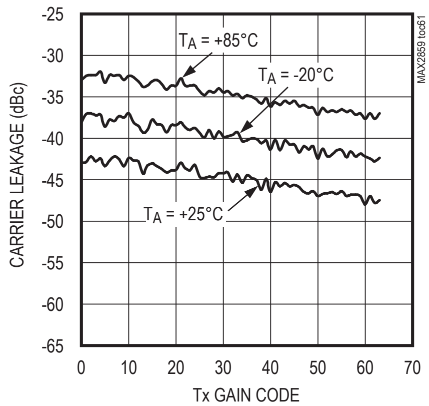


Typical Operating Characteristics (continued)

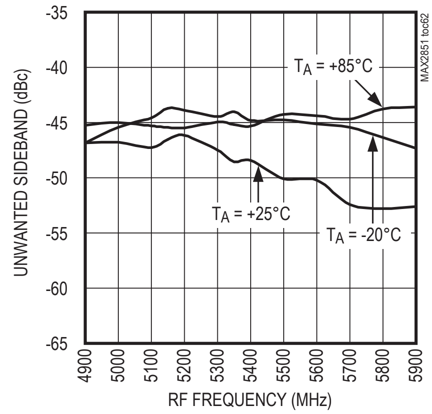
(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)



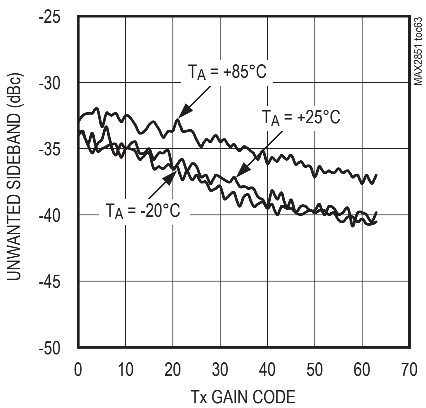
Tx CARRIER LEAKAGE vs. RF FREQUENCY



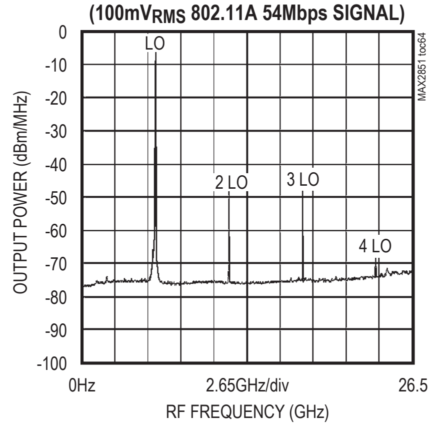
Tx CARRIER LEAKAGE vs. GAIN SETTING



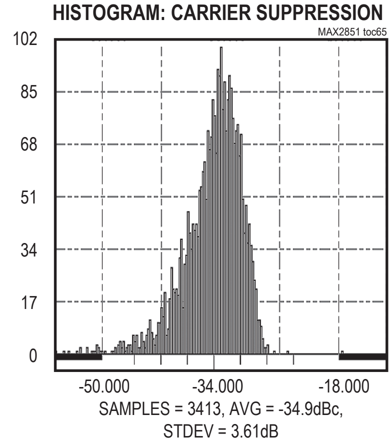
Tx UNWANTED SIDEBAND vs. RF FREQUENCY



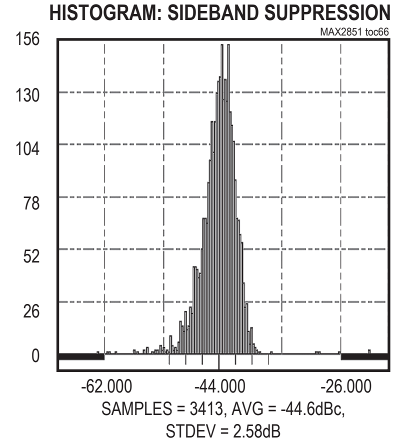
Tx UNWANTED SIDEBAND vs. GAIN SETTING



Tx6 OUTPUT EMISSION SPECTRUM AT MAX GAIN AND COLD (100mV$_{RMS}$ 802.11A 54Mbps SIGNAL)



HISTOGRAM: CARRIER SUPPRESSION



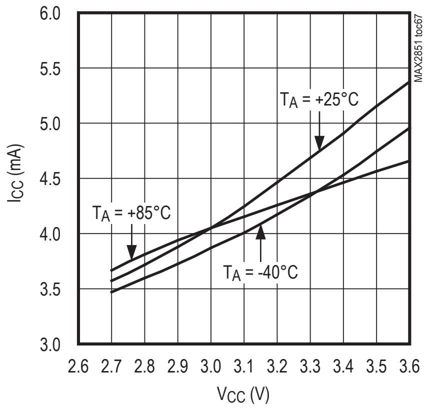
HISTOGRAM: SIDEBAND SUPPRESSION

Typical Operating Characteristics (continued)

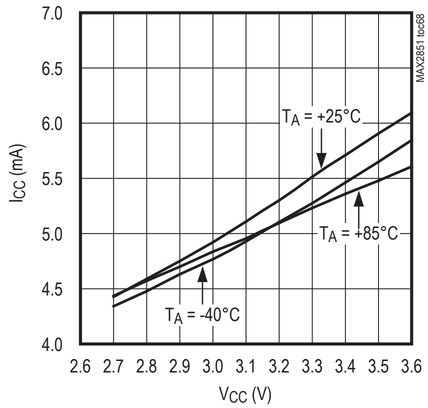
(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

SYNTHESIZER

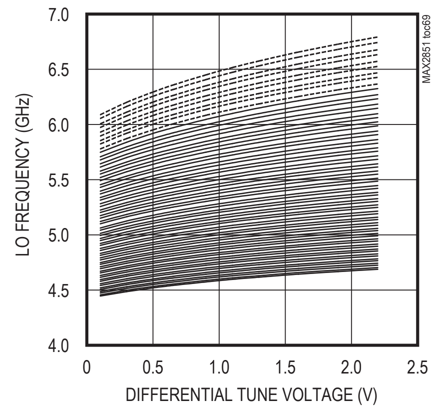
CLKOUT MODE SUPPLY CURRENT



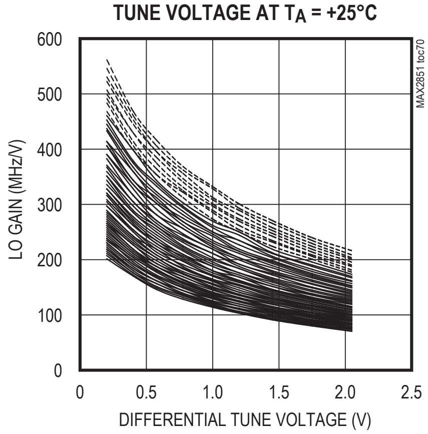
CLKOUT2 MODE SUPPLY CURRENT



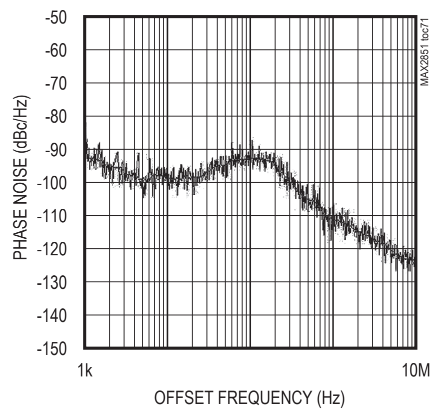
LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE AT T_A = +25°C



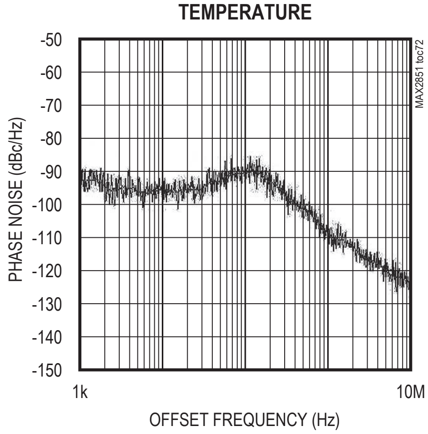
LO GAIN vs. DIFFERENTIAL TUNE VOLTAGE AT T_A = +25°C



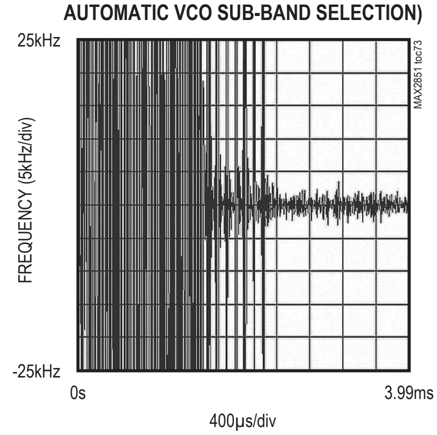
LO PHASE NOISE AT 5350MHz AND ROOM TEMPERATURE



LO PHASE NOISE AT 5900MHz AND HOT TEMPERATURE



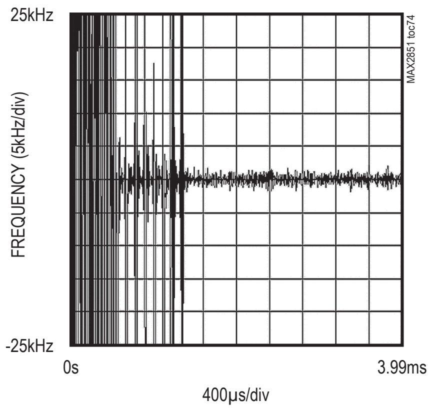
CHANNEL SWITCHING FREQUENCY SETTLING (4900MHz TO 5900MHz, AUTOMATIC VCO SUB-BAND SELECTION)



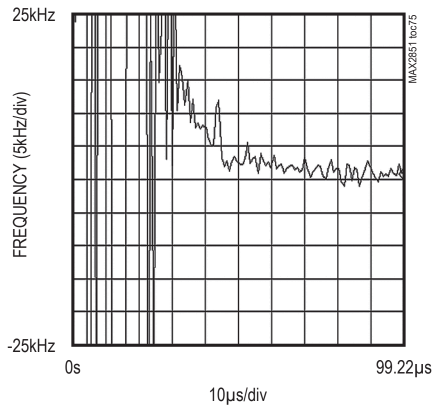
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, T_A = +25°C, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2851 Evaluation Kit, unless otherwise noted.)

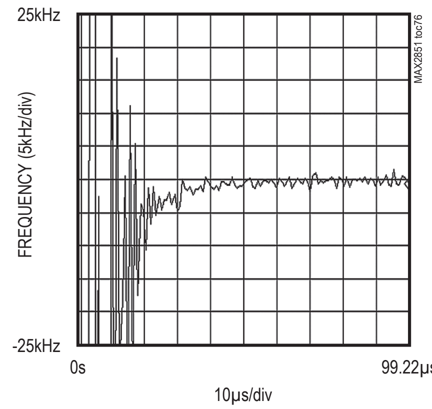
CHANNEL SWITCHING FREQUENCY SETTLING (5900MHz TO 4900MHz, AUTOMATIC VCO SUB-BAND SELECTION)



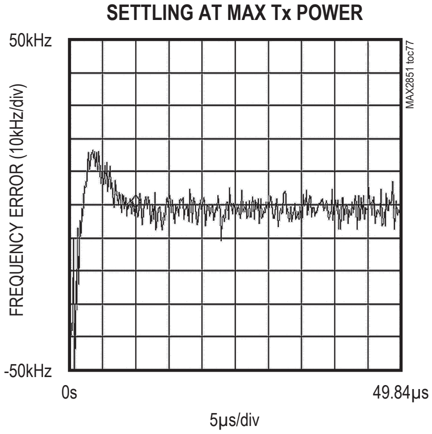
CHANNEL SWITCHING FREQUENCY SETTLING (4900MHz TO 5900MHz, MANUAL VCO SUB-BAND SELECTION)



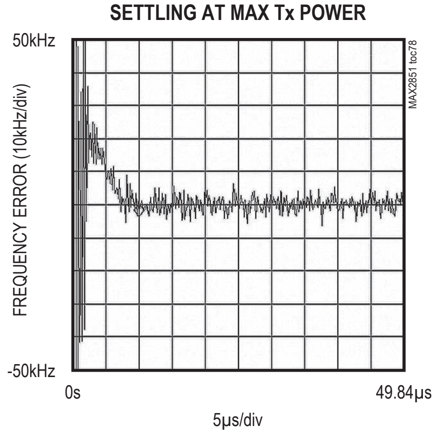
CHANNEL SWITCHING FREQUENCY SETTLING (5900MHz TO 4900MHz, MANUAL VCO SUB-BAND SELECTION)



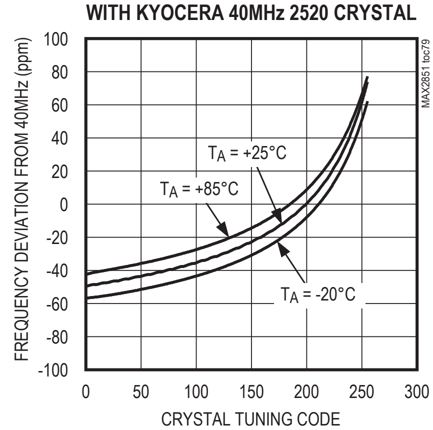
Tx-TO-Rx TURNAROUND FREQUENCY SETTLING AT MAX Tx POWER



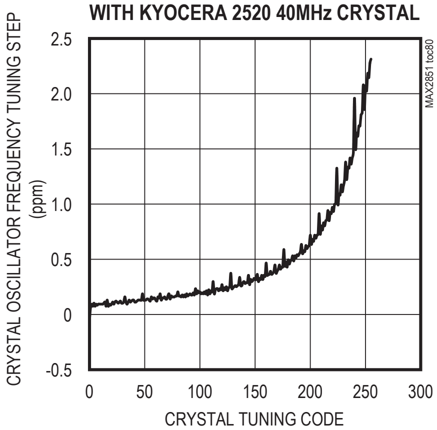
Rx-TO-Tx TURNAROUND FREQUENCY SETTLING AT MAX Tx POWER



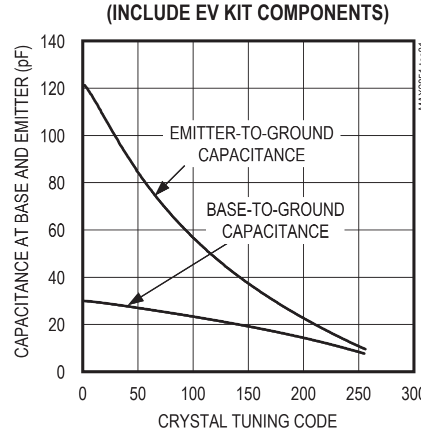
CRYSTAL OSCILLATOR TUNING RANGE WITH KYOCERA 40MHz 2520 CRYSTAL



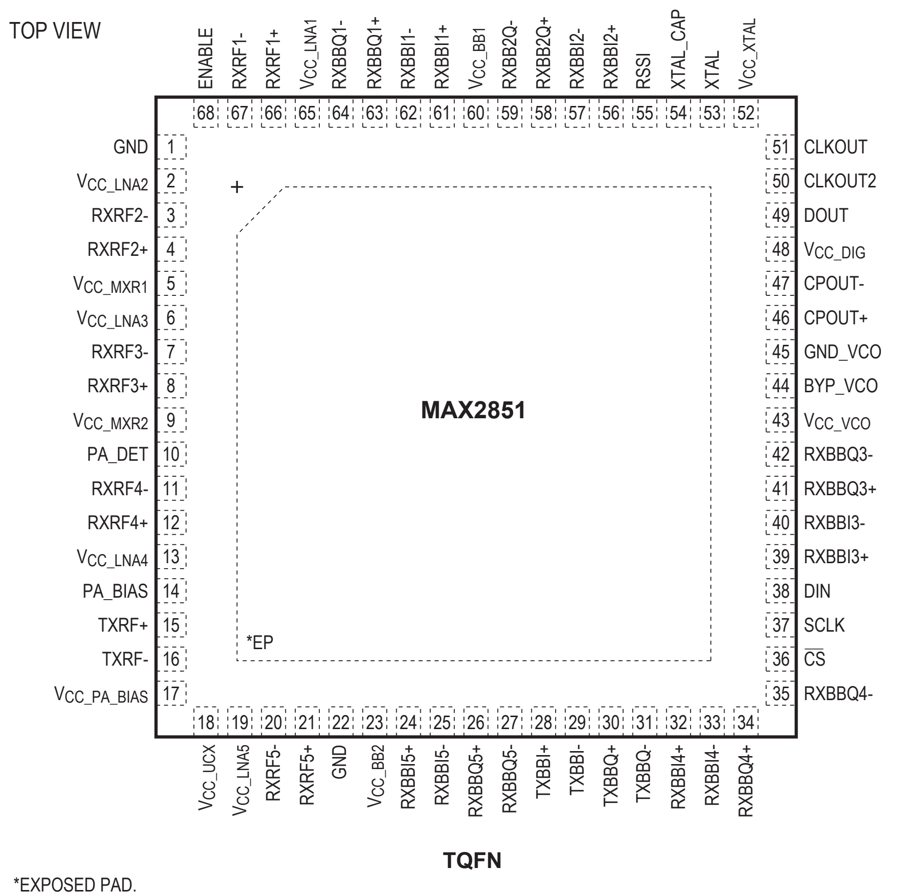
CRYSTAL OSCILLATOR TUNING STEP WITH KYOCERA 2520 40MHz CRYSTAL



CRYSTAL OSCILLATOR TUNING CAPACITANCE AT BASE AND EMITTER (INCLUDE EV KIT COMPONENTS)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 22	GND	Ground
2	V_{CC_LNA2}	Receiver 2 LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
3	RXRF2-	Receiver 2 LNA Differential Input. Input is DC-coupled and biased internally at 1.2V.
4	RXRF2+	
5	V_{CC_MXR1}	Receiver Downconverter Supply Voltage 1. Bypass with a capacitor as close as possible to the pin.
6	V_{CC_LNA3}	Receiver 3 LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
7	RXRF3-	Receiver 3 LNA Differential Input. Input is DC-coupled and biased internally at 1.2V.
8	RXRF3+	
9	V_{CC_MXR2}	Receiver Downconverter Supply Voltage 2. Bypass with a capacitor as close as possible to the pin.
10	PA_DET	External Power-Amplifier Detector Mux Input
11	RXRF4-	Receiver 4 LNA Differential Input. Input is DC-coupled and biased internally at 1.2V.
12	RXRF4+	
13	V_{CC_LNA4}	Receiver 4 LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
14	PA_BIAS	External Power-Amplifier Voltage Bias Output
15	TXRF+	Transmitter Differential Output. These pins are in open-collector configuration. These pins should be biased at the supply voltage with differential impedance terminated at 300Ω.
16	TXRF-	
17	$V_{CC\_PA\_BIAS}$	External Power-Amplifier Voltage Bias and Detector Mux Supply Voltage. Bypass with a capacitor as close as possible to the pin.
18	V_{CC_UCX}	Transmitter Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
19	V_{CC_LNA5}	Receiver 5 LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
20	RXRF5-	Receiver 5 LNA Differential Input. Input is DC-coupled and biased internally at 1.2V.
21	RXRF5+	
23	V_{CC_BB2}	Receiver Baseband Supply Voltage 2. Bypass with a capacitor as close as possible to the pin.
24	RXBBI5+	Receiver 5 Baseband I-Channel Differential Output
25	RXBBI5-	
26	RXBBQ5+	Receiver 5 Baseband Q-Channel Differential Output
27	RXBBQ5-	
28	TXBBI+	Transmitter Baseband I-Channel Differential Input
29	TXBBI-	
30	TXBBQ+	Transmitter Baseband Q-Channel Differential Input
31	TXBBQ-	
32	RXBBI4+	Receiver 4 Baseband I-Channel Differential Output
33	RXBBI4-	
34	RXBBQ4+	Receiver 4 Baseband Q-Channel Differential Output
35	RXBBQ4-	
36	$\overline{CS}$	Active-Low Chip-Select Logic Input of 4-Wire Serial Interface
37	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface
38	DIN	Data Logic Input of 4-Wire Serial Interface
39	RXBBI3+	Receiver 3 Baseband I-Channel Differential Output
40	RXBBI3-	

Pin Description (continued)

PIN	NAME	FUNCTION
41	RXBBQ3+	Receiver 3 Baseband Q-Channel Differential Output
42	RXBBQ3-	
43	V_{CC_VCO}	VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin.
44	BYP_VCO	On-Chip VCO Regulator Output Bypass. Bypass with an external 1µF capacitor to GND_VCO with minimum PCB trace. Do **not** connect other circuitry to this pin.
45	GND_VCO	VCO Ground
46	CPOUT+	Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*).
47	CPOUT-	
48	V_{CC_DIG}	Digital Block Supply Voltage. Bypass with a capacitor as close as possible to the pin.
49	DOUT	Data Logic Output of 4-Wire Serial Interface
50	CLKOUT2	Reference Clock Buffer Output 2
51	CLKOUT	Reference Clock Buffer Output
52	V_{CC_XTAL}	Crystal Oscillator Supply Voltage. Bypass with a capacitor as close as possible to the pin.
53	XTAL	Crystal Oscillator Base Input. AC-couple crystal unit to this pin.
54	XTAL_CAP	Crystal Oscillator Emitter Node
55	RSSI	Receiver Signal Strength Indicator Output
56	RXBBI2+	Receiver 2 Baseband I-Channel Differential Output
57	RXBBI2-	
58	RXBBQ2+	Receiver 2 Baseband Q-Channel Differential Output
59	RXBBQ2-	
60	V_{CC_BB1}	Receiver Baseband Supply Voltage 1. Bypass with a capacitor as close as possible to the pin.
61	RXBBI1+	Receiver 1 Baseband I-Channel Differential Output
62	RXBBI1-	
63	RXBBQ1+	Receiver 1 Baseband Q-Channel Differential Output
64	RXBBQ1-	
65	V_{CC_LNA1}	Receiver 1 LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
66	RXRF1+	Receiver 1 LNA Differential Input. Input is DC-coupled and biased internally at 1.2V.
67	RXRF1-	
68	ENABLE	Enable Logic Input
—	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Table 1. Operating Modes

MODE	MODE CONTROL LOGIC INPUTS		CIRCUIT BLOCK STATES				
	ENABLE PIN	SPI MAIN ADDRESS 0, D[4:2]	Rx PATH	Tx PATH (NOTE 1)	LO PATH	CLKOUT (NOTES 2, 3)	CALIBRATION SECTIONS ON
SHUTDOWN	0	XXX	Off	Off	Off	Off	None
CLOCKOUT	1	000	Off	Off	Off	On	None
STANDBY	1	001	Off	Off	On	On	None
Rx	1	010	On	Off	On	On	None
Tx	1	011	Off	On	On	On	None
Tx CALIBRATION	1	100	Off	On	On	On	AM detector + Rx5 I/Q buffers
RF LOOPBACK	1	101	On (except LNA)	On	On	On	RF loopback
BASEBAND LOOPBACK	1	11X	On (except RXRF)	Off	On	On	Tx baseband buffer

Note 1: PA_BIAS pin can be kept active in nontransmit mode(s) by SPI programming.
Note 2: CLKOUT signal is active independent of SPI, and is only dependent on the ENABLE pin.
Note 3: CLKOUT2 signal can be enabled/disabled through SPI in all operating modes except shutdown mode.

Detailed Description

Modes of Operation

The MAX2851 modes of operation are shutdown, clock-out, standby, receive, transmit, transmitter calibration, RF loopback, and baseband loopback. See Table 1 for a summary of the modes of operation. The logic input pin ENABLE (pin 68) and SPI Main address 0 D[4:2] control the various modes.

Shutdown Mode

The MAX2851 features a low-power shutdown mode. All circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers.

Clockout Mode

In clockout mode, only the crystal oscillator signal is active at the CLKOUT pin. The rest of the transceiver is powered down.

Standby Mode

In standby mode, PLL, VCO, and LO generation are on. Tx or Rx modes can be quickly enabled from this mode. Other blocks can be selectively enabled in this mode

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. The antenna signal is applied; RF is down-converted, filtered, and buffered at the RXBB I and Q outputs.

Transmit (Tx) Mode

In transmit mode, all Tx circuit blocks are powered on and active. The external PA can be powered on through the PA_BIAS pin after a programmable delay.

Transmit Calibration Mode

In transmit calibration mode, all Tx circuit blocks are powered on and active. The AM detector and receiver I/Q channel buffers are also on. Output signals are routed to RXBB I and Q outputs.

The AM detector multiplies the Tx RF output signal with itself. The self-mixing product of the wanted sideband becomes DC voltage and is filtered on-chip. The mixing product between wanted sideband and the carrier leakage forms Ftone at the Rx baseband output. The mixing product between the wanted sideband and the unwanted sideband forms 2Ftone at the Rx baseband output.

As the Tx RF output is self-mixed at the AM detector, the AM detector output responds differently to different gain settings and power levels. When the Tx RF output power changes by 1dB through Tx gain control, the AM detector output changes by 2dB as both the wanted sideband and carrier leakage (or unwanted sideband) change by 1dB. When Tx RF output carrier leakage (or unwanted sideband) changes by 1dB while the wanted sideband output power is constant, the AM detector output changes by 1dB only.

RF Loopback Mode

In RF loopback mode, part of the Rx and Tx circuit blocks except the LNA are powered on and active. The transmitter I/Q input signal is upconverted to RF, and the output of the transmitter is fed to the receiver downconverter input. Output signals are delivered to all receiver baseband I/Q outputs. The I/Q lowpass filters in the transmitter signal path are bypassed.

Baseband Loopback Mode

In baseband loopback mode, part of the Rx and Tx baseband circuit blocks are powered and active. The transmitter I/Q input signal is routed to the receiver lowpass filter input. Output signals are delivered to receiver 5 baseband I/Q outputs.

Power-On Sequence

Set the ENABLE pin to V_{CC} for 2ms to start the crystal oscillator. Program all SPI addresses according to recommended values. Set SPI Main address 0 D[4:2] from 000 to 001 to engage standby mode. To lock the LO frequency, the user can set SPI in order of Main address 15, Main address 16, and then Main address 17 to trigger VCO sub-band autoacquisition; the acquisition takes 2ms. After the LO frequency is locked, set SPI Main address 0 D[4:2] = 010 and 011 for Rx and Tx operating modes, respectively. Before engaging to Rx mode, set Main address 5 D1 = 1 to allow fast DC-offset settling. After engaging to Rx mode and the Rx baseband DC offset settles, the user can set Main address 5 D1 = 0 to complete Rx DC-offset cancellation.

Programmable Registers and 4-Wire SPI Interface

The MAX2851 includes 60 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit (R/W in Figure 1). The next 5 bits are register address (A[4:0] in Figure 1). The 10 least significant bits (LSBs) are register data (D[9:0] in Figure 1). Register data is loaded through the 4-wire SPI/MICROWIRE compatible serial interface. MSB of data at the DIN pin is shifted in first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active and input data is shifted at the rising edge of the clock at the SCLK pin. At $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by the address bits. See Figure 1. To support more than a 32-register address using a 5-bit-wide address word, the bit 0 of address 0 is used to select whether the 5-bit address word is applied to the main address or local address. There is **no** power-on SPI register self-reset functionality in the MAX2851; the user must program all register values after power-up. During the read mode, register data selected by address bits is shifted out to the DOUT pin at the falling edges of the clock.

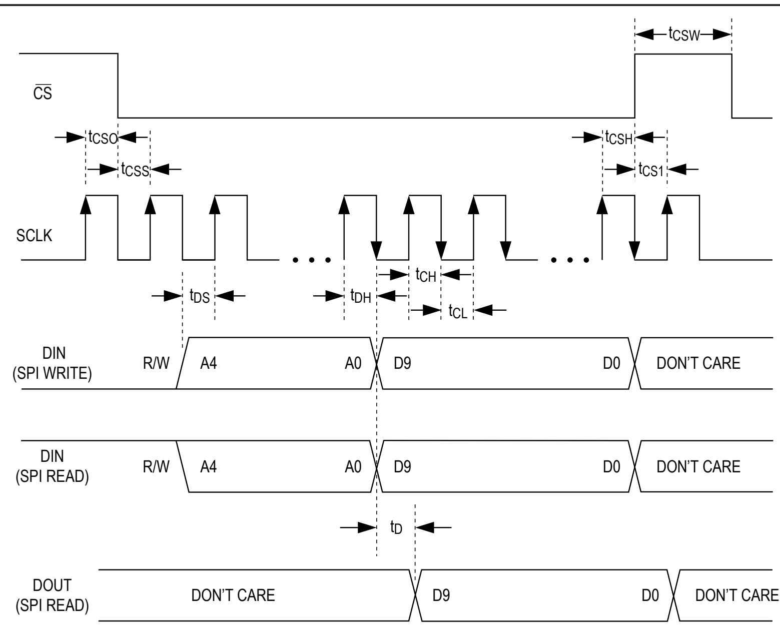


Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

SPI Register Definition

All values in the register definition table are typical numbers. The MAX2851 SPI does not have a power-on-default self-reset feature; the user must program all SPI addresses for normal operation. Prior to use of any untested settings, contact the factory.

Table 2. Register Summary

REGISTER	READ/WRITE AND ADDRESS: MAIN0_D0	READ/WRITE AND ADDRESS: A[4:0]	WRITE (W)/ READ (R)	DATA: D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main 0	0	00000	W/R	RESERVED					MODE[2:0]			RFBW	M/L_SEL
			Default	0	0	0	0	1	0	0	0	1	0
Main 1	0	00001	W/R	RESERVED		LNA_GAIN[2:0]			VGA_GAIN[4:0]				
			Default	0	0	1	1	1	1	1	1	1	1
Main 2	0	00010	W/R	RESERVED			LNA_BAND[1:0]		RESERVED				
			Default	0	1	1	0	1	0	0	0	0	0
Main 3	0	00011	W	RESERVED		TS_EN	TS_ TRIG	RESERVED	RESERVED				
			R						TS_READ[4:0]				
			Default	0	0	0	0	0	0	0	0	0	0
Main 4	0	00100	Reserved	1	1	0	0	0	1	1	1	0	0
Main 5	0	00101	W/R	RESERVED	RSSI_MUX_SEL[2:0]			RSSI_RX_SEL[2:0]			RESERVED	RXHP	RESERVED
			Default	0	0	0	0	0	0	0	0	0	0
Main 6	0	00110	W/R	RX_GAIN_PROG_SEL[5:1]					E_RX[5:1]				
			Reserved	1	1	1	1	1	1	1	1	1	1
Main 7	0	00111	Reserved	0	0	0	0	1	0	0	1	0	0
Main 8	0	01000	W/R	0	0	0	0	0	0	0	0	0	0
Main 9	0	01001	W/R	TX_GAIN[5:0]						RESERVED			
			Default	0	0	0	0	0	0	1	1	1	1
Main 10	0	01010	Reserved	0	0	0	0	0	0	0	0	0	0
Main 11	0	01011	W/R	RESERVED									
			Default	0	0	0	1	1	0	0	0	0	0
Main 13	0	01101	Reserved	0	0	0	0	0	0	0	0	0	0
Main 14	0	01110	W/R	E_CLKOUT2	RESERVED							DOUT_SEL	RESERVED
			Default	1	1	0	1	1	0	0	0	0	0
Main 15	0	01111	W/R	VAS_ TRIG_EN	RESERVED		SYN_CONFIG_N[6:0]						
			Default	1	0	0	1	0	0	0	0	1	0
Main 16	0	10000	W/R	SYN_CONFIG_F[19:10]									
			Default	1	1	1	0	0	0	0	0	0	0
Main 17	0	10001	W/R	SYN_CONFIG_F[9:0]									
			Default	0	0	0	0	0	0	0	0	0	0
Main 18	0	10010	W/R	RESERVED		XTAL_TUNE[7:0]							
			Default	0	0	1	0	0	0	0	0	0	0