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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ultra-Low-Power, Single-Channel Integrated Biopotential (ECG, R-to-R, and Pace Detection) and Bioimpedance (BioZ) AFE

General Description

The MAX30001 is a complete, biopotential and bioimpedance (BioZ), analog front-end (AFE) solution for wearable applications. It offers high performance for clinical and fitness applications, with ultra-low power for long battery life. The MAX30001 is a single biopotential channel providing electrocardiogram (ECG) waveforms, heart rate and pacemaker edge detection, and a single bioimpedance channel capable of measuring respiration.

The biopotential and bioimpedance channels have ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low-power, leads-on detection during standby mode, and extensive calibration voltages for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes. Both channels also have high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high resolution analog-to-digital converter. The biopotential channel is DC coupled, can handle large electrode voltage offsets, and has a fast recovery mode to quickly recover from overdrive conditions, such as defibrillation and electro-surgery. The bioimpedance channel includes integrated programmable current drive, works with common electrodes, and has the flexibility for 2 or 4 electrode measurements. It also has AC lead off detection.

The MAX30001 is available in a 28-pin TQFN and 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

Applications

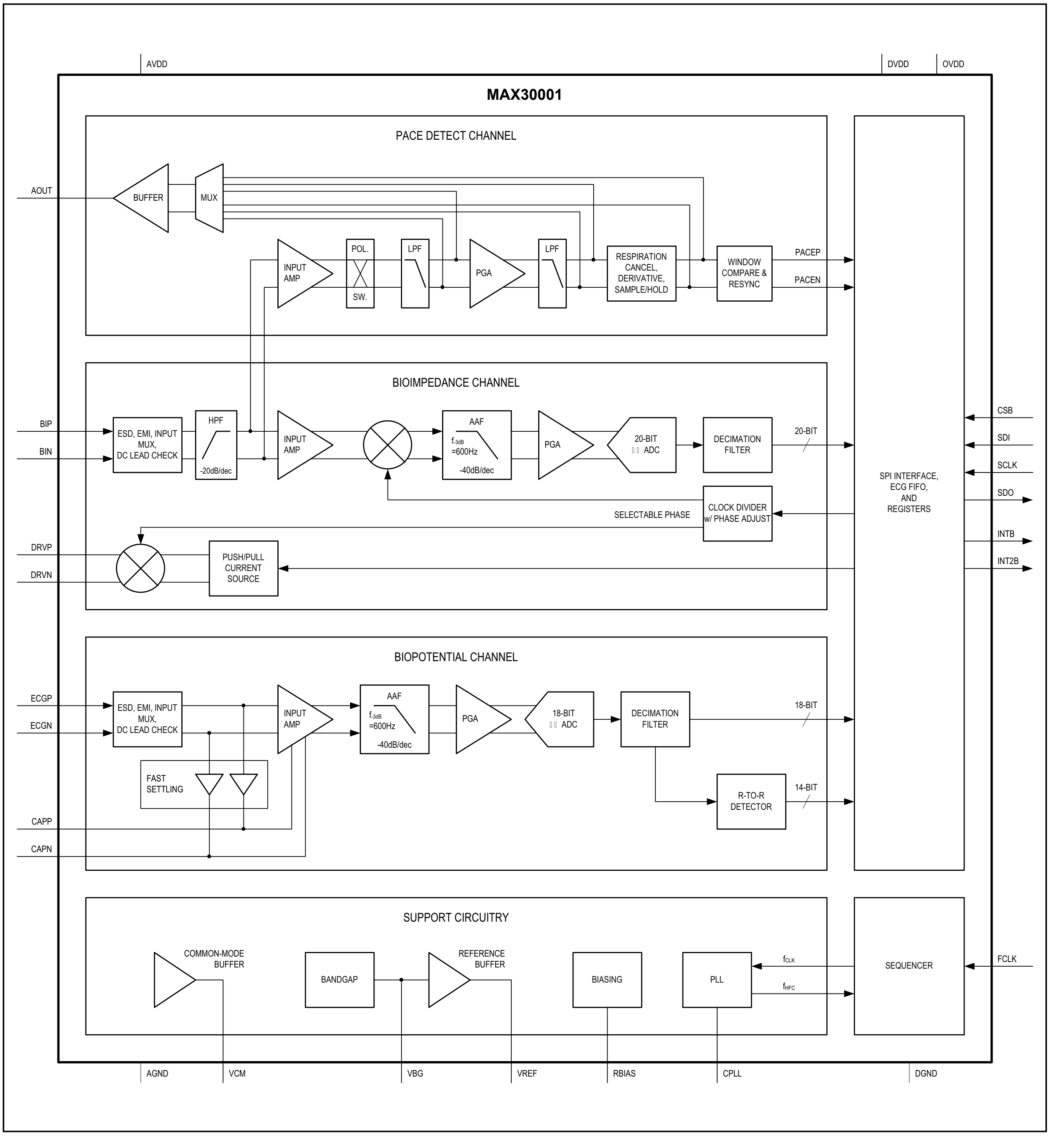
- Single-Lead Event Monitors for Arrhythmia Detection
- Single-Lead Wireless Patches for In-Patient/Out-Patient Monitoring
- Chest Band Heart Rate Monitors for Fitness Applications
- Bio Authentication and ECG-On-Demand Applications
- Respiration and Hydration Monitors
- Impedance Based Heart Rate Detection

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Clinical-Grade ECG and BioZ AFE with High Resolution Data Converter
  - 15.9 Bits ENOB with 3.1µV_{PP} (typ) Noise for ECG
  - 17 Bits ENOB with 1.1µV_{PP} Noise for BioZ
- Better Dry Starts Due to Much Improved Real World CMRR and High Input Impedance
  - Fully Differential Input Structure with CMRR > 100dB
- Offers Better Common-Mode to Differential Mode Conversion Due to High Input Impedance
- High Input Impedance > 1GΩ for Extremely Low Common-to-Differential Mode
- Minimum Signal Attenuation at the Input During Dry Start Due to High Electrode Impedance
- High DC Offset Range of ±650mV (1.8V, typ) Allows to Be Used with Wide Variety of Electrodes
- High AC Dynamic Range of 65mV_{PP} for ECG and 100mV_{PP} for BioZ Will Help Prevent Saturation in the Presence of Motion/Direct Electrode Hits
- Longer Battery Life Compared to Competing Solutions
  - 85µW at 1.1V Supply Voltage for ECG
  - 158µW at 1.1V Supply Voltage for BioZ
- Leads-On Interrupt Feature Allows to Keep µC in Deep Sleep Mode Until Valid Lead Condition is Detected
  - Lead-On Detect Current: 0.7µA (typ)
- Built-In Heart Rate Detection with Interrupt Feature Eliminates the Need to Run HR Algorithm on the µController
  - Robust R-R Detection in High Motion Environment at Extremely Low Power
- Configurable Interrupts Allows the µC Wake-Up Only on Every Heart Beat Reducing the Overall System Power
- High Accuracy Allows for More Physiological Data Extractions
- 32-Word ECG and 8-Word BioZ FIFOs Allows the MCU to Stay Powered Down for 256ms with Full Data Acquisition
- High-Speed SPI Interface
- Shutdown Current of 0.5µA (typ)

Functional Diagram



Absolute Maximum Ratings

AVDD to AGND ....-0.3V to +2.0V
DVDD to DGND...-0.3V to +2.0V
AVDD to DVDD ....-0.3V to +0.3V
OVDD to DGND ....-0.3V to +3.6V
AGND to DGND ....-0.3V to +0.3V
CSB, SCLK, SDI, FCLK to DGND ....-0.3V to +3.6V
SDO, INTB, INT2B
to DGND .... -0.3V to the lower of (3.6V and OVDD + 0.3V)
All Other Pins
to AGND .... -0.3V to the lower of (2.0V and AVDD + 0.3V)
Maximum Current into Any Pin...±50mA

Continuous Power Dissipation (T_A = +70ºC)
28-Pin TQFN
(derate 34.5mW/ºC above +70ºC)..........................2758.6mW
30-Bump WLP
(derate 24.3mW/ºC above +70ºC)..........................1945.5mW
Operating Temperature Range...............................0ºC to +70°C
Junction Temperature..+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (Soldering, 10sec).............................+300°C
Soldering Temperature (reflow).......................................+260°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................2°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....44°C/W

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECG CHANNEL						
AC Differential Input Range		V_{AVDD} = +1.1V, THD < 0.3%	-15		+15	mV_{PP}
		V_{AVDD} = +1.8V, THD < 0.3%		±32.5		
DC Differential Input Range		V_{AVDD} = +1.1V, shift from nominal gain < 2%	-300		+300	mV
		V_{AVDD} = +1.8V		±650		
Common Mode Input Range		V_{AVDD} = +1.1V, from V_{MID}, shift from nominal gain < 2%	-150		+150	mV
		V_{AVDD} = +1.8V, from V_{MID}, shift from nominal gain < 2%		±550		
Common Mode Rejection Ratio	CMRR	0Ω source impedance, f = 64Hz, T_A = +25˚C (Note 3)	100	115		dB
		(Note 4)		77		
ECG Channel Input Referred Noise		BW = 0.05 – 150Hz, G_{CH} = 20x		0.77		μV_{RMS}
				4.6		μV_{PP}
		BW = 0.05 – 40Hz, G_{CH} = 20x (Note 3)		0.46	1.0	μV_{RMS}
				3.1	6.6	μV_{PP}
Input Leakage Current		T_A = +25°C	-1	±0.1	+1	nA
Input Impedance (INA)		Common-mode, DC		45		GΩ
		Differential, DC		1500		MΩ

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECG Channel Total Harmonic Distortion	THD	V_{AVDD} = +1.80V, V_{IN} = 65mV_{PP}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV		0.025		%
		V_{AVDD} = +1.1V, V_{IN} = 30mV_{PP}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV			0.3	
ECG Channel Gain Setting	G_{CH}	Programmable, see register map		20 to 160		V/V
ECG Channel Gain Error (Excluding Reference)		V_{AVDD} = +1.8V, G_{CH} = 20x, ECGP = ECGN = VMID	-2.5		+2.5	%
		V_{AVDD} = +1.1V, G_{CH} = 20x, ECGP = ECGN = VMID	-4.5		+4.5	%
ECG Channel Offset Error		(Note 5)		±0.1		% of FSR
ADC Resolution				18		Bits
ADC Sample Rate		Programmable, see register map		125 to 512		SPS
CAPP to CAPN Impedance	R_{HPF}	FHP = 1/(2π x R_{HPF} x C_{HPF}), C_{HPF} = capacitance between CAPP and CAPN	320	450	600	kΩ
Analog High-Pass Filter Slew Current		Fast recovery enabled (1.8V)		160		µA
		Fast recovery enabled (1.1V)		55		
		Fast recovery disabled		0.09		
Fast Settling Recovery Time		C_{HPF} = 10µF, Note: varies by sample rate, see Table 3.		500		ms
Digital Low-Pass Filter		Linear phase FIR filter. DLPF[0:1] = 01		40		Hz
		Linear phase FIR filter. DLPF[0:1] = 10		100		
		Linear phase FIR filter. DLPF[0:1] = 11		150		
Digital High-Pass Filter		Phase-corrected 1st-order IIR filter. DHPF = 1		0.5		Hz
ECG Power Supply Rejection	PSRR	Lead bias disabled, DC		107		dB
		Lead bias disabled, f_{SW} = 64Hz		110		

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ECG INPUT MUX							
DC Lead Off Check		Pullup/ pulldown	IMAG[2:0] = 001		5		nA
			IMAG[2:0] = 010		10		
			IMAG[2:0] = 011		20		
			IMAG[2:0] = 100		50		
			IMAG[2:0] = 101		100		
DC Lead Off Comparator Low Threshold		VTH[1:0] = 11 (Note 6)			V_{MID} – 0.50		V
		VTH[1:0] = 10 (Note 7)			V_{MID} – 0.45		
		VTH[1:0] = 01 (Note 8)			V_{MID} – 0.40		
		VTH[1:0] = 00			V_{MID} – 0.30		
DC Lead Off Comparator High Threshold		VTH[1:0] = 11 (Note 6)			V_{MID} + 0.50		V
		VTH[1:0] = 10 (Note 7)			V_{MID} + 0.45		
		VTH[1:0] = 01 (Note 8)			V_{MID} + 0.40		
		VTH[1:0] = 00			V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled	RBIASV[1:0] = 00		50		MΩ
			RBIASV[1:0] = 01		100		
			RBIASV[1:0] = 10		200		
Lead Bias Voltage	V_{MID}	Lead bias enabled			V_{AVDD}/ 2.15		V
Calibration Voltage Magnitude		Single-ended	V_{MAG} = 0		0.25		mV
			V_{MAG} = 1		0.50		
Calibration Voltage Magnitude Error		Single-ended (Note 9)		-3		+3	%
Calibration Voltage Frequency		Programmable, see Register Map			0.0156 to 256		Hz
Calibration Voltage Pulse Time		Programmable, see register map	FIFTY = 0		0.03052 to 62.474		ms
			FIFTY = 1		50		%

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOIMPEDANCE (BIOZ) CHANNEL						
Signal Generator Resolution		Square wave generator		1		Bits
DRVP/N Injected Full-Scale Current		Programmable, see Register Map		8 to 96		μA_{PP}
DRVP/N Injected Current Accuracy		Internal bias resistor	-30		+30	%
		External bias resistor (0.1%, 10ppm, 324kΩ)	-10		+10	
DRVP/N Injected Current Power Supply Rejection				<±1		%/V
DRVP/N Injected Current Temperatue Coefficient		External bias resistor, 32µA_{PP}, 0 to 70ºC (0.1%, 10ppm, 324kΩ)		50		ppm/°C
DRVP/N Compliance Voltage		V_{DRVP} - V_{DRVN}		±(V_{AVDD}- 0.5)		V_{PP}
Current Injection Frequency		Programmable, see Register Map		0.125 to 131.072		kHz
AC Differential Input Range		Shift from nominal gain < 1% (1.1V)		25		mV
		Shift from nominal gain < 1% (1.8V)		90		mV
BioZ Channel Gain		Programmable, see Register Map		10 to 80		V/V
ADC Sample Rate		Programmable, see Register Map		24.98 to 64		sps
ADC Resolution				20		Bits
Input Referred Noise (BIP, BIN)		BW = 0.05 to 4Hz, Gain = 20x		0.16		μV_{RMS}
		BW = 0.05 to 4Hz, Gain = 20x		1.1		μV_{PP}
Impedance Resolution		DC to 4Hz, 32µA_{PP}, 40kHz, Gain = 20x, R_{BODY} = 680Ω		40		$m\Omega_{PP}$
Input Analog High Pass Filter		Programmable, see Register Map		125 to 7200		Hz
Demodulation Phase Range		Programmable, see Register Map		0-180		°
Demodulation Phase Resolution		Programmable, see Register Map		11.25		°
Output Digital Low Pass Filter		BIOZ_DLPF[1:0] = 01		4		Hz
		BIOZ_DLPF[1:0] = 10		8		
		BIOZ_DLPF[1:0] = 11		16		
Output Digital High Pass Filter		BIOZ_DHPF[1:0] = 01		0.05		Hz
		BIOZ_DHPF[1:0] = 1x		0.5		Hz

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIOIMPEDANCE (BIOZ) INPUT MUX							
DC Lead Off Check		IMAG[2:0] = 001			5		nA
		IMAG[2:0] = 010			10		
		IMAG[2:0] = 011			20		
		IMAG[2:0] = 100			50		
		IMAG[2:0] = 101			100		
DC Lead Off Comparator Low Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} – 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} – 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} – 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} – 0.30		
DC Lead Off Comparator High Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} + 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} + 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} + 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled, RBIASV[1:0] = 00			50		MΩ
		Lead bias enabled, RBIASV[1:0] = 01			100		
		Lead bias enabled, RBIASV[1:0] = 10			200		
Lead Bias Voltage		Lead bias enabled. Programmable, see Register Map			V_{AVDD}/ 2.15		V
Calibration Voltage Magnitude		Single-ended. V_{MAG} = 0			0.25		mV
		Single-ended. V_{MAG} = 1			0.50		
Calibration Voltage Error		Single-ended. (Note 9)		-3		+3	%
Calibration Voltage Frequency		Programmable, see Register Map			0.0156 to 256		Hz
Calibration Voltage Pulse Time		Programmable, see Register Map	CAL_FIFTY = 0		0.03052 to 62.474		ms
			CAL_FIFTY = 1		50		%
Resistive Load Nominal Value	R_{VAL}	Programmable, see Register Map			0.625 to 5.0		kΩ
Resistive Load Modulation Value	R_{MOD}	Programmable, see Register Map			15 to 2960		mΩ
Resistive Load Modulation Frequency	F_{MOD}	Programmable, see Register Map			0.625 to 4.0		Hz

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PACE DETECTION						
Pace Artifact Width		Programmable, see Register Map		0.05 to 2.0		ms
Minimum Pace Artifact Amplitude				0.5		mV
Time Resolution				16		µs
Recovery Time		Large Pacer Pulse (100mV to 700mV)		500		µs
AOUT Output Voltage Swing		f = 1kHz, THD < 0.2%		100		mV_{PP}
INTERNAL REFERENCE/COMMON-MODE						
V_{BG} Output Voltage	V_{BG}			0.650		V
V_{BG} Output Impedance				100		kΩ
External V_{BG} Compensation Capacitor	C_{VBG}		1			µF
V_{REF} Output Voltage	V_{REF}	T_A = +25ºC	0.995	1.000	1.005	V
V_{REF} Temperature Coefficient	TC_{REF}	T_A = 0ºC to +70ºC		10		ppm/ºC
V_{REF} Buffer Line Regulation				330		µV/V
V_{REF} Buffer Load Regulation		I_{LOAD} = 0 to 100µA		25		µV/µA
External V_{REF} Compensation Capacitor	C_{REF}		1	10		µF
VCM Output Voltage	V_{CM}			0.650		V
External V_{CM} Compensation Capacitor	C_{CM}		1	10		µF
DIGITAL INPUTS (SDI, SCLK, CSB, FCLK)						
Input-Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input-Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}		-1		+1	µA
DIGITAL OUTPUTS (SDO, INTB, INT2B)						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Three-State Leakage Current			-1		+1	µA
Three-State Output Capacitance				15		pF
POWER SUPPLY						
Analog Supply Voltage	V_{AVDD}	Connect AVDD to DVDD	1.1		2.0	V
Digital Supply Voltage	V_{DVDD}	Connect DVDD to AVDD	1.1		2.0	V
Interface Supply Voltage	V_{OVDD}	Power for I/O drivers only	1.65		3.6	V

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{AVDD} + I_{DVDD}	ECG channel	V_{AVDD} = V_{DVDD} = +1.1V		76		µA
			V_{AVDD} = V_{DVDD} = +1.8V		95		
			V_{AVDD} = V_{DVDD} = +2.0V		102	120	
		ECG channel with Pace (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		100		
			V_{AVDD} = V_{DVDD} = +1.8V		124		
			V_{AVDD} = V_{DVDD} = +2.0V		133	150	
		ECG channel with Pace and AOUT (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		114		
			V_{AVDD} = V_{DVDD} = +1.8V		138		
			V_{AVDD} = V_{DVDD} = +2.0V		147	190	
		ECG channel with Pace, and BioZ, LN_BIOZ = 0	V_{AVDD} = V_{DVDD} = +1.1V		205		
			V_{AVDD} = V_{DVDD} = +1.8V		232		
			V_{AVDD} = V_{DVDD} = +2.0V		242	270	
		ECG channel with Pace, and BioZ, LN_BIOZ = 1	V_{AVDD} = V_{DVDD} = +1.1V		220		
			V_{AVDD} = V_{DVDD} = +1.8V		247		
			V_{AVDD} = V_{DVDD} = +2.0V		256	285	
		BioZ channel , LN_BIOZ = 0 (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		144		
			V_{AVDD} = V_{DVDD} = +1.8V		163		
			V_{AVDD} = V_{DVDD} = +2.0V		170	190	
		BioZ channel , LN_BIOZ = 1 (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		158		
			V_{AVDD} = V_{DVDD} = +1.8V		178		
			V_{AVDD} = V_{DVDD} = +2.0V		185	205	
		ECG channel and BioZ, LN_BIOZ = 0 (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		186		
			V_{AVDD} = V_{DVDD} = +1.8V		211		
			V_{AVDD} = V_{DVDD} = +2.0V		220	250	
		ECG channel and BioZ, LN_BIOZ = 1 (Note 3)	V_{AVDD} = V_{DVDD} = +1.1V		200		
			V_{AVDD} = V_{DVDD} = +1.8V		225		
			V_{AVDD} = V_{DVDD} = +2.0V		235	265	
		ULP Lead On Detect	T_A = +70ºC		1.3		
			T_A = +25ºC		0.63	2.5	
Interface Supply Current	I_{OVDD}	V_{OVDD} = +1.65V, ECG channel at 512sps (Note 10)			0.2		µA
		V_{OVDD} = 3.6V, ECG channel at 512sps (Note 10)			0.6	1.6	
Shutdown Current	I_{SAVDD} + I_{SDVDD}	V_{AVDD} = V_{DVDD} = 2.0V (Note 5)	T_A = +70ºC		1.3		µA
			T_A = +25ºC		0.58	2.5	
	I_{SOVDD}	V_{OVDD} = 3.6V, V_{AVDD} = V_{DVDD} = 2.0V				1.1	
ESD PROTECTION							
ECGP, ECGN, BIP, BIN		IEC 61000-4-2 Contact Discharge (Note 11)			±8		kV
		IEC 61000-4-2 Air-Gap Discharge (Note 11)			±15		

Timing Characteristics (Note 3)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (NOTE 3)						
SCLK Frequency	f_{SCLK}		0		12	MHz
SCLK Period	t_{CP}		83			ns
SCLK Pulse Width High	t_{CH}		15			ns
SCLK Pulse Width Low	t_{CL}		15			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge (RE)	15			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE	0			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 32nd RE, executed write	10			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd RE, aborted write sequence	15			ns
SCLK Rise to CSB Fall	t_{CSF}	Applies to 32nd RE	100			ns
CSB Pulse-Width High	t_{CSPW}		20			ns
SDI-to-SCLK Rise Setup Time	t_{DS}		8			ns
SDI to SCLK Rise Hold Time	t_{DH}		8			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pF			40	ns
		C_{LOAD} = 20pF, V_{AVDD} = V_{DVDD} ≥ 1.8V, V_{DVDD} ≥ 2.5V			20	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 20pF	2			ns
CSB Fall to SDO Fall	t_{DOE}	Enable time, C_{LOAD} = 20pF			30	ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			35	ns
FCLK Frequency	f_{FCLK}	External reference clock		32.768		kHz
FCLK Period	t_{FP}			30.52		μs
FCLK Pulse-Width High	t_{FH}	50% duty cycle assumed		15.26		μs
FCLK Pulse-Width Low	t_{FL}	50% duty cycle assumed		15.26		μs

Note 2: All devices are 100% production tested at T_A = +25ºC. Specifications over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization. Not tested in production.
Note 4: One electrode drive with <10Ω source impedance, the other driven with 51kΩ in parallel with a 47nF per IEC60601-2-47.
Note 5: Inputs connected to 51kΩ in parallel with a 47nF to V_{CM}.
Note 6: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.65V.
Note 7: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.55V.
Note 8: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.45V.
Note 9: This specification defines the accuracy of the calibration voltage source as applied to the ECG input, not as measured through the ADC channel.
Note 10: f_{SCLK} = 4MHz, burst mode, EFIT = 8, C_{SDO} = C_{INTB} = 50pF.
Note 11: ESD test performed with 1kΩ series resistor designed to withstand 8kV surge voltage.

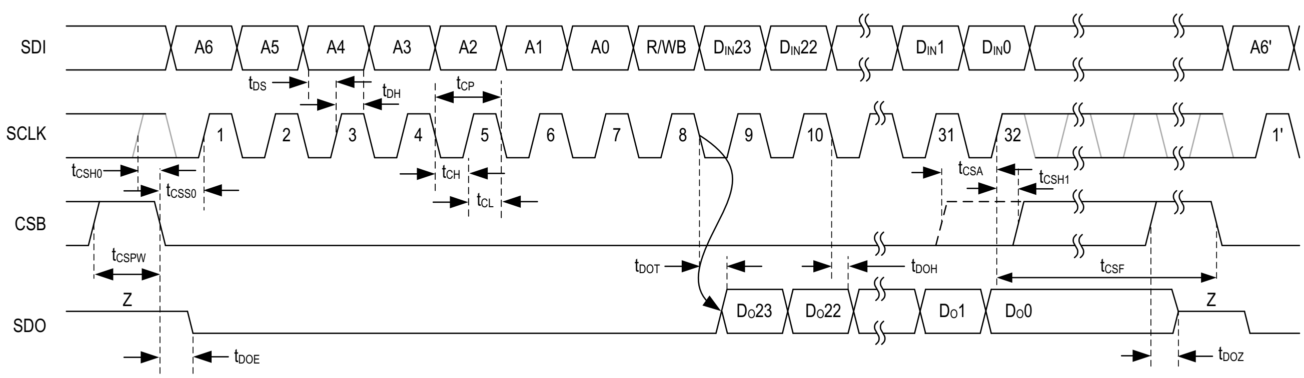


Figure 1a. SPI Timing Diagram

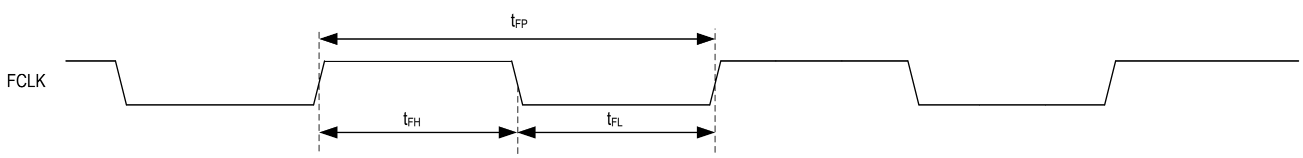
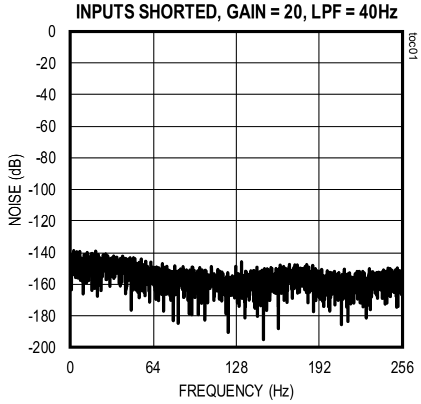


Figure 1b. FCLK Timing Diagram

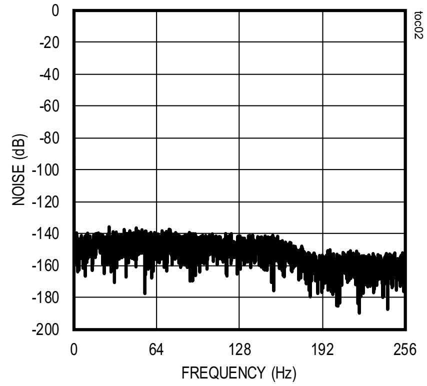
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

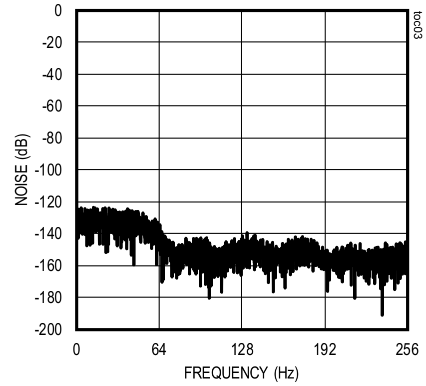
ECG NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 20, LPF = 40Hz



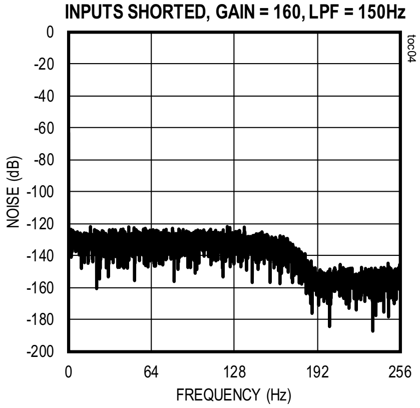
ECG NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 20, LPF = 150Hz



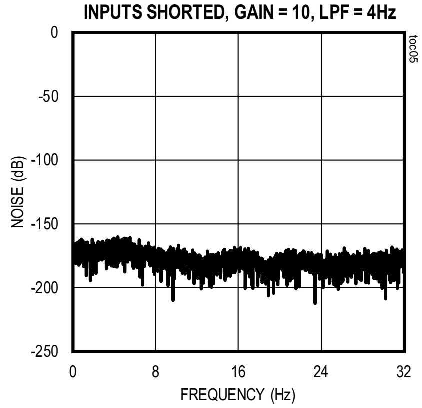
ECG NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 160, LPF = 40Hz



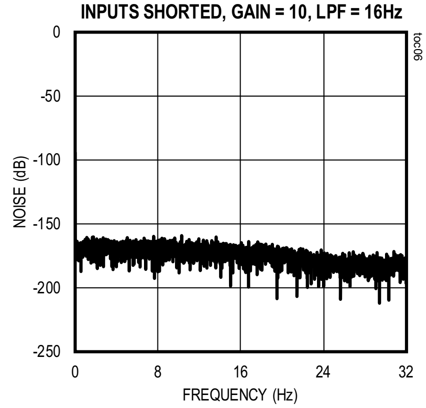
ECG NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 160, LPF = 150Hz



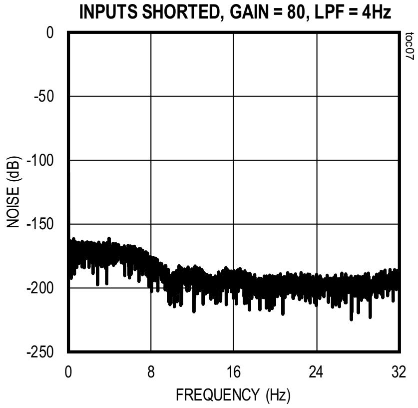
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 4Hz



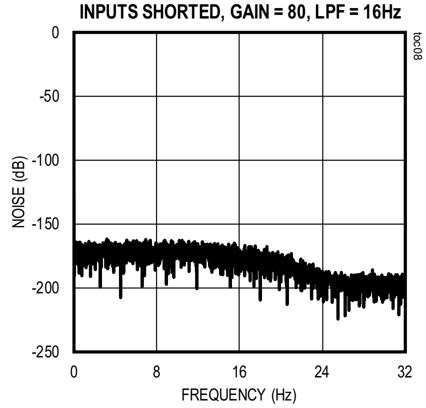
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 16Hz



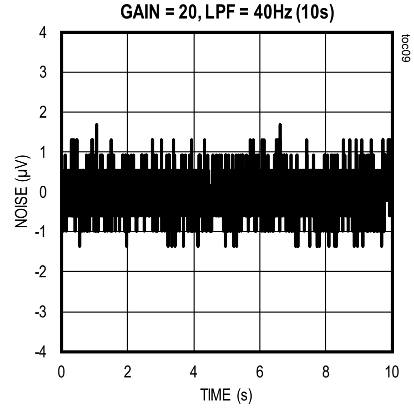
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 4Hz



BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 16Hz



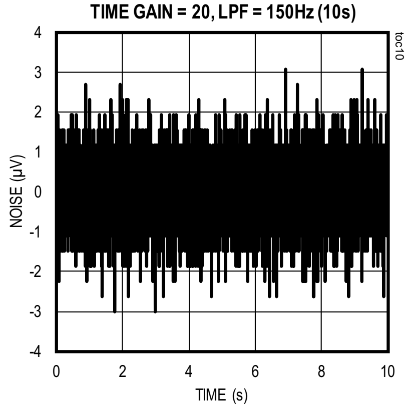
ECG INPUT-REFERRED NOISE vs. TIME
GAIN = 20, LPF = 40Hz (10s)



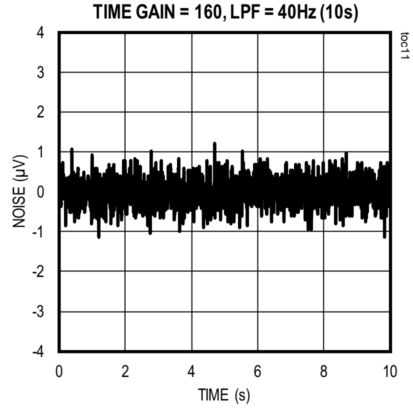
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

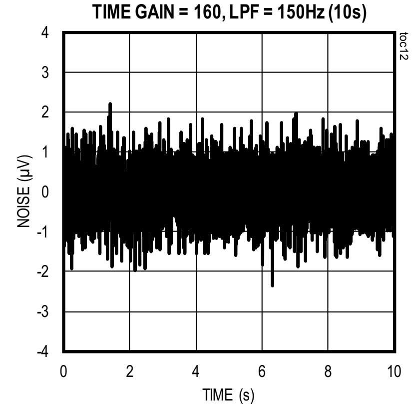
ECG INPUT-REFERRED NOISE vs.
TIME GAIN = 20, LPF = 150Hz (10s)



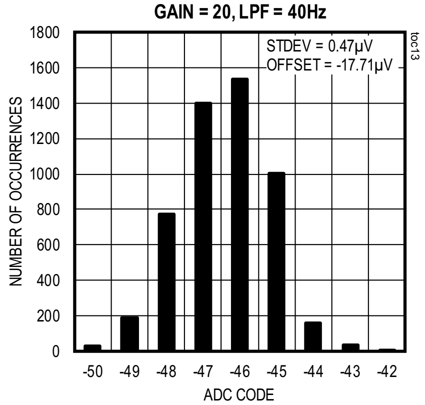
ECG INPUT-REFERRED NOISE vs.
TIME GAIN = 160, LPF = 40Hz (10s)



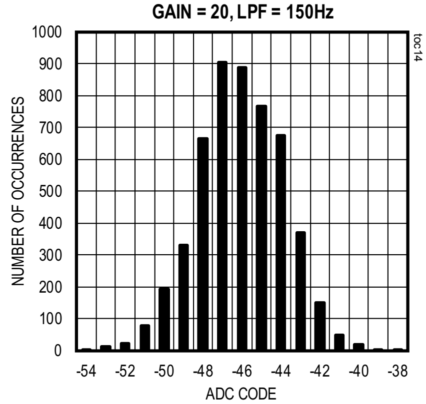
ECG INPUT-REFERRED NOISE vs.
TIME GAIN = 160, LPF = 150Hz (10s)



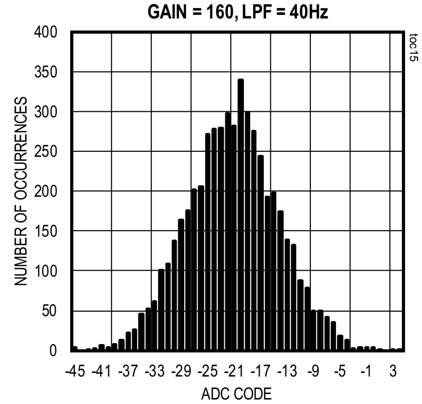
ECG NOISE HISTOGRAM
GAIN = 20, LPF = 40Hz



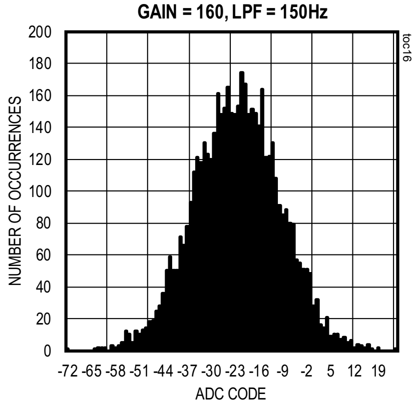
ECG NOISE HISTOGRAM
GAIN = 20, LPF = 150Hz



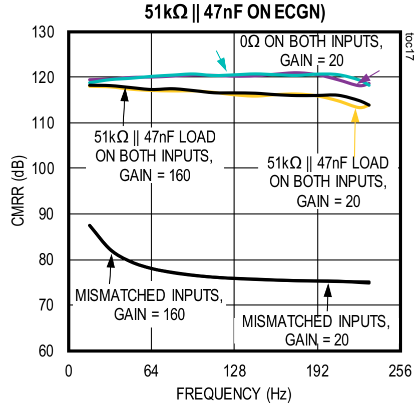
ECG NOISE HISTOGRAM
GAIN = 160, LPF = 40Hz



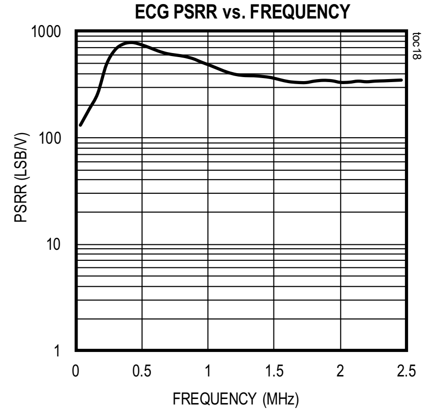
ECG NOISE HISTOGRAM
GAIN = 160, LPF = 150Hz



ECG CMRR vs. FREQUENCY
(MISMATCHED LOAD IS 0Ω ON ECGP,
51kΩ || 47nF ON ECGN)

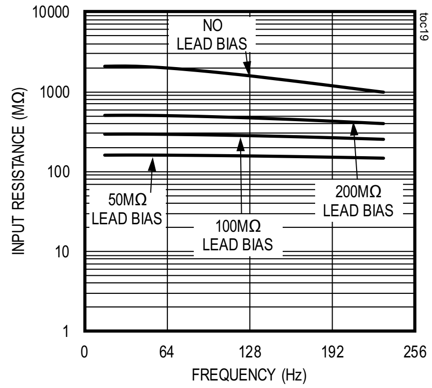


ECG PSRR vs. FREQUENCY

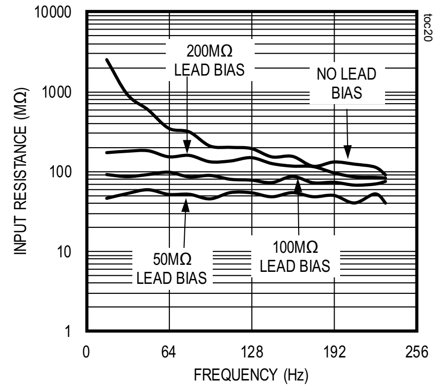


Typical Operating Characteristics (continued)

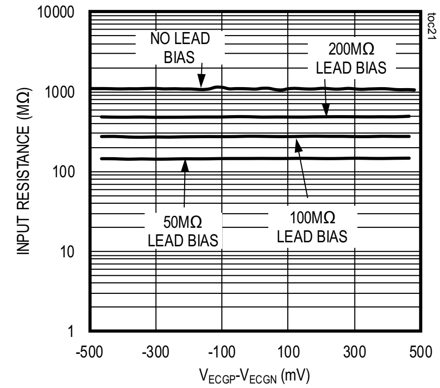
(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)



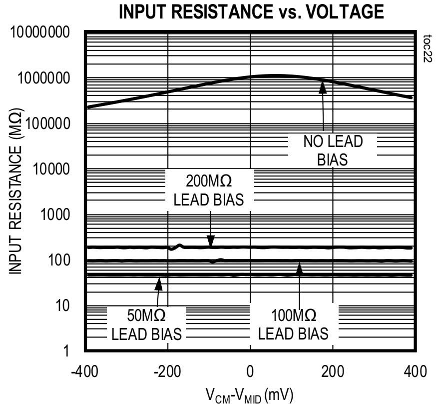
ECG DIFFERENTIAL INPUT RESISTANCE vs. FREQUENCY



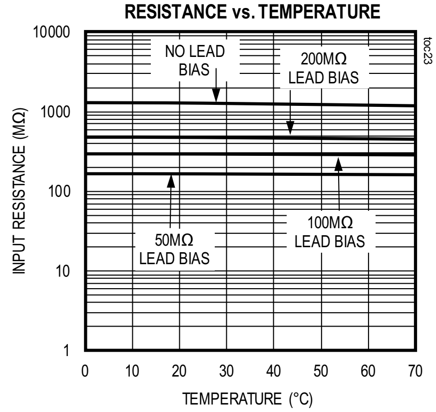
ECG COMMON-MODE INPUT RESISTANCE vs. FREQUENCY



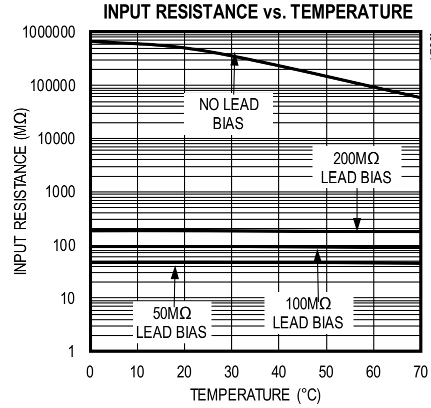
ECG DIFFERENTIAL INPUT RESISTANCE vs. VOLTAGE



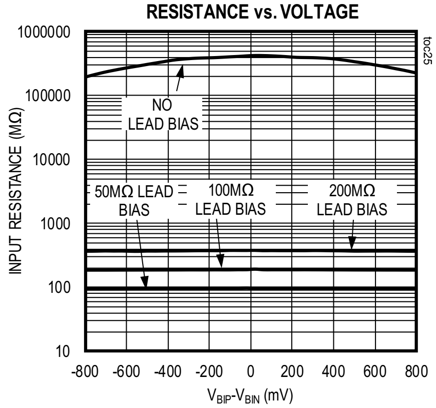
ECG COMMON-MODE INPUT RESISTANCE vs. VOLTAGE



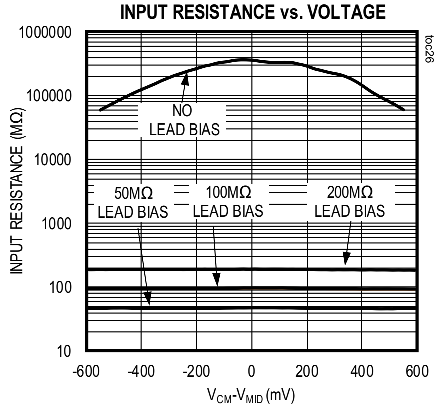
ECG DIFFERENTIAL INPUT RESISTANCE vs. TEMPERATURE



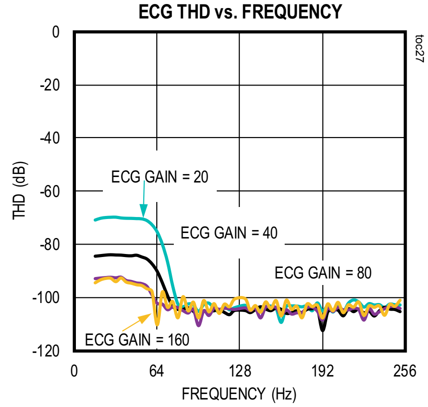
ECG COMMON-MODE INPUT RESISTANCE vs. TEMPERATURE



BIOZ DIFFERENTIAL INPUT RESISTANCE vs. VOLTAGE



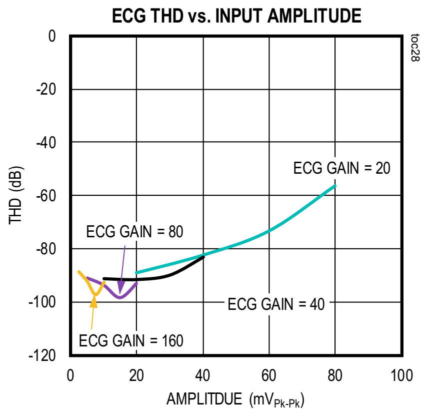
BIOZ COMMON-MODE INPUT RESISTANCE vs. VOLTAGE

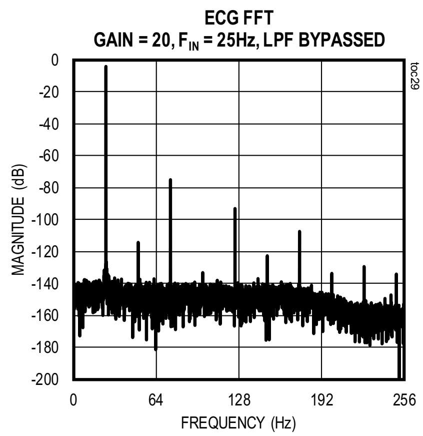


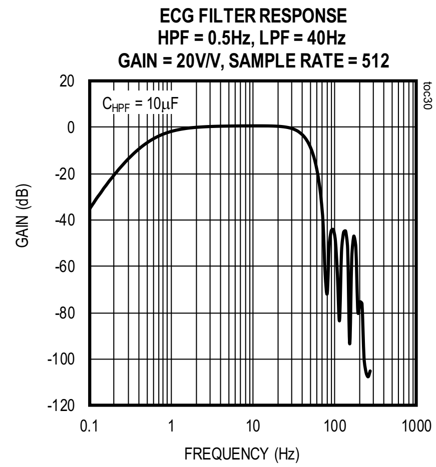
ECG THD vs. FREQUENCY

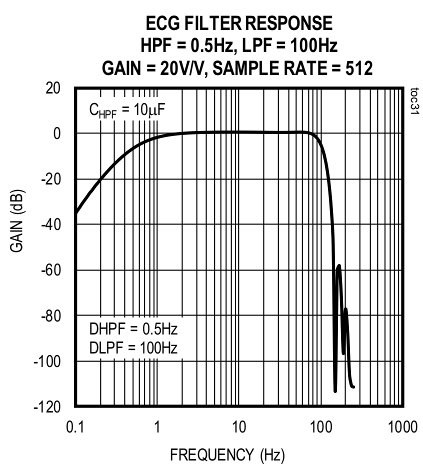
Typical Operating Characteristics (continued)

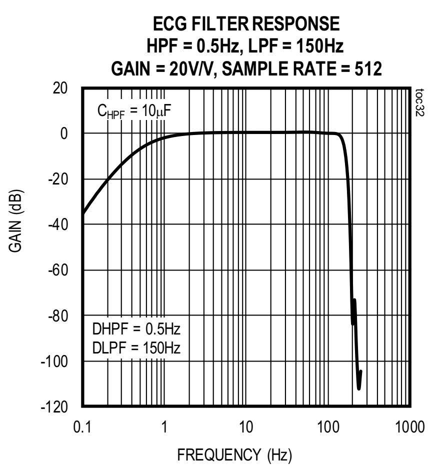
(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

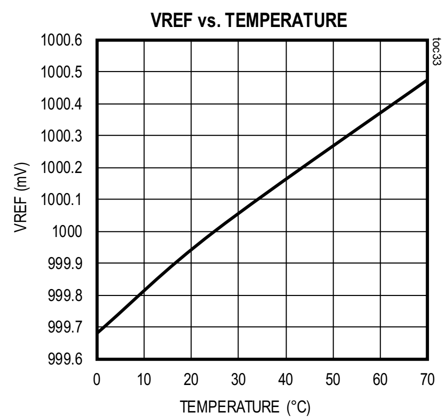


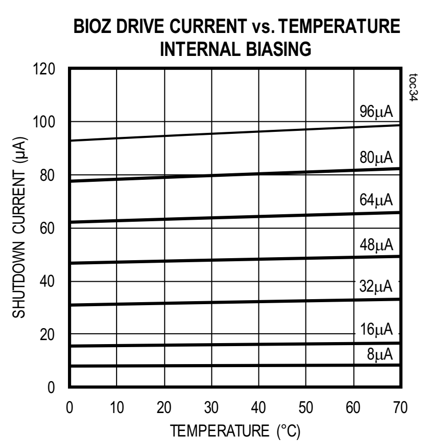


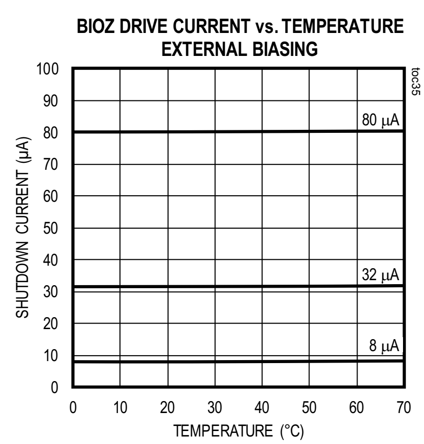


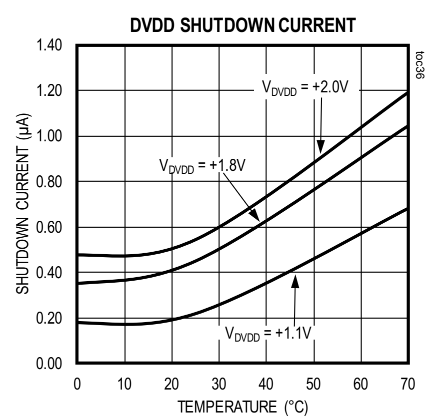






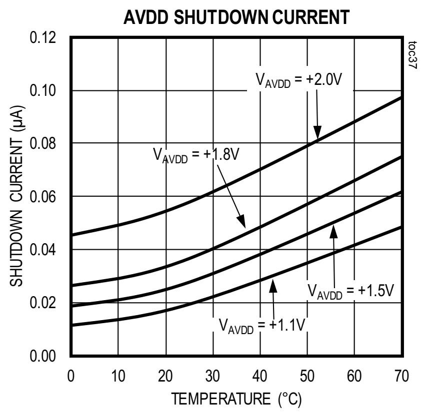


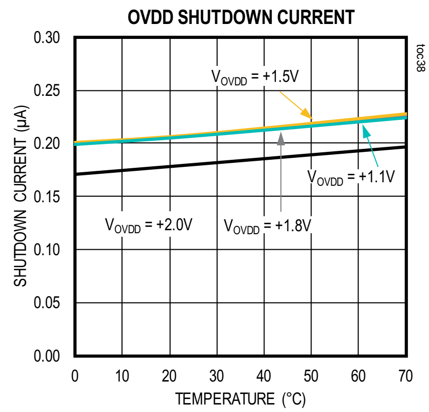


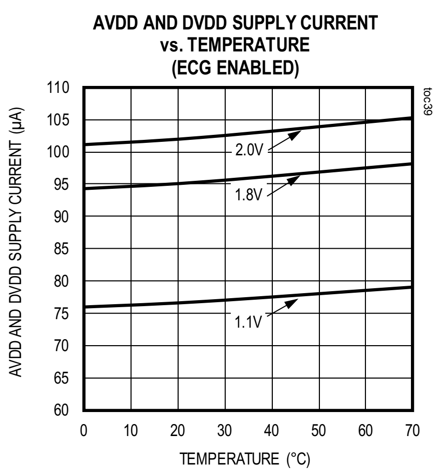


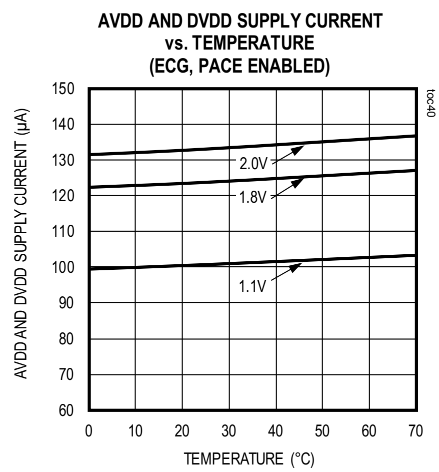
Typical Operating Characteristics (continued)

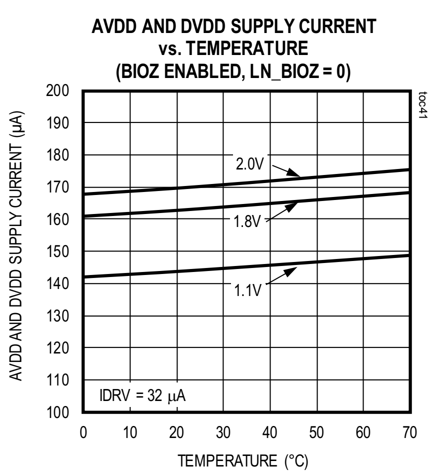
(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

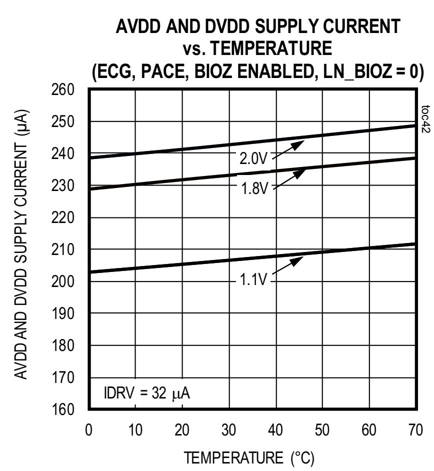






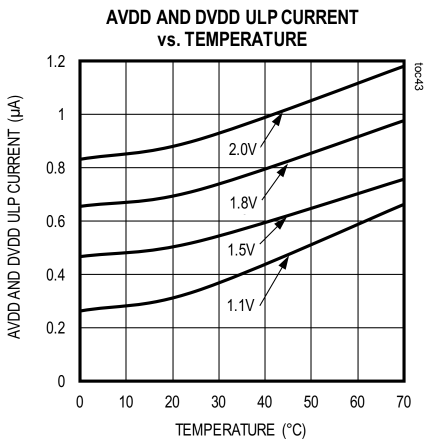


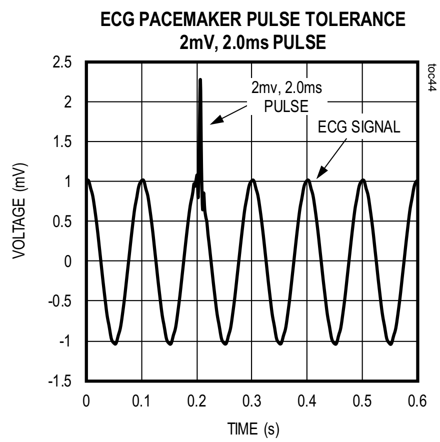


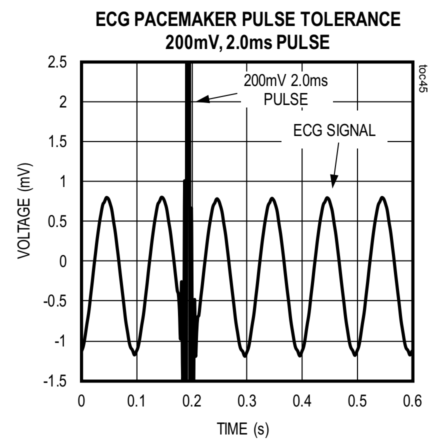


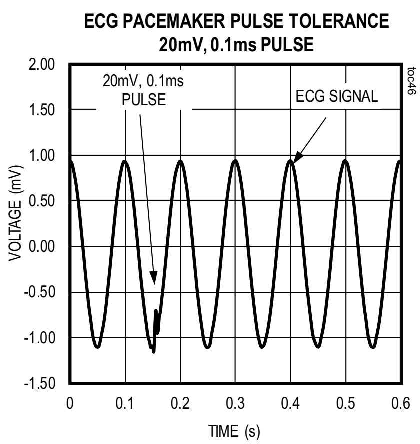
Typical Operating Characteristics (continued)

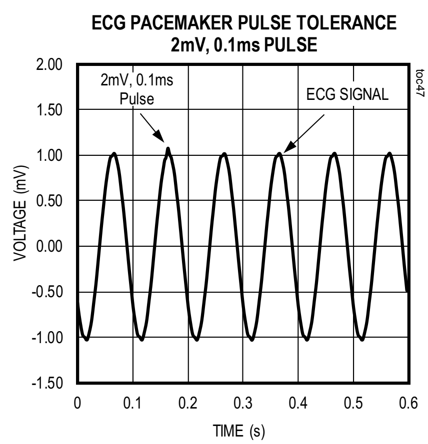
($V_{DVDD} = V_{AVDD} = 1.8V$, $V_{OVDD} = 2.5V$, $T_A = +25°C$, unless otherwise noted.)



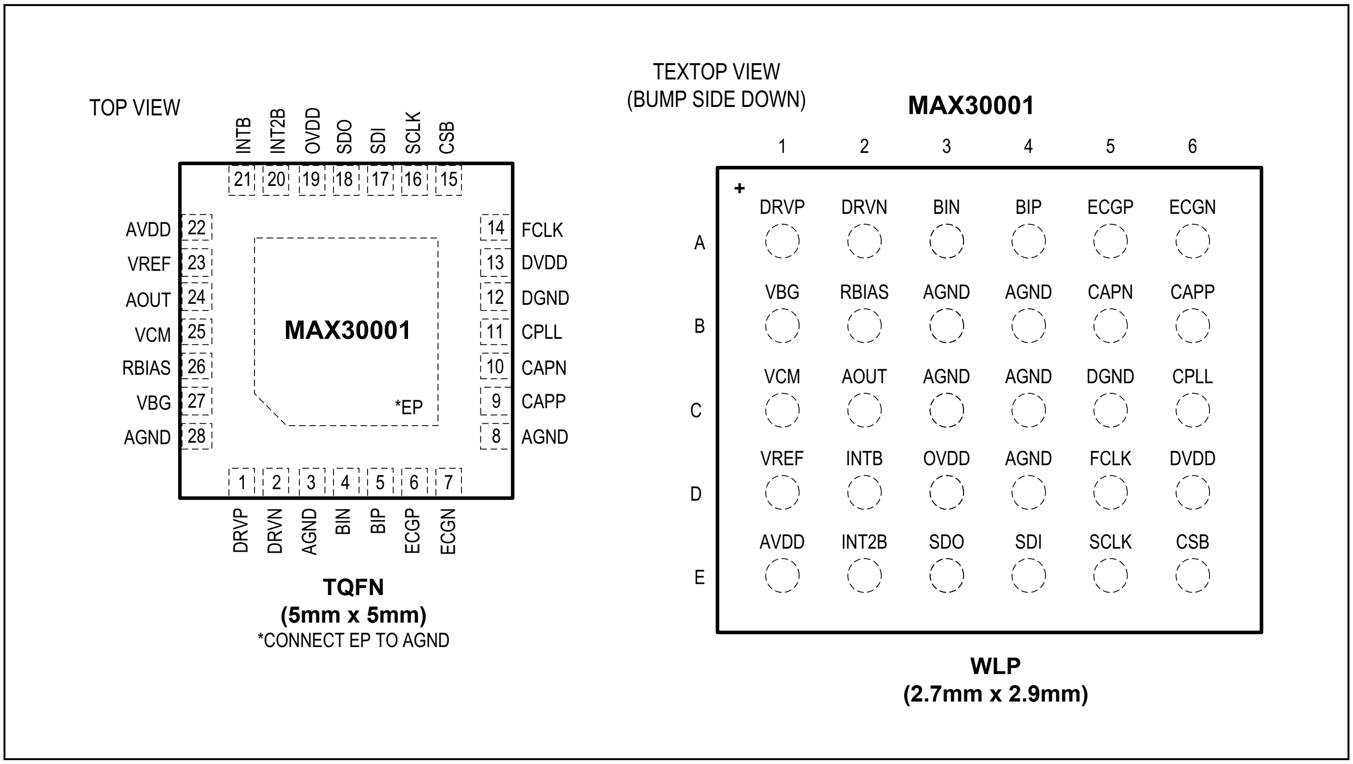








Pin Configurations



Pin Description

BUMP	PIN	NAME	FUNCTION
WLP	TQFN		
A1	1	DRVP	Positive Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A2	2	DRVN	Negative Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A3	4	BIN	Bioimpedance Negative Input.
A4	5	BIP	Bioimpedance Positive Input.
A5	6	ECGP	ECG Positive Input.
A6	7	ECGN	ECG Negative Input.
B1	27	VBG	Bandgap Noise Filter Output. Connect a 1.0µF X7R ceramic capacitor between V_{BG} and AGND.
B2	26	RBIAS	External Resistor Bias. Connect a low tempco resistor between RBIAS and AGND. If external bias generator is not used then RBIAS can be left floating.
B3, B4, C3, C4, D4	3, 8, 28	AGND	Analog Power and Reference Ground. Connect into the printed circuit board ground plane.
B5	10	CAPN	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (C_{HPF}) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel. *Select a capaitor with a high voltage rating (25V) to improve linearity of the ECG signal path.*

Pin Description (continued)

BUMP	PIN	NAME	FUNCTION
WLP	TQFN		
B6	9	CAPP	Analog High-Pass Filter Input. Connect a 1μF X7R capacitor (C_{HPF}) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel. *Select a capaitor with a high voltage rating (25V) to improve linearity of the ECG signal path.*
C1	25	VCM	Common Mode Buffer Output. Connect a 10μF X5R ceramic capacitor between V_{CM} and AGND.
C2	24	AOUT	Analog Output Voltage of the Pace Channel. Programmable to select where in the signal path to output to AOUT.
C5	12		Digital Ground for Both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
C6	11	CPLL	PLL Loop Filter Input. Connect 1nF capacitor between CPLL and AGND.
D1	23	VREF	ADC Reference Buffer Output. Connect a 10μF X5R ceramic capacitor between V_{REF} and AGND.
D2	21	INTB	Interrupt Output. INTB is an active low status output. It can be used to interrupt an external device.
D3	19	OVDD	Logic Interface Supply Voltage.
D5	14	FCLK	External 32.768kHz Clock that Controls the Sampling of the Internal Sigma-Delta Converters and Decimator.
D6	13	DVDD	Digital Core Supply voltage. Connect to AVDD.
E1	22	AVDD	Analog Core Supply Voltage. Connect to DVDD.
E2	20	INT2B	Interrupt 2 Output. INT2B is an active-low status output. It can be used to interrupt an external device.
E3	18	SDO	Serial Data Output. SDO will change state on the falling edge of SCLK when CSB is low. SDO is three-stated when CSB is high.
E4	17	SDI	Serial Data Input. SDI is sampled into the device on the rising edge of SCLK when CSB is low.
E5	16	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
E6	15	CSB	Active-Low Chip-Select Input. Enables the serial interface.
		—	Exposed Pad. Connect EP to AGND.

Detailed Description

ECG Channel

Figure 2 illustrates the ECG channel block diagram, excluding the ADC. The channel comprises an input MUX, a fast-recovering instrumentation amplifier, an anti-alias filter, and a programmable gain amplifier. The input MUX includes several features such as ESD protection, EMI filtering, lead biasing, leads off checking, and ultra-low power leads-on checking. The output of this analog channel drives a high-resolution ADC.

Input MUX

The ECG input MUX shown in Figure 3 contains integrated ESD and EMI protection, DC leads off detect current sources, lead-on detect, series isolation switches, lead biasing, and a programmable calibration voltage source to enable channel built in self-test.

EMI Filtering and ESD Protection

EMI filtering of the ECGP and ECGN inputs consists of a single pole, low pass, differential, and common mode filter with the pole located at approximately 2MHz. The ECGP and ECGN inputs also have input clamps that protect the inputs from ESD events.

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD
- ±15kV using the Air Gap Discharge method specified in IEC61000-4-2 ESD
- For IEC61000-4-2 ESD protection, use 1kΩ series resistors on ECGP and ECGN that is rated to withstand ±8kV surge voltages.

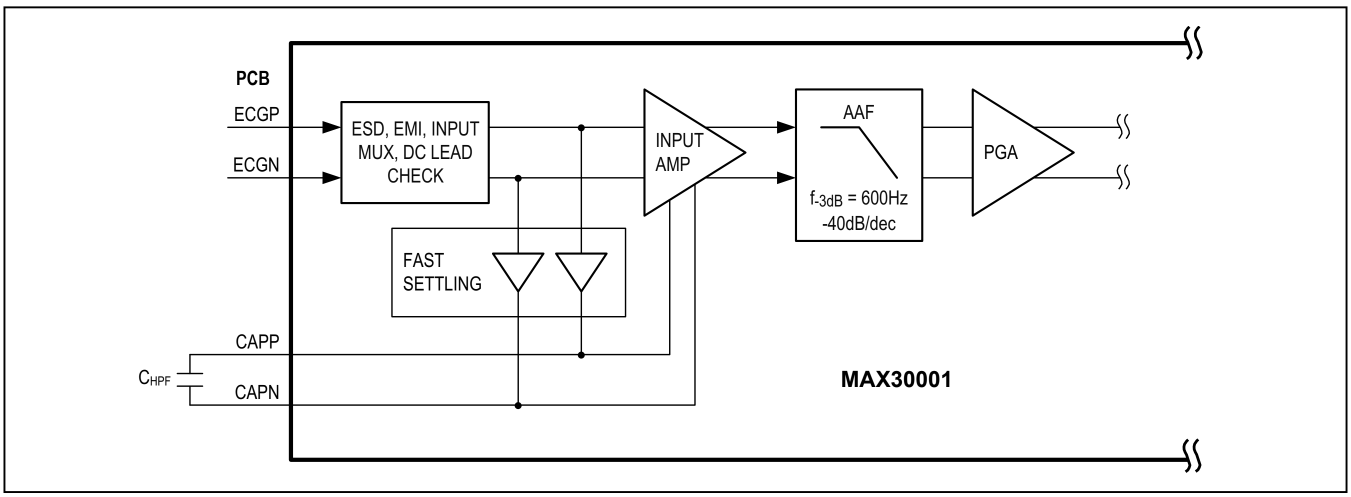


Figure 2. ECG Channel Input Amplifier and PGA Excluding the ADC

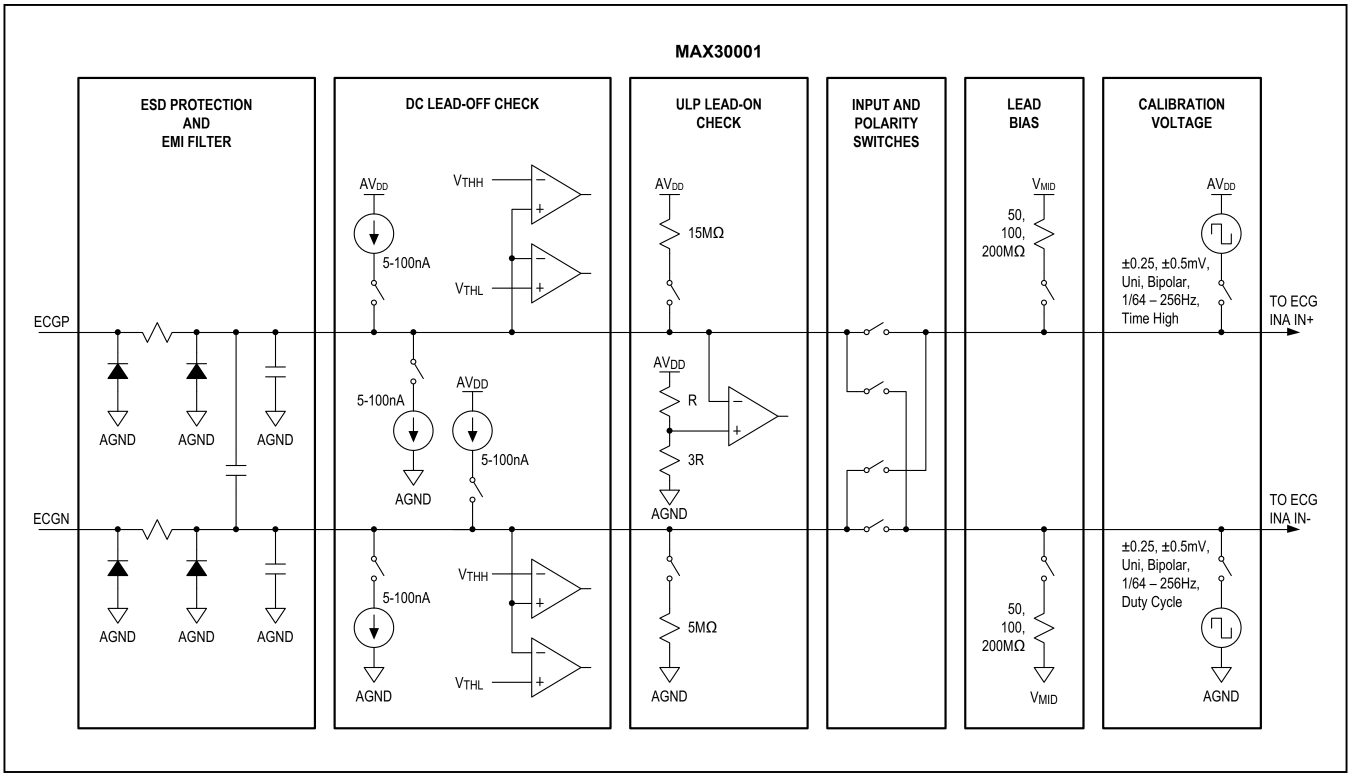


Figure 3. ECG Input MUX

DC Leads-Off Detection and ULP Leads-On Detection

The input MUX leads-off detect circuitry consists of programmable sink/source DC current sources that allow for DC leads-off detection, while the channel is powered up in normal operation and an ultra-low-power (ULP) leads-on detect while the channel is powered-down.

The MAX30001 accomplishes DC leads-off detection by applying a DC current to pull the ECG input voltage up to above V_{MID} + V_{TH} or down to below V_{MID} - V_{TH}. The current sources have user selectable values of 0nA, 5nA, 10nA, 20nA, 50nA, and 100nA that allow coverage of dry and wet electrode impedance ranges. Supported thresholds are V_{MID} ± 300mV (recommended), V_{MID} ±400mV, V_{MID} ± 450mV, and V_{MID} ± 500mV. A threshold of 400mV, 450mV, and 500mV must only be used when V_{AVDD} ≥ 1.45V, 1.55V, and 1.65V, respectively. A dynamic comparator protects against false flags generated by the input amplifier and input chopping. The comparator checks for a minimum continuous violation (or threshold exceeded) of 115ms to 140ms depending on the setting of FMSTR[1:0] before asserting any one of the LDOFF_xx interrupt flags (Figure 4). See registers CNFG_GEN (0x10) and CNFG_EMUX (0x14) for configuration settings and see Table 1 for recommended values given electrode type and supply voltage.

The ULP lead on detect operates by pulling ECGN low with a pulldown resistance larger than 5MΩ and pulling ECGP high with a pullup resistance larger than 15MΩ. A low-power comparator determines if ECGP is pulled below a predefined threshold that occurs when both electrodes make contact with the body. When the impedance between ECGP and ECGN is less than 20MΩ, an interrupt LONINT is asserted, alerting the µC to a leads-on condition.

A 0nA/V_{MID} ± 300mV selection is available allowing monitoring of the input compliance of the INA during non-DC lead-off checks.

Lead Bias

The MAX30001 limits the ECGP and ECGN DC input common mode range to V_{MID} ±150mV. This range can be maintained either through external or internal lead-biasing.

Internal DC lead-biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors to V_{MID} that drive the electrodes within the input common mode requirements of the ECG channel and can drive the connected body to the proper common mode voltage level. See register CNFG_GEN (0x10) to select a configuration.

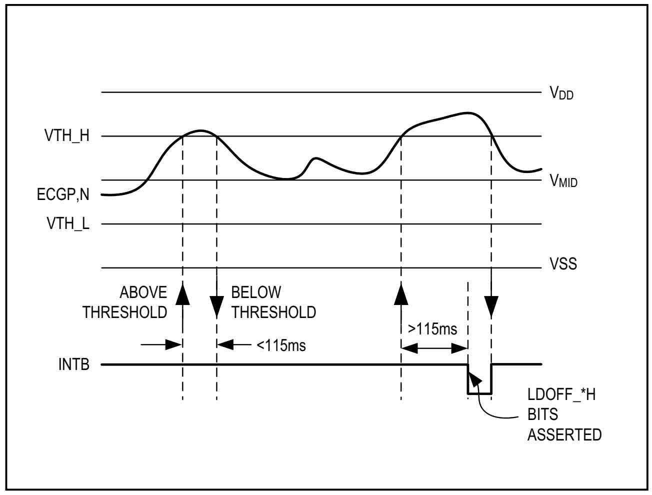


Figure 4. Lead Off Detect Behavior

The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a high value resistor such as 1MΩ to limit current into the body. If this is utilized then the internal lead bias resistors to V_{MID} can be disabled.

Isolation and Polarity Switches

The series switches in the MAX30001 isolate the ECGP and ECGN pins from the internal signal path, isolating it from the subject being monitored. The series switches are disabled by default. They must be enabled to record ECG. There are also polarity switches that will swap the inputs so that ECGP goes to the minus INA input and ECGN goes to the plus INA input.

Calibration Voltage Sources

Calibration voltage sources are available to provide ±0.25mV (0.5mV_{PP}) or ±0.5mV (1.0mV_{PP}) inputs to the ECG channel with programmable frequency and duty cycle. The sources can be unipolar/bipolar relative to V_{MID}.

Figure 5 illustrates the possible calibration waveforms. Frequency selections are available in 4X increments from 15.625mHz to 256Hz with selected pulse widths varying from 30.5µs to 31.723ms and 50% duty cycle. Signals can be single-ended, differential, or common mode. This flexibility allows end-to-end channel-testing of the ECG signal path.

When applying calibration voltage sources with the device connected to a subject, the series input switches must be disconnected so as not to drive signals into the subject. See registers CNFG_CAL (0x12) and CNFG_EMUX (0x14) to select configuration.

Table 1. Recommended Lead Bias, Current Source Values, and Thresholds for Electrode Impedance

<table>
<tr><th rowspan="2">I_{DC}
V_{TH}</th><th colspan="8">ELECTRODE IMPEDANCE</th></tr>
<tr><th><100kΩ</th><th>100kΩ – 200kΩ</th><th>200kΩ – 400kΩ</th><th>400kΩ – 1MΩ</th><th>1MΩ – 2MΩ</th><th>2MΩ – 4MΩ</th><th>4MΩ – 10MΩ</th><th>10MΩ – 20MΩ</th></tr>
<tr><td>I_{DC} = 10nA</td><td colspan="8">All settings of R_b
$V_{TH} = V_{MID} \pm$ 300mV, ± 400mV</td></tr>
<tr><td>I_{DC} = 20nA</td><td colspan="7">All settings of R_b
All settings of V_{TH}</td><td>All settings of R_b
$V_{TH}=V_{MID}$ ± 400mV, ±450mV, ±500mV</td></tr>
<tr><td>I_{DC} = 50nA</td><td colspan="6">All settings of R_b
All settings of V_{TH}</td><td>All settings of R_b
$V_{TH}=V_{MID}$ ±450mV, ±500mV</td><td></td></tr>
<tr><td>I_{DC} = 100nA</td><td colspan="5">All settings of R_b
All settings of V_{TH}</td><td>All settings of R_b
$V_{TH}=V_{MID}$ ± 400mV, ±450mV, ±500mV</td><td></td><td></td></tr>
</table>

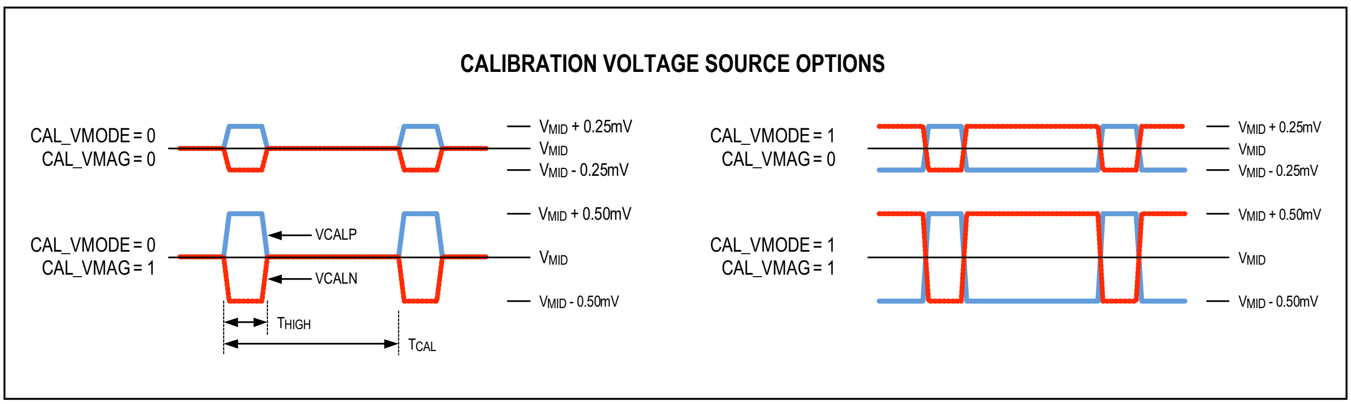


Figure 5. Calibration Voltage Source Options

Gain Settings, Input Range, and Filtering

The device's ECG channel contains an input instrumentation amplifier that provides low-noise, fixed-gain amplification (gain of 20) of the differential signal, rejects differential DC voltage due to electrode polarization, rejects common-mode interference primarily due to AC mains interference, and provides high input impedance to guarantee high CMRR even in the presence of severe electrode impedance mismatch (see Figure 2). The differential DC rejection corner frequency is set by an external capacitor (C_{HPF}) placed between pins CAPP and CAPN, refer to Table 2 for appropriate value selection. There are three recommended options for the cutoff frequency: 5Hz, 0.5Hz, and 0.05Hz. Setting the cutoff frequency to 5Hz provides the most motion artifact rejection at the expense of ECG waveform quality, making it best suited for heart rate monitoring. For ambulatory applications requiring more robust ECG waveforms with moderate motion artifact rejection, 0.5Hz is recommended. Select 0.05Hz for patient monitoring applications in which ECG waveform quality is the primary concern and poor rejection of motion artifacts can be tolerated. The high-pass corner frequency is calculated by the following equation:

$$1/(2\pi \times R_{HPF} \times C_{HPF})$$

R_{HPF} is specified in the Electrical Characteristics table. Following the instrumentation amplifier is a 2-pole active anti-aliasing filter with a 600Hz -3dB frequency that provides 57dB of attenuation at half the modulator sampling rate (approximately 16kHz) and a PGA with programmable gains of 1, 2, 4, and 8V/V for an overall gain of 20, 40, 80, and 160V/V. The instrumentation amplifier and PGA are chopped to minimize offset and 1/f noise. Gain settings are configured via the CNFG_ECG (0x15) register. The useable common-mode range is V_{MID} ±150mV, internal lead biasing can be used to meet this requirement. The useable DC differential range is ±300mV to allow for electrode polarization voltages on each electrode. The input AC differential range is ±32.5mV or 65mV_{PP}.

Fast Recovery Mode

The input instrumentation amplifier has the ability to rapidly recover from an excessive overdrive event such as a defibrillation pulse, high-voltage external pacing, and electro-surgery interference. There are two modes of recovery that can be used: automatic or manual recovery. The mode is programmed by the FAST[1:0] bits in the MNGR_DYN (0x05) register.

Table 2. ECG Analog HPF Corner Frequency Selection

C_{HPF}	HPF CORNER FREQUENCY
0.1µF	≤ 5Hz
1.0µF	≤ 0.5Hz
10µF	≤ 0.05Hz

Table 3. Fast Recovery Mode Recovery Time vs. Number of Samples

SAMPLE RATE (sps)	NUMBER OF SAMPLES	RECOVERY TIME (APPROXIMATE) (ms)
512	255	498
256	127	496
128	63	492
500	249	498
250	124	496
125	64	512
200	99	495
199.8	99	495.5

Automatic mode engages once the saturation counter exceeds approximately 125ms (t_{SAT}). The counter is activated the first time the ADC output exceeds the symmetrical threshold defined by the FAST_TH[5:0] bits in the MNGR_DYN (0x05) register and accumulates the time that the ADC output exceeds either the positive or negative threshold. If the saturation counter exceeds 125ms, it triggers the fast settling mode (if enabled) and resets. The saturation counter can also be reset prior to triggering the fast settling mode if the ADC output falls below the threshold continuously for 125ms (t_{BLW}). This feature is designed to avoid false triggers due to the QRS complex. Once triggered, fast settling mode will be engaged for 500ms, see Figure 6. ECG samples are tagged if they were taken while fast settling mode was asserted.

In manual mode, a user algorithm running on the host microcontroller or an external stimulus input will generate the trigger to enter fast recovery mode. The host microcontroller then enables the manual fast recovery mode in the MNGR_DYN (0x05) register. The manual fast recovery mode can be of a much shorter duration than the automatic mode and allows for more rapid recovery. One such example is recovery from external high-voltage pacing signals in a few milliseconds to allow the observation of a subsequent p-wave.

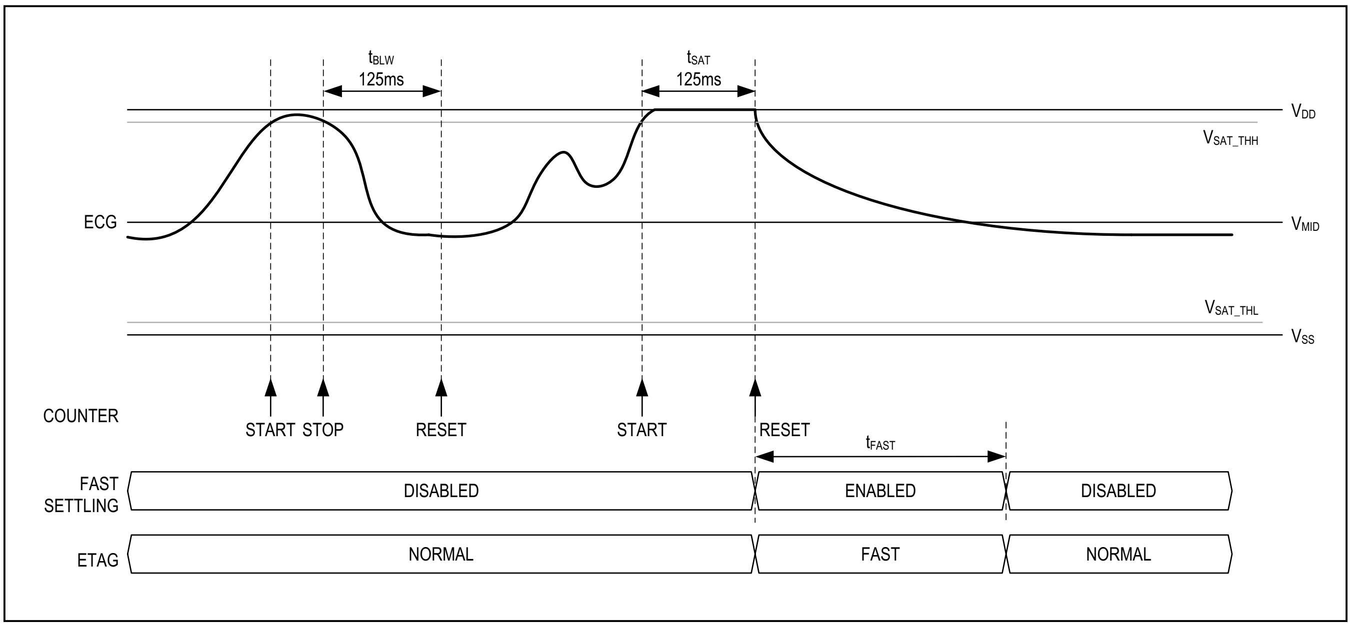


Figure 6. Automatic Fast Settling Behavior