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MAX30002

Ultra-Low-Power, Single-Channel Integrated Bioimpedance (BioZ) AFE

General Description

The MAX30002 is a complete bioimpedance (BioZ), analog front-end (AFE) solution for wearable applications. It offers high performance for clinical and fitness applications, with ultra-low-power for long battery life. The MAX30002 is a single bioimpedance channel capable of measuring respiration.

The bioimpedance channel has ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low-power leads-on detection during standby mode, and a programmable resistive load for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes. The channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high resolution analog-to-digital converter. The bioimpedance channel includes integrated programmable current drive, works with common electrodes, and has the flexibility for 2 or 4 electrode measurements. It also has AC lead off detection.

The MAX30002 is available in a 28-pin TQFN and 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

Applications

- Single-Lead Wireless Patches for In-Patient/Out-Patient Monitoring
- Respiration and Hydration Monitors
- Impedance Based Heart Rate Detection

Benefits and Features

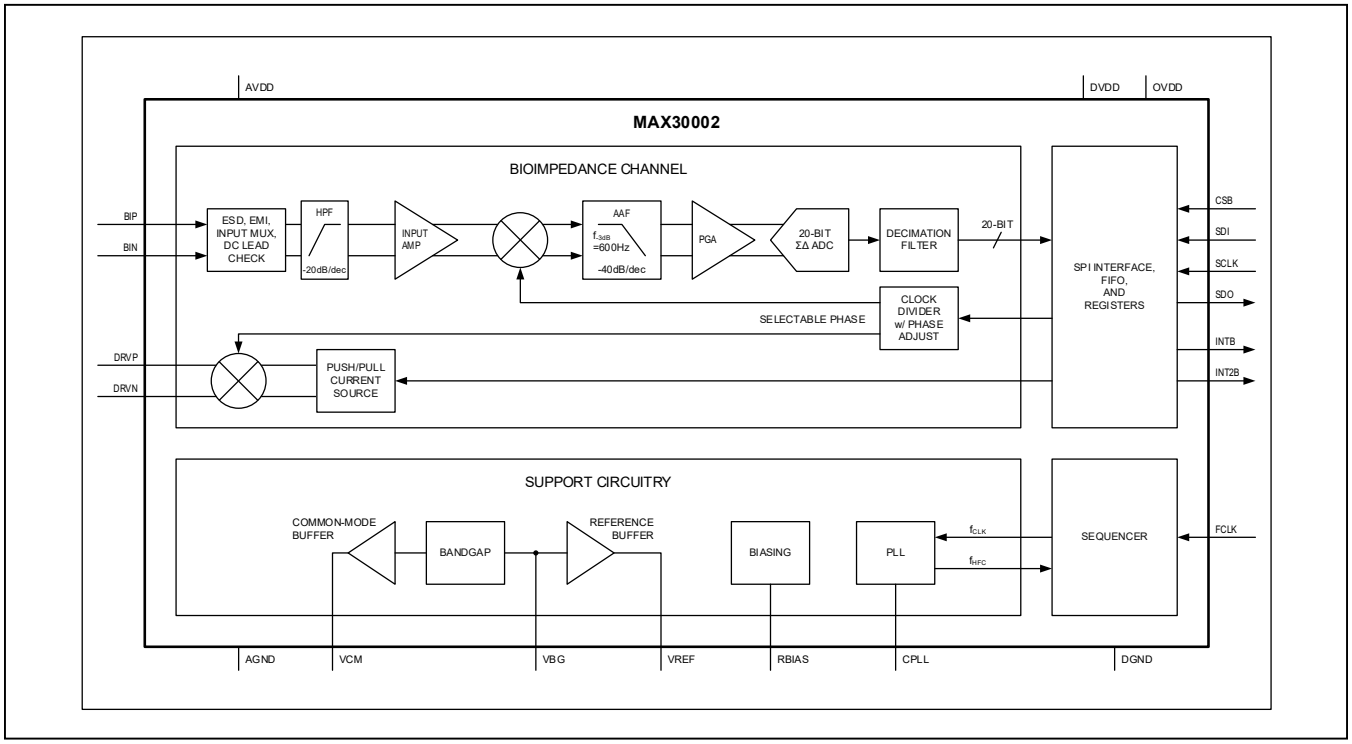
- BioZ AFE with High Resolution Data Converter
  - 17 Bits ENOB with 1.1µV_{P-P} Noise for BioZ
- High AC Dynamic Range of 90mV_{P-P} Will Help Prevent Saturation in the Presence of Motion/Direct Electrode Hits
- Longer Battery Life Compared to Competing Solutions
  - 158µW at 1.1V Supply Voltage
- Leads-On Interrupt Feature Allows to Keep µC in Deep Sleep Mode Until Valid Lead Condition is Detected
  - Lead-On Detect Current: 0.63µA (typ)
- High Accuracy Allows for More Physiological Data Extractions
- 8-Word FIFO Allows the MCU to Stay Powered Down for 256ms with Full Data Acquisition
- High-Speed SPI Interface
- Shutdown Current of 0.58µA (typ)

***Ordering Information* appears at end of data sheet.**

19-100289; Rev 0, 3/18

maxim integrated™

Functional Diagram



Absolute Maximum Ratings

AVDD to AGND .....-0.3V to +2.0V
DVDD to DGND.....-0.3V to +2.0V
AVDD to DVDD .....-0.3V to +0.3V
OVDD to DGND .....-0.3V to +3.6V
AGND to DGND .....-0.3V to +0.3V
CSB, SCLK, SDI, FCLK to DGND .....-0.3V to +3.6V
SDO, INTB, INT2B
to DGND..... -0.3V to the lower of (3.6V and OVDD + 0.3V)
All Other Pins
to AGND ..... -0.3V to the lower of (2.0V and AVDD + 0.3V)
Maximum Current into Any Pin.....±50mA

Continuous Power Dissipation (T_A = +70ºC)
28-Pin TQFN
(derate 34.5mW/ºC above +70ºC).....2758.6mW
30-Bump WLP
(derate 24.3mW/ºC above +70ºC).....1945.5mW
Operating Temperature Range.....0ºC to +70°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10sec).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....44°C/W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOIMPEDANCE (BIOZ) CHANNEL						
Signal Generator Resolution		Square wave generator		1		Bits
DRVP/N Injected Full-Scale Current		Programmable, see Register Map		8 to 96		μA_{P-P}
DRVP/N Injected Current Accuracy		Internal bias resistor	-30		+30	%
		External bias resistor (0.1%, 10ppm, 324kΩ)	-10		+10	
DRVP/N Injected Current Power Supply Rejection				<±1		%/V
DRVP/N Injected Current Temperatue Coefficient		External bias resistor, 32μA_{P-P}, 0 to 70ºC (0.1%, 10ppm, 324kΩ)		50		ppm/°C
DRVP/N Compliance Voltage		V_{DRVP} - V_{DRVN}		±(V_{AVDD}-0.5)		V_{P-P}
Current Injection Frequency		Programmable, see Register Map		0.125 to 131.072		kHz
AC Differential Input Range		Shift from nominal gain < 1% (1.1V)		25		mV
		Shift from nominal gain < 1% (1.8V)		90		
BioZ Channel Gain		Programmable, see Register Map		10 to 80		V/V
ADC Sample Rate		Programmable, see Register Map		24.98 to 64		sps

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				20		Bits
Input Referred Noise (BIP, BIN)		BW = 0.05 to 4Hz, Gain = 20x		0.16		μV_{RMS}
		BW = 0.05 to 4Hz, Gain = 20x		1.1		μV_{P-P}
Impedance Resolution		DC to 4Hz, 32μA_{P-P}, 40kHz, Gain = 20x, R_{BODY} = 680Ω		40		$m\Omega_{P-P}$
Input Analog High Pass Filter		Programmable, see Register Map		125 to 7200		Hz
Demodulation Phase Range		Programmable, see Register Map		0-180		°
Demodulation Phase Resolution		Programmable, see Register Map		11.25		°
Output Digital Low Pass Filter		DLPF[1:0] = 01		4		Hz
		DLPF[1:0] = 10		8		
		DLPF[1:0] = 11		16		
Output Digital High Pass Filter		DHPF[1:0] = 01		0.05		Hz
		DHPF[1:0] = 1x		0.5		
BIOIMPEDANCE (BIOZ) INPUT MUX						
DC Lead Off Check		IMAG[2:0] = 001		5		nA
		IMAG[2:0] = 010		10		
		IMAG[2:0] = 011		20		
		IMAG[2:0] = 100		50		
		IMAG[2:0] = 101		100		
DC Lead Off Comparator Low Threshold		VTH[1:0] = 11 (Note 4)		V_{MID} – 0.50		V
		VTH[1:0] = 10 (Note 5)		V_{MID} – 0.45		
		VTH[1:0] = 01 (Note 6)		V_{MID} – 0.40		
		VTH[1:0] = 00		V_{MID} – 0.30		
DC Lead Off Comparator High Threshold		VTH[1:0] = 11 (Note 4)		V_{MID} + 0.50		V
		VTH[1:0] = 10 (Note 5)		V_{MID} + 0.45		
		VTH[1:0] = 01 (Note 6)		V_{MID} + 0.40		
		VTH[1:0] = 00		V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled, RBIASV[1:0] = 00		50		MΩ
		Lead bias enabled, RBIASV[1:0] = 01		100		
		Lead bias enabled, RBIASV[1:0] = 10		200		
Lead Bias Voltage		Lead bias enabled. Programmable, see Register Map		V_{AVDD}/ 2.15		V

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistive Load Nominal Value	R_{VAL}	Programmable, see Register Map		0.625 to 5.0		kΩ
Resistive Load Modulation Value	R_{MOD}	Programmable, see Register Map		15 to 2960		mΩ
Resistive Load Modulation Frequency	F_{MOD}	Programmable, see Register Map		0.625 to 4.0		Hz
INTERNAL REFERENCE/COMMON-MODE						
V_{BG} Output Voltage	V_{BG}			0.650		V
V_{BG} Output Impedance				100		kΩ
External V_{BG} Compensation Capacitor	C_{BG}		1			µF
V_{REF} Output Voltage	V_{REF}	T_A = +25ºC	0.995	1.000	1.005	V
V_{REF} Temperature Coefficient	TC_{REF}	T_A = 0ºC to +70ºC		10		ppm/ºC
V_{REF} Buffer Line Regulation				330		µV/V
V_{REF} Buffer Load Regulation		I_{LOAD} = 0 to 100µA		25		µV/µA
External V_{REF} Compensation Capacitor	C_{REF}		1	10		µF
VCM Output Voltage	V_{CM}			0.650		V
External V_{CM} Compensation Capacitor	C_{CM}		1	10		µF
DIGITAL INPUTS (SDI, SCLK, CSB, FCLK)						
Input-Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input-Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}		-1		+1	µA
DIGITAL OUTPUTS (SDO, INTB, INT2B)						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Three-State Leakage Current			-1		+1	µA
Three-State Output Capacitance				15		pF

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Analog Supply Voltage	V_{AVDD}	Connect AVDD to DVDD		1.1		2.0	V
Digital Supply Voltage	V_{DVDD}	Connect DVDD to AVDD		1.1		2.0	V
Interface Supply Voltage	V_{OVDD}	Power for I/O drivers only		1.65		3.6	V
Supply Current	I_{AVDD} + I_{DVDD}	BioZ channel , LN_BIOZ = 0 CGMAG[2:0] = 011	V_{AVDD} = V_{DVDD} = +1.1V		144		µA
			V_{AVDD} = V_{DVDD} = +1.8V		163		
			V_{AVDD} = V_{DVDD} = +2.0V		170	190	
		BioZ channel , LN_BIOZ = 1 CGMAG[2:0] = 011	V_{AVDD} = V_{DVDD} = +1.1V		158		
			V_{AVDD} = V_{DVDD} = +1.8V		178		
			V_{AVDD} = V_{DVDD} = +2.0V		185	205	
		ULP Lead On Detect	T_A = +70ºC		1.3		
			T_A = +25ºC		0.63	2.5	
Interface Supply Current	I_{OVDD}	V_{OVDD} = +1.65V, BioZ channel at 64sps (Note 7)			0.1		µA
		V_{OVDD} = 3.6V, BioZ channel at 64sps (Note 7)			0.2	1.1	
Shutdown Current	I_{SAVDD} + I_{SDVDD}	V_{AVDD} = V_{DVDD} = 2.0V	T_A = +70ºC		1.3		µA
			T_A = +25ºC		0.58	2.5	
	I_{SOVDD}	V_{OVDD} = 3.6V, V_{AVDD} = V_{DVDD} = 2.0V				1.1	
ESD PROTECTION							
BIP, BIN, DRVP, DRVN		IEC 61000-4-2 Contact Discharge (Note 8)			±8		kV
		IEC 61000-4-2 Air-Gap Discharge (Note 8)			±15		
		HMM (Human Metal Model)			±8		
TIMING CHARACTERISTICS (NOTE 3)							
SCLK Frequency	f_{SCLK}			0		12	MHz
SCLK Period	t_{CP}			83			ns
SCLK Pulse Width High	t_{CH}			15			ns
SCLK Pulse Width Low	t_{CL}			15			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge (RE)		15			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE		0			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 32nd RE, executed write		10			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd RE, aborted write sequence		15			ns

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise to CSB Fall	t_{CSF}	Applies to 32nd RE	100			ns
CSB Pulse-Width High	t_{CSPW}		20			ns
SDI-to-SCLK Rise Setup Time	t_{DS}		8			ns
SDI to SCLK Rise Hold Time	t_{DH}		8			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pF			40	ns
		C_{LOAD} = 20pF, V_{AVDD} = V_{DVDD} ≥ 1.8V, V_{DVDD} ≥ 2.5V			20	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 20pF	2			ns
CSB Fall to SDO Fall	t_{DOE}	Enable time, C_{LOAD} = 20pF			30	ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			35	ns
FCLK Frequency	f_{FCLK}	External reference clock		32.768		kHz
FCLK Period	t_{FP}			30.52		µs
FCLK Pulse-Width High	t_{FH}	50% duty cycle assumed		15.26		µs
FCLK Pulse-Width Low	t_{FL}	50% duty cycle assumed		15.26		µs

Note 2: All devices are 100% production tested at T_A = +25ºC. Specifications over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization. Not tested in production.
Note 4: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.65V.
Note 5: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.55V.
Note 6: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.45V.
Note 7: f_{SCLK} = 4MHz, burst mode, BFIT[2:0] = 111, C_{SDO} = C_{INTB} = 50pF.
Note 8: ESD test performed with 1kΩ series resistor designed to withstand 8kV surge voltage.

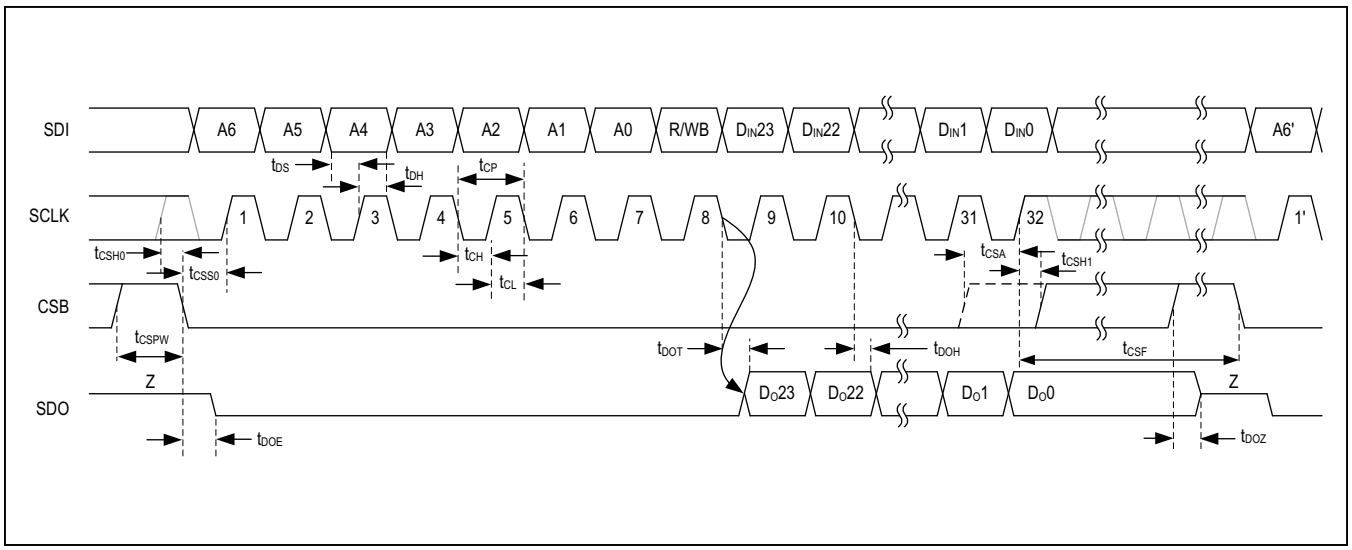


Figure 1a. SPI Timing Diagram

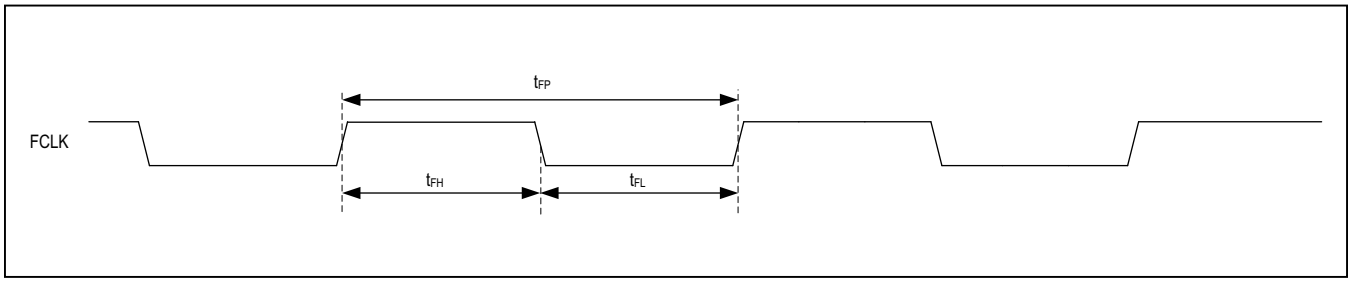
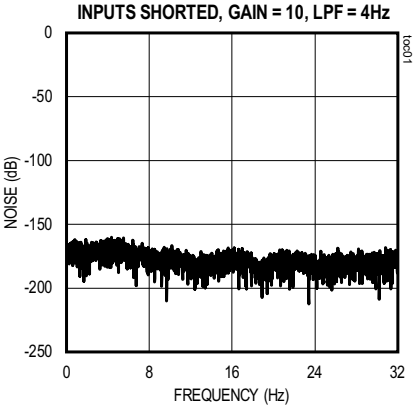


Figure 1b. FCLK Timing Diagram

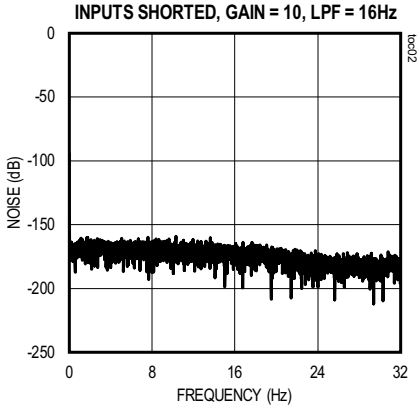
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

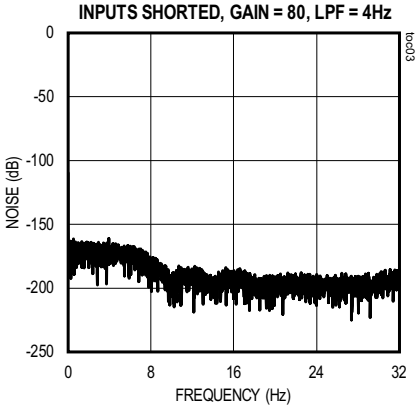
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 4Hz



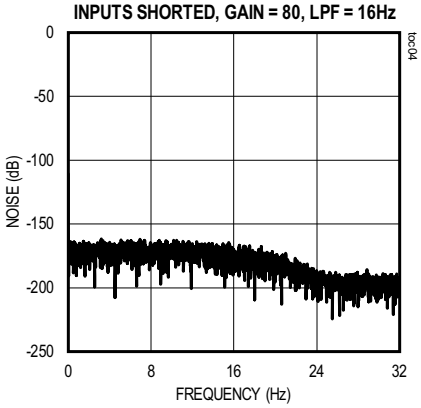
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 16Hz



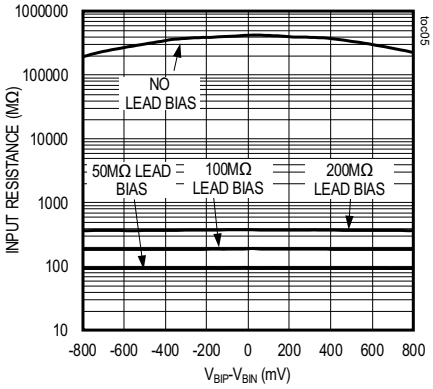
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 4Hz



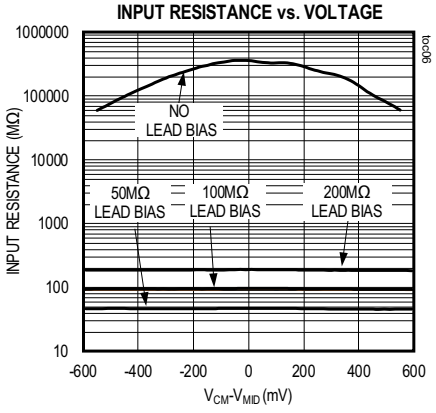
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 16Hz



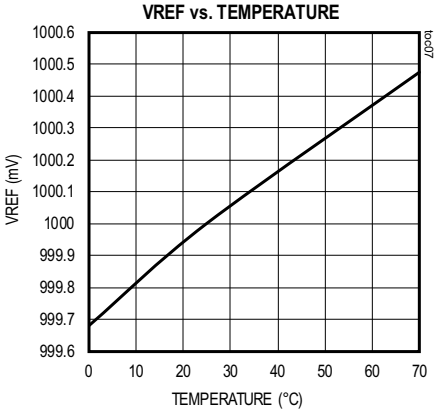
BIOZ DIFFERENTIAL INPUT
RESISTANCE vs. VOLTAGE



BIOZ COMMON-MODE
INPUT RESISTANCE vs. VOLTAGE



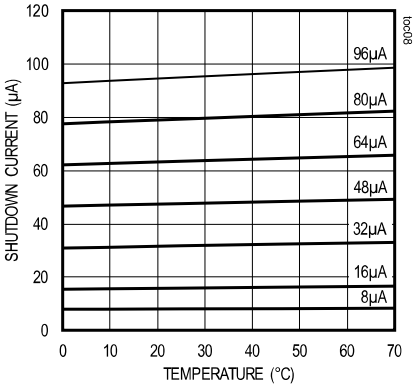
VREF vs. TEMPERATURE



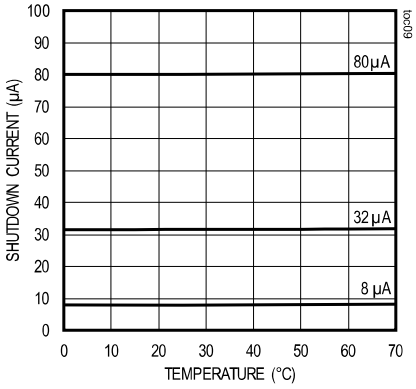
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

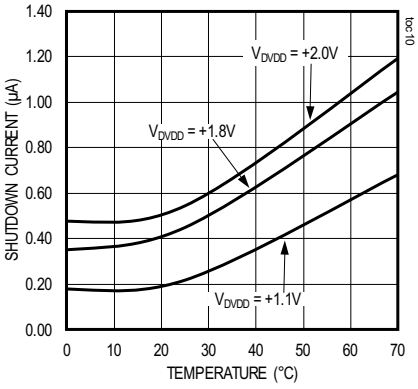
BIOZ DRIVE CURRENT vs. TEMPERATURE
INTERNAL BIASING



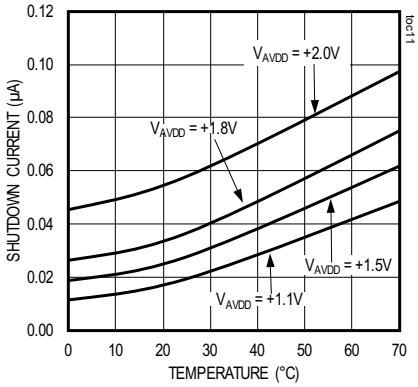
BIOZ DRIVE CURRENT vs. TEMPERATURE
EXTERNAL BIASING



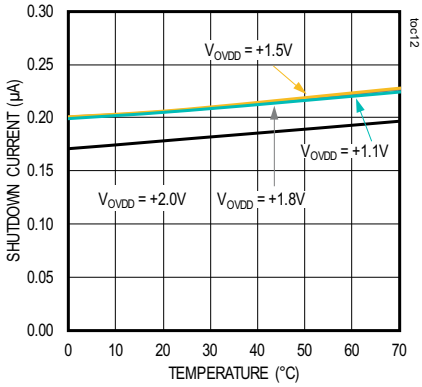
DVDD SHUTDOWN CURRENT



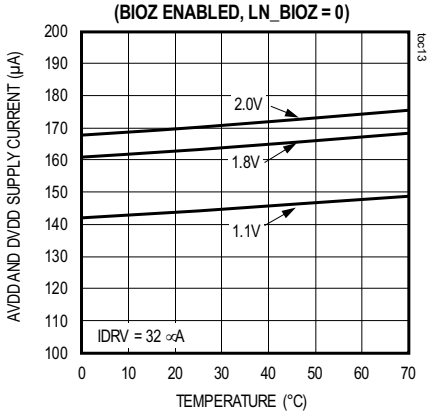
AVDD SHUTDOWN CURRENT



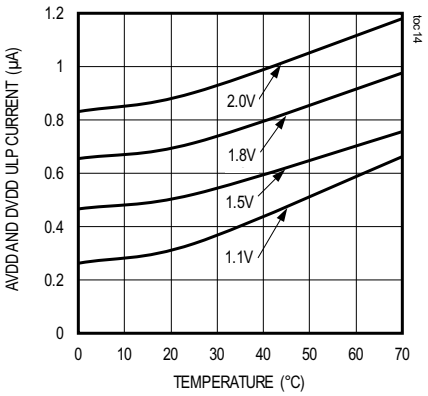
OVDD SHUTDOWN CURRENT



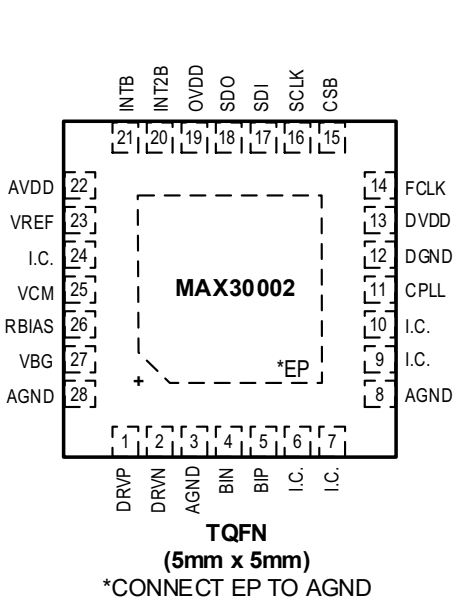
AVDD AND DVDD SUPPLY CURRENT
vs. TEMPERATURE
(BIOZ ENABLED, LN_BIOZ = 0)



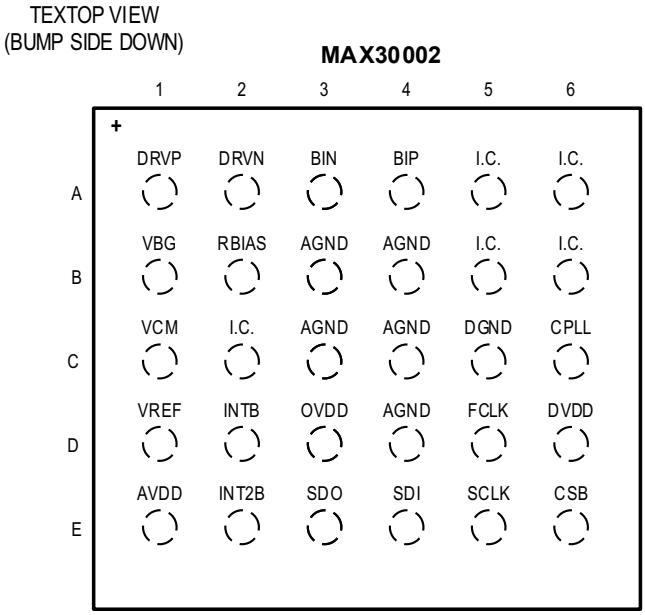
AVDD AND DVDD ULP CURRENT
vs. TEMPERATURE



Pin Configurations



TQFN
(5mm x 5mm)
*CONNECT EP TO AGND



WLP
(2.7mm x 2.9mm)

Pin Description

BUMP	PIN	NAME	FUNCTION
WLP	TQFN		
A1	1	DRVP	Positive Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A2	2	DRVN	Negative Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A3	4	BIN	Bioimpedance Negative Input.
A4	5	BIP	Bioimpedance Positive Input.
A5, A6, B5, B6, C2	6, 7, 9, 10, 24	I.C.	Internally Connected. Connect to AGND.
B1	27	VBG	Bandgap Noise Filter Output. Connect a 1.0µF X7R ceramic capacitor between VBG and AGND.
B2	26	RBIAS	External Resistor Bias. Connect a low tempco resistor between RBIAS and AGND. If external bias generator is not used then RBIAS can be left floating.
B3, B4, C3, C4, D4	3, 8, 28	AGND	Analog Power and Reference Ground. Connect into the printed circuit board ground plane.
C1	25	VCM	Common Mode Buffer Output. Connect a 10µF X5R ceramic capacitor between VCM and AGND.

Pin Description (continued)

BUMP WLP	PIN TQFN	NAME	FUNCTION
C5	12	DGND	Digital Ground for Both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
C6	11	CPLL	PLL Loop Filter Input. Connect 1nF capacitor between CPLL and AGND.
D1	23	VREF	ADC Reference Buffer Output. Connect a 10µF X5R ceramic capacitor between V_{REF} and AGND.
D2	21	INTB	Interrupt Output. INTB is an active-low status output. It can be used to interrupt an external device. INTB is three-stated when disabled.
D3	19	OVDD	Logic Interface Supply Voltage.
D5	14	FCLK	32.768kHz Clock Input. FCLK Controls the sampling of the internal sigma-delta converter and decimator and derives all the internal clocks.
D6	13	DVDD	Digital Core Supply Voltage. Connect to AVDD.
E1	22	AVDD	Analog Core Supply Voltage. Connect to DVDD.
E2	20	INT2B	Interrupt 2 Output. INT2B is an active-low status output. It can be used to interrupt an external device. INT2B is three-stated when disabled.
E3	18	SDO	Serial Data Output. SDO will change state on the falling edge of SCLK when CSB is low. SDO is three-stated when CSB is high.
E4	17	SDI	Serial Data Input. SDI is sampled into the device on the rising edge of SCLK when CSB is low.
E5	16	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
E6	15	CSB	Active-Low Chip-Select Input. Enables the serial interface.
		—	Exposed Pad. Connect EP to AGND.

Detailed Description

BioZ Channel

Figure 2 illustrates the BioZ channel block diagram, excluding the ADC. The channel comprises an input MUX, a programmable analog high-pass filter, an instrumentation amplifier, a mixer, an anti-alias filter, and a programmable gain amplifier. The MUX includes several features such as ESD protection, EMI filtering, lead biasing, leads off checking, and ultra-low-power leads-on checking. The output of this analog channel drives a high-resolution ADC.

Input MUX

The BioZ input MUX shown in Figure 3 contains integrated ESD and EMI protection, DC leads off detect current sources and comparators, lead-on detect, series isolation switches, lead biasing, and a built-in programmable resistor load, for self test.

EMI Filtering and ESD Protection

EMI filtering of the BIP and BIN inputs consists of a single pole, low pass, differential, and common mode filter with the pole located at approximately 2MHz. The BIP and BIN inputs also have input clamps that protect the inputs from ESD events. The DRVP and DRVN outputs also feature ESD protection.

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD.
- ±15kV using the Air Gap Discharge method specified in IEC61000-4-2 ESD.
- ±8kV HMM

For IEC61000-4-2 ESD protection, use 1kΩ or larger series resistors on BIP, BIN, DRVP, and DRVN that are rated to withstand the appropriate surge voltages.

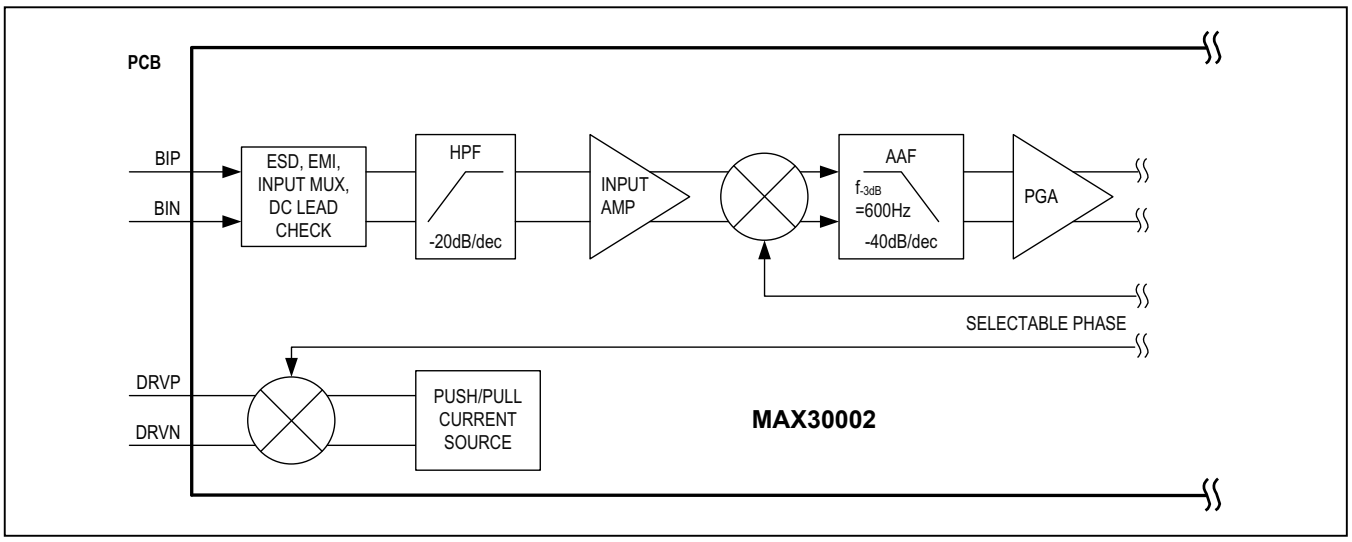


Figure 2. BioZ Channel Input Amplifier, Mixer, and PGA Excluding the ADC and Current Drive Output

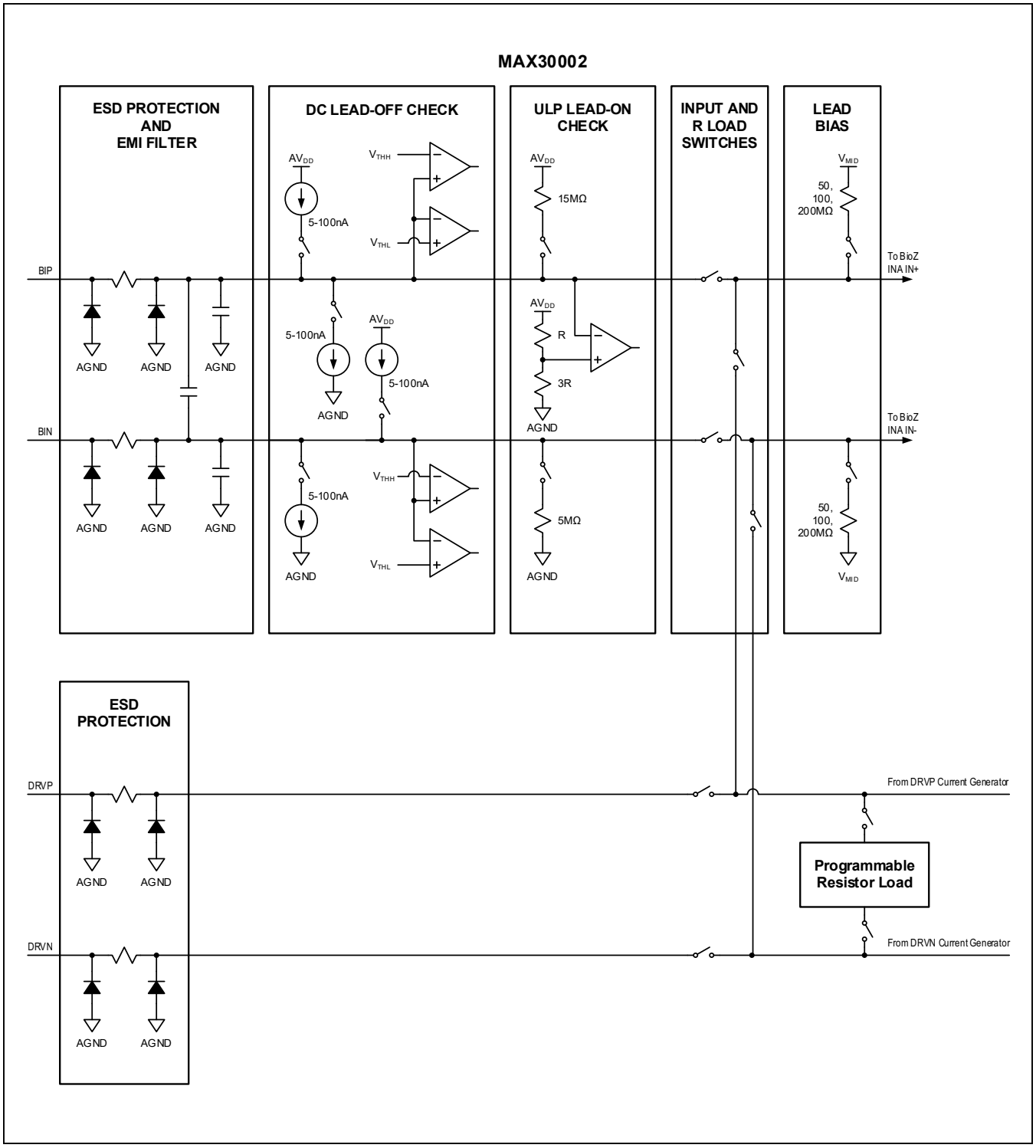


Figure 3. BioZ Input MUX

Leads-Off Detection and ULP Leads-On Detection

MAX30002 provides the capability of detecting lead off scenarios that involve two electrode and four electrode configurations through the use of digital threshold and analog threshold comparisons. There are three methods to detect lead-off for the BioZ channel. There is a compliance monitor for the current generator on the DRVP and DRVN pins detecting when the voltage on the pins is outside its operating range. The CGMON bit in the CNFG_BIOZ (0x18) register enables this function and the BCGMON, BCGMP, and BCGMN bits in the STATUS (0x01) register indicate if the DRVP and DRVN pins are out of compliance. There is a DC lead-off circuit on the BIP and BIN pins that sinks or sources a programmable DC current and window comparators with a programmable threshold to detect the condition. There is a digital lead off detection monitoring the output of the BioZ ADC with programmable under and overvoltage levels performing a digital comparison. The EN_BLOFF bit in the CNFG_GEN (0x10) register enables this function and the BLOFF_HI_IT[7:0] and BLOFF_LO_IT[7:0] bits in the MNGR_DYN (0x05) register sets the digital threshold for detection. Refer to Table 1 for lead off conditions and register settings to allow detection.

The ULP lead-on detect operates by pulling BIN low with a pulldown resistance larger than 5MΩ and pulling BIP high with a pullup resistance larger than 15MΩ. A low-power comparator determines if BIP is pulled below a predefined threshold that occurs when both electrodes make contact with the body. When the impedance between BIP and BIN is less than 20MΩ, the LONINT status bit is asserted, and when the interrupt is enabled on either the INTB or INT2B pin, will alert the µC to a leads-on condition.

A 0nA/V_{MID} ± 300mV selection is available allowing monitoring of the input compliance of the INA during non-DC lead-off checks.

Table 1. BioZ Lead Off Detection Configurations

CONFIGURATION	CONDITION	DRVP/N	BIP/N	MEASURED SIGNAL	REGISTER SETTING TO DETECT
Two-Electrode (Shared DRV/BI)	1 Electrode Off	Rail to Rail	Rail to Rail	Rail to Rail (Saturated Inputs)	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]
Four-Electrode (Force/Sense)	1 DRV Electrode Off, Large Body Coupling	Rail to Rail	Normal	½ Signal	CNFG_BIOZ (0x18), CGMON = 1
	1 DRV Electrode Off, Small Body Coupling	Rail to Rail	Rail to Rail	Rail to Rail (Saturated Inputs)	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]
	1 BI (sense) Electrode Off	Normal	Floating	½ Signal	CNFG_GEN (0x10), EN_DCLOFF = 10
	Both BIP/N (sense) Electrodes Off	Normal	Floating	No Signal	CNFG_GEN (0x10), EN_BLOFF[1:0] = 01 or 11 MNGR_DYN (0x05), BLOFF_LO_IT[7:0]
	1 DRV and 1 BI Electrode Off	Rail to Rail	Wide Swing, Dependent on Body Coupling	Rail to Rail	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]

Lead Bias

The MAX30002 limits the BIP and BIN DC input common mode range to V_{MID} ±150mV. This range can be maintained either through external/internal lead-biasing.

Internal DC lead-biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors to V_{MID} that drive the electrodes within the input common mode requirements of the BioZ channel and can drive the connected body to the proper common mode voltage level. See the EN_RBIAS[1:0], RBIASV[1:0], RBIASP, and RBIASN bits in the CNFG_GEN (0x10) register to select a configuration.

The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a high value resistor such as 1MΩ to limit curent into the body. If this is utilized then the internal lead bias resistors to V_{MID} can be disabled.

Programmable Resistive Load

The programmable resistive load on the DRVP/DRVN pins allows a built in self-test of the current generator (CG) and the entire BioZ channel. Refer to Figure 4 for implementation details.

Nominal resistance can be varied between 5kΩ and 625Ω. The modulation resistance is dependent on the nominal resistance value with resolution of 247.5mΩ to 2.96Ω at the largest nominal resistance (5kΩ) and 15.3mΩ to 46.3mΩ with the smallest nominal resistance (625Ω). Refer to Table 2 for a complete listing of nominal and modulated resistor values. Modulation rate can be programmed between 62.5mHz to 4Hz.

See register CNFG_BMUX (0x17) to select the configuration for modulation rate and resistor value.

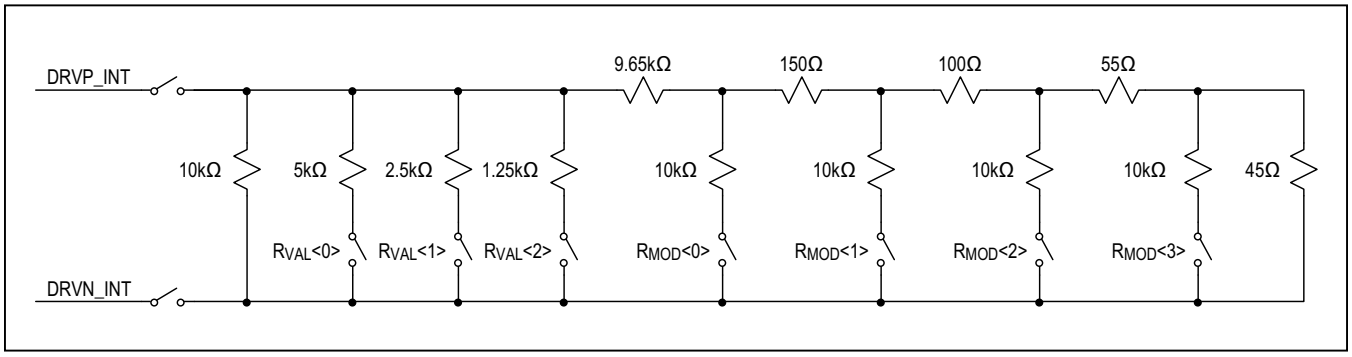


Figure 4. Programmable Resistive Load Topology

Table 2. Programmable Resistive Load Values

R_{NOM} (Ω)	R_{MOD} (mΩ)	R_{VAL}			R_{MOD}			
		<2>	<1>	<0>	<3>	<2>	<1>	<0>
5000.000	-	0	0	0	0	0	0	0
	2960.7	0	0	0	0	0	0	1
	980.6	0	0	0	0	0	1	0
	247.5	0	0	0	0	1	0	0
2500.000	—	0	0	1	0	0	0	0
	740.4	0	0	1	0	0	0	1
	245.2	0	0	1	0	0	1	0
	61.9	0	0	1	0	1	0	0
1666.667	—	0	1	0	0	0	0	0
	329.1	0	1	0	0	0	0	1
	109.0	0	1	0	0	0	1	0
	27.5	0	1	0	0	1	0	0
1250.000	—	0	1	1	0	0	0	0
	185.1	0	1	1	0	0	0	1
	61.3	0	1	1	0	0	1	0
1000.000	—	1	0	0	0	0	0	0
	118.5	1	0	0	0	0	0	1
	39.2	1	0	0	0	0	1	0
833.333	—	1	0	1	0	0	0	0
	82.3	1	0	1	0	0	0	1
	27.2	1	0	1	0	0	1	0
714.286	—	1	1	0	0	0	0	0
	60.5	1	1	0	0	0	0	1
	20.0	1	1	0	0	0	1	0
625.000	—	1	1	1	0	0	0	0
	46.3	1	1	1	0	0	0	1
	15.3	1	1	1	0	0	1	0

Current Generator

The current generator provides square-wave modulating differential current that is AC injected into the body via pins DRVP and DRVN with the bio-impedance sensed differentially through pins BIP and BIN. Two and four electrode configurations are supported for typical wet and dry electrode impedances.

Current amplitudes between $8\mu A_{PK}$ to $96\mu A_{PK}$ are selectable with current injection frequencies between 128Hz and 131.072kHz in power of two increments. See register CNFG_BIOZ (0x18) for configuration selections.

Current amplitude should be chosen so as not exceed $90mV_{P-P}$ at the BIP and BIN pins based on the network impedance at the current injection frequency. A 47nF DC blocking capacitor is required between both DRVP and DRVN and their respective electrodes.

Current Selection and Resolution Calculation Example 1 (Two Terminal with Common Protection)

Selection of the appropriate current is accomplished by first calculating the network impedance at the injection frequency. Worst case electrode impedances should be used.

Given Figure 5 and a current injection frequency of 80kHz, the network impedance is:

$$R_{BODY} + 2R_{P1} + 2R_{P2} + 2R_S + \frac{2R_E}{1 + j\omega R_E C_E} = 2.8k\Omega$$

where R_{BODY} = 100Ω, R_{P1} = 1kΩ, R_{P2} = 200Ω, R_S = 100Ω, R_E = 1MΩ, C_E = 5nF. The maximum current injection is the maximum AC input differential range ($90mV_{PK}$) divided by the network impedance (2.8kΩ) or $32.14\mu A_{PK}$. The closest selectable lower value is $32\mu A_{PK}$.

Given the current injection value and the channel bandwidth (refer to register CNFG_BIOZ (0x18) for digital LPF selection) the resolvable impedance can be calculated by dividing the appropriate input referred noise by the current injection value. For example, with a bandwidth of 4Hz, the input referred noise with a gain of 20V/V is $0.16\mu V_{RMS}$ or $1.1\mu V_{P-P}$. The resolvable impedance is, therefore, $1.1\mu V_{P-P}/32\mu A_{PK}$ = $34m\Omega_{P-P}$ or $5m\Omega_{RMS}$.

Current Selection and Resolution Calculation Example 2 (Four Terminal)

Selection of the appropriate current is accomplished by first calculating the network impedance at the injection frequency. Worst case electrode impedances should be used.

Given Figure 6 and a current injection frequency of 80kHz, the network impedance is:

$$R_{BODY} + 2R_{DP1} + 2R_{DP2} + 2R_S + \frac{2R_E}{1 + j\omega R_E C_E} = 2.7k\Omega$$

where R_{BODY} = 100Ω, R_{DP1} = 1kΩ, R_{DP2} = 200Ω, R_S = 100Ω, R_E = 1MΩ, C_E = 5nF. The maximum current injection is the maximum DRVP/N Compliance Voltage (V_{DD}-0.5V = 0.6V for V_{DD} = 1.1V) divided by the network impedance (2.7kΩ) or $222.2\mu A_{PK}$. The closest selectable lower value is $96\mu A_{PK}$.

Given the current injection value and the channel bandwidth (refer to register CNFG_BIOZ (0x18) for digital LPF selection) the resolvable impedance can be calculated by dividing the appropriate input referred noise by the current injection value. For example, with a bandwidth of 4Hz, the input referred noise with a gain of 40V/V is $0.12\mu V_{RMS}$ or $0.78\mu V_{P-P}$. The resolvable impedance is therefore $0.78\mu V_{P-P}/96\mu A_{PK}$ = $8m\Omega_{P-P}$ or $1.2m\Omega_{RMS}$.

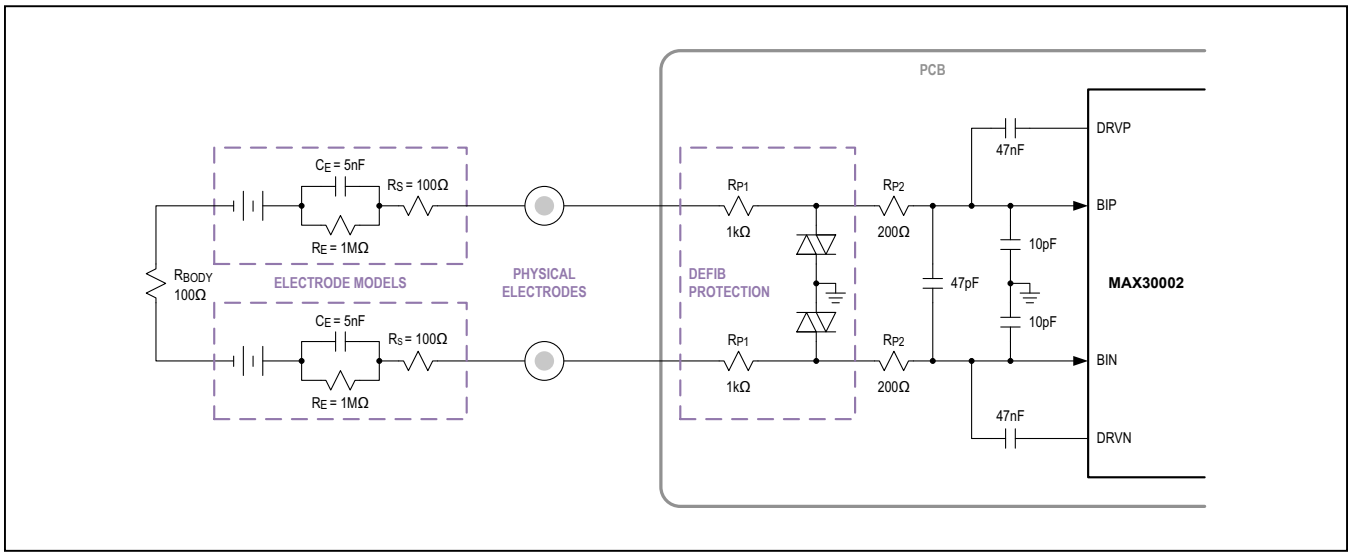


Figure 5. Example Configuration – Two Terminal with Common Protection

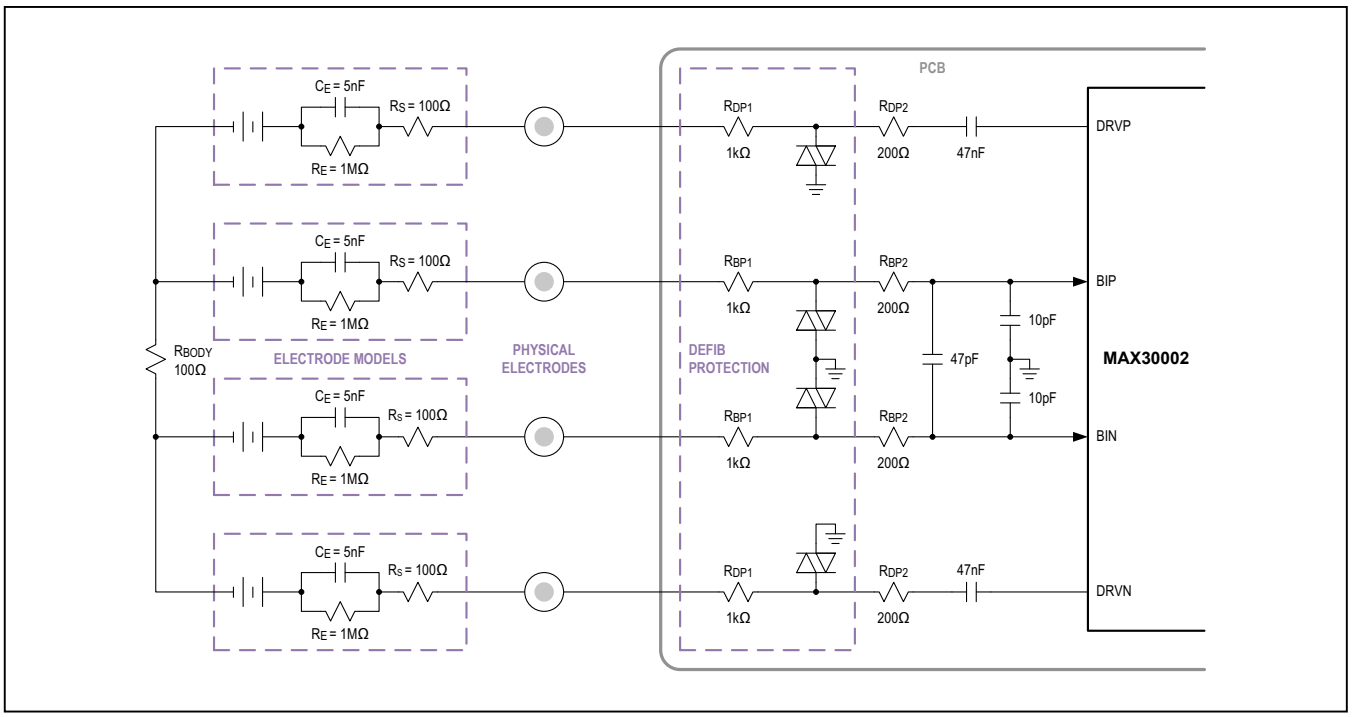


Figure 6. Example Configuration—Four Terminal

Filter Section

The filter section consists of an FIR decimation filter to to convert the ADC sample rate to the final data rate, followed by a programmable IIR and FIR filter to implement HPF and LPF selections, respectively.

The high-pass filter options include a fourth-order IIR Butterworth filter with a 0.05Hz or 0.5Hz corner frequency along with a pass through setting for DC coupling. Lowpass filter options include a 12-tap linear phase (constant group delay) FIR filter with 4Hz, 8Hz, or 16Hz corner frequencies. See register CNFG_BIOZ (0x18) to configure the filters. Table 3 illustrates the BioZ latency in samples and time for each ADC data rate.

Noise Measurements

Table 4 shows the noise performance of the BioZ channel of MAX30002 referred to the BioZ inputs.

Reference and Common Mode Buffer

The MAX30002 features internally generated reference voltages. The bandgap output (V_{BG}) pin requires an external 1.0µF capacitor to AGND and the reference output (V_{REF}) pin requires a 10µF external capacitor to AGND for compensation and noise filtering.

A common-mode buffer is provided to buffer 650mV which is used to drive common mode voltages for internal blocks. Use a 10µF external capacitor between V_{CM} to AGND to provide compensation and noise filtering. The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a high value resistor such as 1MΩ. If this is utilized then the internal lead bias resistors to V_{MID} may be disabled if the input signals are within the common-mode input range.

Table 3. BioZ Latency in Samples and Time as a Function of BioZ Data Rate and Decimation

BIOZ CHANNEL SETTINGS			LATENCY			
INPUT SAMPLE RATE (Hz)	OUTPUT DATA RATE (sps)	DECIMATION RATIO	WITHOUT LPF (INPUT SAMPLES)	WITH LPF (INPUT SAMPLES)	WITHOUT LPF(ms)	WITH LPF (ms)
32,768	64	512	3,397	6,469	103.668	197.418
32,000	62.5	512	3,397	6,469	106.156	202.156
32,000	50	640	5,189	9,029	162.156	282.156
31,968	49.95	640	5,189	9,029	162.319	282.439
32,768	32	1,024	7,557	13,701	230.621	418.121
32,000	31.25	1,024	7,557	13,701	236.156	428.156
32,000	25	1,280	9,605	17,285	300.156	540.156
31,968	24.975	1,280	9,605	17,285	300.457	540.697

Table 4. BioZ Channel Noise Performance

GAIN	BANDWIDTH	NOISE		SNR	ENOB
V/V	Hz	μV_{RMS}	μV_{P-P}	dB	Bits
10	4	0.23	1.55	101.6	16.6
	8	0.28	1.87	100.0	16.3
	16	0.35	2.34	98.0	16.0
20	4	0.16	1.10	104.9	17.1
	8	0.19	1.27	103.4	16.9
	16	0.26	1.68	100.9	16.5
40	4	0.12	0.78	107.6	17.6
	8	0.16	1.07	104.9	17.1
	16	0.22	1.48	102.0	16.7
80	4	0.11	0.72	108.3	17.7
	8	0.15	1.01	105.3	17.2
	16	0.21	1.42	102.4	16.7

$SNR = 20log(V_{IN}(RMS)/V_N(RMS))$, $ENOB = (SNR – 1.76)/6.02$

V_{INP-P} = 100mV, V_{INRMS} = 35.4mV for a gain of 10V/V. The input amplitude is reduced accordingly for high gain settings.

SPI Interface Description

32 Bit Normal Mode Read/Write Sequences

The MAX30002 interface is SPI/QSPI/Micro-wire/DSP compatible. The operation of the SPI interface is shown in Figure 1a. Data is strobed into the MAX30002 on SCLK rising edges. The device is programmed and accessed by a 32 cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one byte command word (comprised of a seven bit address and a Read/Write mode indicator, i.e., A[6:0] + R/$\overline{W}$) followed by a three-byte data word. The MAX30002 is compatible with CPOL = 0/CPHA = 0 and CPOL = 1/CPHA = 1 modes of operation.

Write mode operations will be executed on the 32nd SCLK rising edge using the first four bytes of data available. In write mode, any data supplied after the 32nd SCLK rising edge will be ignored. Subsequent writes require CSB to de-assert high and then assert low for the next write command. In order to abort a command sequence, the rise of CSB must precede the updating (32nd) rising-edge of SCLK, meeting the t_{CSA} requirement.

Read mode operations will access the requested data on the 8th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the µC to sample the data MSB on the 9th SCLK rising edge. Configuration, Status, and FIFO data are all available via normal mode read back sequences. If more than 32 SCLK rising edges are provided in a normal read sequence then the excess edges will be ignored and the device will read back zeros.

If accessing the STATUS register or the BIOZ FIFO memory, all interrupt updates will be made and the internal FIFO read pointer will be incremented in response to the 30th SCLK rising edge, allowing for internal synchronization operations to occur. See the data tag structures used within the FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing normal mode read back operations.

Burst Mode Read Sequence

The MAX30002 provides commands to read back the BIOZ FIFO memory in a burst mode to increase data transfer efficiency. Burst mode uses different register addresses than the normal read sequence register addresses. The first 32 SCLK cycles operate exactly as described for the normal mode. If the µC continues to provide SCLK edges beyond the 32nd rising edge, the MSB of the next available FIFO word will be presented on the next falling SCLK edge, allowing the µC to sample the MSB of the next word on the 33rd SCLK rising edge. Any affected interrupts and/or FIFO read pointers will be incremented in response to the (30+nx24)th SCLK rising edge where n is an integer starting at 0. (i.e., on the 30th, 54th, and 78th SCLK rising-edges for a three-word, burst-mode transfer).

This mode of operation will continue for every 24 cycle sub frame, as long as there is valid data in the FIFO. See the data tag structures used within each FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing burst mode read back operations.

There is no burst mode equivalent in write mode.

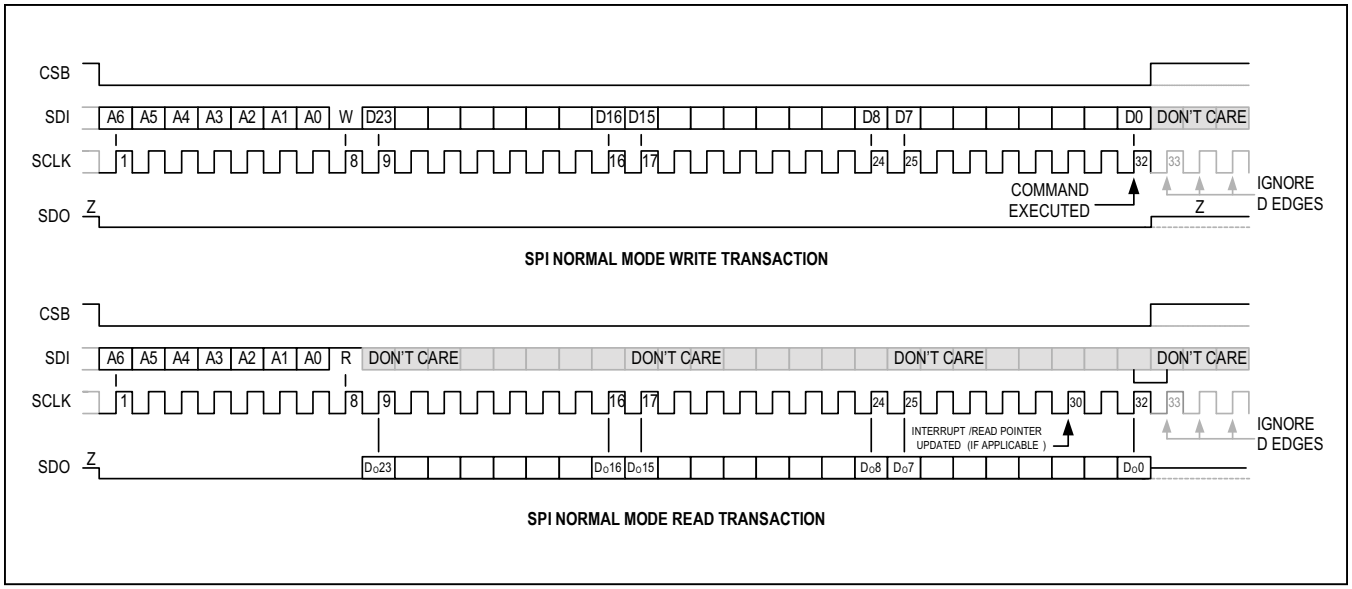


Figure 7. SPI Normal Mode Transaction Diagram

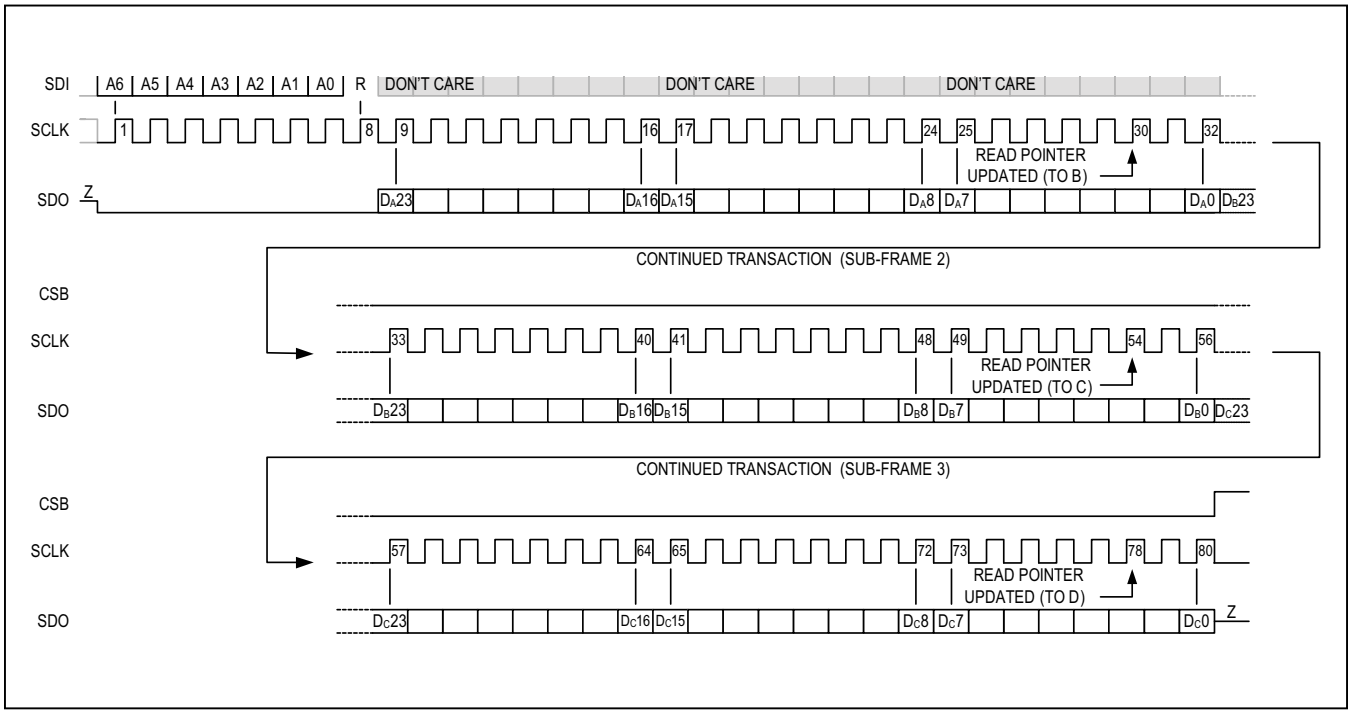


Figure 8. SPI Burst Mode Read Transactions Diagram

User Command and Register Map

REG [6:0]	NAME	R/W MODE	DATA INDEX							
			23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x00	NO-OP	R/W	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x
0x01	STATUS	R	x	x	x	DCLOFFINT	BINT	BOVF	BOVER	BUNDR
			BCGMON	x	x	x	LONINT	x	SAMP	PLLINT
			x	x	BCGMP	BCGMN	LDOFF_PH	LDOFF_PL	LDOFF_NH	LDOFF_NL
0x02 0x03	EN_INT EN_INT2	R/W	x	x	x	EN_DCLOFFINT	EN_BINT	EN_BOVF	EN_BOVER	EN_BUNDR
			EN_BCGMON	x	x	x	EN_ LONINT	x	EN_SAMP	EN_ PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	
0x04	MNGR_ INT	R/W	x	x	x	x	x	BFIT[2:0]		
			x	x	x	x	x	x	x	x
			x	x	x	x	CLR_PEDGE	CLR_ SAMP	SAMP_IT[1:0]	
0x05	MNGR_ DYN	R/W	x	x	x	x	x	x	x	x
			BLOFF_HI_IT[7:0]							
			BLOFF_LO_IT[7:0]							
0x08	SW_RST	W	Data Required for Execution = 0x000000							
0x09	SYNCH	W	Data Required for Execution = 0x000000							
0x0A	FIFO_ RST	W	Data Required for Execution = 0x000000							
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	x	1	0	x	x	x	x
			x	x	x	x	x	x	x	x
0x10	CNFG_ GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		x	EN_BIOZ	x	x
			EN_BLOFF[1:0]		EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN
0x17	CNFG_ BMUX	R/W	x	x	OPENP	OPENN	CALP_SEL[1:0]		CALN_SEL[1:0]	
			x	x	CG_MODE[1:0]		EN_BIST	RNOM[2:0]		
			x	RMOD[2:0]			x	x	FBIST[1:0]	
0x18	CNFG_ BIOZ	R/W	RATE	AHPF[2:0]			EXT_RBIAS	LN_BIOZ	GAIN[1:0]	
			DHPF[1:0]		DLPF[1:0]		FCGEN[3:0]			
			CGMON	CGMAG[2:0]			PHOFF[3:0]			
0x22	BIOZ_ FIFO_ BURST	R+	BIOZ FIFO Burst Mode Read Back				See FIFO Description for details			
0x23	BIOZ_ FIFO	R	BIOZ FIFO Normal Mode Read Back				See FIFO Description for details			
0x7F	NO-OP	R/W	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x

Note: *R/W Mode R+ denotes burst mode.*

x = Don't Care

Register Description

NO_OP (0x00 and 0x7F) Registers

No Operation (NO_OP) registers are read-write registers that have no internal effect on the device. If these registers are read back, DOUT remains zero for the entire SPI transaction. Any attempt to write to these registers is ignored without impact to internal operation.

STATUS (0x01) Register

STATUS is a read-only register that provides a comprehensive overview of the current status of the device. The first two bytes indicate the state of all interrupt bits (regardless of whether interrupts are enabled in registers EN_INT (0x02) or EN_INT2 (0x03)). All interrupt bits are active high. The last byte includes detailed status information for conditions associated with the other interrupt bits.

Table 5. STATUS (0x01) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x01	STATUS	R	x	x	x	DCLOFF INT	BINT	BOVF	BOVER	BUNDR
			BCGMON	x	x	x	LONINT	x	SAMP	PLLINT
			x	x	BCGMP	BCGMN	LDOFF_PH	LDOFF_PL	LDOFF_NH	LDOFF_NL

Table 6. Status (0x01) Register Meaning

INDEX	NAME	MEANING
D[20]	DCLOFFINT	DC Lead-Off Detection Interrupt. Indicates that the MAX30002 has determined it is in a BioZ leads off condition (as selected in CNFG_GEN) for more than 90ms. Remains active as long as the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[19]	BINT	BIOZ FIFO Interrupt. Indicates BIOZ records meeting/exceeding the BIOZ FIFO Interrupt Threshold (BFIT) are available for read back. Remains active until BIOZ FIFO is read back to the extent required to clear the BFIT condition.
D[18]	BOVF	BIOZ FIFO Overflow. Indicates the BIOZ FIFO has overflowed and the data record has been corrupted. Remains active until a FIFO Reset (recommended) or SYNCH operation is issued.
D[17]	BOVER	BIOZ Over Range. Indicates the BIOZ output magnitude has exceeded the BIOZ High Threshold (BLOFF_HI_IT) for at least 100ms, recommended for use in 2 and 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[16]	BUNDR	BIOZ Under Range. Indicates the BIOZ output magnitude has been bounded by the BIOZ Low Threshold (BLOFF_LO_IT) for at least 1.7 seconds, recommended for use in 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[15]	BCGMON	BIOZ Current Generator Monitor. Indicates the DRVP and/or DRVN current generator has been in a Lead Off condition for at least 128ms, recommended for use in 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).

Table 6. Status (0x01) Register Meaning (continued)

INDEX	NAME	MEANING
D[11]	LONINT	Ultra-Low Power (ULP) Leads-On Detection Interrupt. Indicates that the MAX30002 has determined it is in a leads-on condition (as selected in CNFG_GEN). LONINT is asserted whenever EN_ULP_LON[1:0] in register CNFG_GEN is set to either 01 or 10 to indicate that the ULP leads on detection mode has been enabled. The STATUS register has to be read back once after ULP leads on detection mode has been activated to clear LONINT and enable leads on detection. LONINT remains active while the leads-on condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[9]	SAMP	Sample Synchronization Pulse. Issued on the BioZ base-rate sampling instant, for use in assisting µC monitoring and synchronizing other peripheral operations and data, generally recommended for use as a dedicated interrupt. Frequency is selected by SAMP_IT[1:0], see MNGR_INT for details. Clear behavior is defined by CLR_SAMP, see MNGR_INT for details.
D[8]	PLLINT	PLL Unlocked Interrupt. Indicates that the PLL has not yet achieved or has lost its phase lock. PLLINT will only be asserted when the PLL is powered up and active (BIOZ Channel enabled). Remains asserted while the PLL unlocked condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[5]	BCGMP	BIOZ Current Generator Monitor Positive Output. Indicates the DRVP current generator has been in a Lead Off condition for at least 128ms. This is not strictly an interrupt bit, but is a detailed status bit, covered by the BCGMON interrupt bit.
D[4]	BCGMN	BIOZ Current Generator Monitor Negative Output. Indicates the DRVN current generator has been in a Lead Off condition for at least 128ms. This is not strictly an interrupt bit, but is a detailed status bit, covered by the BCGMON interrupt bit.
D[3]	LDOFF_PH	DC Lead Off Detection Detailed Status. Indicates that the MAX30002 has determined (as selected by CNFG_GEN): BIP is above the high threshold (V_{THH}), BIP is below the low threshold (V_{THL}), BIN is above the high threshold (VT_{HH}), BIN is below the low threshold (V_{THL}), respectively. Remains active as long as the leads-off detection is active and the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK). LDOFF_PH to LDOFF_NL are detailed status bits that are asserted at the same time as DCLOFFINT.
D[2]	LDOFF_PL	
D[1]	LDOFF_NH	
D[0]	LDOFF_NL	