Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-1453; Rev 1; 9/10

MAXIM

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

General Description

The MAX3140 is a complete universal asynchronous receiver-transmitter (UART) and a true fail-safe RS-485/RS-422 transceiver combined in a single 28-pin QSOP package for space-, cost-, and power-constrained applications. The MAX3140 saves additional board space as well as microcontroller (µC) I/O pins by featuring an SPI™/QSPI™/MICROWIRE™-compatible serial interface. It is pin-programmable for configuration in all RS-485/RS-422 networks.

The MAX3140 includes a single RS-485/RS-422 driver and receiver featuring true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This feature provides immunity to faults without requiring complex termination. The MAX3140 provides software-selectable control of half- or full-duplex operation, data rate, slew rate, and transmitter and receiver phase. The RS-485 driver slew rate is programmable to minimize EMI and results in maximum data rates of 115kbps, 500kbps, and 10Mbps. Independent transmitter/receiver phase control enables software correction of twisted-pair polarity reversal. A 1/8-unit-load receiver input impedance allows up to 256 transceivers on the bus.

The MAX3140's UART includes an oscillator circuit derived from an external crystal, and a baud-rate generator with software-programmable divider ratios for all common baud rates from 300 baud to 230k baud. The UART features an 8-word-deep receive FIFO that minimizes processor overhead and provides a flexible interrupt with four maskable sources, including address recognition on 9-bit networks. Two control lines are included for hardware handshaking—one input and one output.

The MAX3140 operates from a single +5V supply and typically consumes only 645µA with the receiver active. Hardware-invoked shutdown reduces supply current to only 20µA. The UART and RS-485/RS-422 functions can be used together or independently since the two functions share only supply and ground connections (the MAX3140 is hardware- and software-compatible with the MAX3100 and MAX3089).

Applications

Industrial-Control Local Area Networks	Transceivers for EMI-Sensitive Applications
HVAC and Building Control	Embedded Systems
Point-of-Sale Devices	Intelligent Instrumentation

SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Pin Configuration appears at end of data sheet.

Features

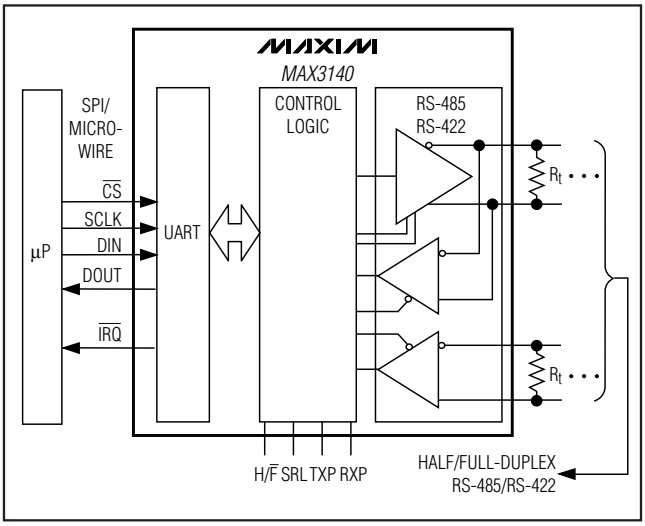
- **Integrated UART and RS-485/RS-422 Transceiver in a Single 28-Pin QSOP**
- **SPI/MICROWIRE-Compatible Interface Saves µC I/O Pins**
- **True Fail-Safe Receiver Output Eliminates Complex Network Termination**
- **Pin-Programmable RS-485/RS-422 Features**
  - **Half/Full-Duplex Operation**
  - **Slew-Rate Limiting for Reduced EMI**
  - **115kbps/500kbps/10Mbps Data Rates**
  - **Receiver/Transmitter Phase for Twisted-Pair Polarity Reversal**
- **Full-Featured UART**
  - **Programmable Up to 230k baud with a 3.6864MHz Crystal**
  - **8-Word Receive FIFO Minimizes Processor Overhead**
  - **9-Bit Address-Recognition Interrupt**
- **Allows Up to 256 Transceivers on the Bus**
- **Low 20µA Hardware Shutdown Mode**
- **Hardware/Software-Compatible with MAX3100 and MAX3089**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3140CEI+	0°C to +70°C	28 QSOP
MAX3140EEI+	-40°C to +85°C	28 QSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Application Circuit



SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....+6V
Input Voltage to GND ($\overline{CS}$, $\overline{SHDN}$, X1, $\overline{CTS}$, RX, DIN, SCLK, $\overline{RE}$, DE, H/$\overline{F}$, SRL, TXP, RXP, DI) .....-0.3V to (V_{CC} + 0.3V)
Output Voltage to GND
DOUT, $\overline{RTS}$, TX, X2, RO.....-0.3V to (V_{CC} + 0.3V)
$\overline{IRQ}$ .....-0.3V to +6V
Driver Output Voltage (Y, Z) .....±13V
Receiver Input Voltage, Half Duplex (Y, Z)..... ±13V
Receiver Input Voltage, Full Duplex (A, B) .....±25V
TX, $\overline{RTS}$ Output Current 100mA
X2, DOUT, $\overline{IRQ}$ Short-Circuit Duration (to V_{CC} or GND) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-pin QSOP (derate 10.8mW/°C above +70°C).....860mW
Operating Temperature Ranges
MAX3140CEI .....0°C to +70°C
MAX3140EEI .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, DE = V_{CC}, $\overline{RE}$ = GND, $\overline{SHDN}$ = V_{CC}, f_{XTL} = 1.8432MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured with V_{CC} = +5V, UART configured for 9600 baud, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLY								
Supply Voltage	V_{CC}				4.75		5.25	V
Supply Current	I_{CC}	$\overline{SHDN}$ = V_{CC}; SHDNi bit = 0, no load	SRL = V_{CC}	DE = V_{CC}		0.7	1.9	mA
				DE = GND		0.64	1.6	
			SRL = GND or open	DE = V_{CC}		0.74	2	
				DE = GND		0.69	1.8	
Supply Current with Only UART Shut Down	I_{CC} SHDN UART	$\overline{SHDN}$ = GND or SHDNi bit = 1				0.47	1	mA
Supply Current with Both RS-485 Transceiver and UART Shut Down	I_{CC} SHDN (FULL)	$\overline{SHDN}$ = GND or SHDNi bit = 1; DE = GND; $\overline{RE}$ = V_{CC}					20	µA
UART OSCILLATOR INPUT (X1)								
Input High Voltage	V_{IH1}				0.7V_{CC}			V
Input Low Voltage	V_{IL1}						0.2V_{CC}	V
Input Current	I_{IN1}	V_{X1} = 0 or V_{CC}	SHDNi bit = 0				25	µA
			SHDNi bit = 1				2	
Input Capacitance	C_{IN1}					5		pF
UART LOGIC INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$, $\overline{CTS}$, RX)								
Input High Voltage	V_{IH2}				0.7V_{CC}			V
Input Low Voltage	V_{IL2}						0.3V_{CC}	V
Input Hysteresis	V_{HYST2}					250		mV
Input Leakage Current	I_{LKG1}						±1	µA
Input Capacitance	C_{IN2}					5		pF
UART OUTPUTS (DOUT, TX, $\overline{RTS}$)								
Output High Voltage	V_{OH1}	I_{SOURCE} = 5mA; DOUT, $\overline{RTS}$			V_{CC} - 0.5			V
		I_{SOURCE} = 10mA; TX only			V_{CC} - 0.5			
Output Low Voltage	V_{OL1}	I_{SINK} = 4mA; DOUT, $\overline{RTS}$					0.4	V
		I_{SINK} = 25mA; TX only					0.9	
Output Leakage	I_{LKG2}	$\overline{CS}$ = V_{CC}; D_{OUT} only					±1	µA
Output Capacitance	C_{OUT1}					5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, DE = V_{CC}, $\overline{RE}$ = GND, $\overline{SHDN}$ = V_{CC}, f_{XTL} = 1.8432MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured with V_{CC} = +5V, UART configured for 9600 baud, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UART $\overline{IRQ}$ OUTPUT (Open Drain)							
Output Low Voltage	V_{OL2}	I_{SINK} = 4mA				0.4	V
Output Leakage	I_{LKG3}	$V_{\overline{IRQ}}$ = V_{CC}				±1	µA
Output Capacitance	C_{OUT2}				5		pF
RS-485 DRIVER							
Differential Output Voltage	V_{OD1}	No load, Figure 1				5	V
	V_{OD2}	R = 50Ω (RS-422), Figure 1		2.0			
		R = 27Ω (RS-422), Figure 1		1.5			
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R = 50Ω or R = 27Ω, Figure 1 (Note 2)				0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω or R = 27Ω, Figure 1				3	V
Change In Magnitude of Common-Mode Voltage	ΔV_{OC}	R = 50Ω or R = 27Ω, Figure 1 (Note 2)				0.2	V
Input High Voltage	V_{IH1}	DE, DI, $\overline{RE}$		2.0			V
		H/$\overline{F}$, TXP, RXP		2.4			
Input Low Voltage	V_{IL1}	DE, DI, RE, H/$\overline{F}$, TXP, RXP				0.8	V
DI Input Hysteresis	V_{HYS}	SRL = V_{CC} or unconnected			100		mV
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
	I_{IN2}	H/$\overline{F}$, TXP, RXP, internal pull-down		10		40	
SRL Input High Voltage	V_{IH2}			V_{CC} - 0.8			V
SRL Input Middle Voltage	V_{IM2}	(Note 3)		0.4 • V_{CC}		0.6 • V_{CC}	V
SRL Input Low Voltage	V_{IL2}					0.8	V
SRL Input Current	I_{IN3}	SRL = V_{CC}				75	µA
		SRL = GND (Note 3)		-75			
Full-Duplex Input Current (A and B)	I_{IN4}	DE = GND	V_{IN} = 12V			125	µA
		V_{CC} = GND or 5.25V	V_{IN} = -7V			-75	
Full-Duplex Output Leakage (Y and Z)	I_O	DE = GND	V_{IN} = 12V			125	µA
		V_{CC} = GND or 5.25V	V_{IN} = -7V	-100			
Short-Circuit Output Current	I_{OSD}	(Note 4)	-7V ≤ V_{OUT} ≤ V_{CC}	-250			mA
			0 ≤ V_{OUT} ≤ 12V			250	
			0 ≤ V_{OUT} ≤ V_{CC}	±25			
RS-485 RECEIVER							
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200	-125	-50	mV
Input Hysteresis	ΔV_{TH}				25		mV
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA, V_{ID} = -50mV		V_{CC} - 1.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA, V_{ID} = -200mV				0.4	V
Three-State Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		96			kΩ
Output Short-Circuit Current	I_{OSR}	0 ≤ V_{RO} ≤ V_{CC}		±7		±95	mA

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

UART SWITCHING CHARACTERISTICS

(V_{CC} = +5V ±5%, f_{XTL} = 1.8432MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured with V_{CC} = +5V, UART configured for 9600 baud, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UART AC TIMING (Figure 1)						
$\overline{CS}$ Low to DOUT Valid	t_{DV}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ High to DOUT Tri-State	t_{TR}	C_{LOAD} = 100pF, $R_{\overline{CS}}$ = 10kΩ			100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Hold Time	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns
DIN to SCLK Setup Time	t_{DS}		100			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Period	t_{CP}		238			ns
SCLK High Time	t_{CH}		100			ns
SCLK Low Time	t_{CL}		100			ns
SCLK Rising Edge to $\overline{CS}$ Falling	t_{CS0}		100			ns
$\overline{CS}$ Rising Edge to SCLK Rising	t_{CS1}		200			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
Output Rise Time	t_r	TX, $\overline{RTS}$, DOUT; C_{LOAD} = 100pF		10		ns
Output Fall Time	t_f	TX, $\overline{RTS}$, DOUT, $\overline{IRQ}$; C_{LOAD} = 100pF		10		ns

SWITCHING CHARACTERISTICS—SRL = Unconnected

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	500	2030	2600	ns
	t_{DPHL}		500	2030	2600	
Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-3	±200	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	667	1320	2500	ns
Maximum Data Rate	f_{MAX}		115			kbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed			3500	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed			3500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		127	200	ns
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Differential Receiver Skew	t_{RSKD}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 15pF, S2 closed			6000	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 15pF, S1 closed			6000	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 100pF, S1 closed			3500	ns

SWITCHING CHARACTERISTICS—SRL = V_{CC}

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	720	1000	ns
	t_{DPHL}		250	720	1000	
Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-3	±100	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	200	530	950	ns
Maximum Data Rate	f_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed			2500	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed			2500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		127	200	ns
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Differential Receiver Skew	t_{RSKD}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 15pF, S2 closed			4500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 15pF, S1 closed			4500	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 100pF, S1 closed			3500	ns

SWITCHING CHARACTERISTICS—SRL = GND

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		34	60	ns
	t_{DPHL}			34	60	
Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		-2.5	±10	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		14	25	ns
Maximum Data Rate	f_{MAX}		10			Mbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed			150	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed			150	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		106	150	ns
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Differential Receiver Skew	t_{RSKD}	Figures 7 and 9, $\lvert V_{ID} \rvert \geq 2.0V$, rise and fall time of $V_{ID} \leq 15ns$		0	±10	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 15pF, S2 closed			250	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 15pF, S1 closed			250	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 100pF, S1 closed			3500	ns

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 3: The SRL pin is internally biased to $V_{CC}/2$ by a 100kΩ/100kΩ resistor-divider. It is guaranteed to be $V_{CC}/2$ if left unconnected.

Note 4: Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.

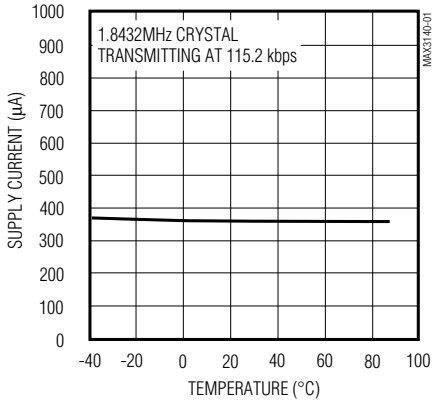
Note 5: The device is put into shutdown by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

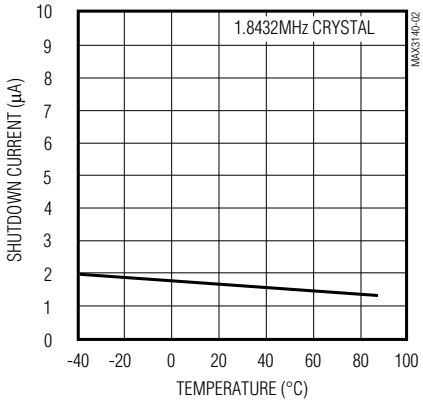
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

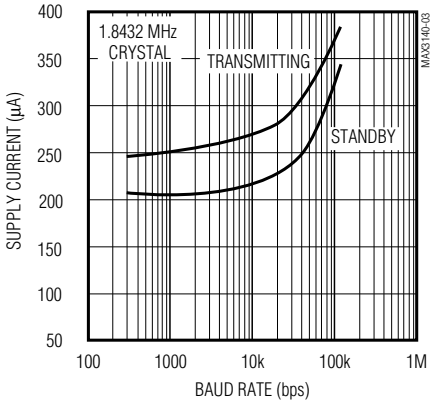
UART SUPPLY CURRENT vs. TEMPERATURE



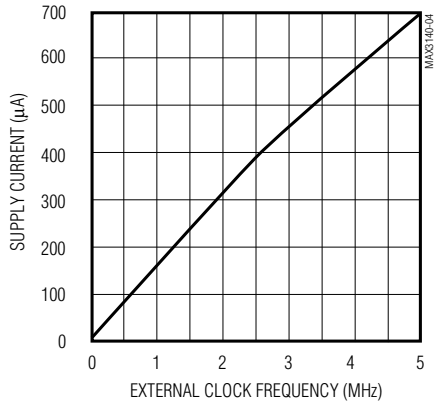
UART SHUTDOWN CURRENT vs. TEMPERATURE



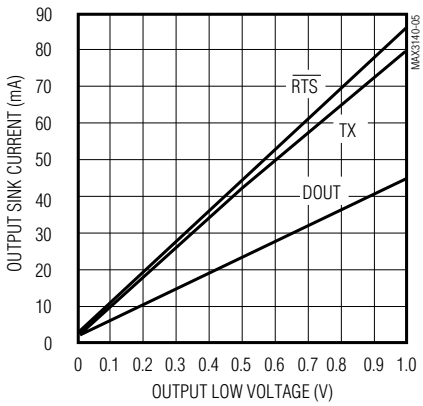
UART SUPPLY CURRENT vs. BAUD RATE



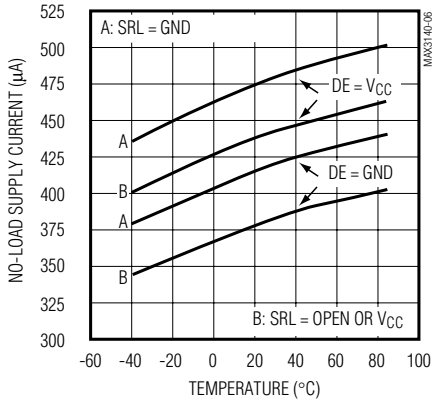
UART SUPPLY CURRENT vs. EXTERNAL CLOCK FREQUENCY



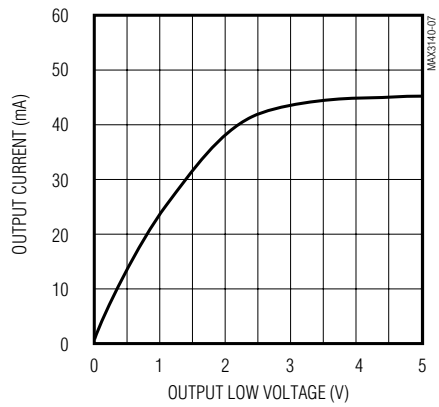
TX, $\overline{RTS}$, DOUT OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE



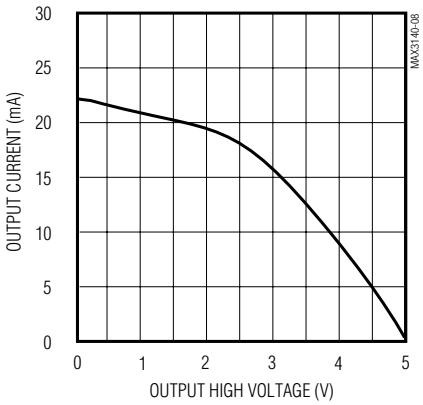
RS-485 TRANSCEIVER NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



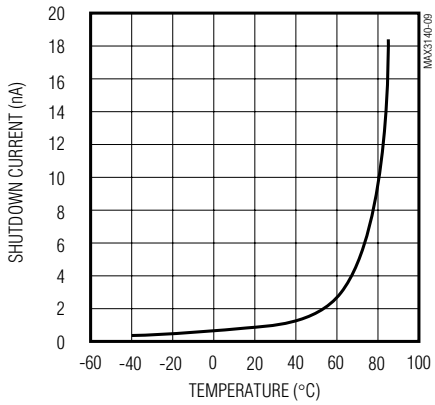
RS-485 OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



RS-485 OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



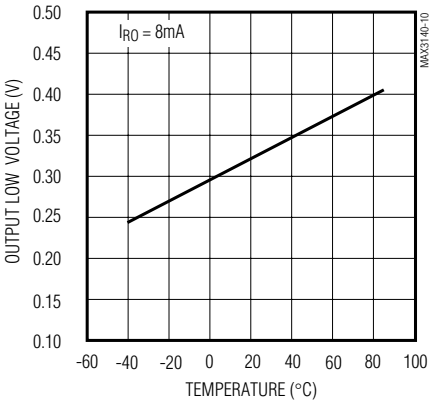
RS-485 TRANSCEIVER SHUTDOWN CURRENT vs. TEMPERATURE



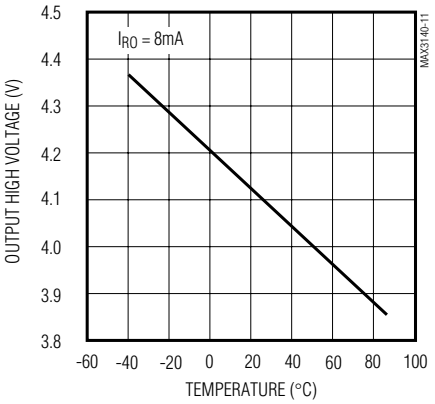
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

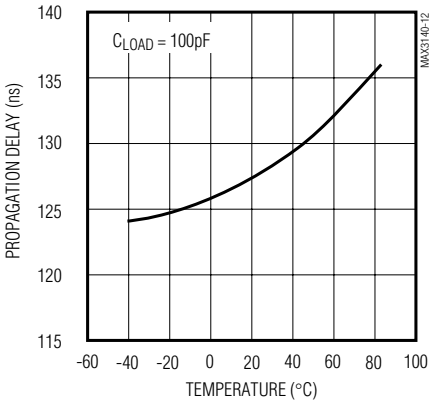
RS-485 RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



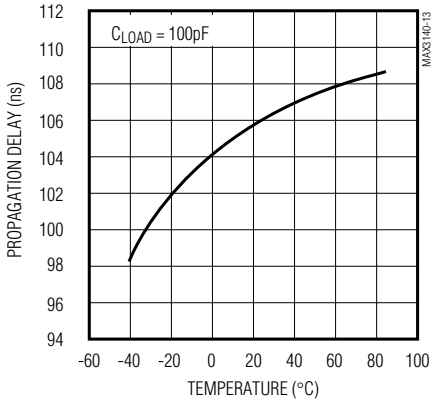
RS-485 RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



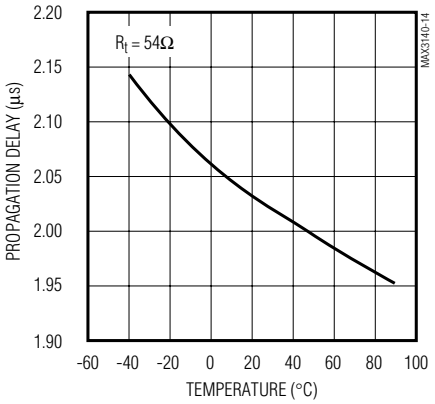
RS-485 RECEIVER PROPAGATION DELAY (500kbps MODE) vs. TEMPERATURE



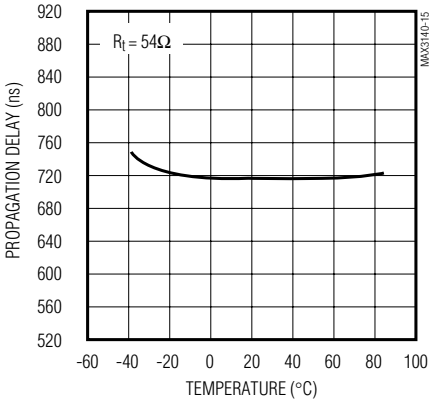
RS-485 RECEIVER PROPAGATION DELAY (10Mbps MODE) vs. TEMPERATURE



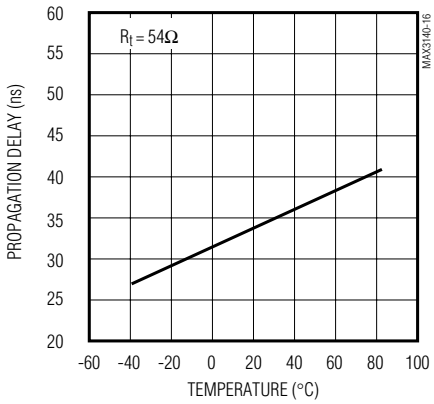
RS-485 DRIVER PROPAGATION DELAY (115kbps MODE) vs. TEMPERATURE



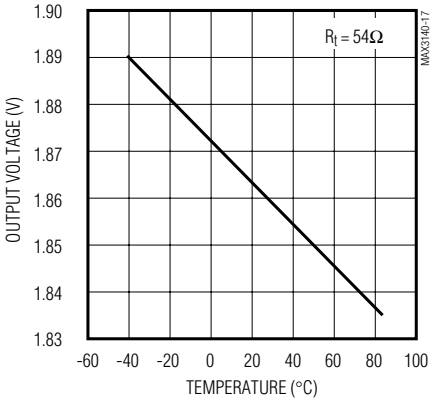
RS-485 DRIVER PROPAGATION DELAY (500kbps MODE) vs. TEMPERATURE



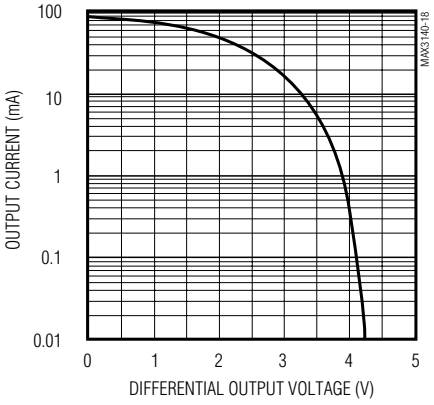
RS-485 DRIVER PROPAGATION DELAY (10Mbps MODE) vs. TEMPERATURE



RS-485 DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



RS-485 DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE

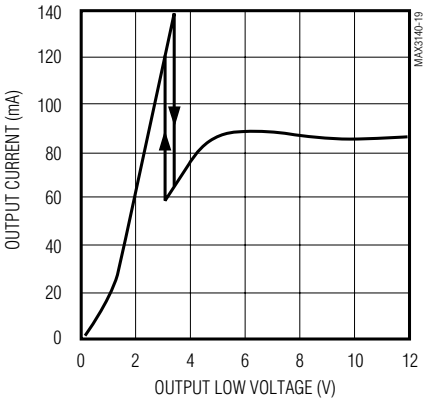


SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

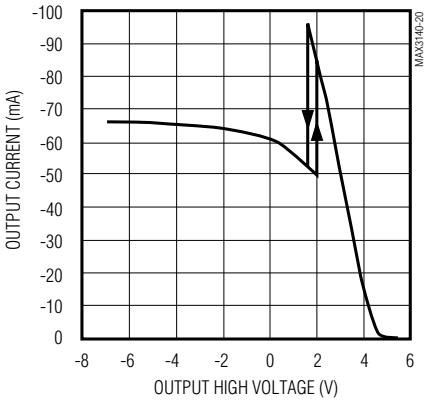
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

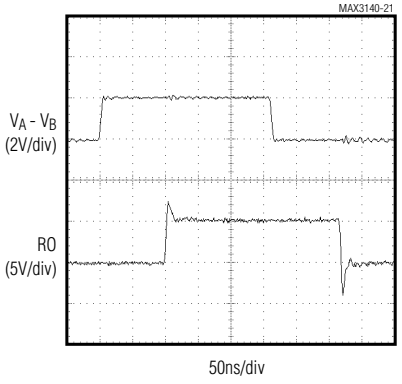
OUTPUT CURRENT vs. RS-485 DRIVER OUTPUT LOW VOLTAGE



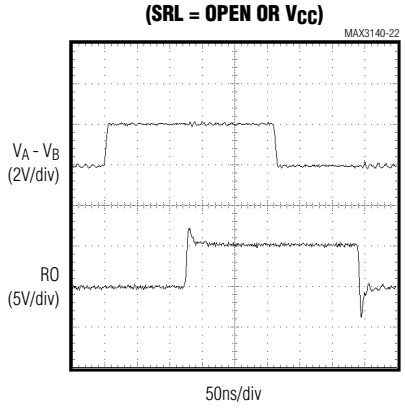
OUTPUT CURRENT vs. RS-485 DRIVER OUTPUT HIGH VOLTAGE



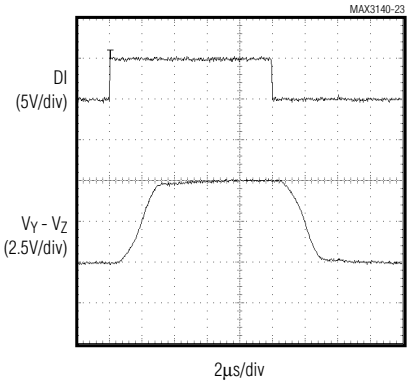
RS-485 RECEIVER PROPAGATION DELAY (SRL = GND)



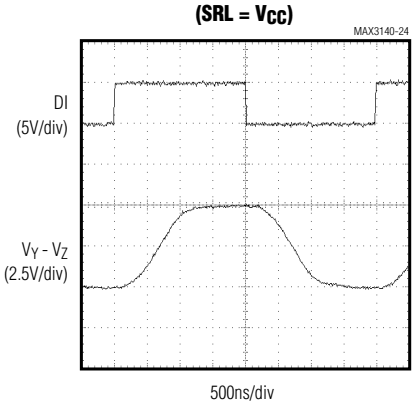
RS-485 RECEIVER PROPAGATION DELAY (SRL = OPEN OR V_{CC})



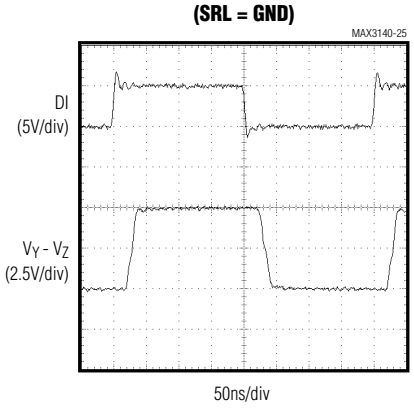
RS-485 DRIVER PROPAGATION DELAY (SRL = OPEN)



RS-485 DRIVER PROPAGATION DELAY (SRL = V_{CC})



RS-485 DRIVER PROPAGATION DELAY (SRL = GND)



Pin Description

PIN		NAME	FUNCTION
FULL DUPLEX	HALF DUPLEX		
1	1	X2	UART Crystal Connection. Leave X2 unconnected for external clock. See the *Crystals, Oscillators, and Ceramic Resonators* section.
2	2	X1	UART Crystal Connection. X1 also serves as an external clock input. See the *Crystals, Oscillators, and Ceramic Resonators* section.
3	3	$\overline{CTS}$	UART Clear-to-Send Active-Low Input. Read via the CTS bit.
4	4	$\overline{RTS}$	UART Request-to-Send Active-Low Output. Controlled by the RTS bit. Use to control the driver enable in RS-485 networks.
5	5	RX	UART Asynchronous Serial-Data (receiver) Input. The serial information received from the modem or RS-232/RS-485 receiver. A transition on RX while in shutdown generates an interrupt (Table 1).
6	6	TX	UART Asynchronous Serial-Data (transmitter) Output
7	7	H/$\overline{F}$	RS-485 Half/Full-Duplex Selector Pin. Connect H/$\overline{F}$ to V_{CC} for half-duplex mode; connect H/$\overline{F}$ to GND or leave it unconnected for full-duplex mode.
8	8	GND	Ground
9	9	RO	RS-485 Receiver Output. When $\overline{RE}$ is low and if A - B ≥ -50mV, RO will be high; if A - B ≤ -200mV, RO will be low.
10	10	$\overline{RE}$	RS-485 Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
11	11	DE	RS-485 Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
12	12	DI	RS-485 Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
13	13	SRL	RS-485 Transceiver Slew-Rate-Limit Selector Pin. Connect SRL to GND for a 10Mbps communication rate, connect SRL to V_{CC} for a 500kbps rate, or leave SRL unconnected for a 115kbps rate.
14	14	N.C.	No Connection. Not internally connected.
15	15	TXP	RS-485 Transmitter Phase. Connect TXP to GND or leave it unconnected for normal transmitter phase/polarity. Connect TXP to V_{CC} to invert the transmitter phase/polarity.
16	—	Y	RS-485 Noninverting Driver Output
—	16	Y	RS-485 Noninverting Receiver Input and RS-485 Noninverting Driver Output*
17	17	N.C.	No Connection. Not internally connected.
18	—	Z	RS-485 Inverting Driver Output
—	18	Z	RS-485 Inverting Receiver Input and RS-485 Inverting Driver Output*
19	—	B	RS-485 Inverting Receiver Input
—	19	B	RS-485 Receiver Input Resistors*
20	—	A	RS-485 Noninverting Receiver Input
—	20	A	RS-485 Receiver Input Resistors*

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

Pin Description (continued)

PIN		NAME	FUNCTION
FULL DUPLEX	HALF DUPLEX		
21	21	RXP	RS-485 Receiver Phase. Connect RXP to GND or leave it unconnected for normal receiver phase/polarity. Connect RXP to V_{CC} to invert the receiver phase/polarity.
22	22	V_{CC}	Positive Supply (4.75V to 5.25V)
23	23	DIN	UART SPI/MICROWIRE Serial-Data Input. Schmitt-trigger input.
24	24	DOUT	UART SPI/MICROWIRE Serial-Data Output. High impedance when $\overline{CS}$ is high.
25	25	SCLK	UART SPI/MICROWIRE Serial-Clock Input. Schmitt-trigger input.
26	26	$\overline{CS}$	UART Active-Low Chip-Select Input. DOUT goes high impedance when $\overline{CS}$ is high. $\overline{IRQ}$, TX, and $\overline{RTS}$ are always active. Schmitt-trigger input.
27	27	$\overline{IRQ}$	UART Active-Low Interrupt Output. Open-drain interrupt output to microprocessor.
28	28	$\overline{SHDN}$	UART Hardware Shutdown Input. When shut down ($\overline{SHDN}$ = 0), the UART oscillator turns off immediately without waiting for the current transmission to end, reducing the supply current to just leakage currents.

**In half-duplex mode, the driver outputs serve as receiver inputs. The full-duplex receiver inputs (A and B) still have a 1/8-unit load, but do not affect the receiver output.*

Transceiver Function Tables

TRANSMITTING					
INPUTS				OUTPUTS	
TXP	$\overline{RE}$	DE	DI	Z	Y
0	X	1	1	0	1
0	X	1	0	1	0
1	X	1	1	1	0
1	X	1	0	0	1
X	0	0	X	High-Z	High-Z
X	1	0	X	Shutdown (High-Z)	

RECEIVING						
INPUTS						OUTPUTS
H/$\overline{F}$	RXP	$\overline{RE}$	DE	A-B	Y-Z	RO
0	0	0	X	≥ -0.05V	X	1
0	0	0	X	≤ -0.2V	X	0
0	1	0	X	≥ -0.05V	X	0
0	1	0	X	≤ -0.2V	X	1
1	0	0	X	X	≥ -0.05V	1
1	0	0	X	X	≤ -0.2V	0
1	1	0	X	X	≥ -0.05V	0
1	1	0	X	X	≤ -0.2V	1
0	0	0	X	Open/ Shorted	X	1
1	0	0	X	X	Open/ Shorted	1
0	1	0	X	Open/ Shorted	X	0
1	1	0	X	X	Open/ Shorted	0
X	X	1	1	X	X	High-Z
X	X	1	0	X	X	Shutdown (High-Z)

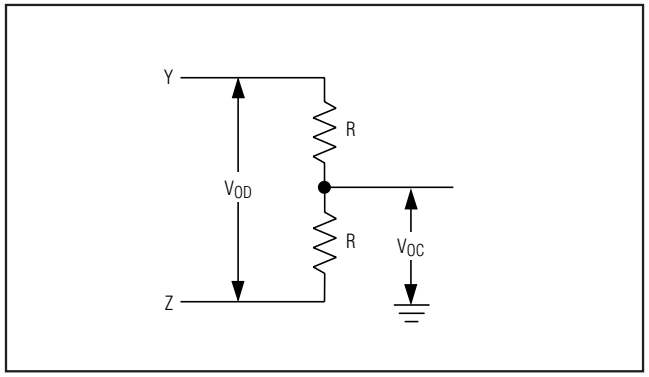


Figure 1. Driver DC Test Load

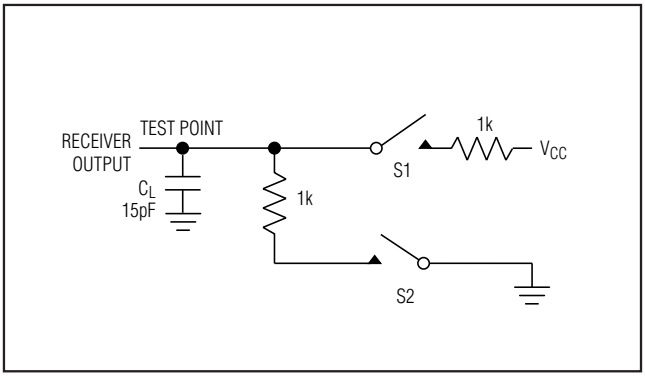


Figure 2. Receiver Enable/Disable Timing Test Load

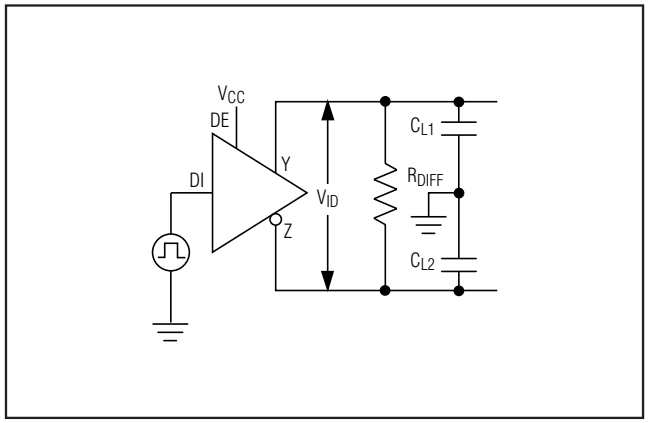


Figure 3. Driver Timing Test Circuit

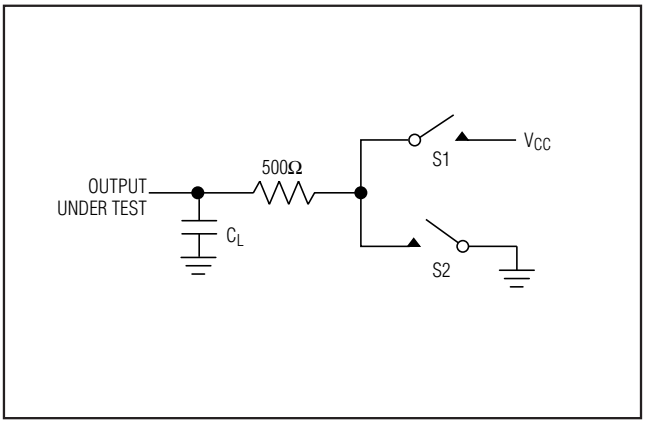


Figure 4. Driver Enable/Disable Timing Test Load

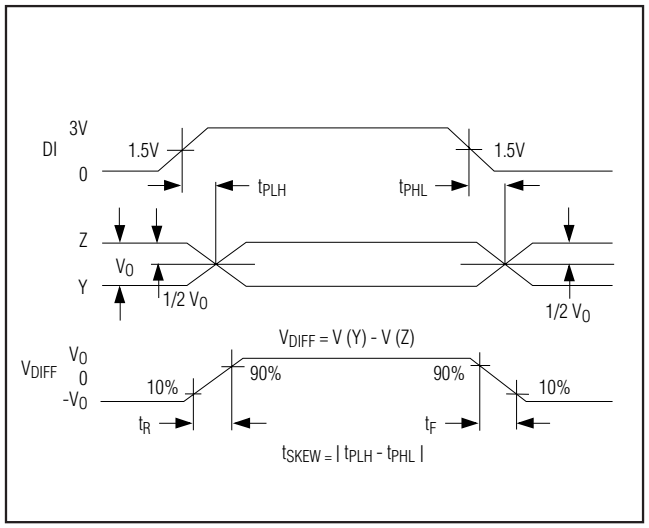


Figure 5. Driver Propagation Delays

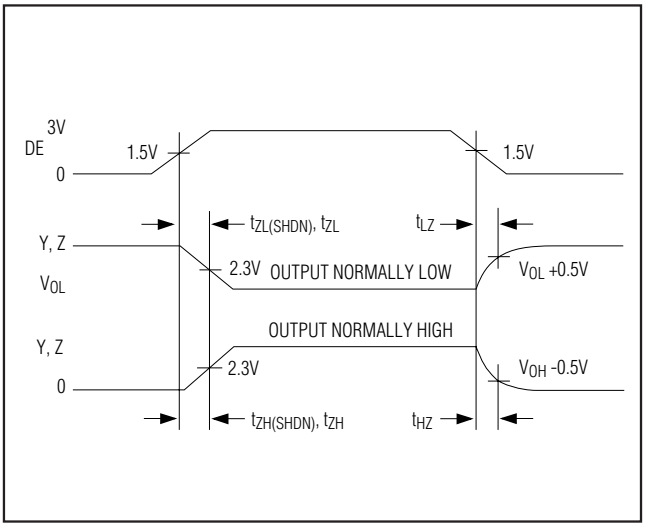


Figure 6. Driver Enable and Disable Times

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

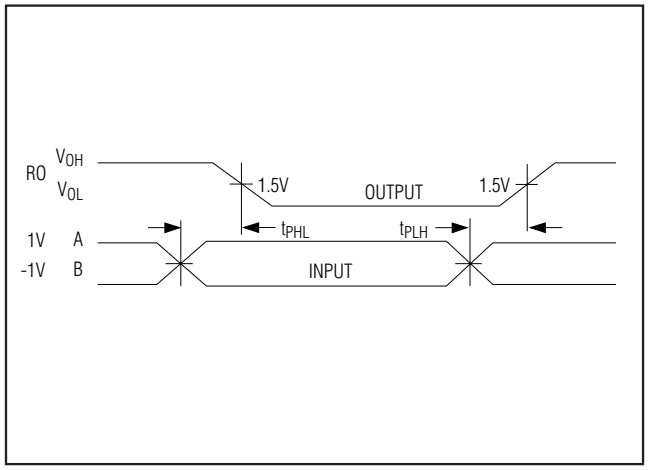


Figure 7. Receiver Propagation Delays

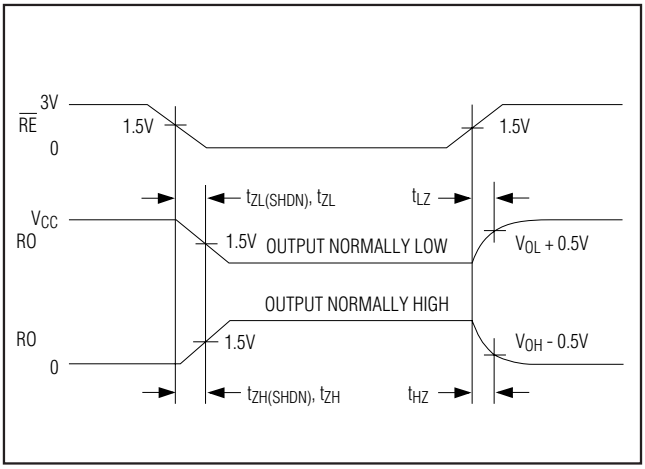


Figure 8. Receiver Enable and Disable Times

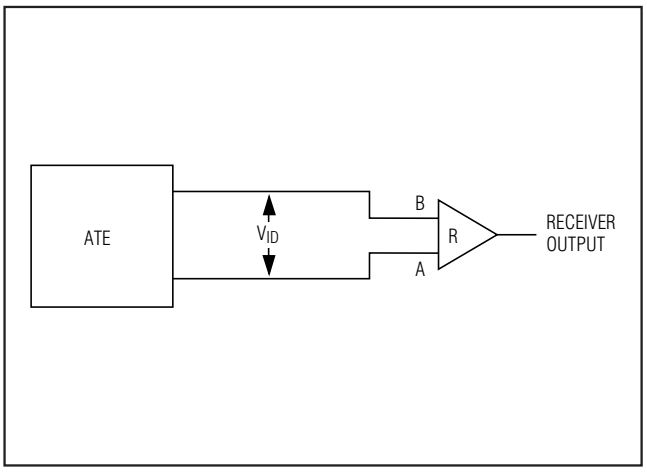


Figure 9. Receiver Propagation Delay Test Circuit

Detailed Description

The MAX3140 combines an SPI/QSPI/MICROWIRE-compatible UART (MAX3100) and an RS-485/RS-422 transceiver (MAX3089) in one package. The UART supports data rates up to 230k baud for both standard UART bit streams as well as IrDA, and includes an 8-word receive FIFO. Also included is a parity-bit interrupt useful in 9-bit address recognition.

The RS-485/RS-422 transceiver has a true fail-safe receiver and allows up to 256 transceivers on the bus. Other features include pin-selectable full/half-duplex operation and a phase control to correct for twisted-pair reversal. The slew rate of the RS-485/RS-422 transceiver is selectable, limiting the maximum data rate to 115kbps, 500kbps, or 10Mbps. The RS-485/RS-422 drivers are output short-circuit current limited, and thermal shutdown circuitry protects the RS-485/RS-422 drivers against excessive power dissipation.

The UART and RS-485/RS422 functions can be used together or independently since the two functions only share supply and ground connections. This part operates from a single +5V supply.

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

UART

The universal asynchronous receiver transmitter (UART) interfaces the SPI/MICROWIRE-compatible synchronous serial data from a microprocessor (µP) to asynchronous, serial-data communication ports (RS-485, IrDA). Figure 10 shows the MAX3140 functional diagram. Included in the UART function is an SPI/MICROWIRE interface, a baud-rate generator, and an interrupt generator.

SPI Interface

The MAX3140 is compatible with SPI, QSPI (CPOL = 0, CPHA = 0), and MICROWIRE serial-interface standards (Figure 11). The MAX3140 has a unique full-duplex architecture that expects a 16-bit word for DIN and simultaneously produces a 16-bit word for DOUT regardless of which read/write register used. The DIN stream is monitored for its first two bits to tell the UART the type of data transfer being executed (see the *WRITE CONFIGURATION register, READ CONFIGURATION register, WRITE DATA register,* and *READ DATA register* sections). DIN (MOSI) is latched on

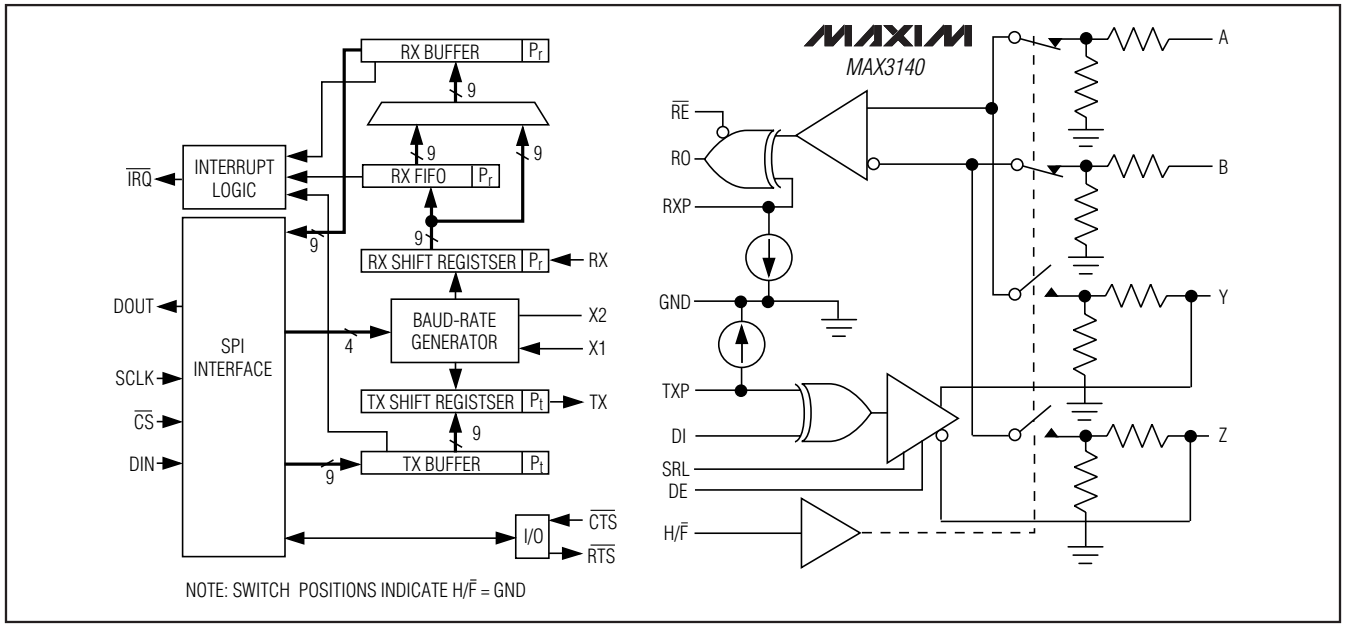


Figure 10. Functional Diagram

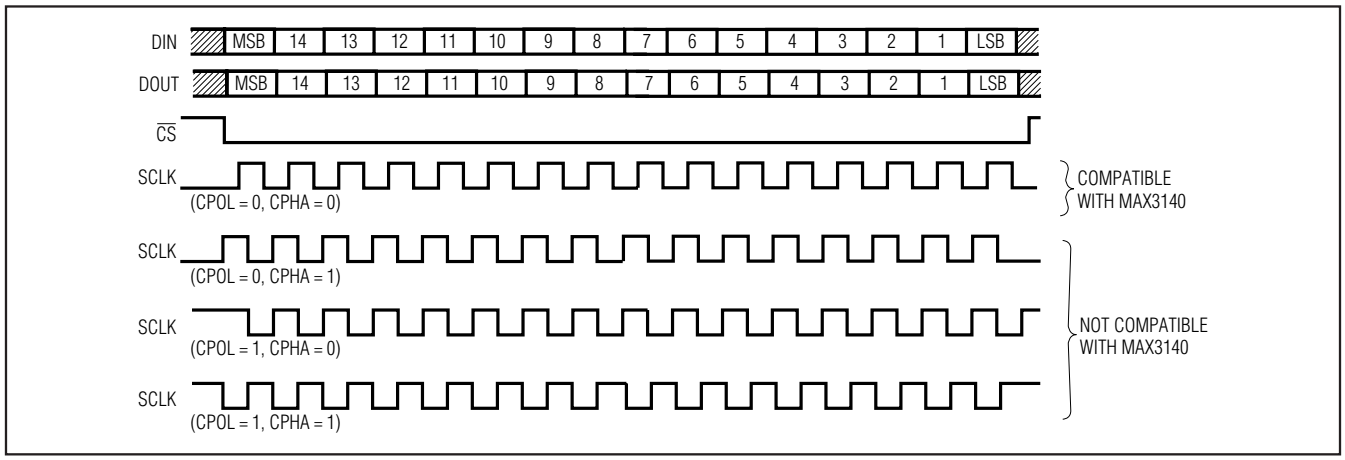


Figure 11. Compatible CPOL and CPHA Modes

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

SCLK's rising edge. DOUT (MISO) is read into the µP on SCLK's rising edge. The first bit (bit 15) of DOUT transitions on $\overline{CS}$'s falling edge, and bits 14–0 transition on SCLK's falling edge. Figure 12 shows the detailed serial timing specifications for the synchronous SPI port.

Only 16-bit words are expected. If $\overline{CS}$ goes high in the middle of a transmission (any time before the 16th bit), the sequence is aborted (i.e., data does not get written to individual registers). Most operations, such as the clearing of internal registers, are executed only on $\overline{CS}$'s rising edge. Every time $\overline{CS}$ goes low, a new 16-bit stream is expected. Figure 13 shows an example of using the WRITE CONFIGURATION register.

Table 1 describes the bits located in the WRITE CONFIGURATION, READ CONFIGURATION, WRITE DATA, and READ DATA registers. This table also describes whether the bit is a read or write bit and what the power-on reset states (POR) of the bits are. Figure 14 shows an example of parity and word length control.

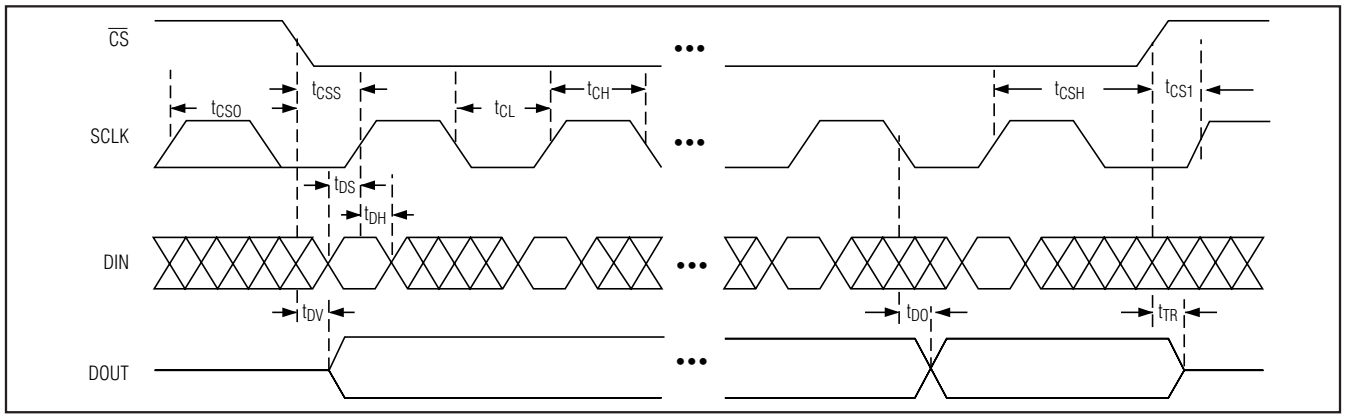


Figure 12. Detailed Serial Timing Specifications for the Synchronous Port

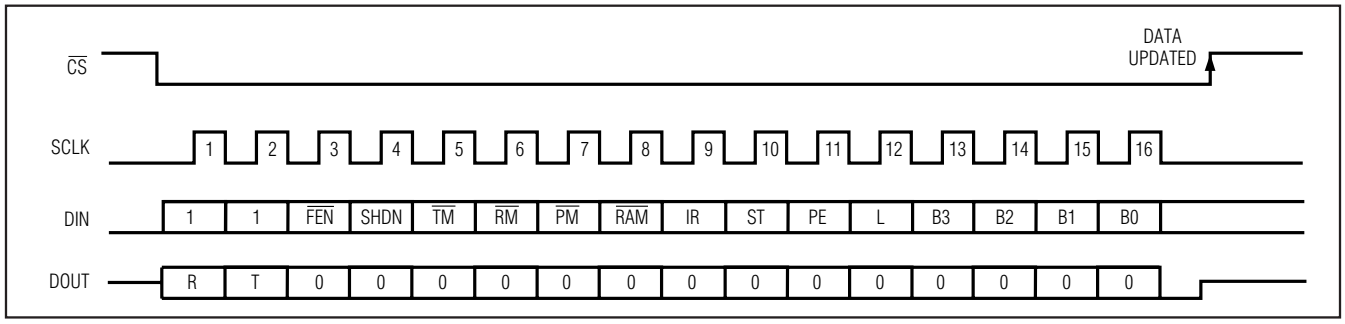


Figure 13. SPI Interface (Write Configuration)

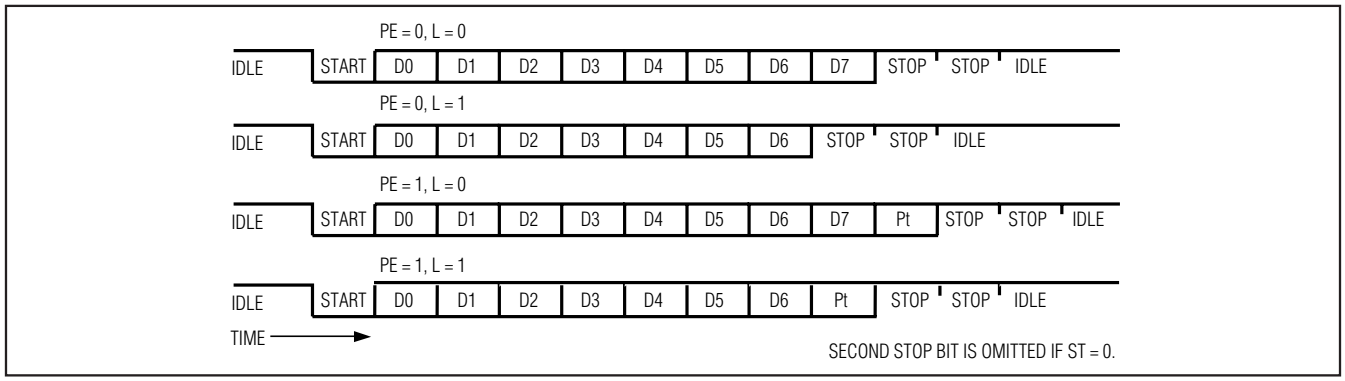


Figure 14. Parity and Word Length Control

Table 1. Bit Descriptions

BIT NAME	BIT TYPE	POR STATE	DESCRIPTION
B0–B3	write	0000	Baud-Rate Divisor Select Bits. Sets the baud clock's value (Table 6).
B0–B3	read	0000	Baud-Rate Divisor Select Bits. Reads the 4-bit baud clock value assigned to these registers.
CTS	read	No change	Clear-to-Send-Input. Records the state of the $\overline{CTS}$ pin (CTS bit = 0 implies $\overline{CTS}$ pin = logic high).
D0t–D7t	write	XXXXXXXX	Transmit-Buffer Register. Eight data bits written into the transmit-buffer register. D7t is ignored when L = 1.
D0r–D7r	read	00000000	Eight data bits read from the receive FIFO or the receive-buffer register. When L = 1, D7r is always 0.
$\overline{FEN}$	write	0	FIFO Enable. Enables the receive FIFO when $\overline{FEN}$ = 0. When $\overline{FEN}$ = 1, FIFO is disabled.
$\overline{FEN}$	read	0	FIFO-Enable Readback. $\overline{FEN}$'s state is read.
IR	write	0	Enables the IrDA timing mode when IR = 1.
IR	read	0	Reads the value of the IR bit.
L	write	0	Bit to set the word length of the transmitted or received data. L = 0 results in 8-bit words (9-bit words if PE = 1) (see Figure 5). L = 1 results in 7-bit words (8-bit words if PE = 1).
L	read	0	Reads the value of the L bit.
Pt	write	X	Transmit-Parity Bit. This bit is treated as an extra bit that is transmitted if PE = 1. In 9-bit networks, the MAX3140 does not calculate parity. If PE = 0, then this bit (Pt) is ignored in transmit mode (see the *9-Bit Networks* section).
Pr	read	X	Receive-Parity Bit. This bit is the extra bit received if PE = 1. Therefore, PE = 1 results in 9-bit transmissions (L = 0). If PE = 0, then Pr is set to 0. Pr is stored in the FIFO with the receive data (see the *9-Bit Networks* section).
PE	write	0	Parity-Enable Bit. Appends the Pt bit to the transmitted data when PE = 1, and sends the Pt bit as written. No parity bit is transmitted when PE = 0. With PE = 1, an extra bit is expected to be received. This data is put into the Pr register. Pr = 0 when PE = 0. The MAX3140 does not calculate parity.
PE	read	0	Reads the value of the Parity-Enable bit.
$\overline{PM}$	write	0	Mask for Pr bit. $\overline{IRQ}$ is asserted if $\overline{PM}$ = 1 and Pr = 1 (Table 7).
$\overline{PM}$	read	0	Reads the value of the $\overline{PM}$ bit (Table 7).
R	read	0	Receive Bit or FIFO Not Empty Flag. R = 1 means new data is available to be read or is being read from the receive register or FIFO. If performing a READ DATA or WRITE DATA operation, the R bit will clear on the falling edge of SCLK's 16th pulse if no new data is available.
$\overline{RM}$	write	0	Mask for R bit. $\overline{IRQ}$ is asserted if $\overline{RM}$ = 1 and R = 1 (Table 7).
$\overline{RM}$	read	0	Reads the value of the $\overline{RM}$ bit (Table 7).
$\overline{RAM}$	write	0	Mask for RA/FE bit. $\overline{IRQ}$ is asserted if $\overline{RAM}$ = 1 and RA/FE = 1 (Table 7).
$\overline{RAM}$	read	0	Reads the value of the $\overline{RAM}$ bit (Table 7).
RTS	write	0	Request-to-Send Bit. Controls the state of the $\overline{RTS}$ output. This bit is reset on power-up (RTS bit = 0 sets the $\overline{RTS}$ pin = logic high).

Table 1. Bit Descriptions (continued)

BIT NAME	BIT TYPE	POR STATE	DESCRIPTION
RA/FE	read	0	Receiver-Activity/Framing-Error Bit. In shutdown mode, this is the RA bit. In normal operation, this is the FE bit. In shutdown mode, a transition on RX sets RA = 1. In normal mode, a framing error sets FE = 1. A framing error occurs if a zero is received when the first stop bit is expected. FE is set when a framing error occurs, and cleared upon receipt of the next properly framed character independent of the FIFO being enabled. When the device wakes up, it is likely that a framing error will occur. This error is cleared with a WRITE CONFIGURATION. The FE bit is not cleared on a READ DATA operation. When an FE is encountered, the UART resets itself to the state where it is looking for a start bit.
SHDNi	write	0	Software-Shutdown Bit. Enter software shutdown with a WRITE CONFIGURATION where SHDNi = 1. Software shutdown takes effect after $\overline{CS}$ goes high, and causes the oscillator to stop as soon as the transmitter becomes idle. Software shutdown also clears R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, Pt, and all data in the receive FIFO. RTS and CTS can be read and updated while in shutdown. Exit software shutdown with a WRITE CONFIGURATION where SHDNi = 0. The oscillator restarts typically within 50ms of $\overline{CS}$ going high. RTS and CTS are unaffected. Refer to the *Pin Description* for hardware shutdown ($\overline{SHDN}$ input).
SHDNo	read	0	Shutdown Read-Back Bit. The READ CONFIGURATION register outputs SHDNo = 1 when the UART is in shutdown. Note that this bit is not sent until the current byte in the transmitter is sent (T = 1). This tells the processor when it may shut down the RS-485/RS-422 driver. This bit is also set immediately when the device is shut down through the $\overline{SHDN}$ pin.
ST	write	0	Transmit-Stop Bit. One stop bit will be transmitted when ST = 0. Two stop bits will be transmitted when ST = 1. The receiver only requires one stop bit.
ST	read	0	Reads the value of the ST bit.
T	read	1	Transmit-Buffer-Empty Flag. T = 1 means that the transmit buffer is empty and ready to accept another data word.
$\overline{TE}$	write	0	Transmit-Enable Bit. If $\overline{TE}$ = 1, then only the $\overline{RTS}$ pin is updated on $\overline{CS}$'s rising edge. The contents of $\overline{RTS}$, Pt, and D0t–D7t transmit on $\overline{CS}$'s rising edge when $\overline{TE}$ = 0.
$\overline{TM}$	write	0	Mask for T Bit. $\overline{IRQ}$ is asserted if $\overline{TM}$ = 1 and T = 1 (Table 7).
$\overline{TM}$	read	0	Reads the value of the $\overline{TM}$ bit (Table 7).

Notice to High-Level Programmers

The MAX3140 follows the SPI convention of providing a bidirectional data path for writes and reads. Whenever the data is written, data is also read back. This speeds operation over the SPI bus, as required, when operating at high baud rates. In most high-level languages, like C, there are commands for writing and reading stream I/O devices like the console or serial port. In C specifically, there is a "PUTCHAR" command that transmits a character and a "GETCHAR" command that receives a character. Implementing direct write and read commands in C with no underlying driver code causes an intended PUTCHAR command to become a PUTGETCHAR command. These C commands assume that they'll receive some form of BIOS-level support. The proper way to implement these commands is to use driver code—usually in the form of an assembly language interrupt service routine and a callable routine used by high-level routines. This driver handles the interrupts and manages the receive and transmit buffers for the MAX3140. When a PUTCHAR executes, this driver is called and it safely buffers any characters received when the current character is transmitted. Likewise, when a GETCHAR executes, it checks its own receive buffer before getting data from the MAX3140. See the C-language outline of a MAX3140 software driver in Listing 1.

WRITE CONFIGURATION Register (D15, D14 = 1, 1)

Configure the UART by writing a 16-bit word to the WRITE CONFIGURATION register, which programs the baud rate, data-word length, parity enable, and enable of the 8-word receive FIFO. Set bits 15 and 14 of the DIN configuration word to 1 to enable the WRITE CONFIGURATION mode. Bits 13–0 of the DIN configuration word set the configuration of the UART. Table 2 shows the bit assignment for the WRITE CONFIGURATION register. The WRITE CONFIGURATION register allows selection between normal UART timing and IrDA timing, shutdown control, and contains four interrupt mask bits.

Setting the WRITE CONFIGURATION register clears the receive FIFO and the R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, and Pt registers. Bits RTS and CTS remain unchanged. The new configuration is valid on $\overline{CS}$'s rising edge if the transmit buffer is empty (T = 1) and transmission is over. If the latest transmission has not been completed (T = 0), the registers are updated when the transmission is over.

The WRITE CONFIGURATION register bits ($\overline{FEN}$, SHDNi, IR, ST, PE, L, B3–B0) take effect after the current transmission is over. The mask bits ($\overline{TM}$, $\overline{RM}$, $\overline{PM}$, $\overline{RAM}$) take effect immediately after SCLK's 16th rising edge.

Table 2. WRITE CONFIGURATION Register Bit Assignment (D15, D14 = 1, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	1	$\overline{FEN}$	SHDNi	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0
DOUT	R	T	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes:

bit 15, 14: DIN

1, 1 = Write Configuration

bit 13: DIN

$\overline{FEN}$ = 0, FIFO is enabled

$\overline{FEN}$= 1, FIFO is disabled

bit 12: DIN

SHDNi = 1, Enter software shutdown

SHDNi = 0, Exit software shutdown

bit 11: DIN

$\overline{TM}$ = 1, Transmit-buffer-empty interrupt is enabled.

$\overline{TM}$ = 0, Transmit-buffer-empty interrupt is disabled.

bit 10: DIN

$\overline{RM}$ = 1, Data available in the receive register or FIFO interrupt is enabled.

$\overline{RM}$ = 0, Data available in the receive register or FIFO interrupt is disabled.

bit 9: DIN

$\overline{PM}$ = 1, Parity-bit-received interrupt is enabled.

$\overline{PM}$ = 0, Parity-bit-received interrupt is disabled.

bit 8: DIN

$\overline{RAM}$ = 1, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is enabled.

$\overline{RAM}$ = 0, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is disabled.

bit 7: DIN

IR = 1, IrDA mode is enabled.

IR = 0, IrDA mode is disabled.

bit 6: DIN

ST = 1, Transmit two stop bits

ST = 0, Transmit one stop bit

bit 5: DIN

PE = 1, Parity is enabled for both transmit (state of Pt) and receive.

PE = 0, Parity is disabled for both transmit and receive.

bit 4: DIN

L = 1, 7-bit words (8-bit words if PE = 1)

L = 0, 8-bit words (9-bit words if PE = 1)

bit 3–0: DIN

B3–B0 = XXXX Baud-Rate Divisor select bits. See Table 6.

bit 15: DOUT

R = 1, Data is available to be read from the receive.

register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bit 13–0: DOUT

Zeros

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

Bits 15 and 14 of the DOUT WRITE CONFIGURATION word (R and T) are sent out of the MAX3140 along with 14 trailing zeros. The use of the R and T bits is optional, but ignore the 14 trailing zeros.

Warning! The UART requires stable crystal oscillator operation before configuration (typically ~25ms after power-up). At power-up, compare the WRITE CONFIGURATION bits with the READ CONFIGURATION bits in a software loop until both match. This ensures that the oscillator is stable and the UART is configured correctly.

READ CONFIGURATION Register (D15, D14 = 0, 1)

Use the READ CONFIGURATION register to read back the last configuration written to the UART. In this mode, bits 15 and 14 of the DIN configuration word are required to be 0 and 1, respectively, to enable the READ CONFIGURATION mode. Clear bits 13–1 of the DIN word. Bit 0 is the test bit to put the UART in test mode (see the *Test Mode* section). Table 3 shows the bit assignment for the READ CONFIGURATION register.

Table 3. READ CONFIGURATION Register Bit Assignment (D15, D14 = 0, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST
DOUT	R	T	$\overline{FEN}$	SHDNo	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0

Notes:

bit 15: DOUT

R = 1, Data is available to be read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bit 13: DOUT

$\overline{FEN}$ = 0, FIFO is enabled

$\overline{FEN}$ = 1, FIFO is disabled

bit 12: DOUT

SHDNo = 1, Software shutdown is enabled.

SHDNo = 0, Software shutdown is disabled.

bit 11: DOUT

$\overline{TM}$ = 1, Transmit-buffer-empty interrupt is enabled.

$\overline{TM}$ = 0, Transmit-buffer-empty interrupt is disabled.

bit 10: DOUT

$\overline{RM}$ = 1, Data available in the receive register or FIFO interrupt is enabled.

$\overline{RM}$ = 0, Data available in the receive register or FIFO interrupt is disabled.

bit 9: DOUT

$\overline{PM}$ = 1, Parity-bit-received interrupt is enabled.

$\overline{PM}$ = 0, Parity-bit-received interrupt is disabled.

bit 8: DOUT

$\overline{RAM}$ = 1, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is enabled.

$\overline{RAM}$ = 0, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is disabled.

bit 7: DOUT

IR = 1, IrDA mode is enabled.

IR = 0, IrDA mode is disabled.

bit 6: DOUT

ST = 1, Transmit two stop bits.

ST = 0, Transmit one stop bit.

bit 5: DOUT

PE = 1, Parity is enabled for both transmit (state of Pt) and receive.

PE = 0, Parity is disabled for both transmit and receive.

bit 4: DOUT

L = 1, 7-bit words (8-bit words if PE = 1)

L = 0, 8-bit words (9-bit words if PE = 1)

bit 3–0: DOUT

B3–B0 = XXXX Baud-Rate Divisor select bits. See Table 6.

bit 15, 14: DIN

0, 1 = Read Configuration

bit 13–1: DIN

Zeros

bit 0: DIN

If TEST = 1 and $\overline{CS}$ = 0, then $\overline{RTS}$ = 16xBaudCLK

TEST = 0, Disables TEST mode.

Test Mode

The device enters a test mode if bit 0 of the DIN configuration word equals 1 when performing a READ CONFIGURATION. In this mode, if $\overline{CS}$ = 0, the $\overline{RTS}$ pin transmits a clock that is 16 times the baud rate. The TX pin is low as long as $\overline{CS}$ remains low while in test mode. Table 3 shows the bit assignment for the READ CONFIGURATION register.

WRITE DATA Register (D15, D14 = 1, 0)

Use the WRITE DATA register for transmitting to the TX buffer and receiving from the RX buffer (and RX FIFO when enabled). When using this register, the DIN and DOUT WRITE DATA words are used simultaneously and bits 13–11 for both the DIN and DOUT WRITE DATA words are meaningless zeros. The DIN WRITE DATA word contains the data that is being transmitted, and the DOUT WRITE DATA word contains the data that is being received from the RX FIFO. Table 4 shows the bit assignment for the WRITE DATA register. To change the $\overline{RTS}$ pin's output state without transmitting data, set the $\overline{TE}$ bit high. If performing a WRITE DATA operation, the R bit clears on the falling edge of SCLK's 16th clock pulse if no new data is available.

READ DATA Register (D15, D14 = 0, 0)

Use the READ DATA register for receiving data from the RX FIFO. When using this register, bits 15 and 14 of DIN must both be 0. Clear bits 13–0 of the DIN READ DATA word. Table 5 shows the bit assignments for the READ DATA register. Reading all available data clears the R bit and interrupt $\overline{IRQ}$. If performing a READ DATA operation, the R bit clears on the falling edge of SCLK's 16th clock pulse if no new data is available.

Table 4. WRITE DATA Register Bit Assignment (D15, D14 = 1, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	0	0	0	0	$\overline{TE}$	RTS	Pt	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

Notes:

5, 14: DIN

1, 0 = Write Data

bit 13–11: DIN

Zeros

bit 10: DIN

$\overline{TE}$ = 1, Disables transmit, and only $\overline{RTS}$ will be updated.

$\overline{TE}$ = 0, Enables transmit.

bit 9: DIN

RTS = 1, Configures $\overline{RTS}$ = 0 (Logic Low).

RTS = 0, Configures $\overline{RTS}$ = 1 (Logic High).

bit 8: DIN

Pt = 1, Transmit parity bit is high. If PE = 1, a high parity bit will be transmitted. If PE = 0, then no parity bit will be transmitted.

Pt = 0, Transmit parity bit is low. If PE = 1, a low parity bit will be transmitted. If PE = 0, then no parity bit will be transmitted.

bit 7–0: DIN

D7t–D0t = Transmitting Data bits. D7t is ignored when L = 1.

bit 15: DOUT

R = 1, Data is available to be read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bit 13–11: DOUT

Zeros

bit 10: DOUT

RA/FE = Receive-activity (UART shutdown)/Framing-error (normal operation) bit.

bit 9: DOUT

CTS = $\overline{CTS}$ input state. If CTS = 0, then $\overline{CTS}$ = 1 and vice versa.

bit 8: DOUT

Pr = Received parity bit. This is only valid if PE = 1.

bit 7–0: DOUT

D7t–D0t = Received Data bits. D7r = 0 for L = 1.

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

Table 5. READ DATA Register Bit Assignment (D15, D14 = 0, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

Notes:

bit 15, 14: DIN

0, 0 = Read Data

bit 13–0: DIN

Zeros

bit 15: DOUT

R = 1, Data is available to be read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bit 13–11: DOUT

Zeros

bit 10: DOUT

RA/FE = Receive-activity (UART shutdown)/Framing-error (normal operation) bit

bit 9: DOUT

CTS = $\overline{CTS}$ input state. If CTS = 0, then $\overline{CTS}$ = 1 and vice versa.

bit 8: DOUT

Pr = Received parity bit. This is only valid if PE = 1.

bit 7–0: DOUT

D7t–D0t = Received Data bits. D7r = 0 for L = 1.

Baud-Rate Generator

The baud-rate generator determines the rate at which the transmitter and receiver operate. Bits B3–B0 in the WRITE CONFIGURATION register determine the baud-rate divisor (BRD), which divides the X1 oscillator frequency. The on-board oscillator operates with either a 1.8432MHz or a 3.6864MHz crystal, or is driven at X1 with a 45% to 55% duty-cycle square wave. Table 6 shows baud-rate divisors for given input codes, as well as the baud rate for 1.8432MHz and 3.6864MHz crystals. The generator's clock is 16 times the baud rate.

Interrupt Sources and Masks

Using the READ DATA or WRITE DATA register clears the interrupt $\overline{IRQ}$, assuming the conditions that initiated the interrupt no longer exist. Table 7 gives the details for each interrupt source. Figure 15 shows the functional diagram for the interrupt sources and mask blocks.

Two examples of setting up an IRQ for the MAX3140 are shown below.

Example 1: Setting up only the transmit buffer-empty interrupt.

Send the 16-bit word below into DIN of the MAX3140 using the WRITE CONFIGURATION register. This 16-bit word configures the MAX3140 for 9600bps, 8-bit words, no parity, and one stop bit with a 1.8432MHz crystal.

binary 1100100000001010

HEX C80A

Table 6. Baud-Rate Selection Table*

BAUD B3	B2	B1	B0	DIVISION RATIO	BAUD RATE (f_{OSC} = 1.8432MHz)	BAUD RATE (f_{OSC} = 3.6864MHz)
0	0	0	0**	1	**115.2k****	**230.4k****
0	0	0	1	2	**57.6k**	**115.2k**
0	0	1	0	4	28.8k	**57.6k**
0	0	1	1	8	14.4k	28.8k
0	1	0	0	16	7200	14.4k
0	1	0	1	32	3600	7200
0	1	1	0	64	1800	3600
0	1	1	1	128	900	1800
1	0	0	0	3	**38.4k**	76.8k
1	0	0	1	6	**19.2k**	**38.4k**
1	0	1	0	12	**9600**	**19.2k**
1	0	1	1	24	**4800**	**9600**
1	1	0	0	48	**2400**	**4800**
1	1	0	1	96	**1200**	**2400**
1	1	1	0	192	**600**	**1200**
1	1	1	1	384	**300**	**600**

**Standard baud rates shown in bold*
***Default baud rate*

Table 7. Interrupt Sources and Masks—Bit Descriptions

BIT NAME	MASK BIT	MEANING WHEN SET	DESCRIPTION
Pr	$\overline{PM}$	Received parity bit = 1	The Pr bit reflects the value in the word currently in the receive-buffer register (oldest data available). The Pr bit is set when parity is enabled (PE = 1) and the received parity bit is 1. The Pr bit is cleared either when parity is not enabled (PE = 0), or when parity is enabled and the received bit is 0. An interrupt is issued based on the oldest Pr value in the receiver FIFO. The oldest Pr value is the next value read by a READ DATA operation.
R	$\overline{RM}$	Data available	The R bit is set when new data is available to be read or when data is being read from the receive register/FIFO. FIFO is cleared when all data has been read. An interrupt is asserted as long as R = 1 and $\overline{RM}$ = 1.
RA/FE	$\overline{RAM}$	Transition on RX when in shutdown; framing error when not in shutdown	This is the RA (RX-transition) bit in shutdown, and the FE (framing-error) bit in operating mode. RA is set if there has been a transition on RX since entering shutdown. RA is cleared when the MAX3140 exits shutdown. $\overline{IRQ}$ is asserted when RA is set and $\overline{RAM}$ = 1. FE is determined solely by the currently received data, and is not stored in FIFO. The FE bit is set if a zero is received when the first stop bit is expected. FE is cleared upon receipt of the next properly framed character. $\overline{IRQ}$ is asserted when FE is set and $\overline{RAM}$ = 1.
T	$\overline{TM}$	Transmit buffer is empty	The T bit is set when the transmit buffer is ready to accept data. $\overline{IRQ}$ is asserted low if $\overline{TM}$ = 1 and the transmit buffer becomes empty. This source is cleared on the rising edge of SCLK's 16th pulse when using a READ DATA or WRITE DATA operation. Although the interrupt is cleared, poll T to determine transmit-buffer status.

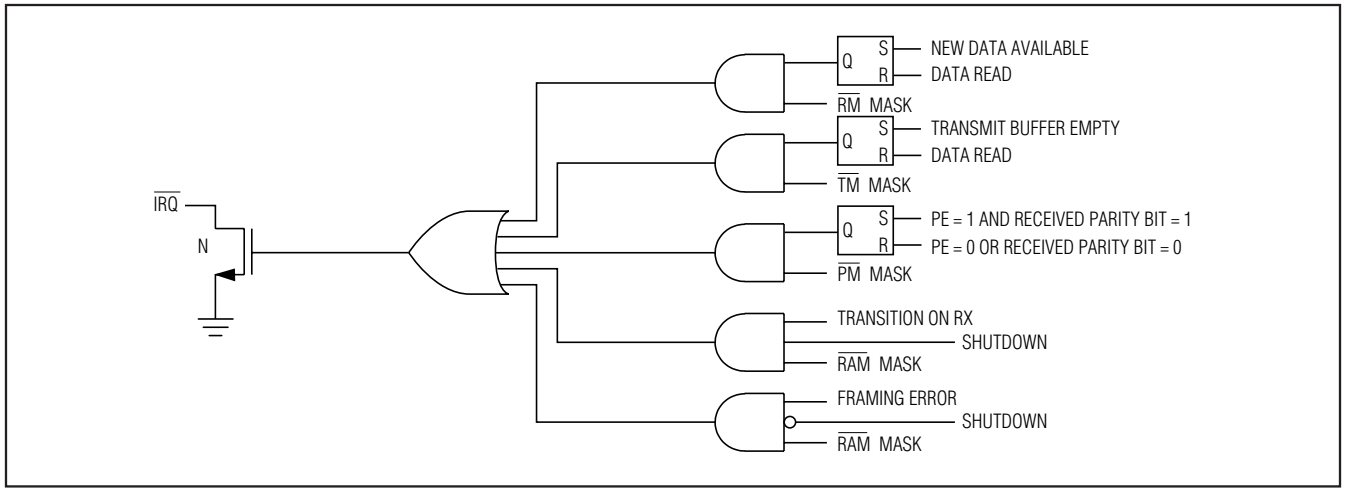


Figure 15. Functional Diagram for Interrupt Sources and Mask Blocks

SPI/MICROWIRE-Compatible UART with Integrated True Fail-Safe RS-485/RS-422 Transceivers

Example 2: Setting up only the data-available (or data-being-read) interrupt.

Send the 16-bit word below into DIN of the MAX3140 using the WRITE CONFIGURATION register. This 16-bit word configures the MAX3140 for 9600bps, 8-bit words, no parity, and one stop bit with a 1.8432MHz crystal.

binary 1100010000001010

HEX C40A

Receive FIFO

The MAX3140 contains a receive FIFO for data received by the UART to minimize processor overhead. The receive FIFO is 8 words deep and clears automatically if it overflows. Shutting down the UART also clears the receive FIFO. Upon power-up, the receive FIFO is enabled. To disable the receive FIFO, set the $\overline{FEN}$ bit high when writing to the WRITE CONFIGURATION register. To check whether the FIFO is enabled or disabled, read back the $\overline{FEN}$ bit using the READ CONFIGURATION.

UART Shutdown

In shutdown, the oscillator turns off to reduce power consumption ($I_{CCSHDN\ UART}$ < 1mA). The UART enters shutdown in one of two ways: by a software command (SHDNi bit = 1) or by a hardware command ($\overline{SHDN}$ = logic low). The hardware shutdown immediately terminates any transmission in progress. The software shutdown, requested by setting SHDNi bit = 1, is entered upon completing the transmission of the data in both the transmit-shift register and the transmit-buffer register. The SHDNo bit is set when the UART enters shutdown (either hardware or software). The microcontroller (µC) can monitor the SHDNo bit to determine when all data has been transmitted, then shut down RS-485 transceivers at that time.

Shutdown clears the receive FIFO, R, RA/FE, D0r–D7r, Pr, and Pt registers and sets the T bit high. Configuration bits ($\overline{RM}$, $\overline{TM}$, $\overline{PM}$, $\overline{RAM}$, IR, ST, PE, L, B0-3, and RTS) can be modified when SHDNo = 1 and CTS can also be read. Even though RA is reset upon entering shutdown, it goes high when a transition is detected on the RX pin. This allows the UART to monitor activity on the receiver when in shutdown.

The command to power up (SHDNi = 0) turns on the oscillator when $\overline{CS}$ goes high if $\overline{SHDN}$ = logic high, with a start-up time of at least 25ms. This is done by writing to the WRITE CONFIGURATION register, which clears all registers but RTS and CTS. Since the crystal oscillator typically requires at least 25ms to start, the first received characters can be garbled and a framing error may occur.

RS-485/RS-422 Transceiver

The RS-485/RS-422 transceiver is equipped with numerous features allowing it to be configured for any RS-485/RS-422 application. Figure 10 shows the MAX3140 functional diagram. Included in the RS-485/RS-422 transceiver function is full- and half-duplex selectability, true fail-safe circuitry, programmable slew-rate limiting, receiver input filtering, and phase control circuitry.

Full Duplex or Half Duplex

The MAX3140 operates in either full- or half-duplex mode. Drive the H/$\overline{F}$ pin low, leave it unconnected (internal pull-down), or connect it to GND for full-duplex operation or drive it high for half-duplex operation. In half-duplex mode, the receiver inputs are switched to the driver outputs, connecting outputs Y and Z to inputs A and B, respectively. In half-duplex mode, the internal full-duplex receiver input resistors are still connected to inputs A and B.

True Fail-Safe Circuitry

The MAX3140 **guarantees** a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A-B) is greater than or equal to -50mV, RO is logic high. If A-B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0 by the termination. With the receiver thresholds of the MAX3140, this results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Programmable Slew-Rate Limiting

The MAX3140 has several programmable operating modes. Transmitter rise and fall times are programmable at 2500ns, 750ns, or 25ns, resulting in maximum data rates of 115kbps, 500kbps, or 10Mbps, respectively. To select the desired data rate, drive SRL to one of three possible states by using a three-state driver, by connecting it to V_{CC} or GND, or by leaving it unconnected. For 115kbps operation, set the three-state device in high-impedance mode or leave SRL unconnected. For 500kbps operation, drive SRL high or connect it to V_{CC}. For 10Mbps operation, drive SRL low or connect it to GND. SRL can be changed during operation without interrupting data communications.

Receiver Input Filtering

The receivers of the MAX3140, when operating in 115kbps or 500kbps mode, incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 20% due to this filtering.

Phase Control Circuitry

Occasionally, twisted-pair lines are connected backward from normal orientation. The MAX3140 has two pins that invert the phase of the driver and the receiver to correct for this problem. For normal operation, drive TXP and RXP low, connect them to ground, or leave them unconnected (internal pull-down). To invert the driver phase, drive TXP high or connect it to V_{CC}. To invert the receiver phase, drive RXP high or connect it to V_{CC}. Note that the receiver threshold is positive when RXP is high.

Applications Information

Crystals, Oscillators, and Ceramic Resonators

The MAX3140 includes an oscillator circuit derived from an external crystal for baud-rate generation. For standard baud rates, use a 1.8432MHz or 3.6864MHz crystal. The 1.8432MHz crystal results in lower operating current; however, the 3.6864MHz crystal may be more readily available in surface-mount packages.

Ceramic resonators are low-cost alternatives to crystals and operate similarly, though the Q and accuracy are lower. Some ceramic resonators are available with integral load capacitors, which can further reduce cost. The trade-off between crystals and ceramic resonators is in initial frequency accuracy and temperature drift. Keep the total error in the baud-rate generator below 1% for reliable operation with other systems. This is accomplished easily with a crystal, and in most cases is achieved with ceramic resonators. Table 8 lists different types of crystals and resonators and their suppliers.

The MAX3140's oscillator supports parallel-resonant mode crystals and ceramic resonators, or can be driven from an external clock source. Internally, the oscillator consists of an inverting amplifier with its input (X1) tied to its output (X2) by a bias network that self-biases the inverter at approximately $V_{CC}/2$. The external feedback circuit, usually a crystal from X2 to X1, provides 180° of phase shift, causing the circuit to oscillate. As shown in the standard application circuit, the crystal or resonator is connected between X1 and X2, with the load capacitance for the crystal being the series combination of C1 and C2. For example, for a 1.8432MHz crystal with a specified load capacitance of 11pF, use 22pF capacitors on either side of the crystal to ground. Series-resonant mode crystals have a slight frequency error, typically oscillating 0.03% higher than specified series-resonant frequency when operated in parallel mode.

Note: It is very important to keep crystal, resonator, and load-capacitor leads and traces as short and direct as possible. Make the X1 and X2 trace lengths and ground tracks short, with no intervening traces. This helps minimize parasitic capacitance and noise pickup in the oscillator, and reduces EMI. Minimize capacitive loading on X2 to minimize supply current. The MAX3140's X1 input can be driven directly by an external CMOS clock source. The trip level is approximately equal to $V_{CC}/2$. Make no connection to X2 in this mode. If a TTL or non-CMOS clock source is used, AC-couple with a 10nF capacitor to X1. A 2V peak-to-peak swing on the input is required for reliable operation.

Table 8. Component and Supplier List

DESCRIPTION	FREQUENCY (MHz)	TYPICAL C1, C2 (pF)	SUPPLIER	PART NUMBER	PHONE NUMBER
Through-Hole Crystal (HC-49/U)	1.8432	25	ECS International, Inc.	ECS-18-13-1	(913) 782-7787
Through-Hole Ceramic Resonator	1.8432	47	Murata North America	CSA1.84MG	(800) 831-9172
Through-Hole Crystal (HC-49/US)	3.6864	33	ECS International, Inc.	ECS-36-18-4	(913) 782-7787
SMT Crystal	3.6864	39	ECS International, Inc.	ECS-36-20-5P	(913) 782-7787
SMT Ceramic Resonator	3.6864	None (integral)	AVX/Kyocera	PBRC-3.68B	(803) 448-9411