EVALUATION KIT AVAILABLE

MAX31790

6-Channel PWM-Output Fan RPM Controller

General Description

The MAX31790 controls the speeds of up to six fans using six independent PWM outputs. The desired fan speeds (or PWM duty cycles) are written through the I2C interface. The outputs drive "4-wire" fans directly, or can be used to modulate the fan's power terminals using an external pass transistor.

Tachometer inputs monitor fan tachometer logic outputs for precise (±1%) monitoring and control of fan RPM as well as detection of fan failure. Six pins are dedicated tachometer inputs. Any of the six PWM outputs can also be configured to serve as tachometer inputs.

The PWM_START inputs select the PWM output status at startup to ensure appropriate fan drive when power is first applied.

To ensure low acoustic impact of fan control, all changes in PWM duty cycle take place at a controlled, programmable rate.

The MAX31790's 3.0V to 5.5V supply voltage range and I2C-compatible interface make it ideal for fan control in a wide range of cooling applications. The MAX31790 is available in a 28-pin TQFN package and operates over the -40°C to +125°C temperature range.

Features

- ♦ **Controls Up to Six Independent Fans with PWM Drive**
- ♦ **Up to 12 Tachometer Inputs**
- ♦ **Controlled Duty Cycle Rate-of-Change for Best Acoustics**
- ♦ **I2C Bus Interface with Timeout and Watchdog**
- ♦ **3.0V to 5.5V Supply Voltage Range**
- ♦ **1.5mA (typ) Operating Supply Current**

Applications

Servers

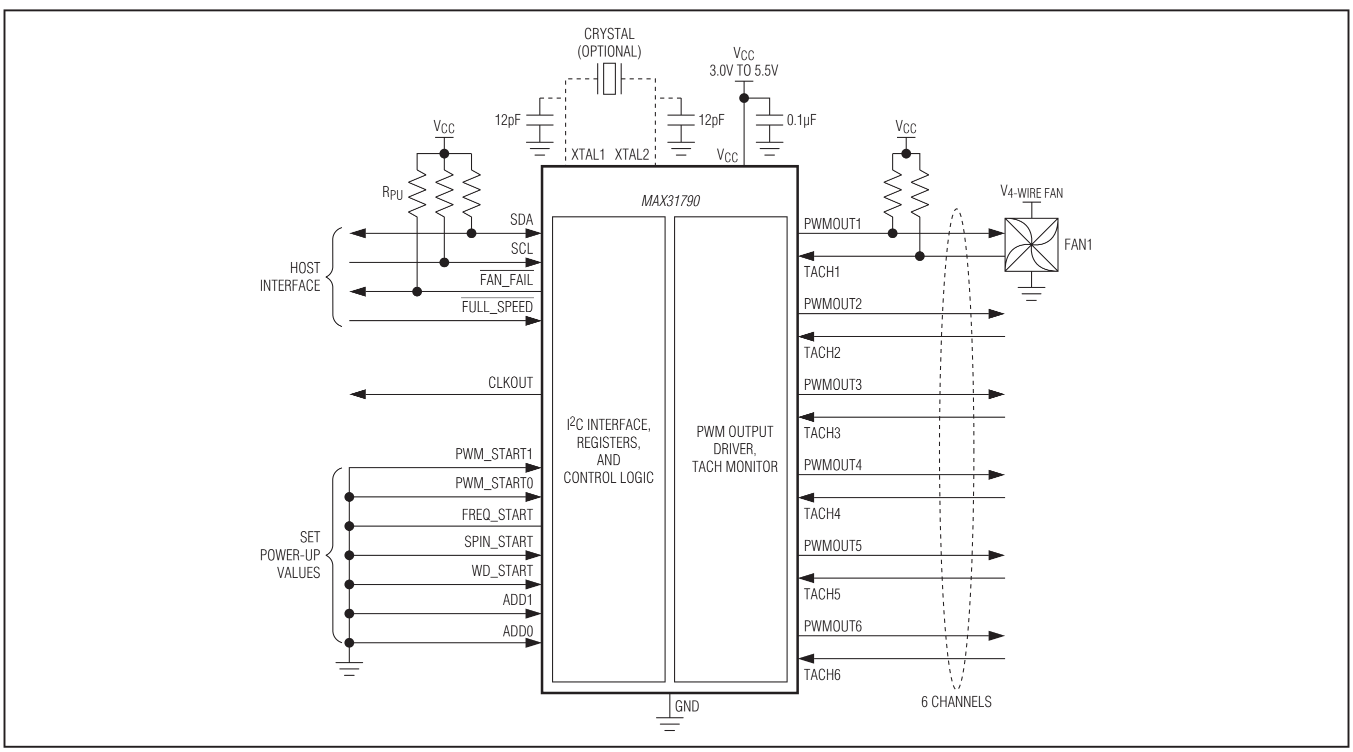
Networking

Telecom

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX31790.related***

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, SCL, ADD0, ADD1, $\overline{\text{FAN\_FAIL}}$, PWMOUTn Relative to GND...........-0.3V to +6.0V
Voltage Range on TACHn, $\overline{\text{WD\_START}}$, SPIN_START, FREQ_START, CLKOUT, $\overline{\text{FULL\_SPEED}}$, PWM_STARTn Relative to GND ....-0.3V to V_{CC} + 0.3V (not to exceed +6.0V)
Input Current at Any Pin.. +5mA
Package Input Current.. +20mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 20.8 mW/°C above +70°C).............1666.7 mW
Operating Temperature Range........................ -40°C to +125°C
Storage Temperature Range........................... -65°C to +150°C
Junction Temperature ....+150°C
ESD Protection (All Pins, HBM) (Note 1)........................ ±2000V
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Human Body Model, 100pF discharged through a 1.5kΩ resistor.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +125°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}		3.0	3.3	5.5	V
Input High Voltage	V_{IH}		V_{CC} x 0.7			V
Input Low Voltage	V_{IL}				V_{CC} x 0.3	V

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +125°C, typical values are V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current (Note 4)	I_{CC}	3.0V < V_{CC} < 3.6V		1.5	3	mA
		4.5V < V_{CC} < 5.5V		2.5	8	
POR Threshold	V_{POR}			2		V
Watchdog Timer Accuracy		f_{TOSC} = 32.768kHz (Note 5)	-0.5		+0.5	s
Output Low Voltage (SDA, $\overline{\text{FAN\_FAIL}}$, PWMOUTn, CLKOUT)		I_{OL} = 3mA			0.4	V
Output High Voltage (CLKOUT)		I_{OH} = 1mA, V_{CC} = 3.0V	2.7			V
XTAL1 Input Threshold				0.85		V
Input Leakage	I_L	(Note 6)	-1		+1	µA
Input Capacitance		All digital inputs		5		pF

FAN CONTROL CHARACTERISTICS

(T_A = -40°C to +125°C, typical values are V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Resolution			9		9	Bits
PWM Frequency Accuracy			-6		+6	%
TACH Count Resolution			11		11	Bits
TACH Count Oscillator and CLKOUT Clock	f_{TOSC}	(Note 7)		32.768		kHz
TACH Count Oscillator and CLKOUT Accuracy (Note 7)	$f_{ERR:TOSC}$	Using internal oscillator: T_A = +25°C, V_{CC} = 3.3V	-0.5		+0.5	%
		Using internal oscillator: 0°C < T_A < +70°C, 3.0V < V_{CC} < 3.6V	-2.5		+2.5	
		Using internal oscillator: -40°C < T_A < +125°C, 3.0V < V_{CC} < 3.6V	-4.0		+4.0	
		Using internal oscillator: -40°C < T_A < +125°C, 3.0V < V_{CC} < 5.5V	-7.0		+7.0	
		Using external crystal	-0.1		+0.1	
TACH Minimum Input Pulse Width	$t_{TACHMIN}$	Pulse width must be greater than this value to be detected	25		75	µs

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Notes 3, 8) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	600			ns
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
START Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA	100			ns
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL	100			ns
Data In Hold Time	$t_{HD:DAT}$	10% of SCL to 10% of SDA (Note 9)	0		0.9	µs
Maximum Receive SCL/SDA Rise Time	t_R	(Note 10)		300		ns
Minimum Receive SCL/SDA Rise Time	t_R	(Note 10)		$20 + 0.1 \times C_B$		ns

I²C AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Notes 3, 8) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Receive SCL/SDA Fall Time	t_F	(Note 10)		300		ns
Minimum Receive SCL/SDA Fall Time	t_F	(Note 10)		20 + 0.1 x C_B		ns
Transmit SDA Fall Time	t_F	10pF ≤ C_B ≤ 400pF (Note 10)	20 + 0.1 x C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}			35		ns
SDA Time Low for Reset of Serial Interface	$t_{TIMEOUT}$	(Note 11)	25		45	ms

Note 2: All voltages referenced to ground. Currents entering the IC are specified as positive.
Note 3: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 4: SDA = SCL = V_{CC}, PWM active with PWM_FREQUENCY = 25kHz.
Note 5: The watchdog timer is derived from f_{TOSC} and the watchdog timer accuracy specifications do not include the oscillator's associated error $f_{ERR:TOSC}$.
Note 6: Applies to pins SDA, SCL, PWM_STARTn, WD_START, FREQ_START, SPIN_START, ADDn, TACHn, PWMOUTn, $\overline{\text{FULL\_SPEED}}$.
Note 7: f_{TOSC} is used to measure fan speed by counting the number of 8192Hz (f_{TOSC}/4) clock cycles that take place during a selectable number of tachometer periods. For internal oscillator only, typical frequency shift due to aging is within ±0.5%. Aging stressing includes level 1 moisture reflow preconditioning (24hr +125°C bake, 168hr +85°C/85%RH moisture soak, and three solder reflow passes +260°C +0°C/-5°C peak) followed by 192hr (max) V_{CC} biased.
Note 8: All timing specifications are guaranteed by design.
Note 9: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.
Note 10: C_B—total capacitance of one bus line in pF.
Note 11: Holding the SDA line low for a time greater than $t_{TIMEOUT}$ causes the device to reset SDA to the idle state of the serial bus communication (SDA set high).

EXTERNAL CRYSTAL PARAMETERS

(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Oscillator Startup Time				1		s
Nominal Frequency	f_O			32.768		kHz
Series Resistance	ESR				50	kΩ
Load Capacitance	C_L			12		pF

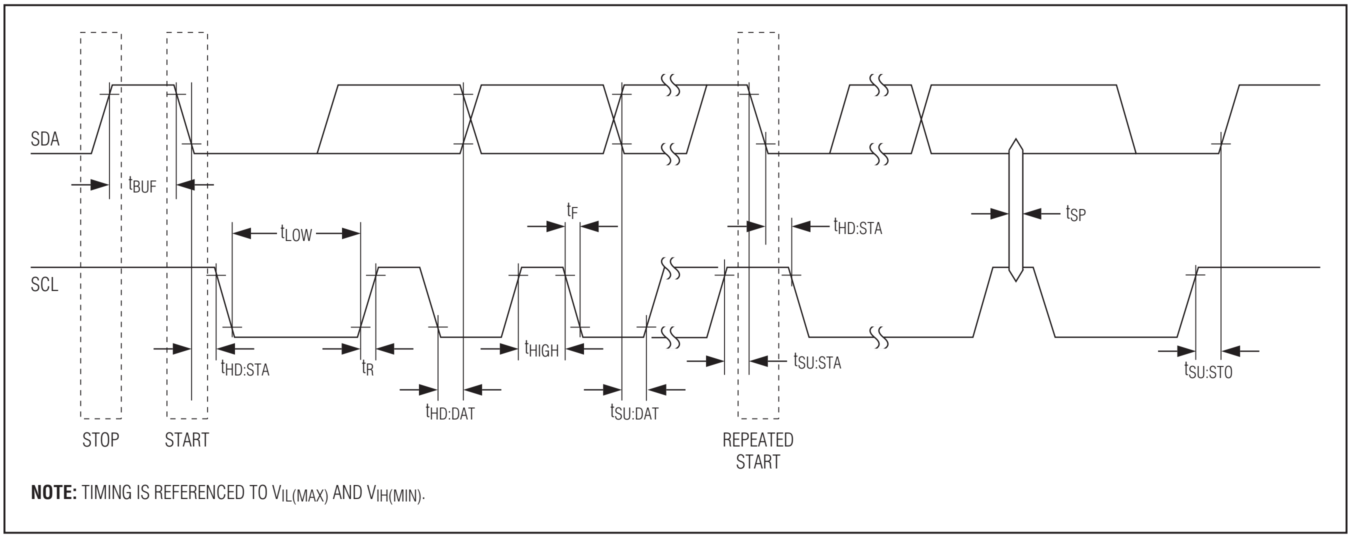
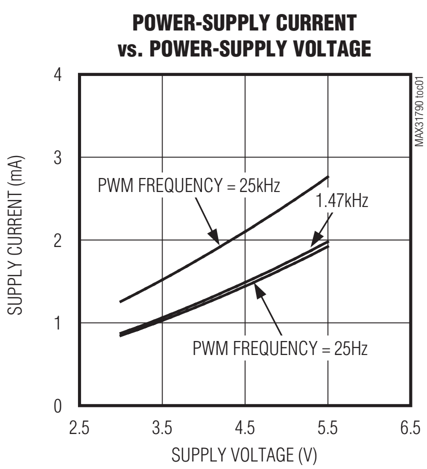
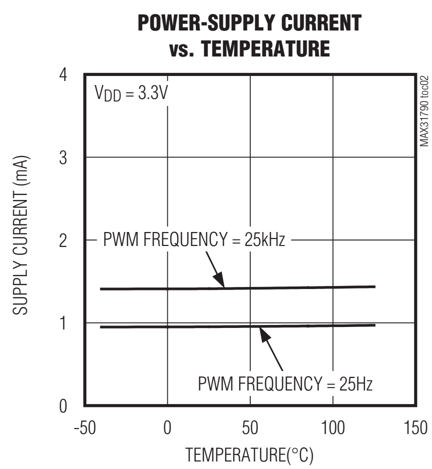


Figure 1. I²C Timing Diagram

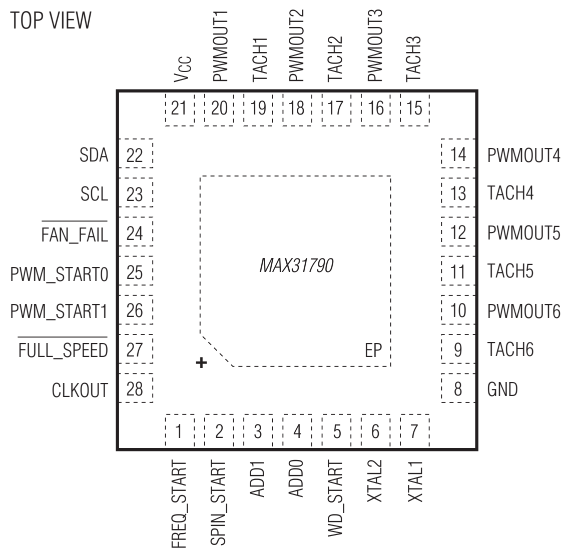
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)





Pin Configuration



TQFN
(4mm x 4mm)

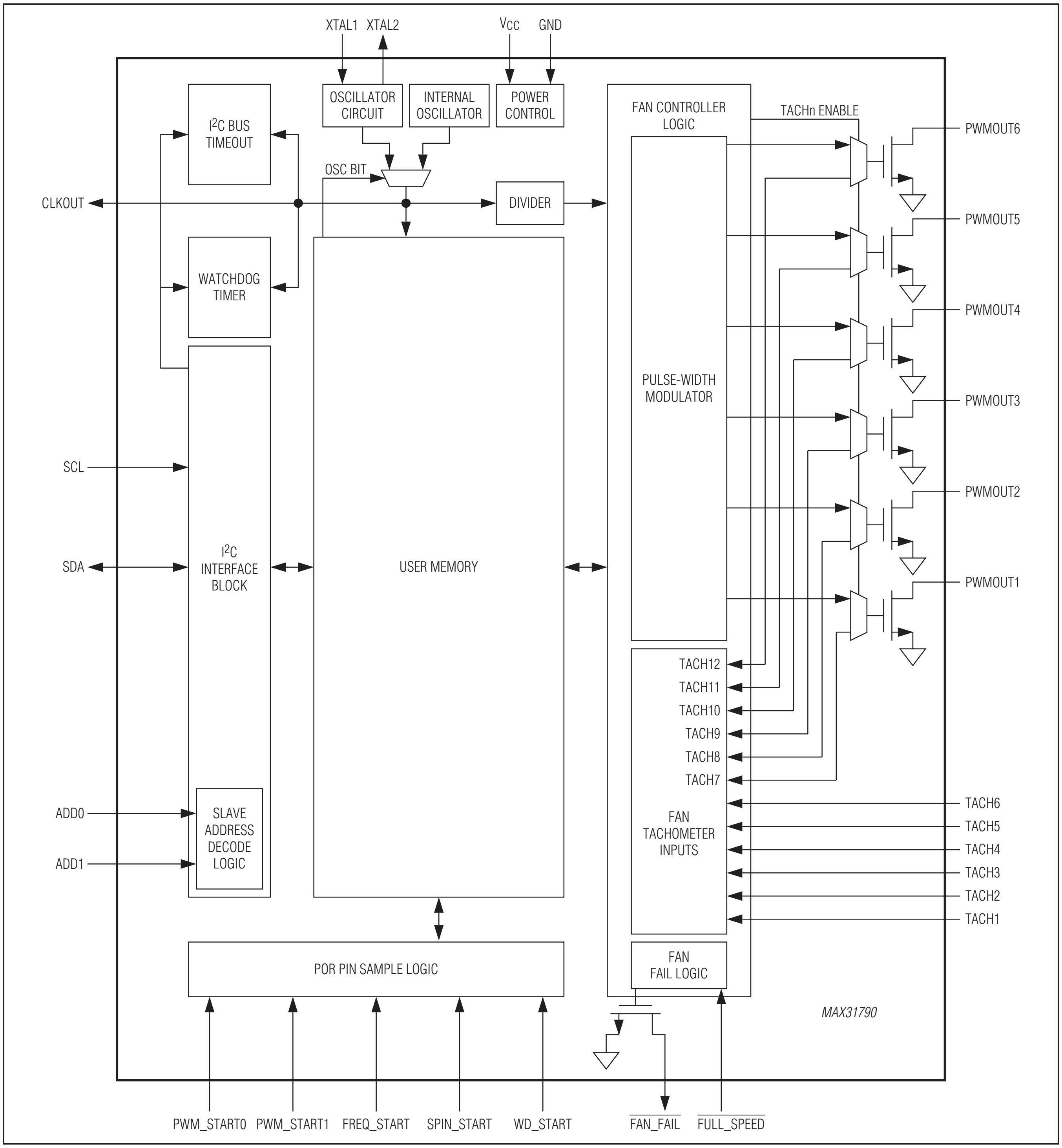
Pin Description

PIN	NAME	FUNCTION
1	FREQ_START	This input is sampled at power-up and sets the power-up value for the PWM output frequency. See the *Register Map* for values.
2	SPIN_START	This input is sampled at power-up and sets the initial spin-up behavior. See the *Register Map* for values.
3	ADD1	Address Select Inputs. Sampled at the start of every I²C transaction. One of 16 possible addresses can be selected by connecting ADD0 and ADD1 to GND, V_{CC}, SDA, or SCL.
4	ADD0	
5	WD_START	This input is sampled at power-up and sets the initial I²C watchdog behavior. See the *Register Map* for values.
6	XTAL2	Pins for Connecting to Optional 32,768Hz Crystal. The crystal can be used when the best RPM precision is required. At POR the internal oscillator is used, and a nominal 32,768Hz clock is produced at CLKOUT. If a crystal is connected between XTAL1 and XTAL2, the crystal oscillator can be enabled by writing to a register. If no crystal is present, ground XTAL1 and leave XTAL2 unconnected.
7	XTAL1	
8	GND	Ground

Pin Description (continued)

PIN	NAME	FUNCTION
9	TACH6	Logic/Analog Inputs for Tach Signals. If a fan has a logic tach output, it can be used for RPM control. For a 2-wire fan, analog input can be used for fan-failure detection. Also functions as a "locked rotor" input.
11	TACH5	
13	TACH4	
15	TACH3	
17	TACH2	
19	TACH1	
10	PWMOUT6	Open-Drain Output to 4-Wire Fan's PWM Input or (Less Frequently) to Power Transistor Modulating Fan Power Supply. Can also be used as a tachometer signal input. Can be pulled up as high as 5.5V.
12	PWMOUT5	
14	PWMOUT4	
16	PWMOUT3	
18	PWMOUT2	
20	PWMOUT1	
21	V_{CC}	Power-Supply Input. 3.3V nominal. Bypass V_{CC} to GND with a 0.1μF capacitor.
22	SDA	I^2C Serial-Data Input/Output, Open Drain. Can be pulled up to 5.5V regardless of V_{CC}.
23	SCL	I^2C Serial-Clock Input. Can be pulled up to 5.5V regardless of V_{CC}.
24	$\overline{\text{FAN\_FAIL}}$	Active-Low, Open-Drain Fan-Failure Output. Active only when fault is present.
25	PWM_START0	These inputs are sampled at power-up and set the power-up value for all PWMOUT duty cycles. See the *Register Map* for values.
26	PWM_START1	
27	$\overline{\text{FULL\_SPEED}}$	When low, this input forces all PWM outputs to 100%. Exception: If a fan has failed and "Duty Cycle = 0 on Failure" has been selected for that fan.
28	CLKOUT	CMOS Push-Pull 32,768Hz Clock Output. Signal generated from internal oscillator when external crystal is not used. If a crystal is connected between XTAL1 and XTAL2 and enabled, the crystal oscillator generates the output. Output is always active.
—	EP	Exposed Pad. Connect to GND.

Block Diagram



Detailed Description

The MAX31790 controls the speeds of up to six fans using six independent PWM outputs. The desired fan speeds (or PWM duty cycles) are written through the I^2C interface. The outputs drive "4-wire" fans directly or can be used to control 2-wire or 3-wire fans by modulating the fan's power supply voltage. Modulating the power supply voltage can be achieved by various techniques and are described in the Controlling 2-Wire and 3-Wire Fans section.

The MAX31790 has two main methods for controlling fan speeds: PWM mode and RPM mode. Additional level of control is achieved by the incorporated rate-of-change control that allows the device to control the max rate at which the PWM duty cycle is incremented/decremented.

Tachometer inputs monitor fan tachometer logic outputs for precise (±1%) monitoring and control of fan RPM as well as detection of fan failure. Six pins are dedicated tachometer inputs. Any of the six PWM outputs can also be configured to serve as tachometer inputs, allowing for up to 12 fans to be monitored.

The device can monitor the TACHn inputs and determine when a fan has failed. Failure is detected in various ways depending on the fan control mode. Once a selectable number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan).

Power-on values for PWM duty cycles, PWM frequencies, fan spin-up, and the watchdog are achieved by five pin inputs.

Fan Control

The device has two main methods for controlling fan speeds: PWM mode and RPM mode.

PWM Mode

In PWM mode, the device produces a PWM waveform that drives the fan's PWM speed control input. The fan's speed is proportional to the PWM duty cycle delivered to its PWM input terminal. The duty cycle is set by the fan's associated PWMOUT Target Duty Cycle registers and the actual duty cycle can be read from the corresponding PWMOUT Duty Cycle register. Because the duty cycle ramps to new values at a controlled rate, the values in the two registers can be different. See the Register Descriptions section for details.

RPM Mode

In RPM mode, the device monitors tachometer output pulses from the fan and adjusts the PWM duty cycle to force the fan's speed to the desired value. Fan speed is measured by counting the number of internal 8192Hz (f_{TOSC}/4) clock cycles that take place during a selectable number of tachometer periods. The number of clock cycles counted (11-bit value) is stored in the associated TACH Count registers and the desired number of cycles is stored in the TACH Target Count registers. See the Register Descriptions section for details.

Rate-of-Change Control

Sudden changes in fan speed can be easily heard by users. The device helps reduce the audibility of fan-speed changes by controlling the rate at which the PWM duty cycle is incremented. Three bits in the associated Fan Dynamics register sets the rate at which the duty cycle is incremented/decremented. This allows the time required for an LSB of change in the PWM duty cycle to vary from 0ms to 125ms.

The selected rate of change also applies when the $\overline{\text{FULL\_SPEED}}$ input is asserted or when the fans are forced to 100% due to a fan failure. See the Register Descriptions section for details.

In RPM mode when the fan's speed is near the target speed, that is, when the TACH count is near the TACH target count, the control loop dynamics can often be improved by slowing the rate of change of the PWM duty cycle. This operates as follows: First, set a value for the count "window" and store it in the appropriate Window register. In RPM mode, calculate the difference between the current TACH count and the target TACH count. If the absolute value of this difference is less than the value in the appropriate Window register, the update rate of the PWM duty cycle is slowed to 1 LSB per second. When the current TACH count falls outside of the window, the duty cycle rate of change reverts to the selected value.

Spin-Up

When a fan is not spinning, and a low duty cycle waveform is applied to its PWM terminal, it can fail to overcome inertia and start spinning. To overcome this potential problem, a 100% duty cycle waveform can be applied to the fan's PWM input for a short time before a lower duty cycle waveform is applied. This "spin-up" period allows the fan to overcome inertia and begin operating. Spin-up is controlled using the corresponding Fan

Configuration register. Spin-up can be disabled, or it can cause the fan to be driven with a 100% duty cycle until it produces two tachometer pulses, up to a maximum of 0.5s, 1s, or 2s. When spin-up is enabled and the duty cycle is making a transition from 0% to a value that is less than 100% (from 0% to 50%, for example), the duty cycle first goes to 100%. When two tachometer pulses have been detected, or when the maximum spin-up period has elapsed, the duty cycle drops to the target value (50% in this example). The SPIN_START pin sets the spin-up value at power-up.

Sequential Fan Activation

When multiple high-current fans are activated simultaneously, the startup current can stress the system's power supply. To minimize this effect, the device includes a selectable sequential fan activation feature. When selected, this feature inserts a short minimum delay between the activation times of fans.

The bits for controlling sequential fan activation are located in the Failed Fan Options/Sequential Start register. They select the time delay between fan activations to be one of the following: 0, 250ms, 500ms, 1s, 2s, or 4s. The default time is 500ms per channel.

Sequential fan activation applies to POR, fan failure forcing the fans to full speed, and assertion of the $\overline{\text{FULL\_SPEED}}$ input, which forces all the fans to full speed. In all these cases, all fans are forced to full speed. The sequence operates as follows:

- PWM1 activates. The PWM duty cycle begins to increase at the selected rate of change.
- After the selected delay time has elapsed, PWM2 activates. Again, the PWM duty cycle begins to increase at the selected rate of change.
- The other PWM channels activate in sequence, each delayed by the selected delay time relative to the previous channel. Note that the time delay applies to unused or disabled channels.

$\overline{\text{FULL\_SPEED}}$ Input

Driving this input low forces all fans to full speed with the exception of any failed fans (if 0% on failure has been selected). This input allows an external temperature switch to provide fail-safe overtemperature protection. In systems with multiple MAX31790s, all $\overline{\text{FAN\_FAIL}}$ outputs can be connected to all $\overline{\text{FULL\_SPEED}}$ inputs, thereby providing full-speed operation if any fan fails, regardless of which MAX31790 controls it. This input is active even in standby mode.

POR Options

Five inputs allow setup of the device's behavior at power-up. The following inputs are sampled when power is first applied to the device:

WD_START: At power-up the watchdog operation is controlled by the WD_START pin. Connect WD_START to V_{CC} to enable, or to GND to disable the watchdog function. When enabled using WD_START, the timeout period is 30s. After power is applied, the watchdog function can be enabled or disabled, and the timeout period can be changed by editing the Global Configuration register.

SPIN_START: At power-up, spin-up operation is controlled by the SPIN_START pin. Connect SPIN_START to GND to disable, V_{CC} to enable spin-up for a maximum of 1s, or unconnected to enable spin-up for a maximum of 0.5s. After power is applied, the spin-up function can be enabled or disabled, and the spin-up period can be changed by editing the associated Fan Configuration register.

PWM_START0, PWM_START1: At power-up, the PWM output duty cycles are controlled by the PWM_START0 and PWM_START1 pins. Connect PWM_START0/ PWM_START1 to GND, V_{CC}, or leave unconnected to achieve different duty cycles for all PWM outputs. See the PWMOUT Target Duty Cycle register for the corresponding values and connections. After power is applied, the PWM duty cycles can be changed, by editing that PWM's associated PWMOUT Target Duty Cycle register.

FREQ_START: At power-up, all PWM output frequencies are controlled by the FREQ_START pin. Connect FREQ_START to GND for 30Hz, V_{CC} for 25kHz, or unconnected for 1.47kHz. After power is applied, the PWM output frequencies can be changed by editing the PWM Frequency register.

Watchdog

The device includes an optional I^2C watchdog function that monitors the I^2C bus for transactions. When the watchdog function is enabled, all fans (with the exception of failed fans "0% on fail" selected) are forced to full speed if no I^2C transactions occur within a selected period (5s, 10s, or 30s). Watchdog timing is selected using the Global Configuration register.

Fan Monitoring

Monitoring Tachometer Signals

The TACH inputs accept either tachometer or "locked rotor" output signals from 3-wire or 4-wire fans. When measuring fan speed, the device counts the number of internal 8192Hz ($f_{TOSC}/4$)clock cycles that occur during 1, 2, 4, 8, 16, or 32 tachometer periods. (The speed of each fan is measured once per second.) The number of tachometer periods is selectable for each fan by using the appropriate Fan Dynamics register. Tachometer pulses less than $t_{TACHMIN}$ in duration are ignored to minimize the effect of noise on the tachometer lines. The TACH count for a given RPM can be obtained from the following equation:

$$\text{TACH Count} = \frac{60}{NP \times RPM} \times SR \times 8192$$

where:

NP = number of tachometer pulses per revolution. Most general-purpose brushless DC fans produce two tachometer pulses per revolution.

SR = 1, 2, 4, 8, 16, or 32. This is the number of tachometer periods over which the tachometer clock is counted. See the Speed Range bit information described in the corresponding Fan Dynamics register description.

The tachometer count consists of 11 bits in the TACH Count registers and is available in RPM and PWM modes. In RPM mode, the desired fan count is written to the associated TACH Target Count register. In PWM mode, the desired fan duty cycle is written to the associated PWMOUT Target Duty Cycle register.

Note that the device is intended to be used with 4-wire fans. Modulating a fan's power supply with a PWM waveform, as is sometimes done with 2-wire and 3-wire fans, results in incorrect tachometer counts due to the periodic removal of power from the fan's internal circuitry. Therefore, it is suggested to use PWM mode when interfacing with 2-wire or 3-wire fans.

Using PWM Outputs as Tachometer Inputs

Each Fan Configuration register includes a $\overline{\text{PWM}}$/TACH bit that allows the PWMOUT to be configured as a TACH input. In TACH mode, the settings for TACH input enable, locked rotor operation, and TACH pulses counted that have been selected for a given fan channel apply to that channel's TACH input and also to TACH signals sensed by that channel's PWM output.

Figure 2 to Figure 6 show some examples of TACH-PWM connections for various fan configurations

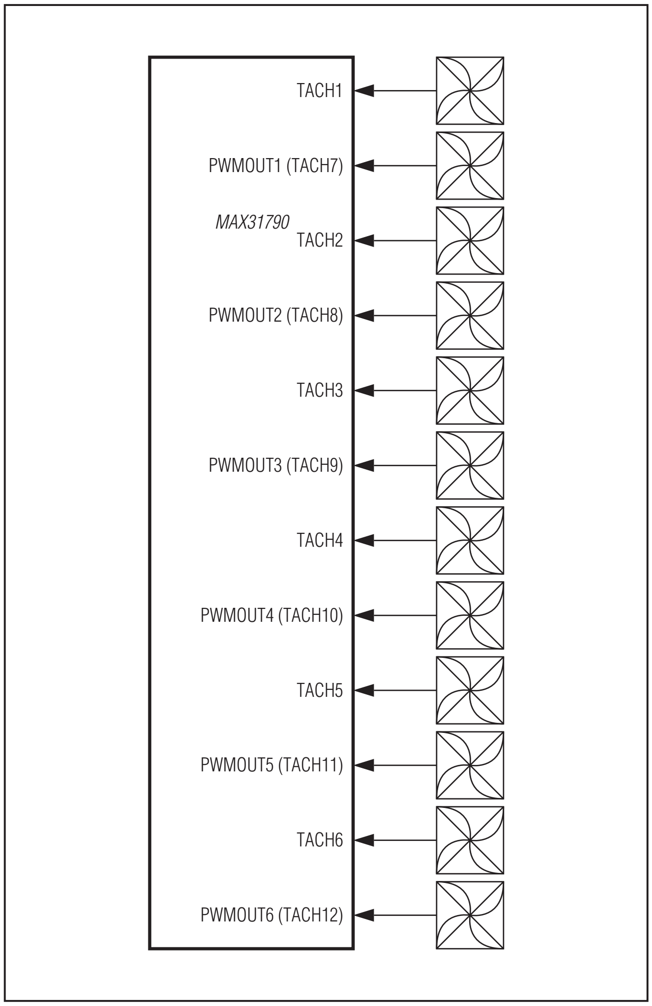


Figure 2. 12 Fans, 12 TACH Monitors, No PWM

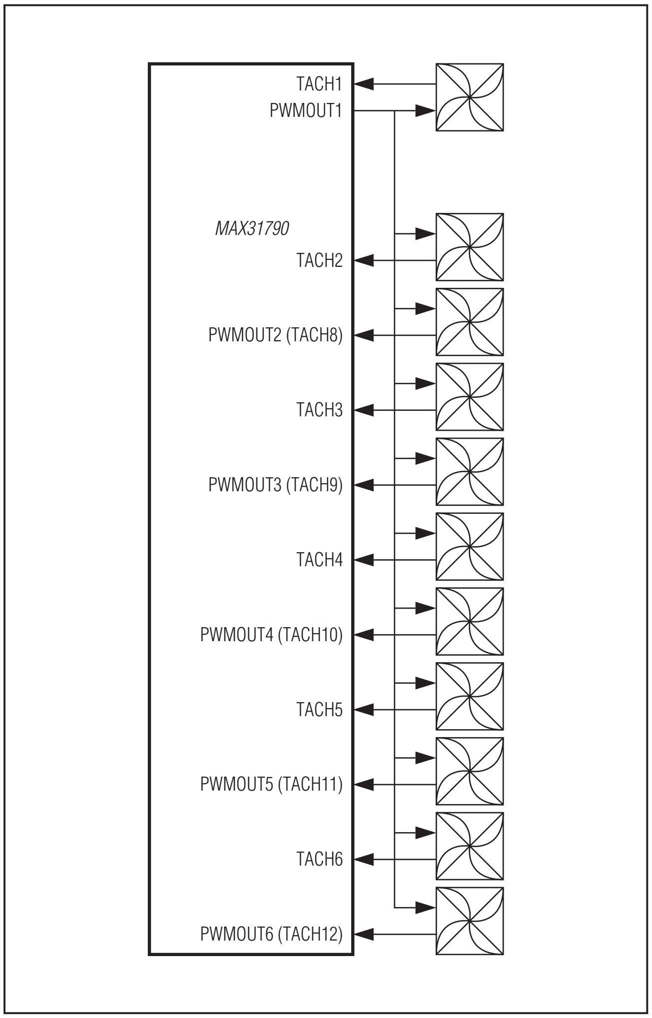


Figure 3. 11 Fans, 11 TACH Monitors,1 PWM

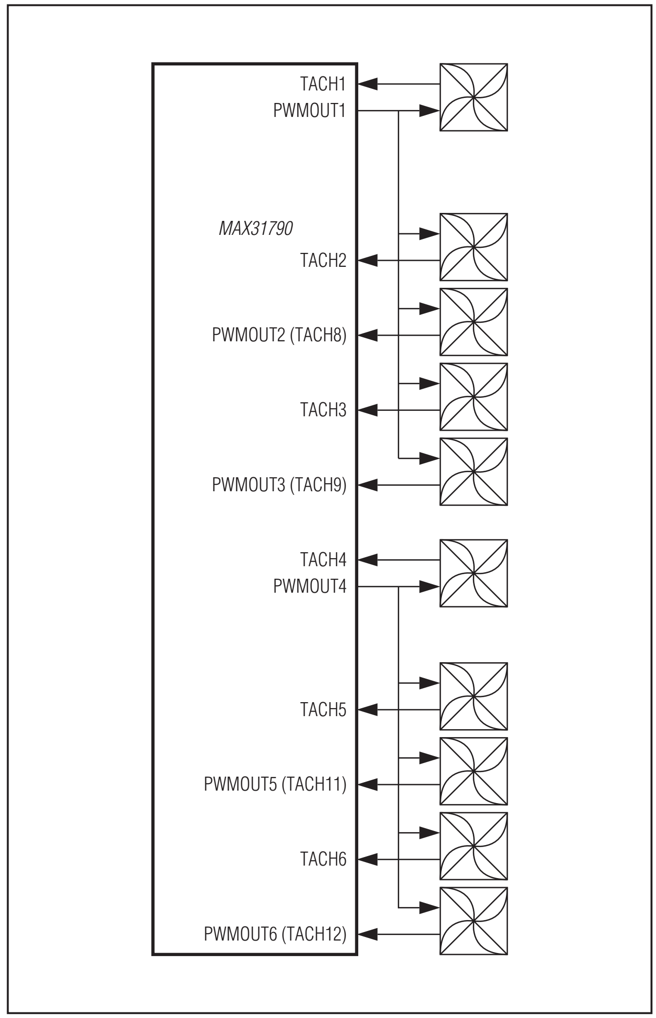


Figure 4. 10 Fans, 10 TACH Monitors, 2 PWMs

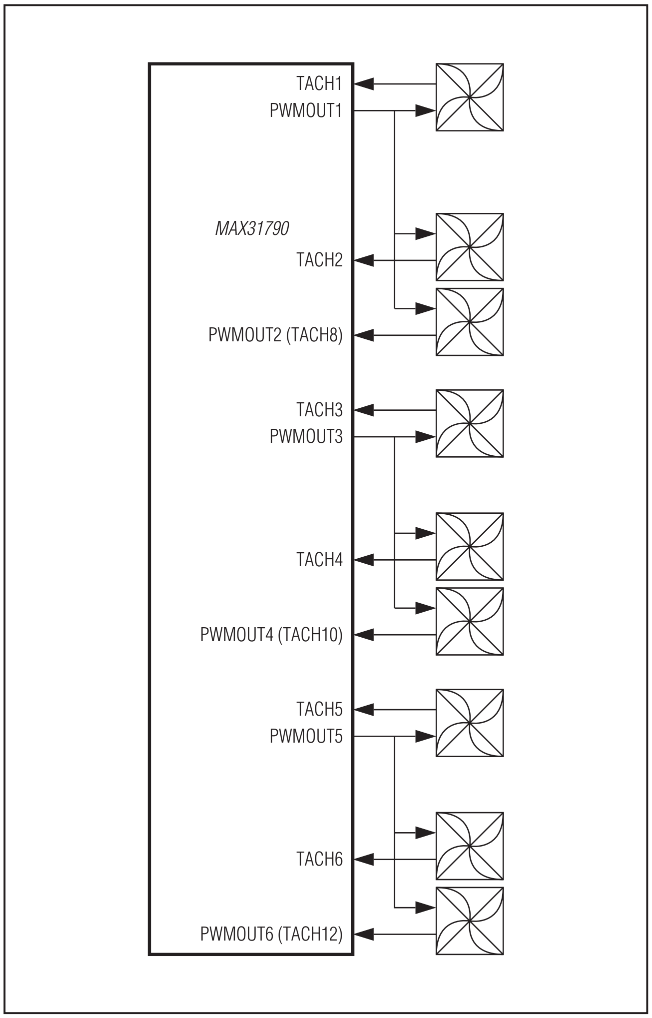


Figure 5. 9 Fans, 9 TACH Monitors, 3 PWMs

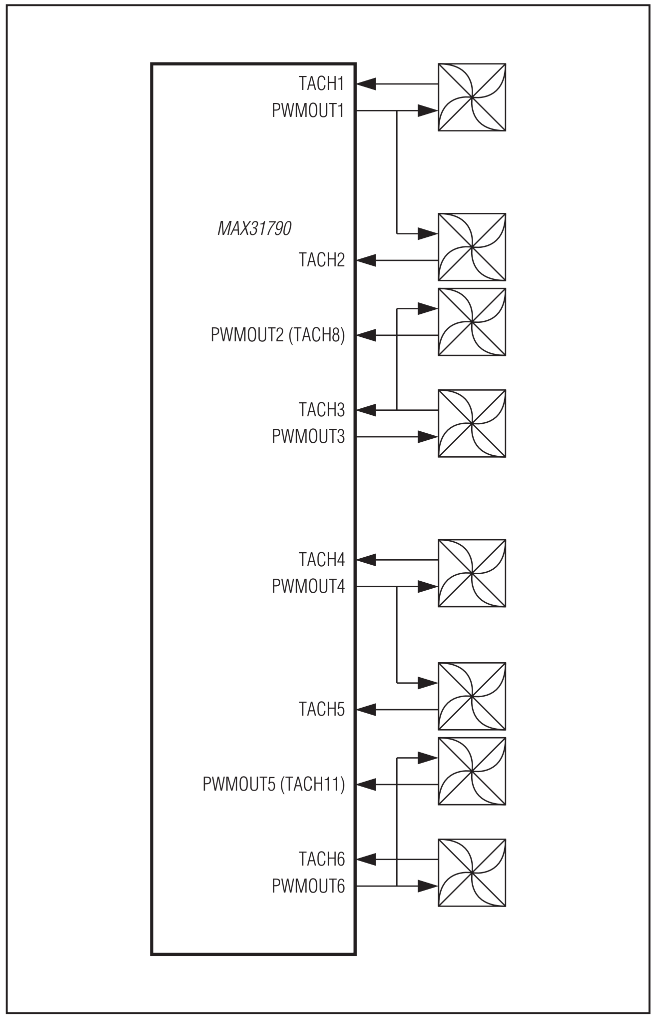


Figure 6. 8 Fans, 8 TACH Monitors, 4 PWMs

Fan Failure

When enabled, the device monitors the TACH inputs to determine when a fan has failed. For fans with tachometer outputs, failure is detected in various ways depending on the fan control mode. In every case, from one to six consecutive fault detections (selected by the Fan Fault Queue bits) are required to decide that the fan has failed. When the selected number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan).

PWM Mode Failure Detection

In PWM mode, the TACH Target Count register holds the upper limit for tachometer count values. A potential fault condition is identified when the TACH count exceeds the value written to the TACH Target Count register. If the Fan Fault Queue bit value is 1 and the following tachometer count (1 second later) also exceeds the limit value, the fan is considered to have failed. A higher Fan Fault Queue bit value requires a larger number of consecutive values in excess of the limit value. When a PWM output is used as a TACH input, the PWM-mode failure criteria apply. In PWM mode, fan-failure detection is masked when the target duty cycle is set to zero.

RPM Mode Failure Detection

In RPM mode, a potential fault condition is identified when any of the following three conditions occur: 1) the TACH count exceeds the associated value stored in the TACH Target Count register while the PWM duty cycle is 100%, 2) the TACH count exceeds two times the TACH Target Count register value while the duty cycle is less than 100%, or 3) the TACH count reaches its maximum value of 7FFh. If the Fan Fault Queue bit value is 1 and the TACH Count value also exceeds the limit value, the fan is considered to have failed. A higher Fan Fault Queue value requires a larger number of consecutive values in excess of the limit value. In RPM mode, fan-failure detection is masked when the TACH Target Count register is set to full scale.

Locked Rotor Mode Failure Detection

Some fans have a locked rotor output that produces a logic-level output to indicate that the fan has stopped spinning. Locked rotor signals can be monitored by setting the TACH/Locked Rotor bit in the associated Fan Configuration register. The polarity of the locked rotor signal can be adjusted in this same register. A fan fault is detected when a locked rotor signal has been present for 1 second.

Failure Indication

Fan failure is indicated in the Fan Fault register and also with the open-drain FAN_FAIL output after the number of consecutive faults selected by the Fan Fault Queue bits have occurred. The FAN_FAIL output can be masked using the mask bits in the Fan Fault Mask register.

When a fan has failed, PWM to the affected fan can continue as though the fan is still operational, or the duty cycle can be automatically set to 0 or 100% as determined by the Failed Fan Options bits. See the *Register Descriptions* section for full details.

The failed condition can be cancelled by writing PWM Target duty cycle or TACH target count to the fan's control registers. The new value can be the same as the value already in the register. After writing to the register, the fan-failure detection process begins again. If the fan is still in a failed state, fan failure again is detected.

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus an R/W bit (Figure 7). The device's slave address is determined by the state of the ADD0 and ADD1 address pins during a START condition of an I²C transaction. The ADD0 and ADD1 pins can be connected to GND, V_{CC}, SDA, or SCL. These pins allow up to 16 MAX31790s to reside on the same I²C bus. See Table 1 for a complete list of all 16 possibilities and the corresponding ADD0 and ADD1 pin connections.

For example, the device's slave address byte is 40h when ADD0 and ADD1 pins are grounded during a START condition. I²C communication is described in detail in the *I²C Serial Interface Description* section.

Note: If the state of the ADD0 and ADD1 pins is changing during normal operation, the slave address of the device dynamically changes to reflect the pins states at every START condition. The ADD0 and ADD1 pins cannot change during an I²C transaction.

Table 1. Slave Address Table

ADD1 CONNECTION	ADD0 CONNECTION	SLAVE ADDRESS BYTE (HEX)
GND	GND	40
GND	SCL	42
GND	SDA	44
GND	VCC	46
SCL	GND	48
SCL	SCL	4A
SCL	SDA	4C
SCL	VCC	4E
SDA	GND	50
SDA	SCL	52
SDA	SDA	54
SDA	VCC	56
VCC	GND	58
VCC	SCL	5A
VCC	SDA	5C
VCC	VCC	5E

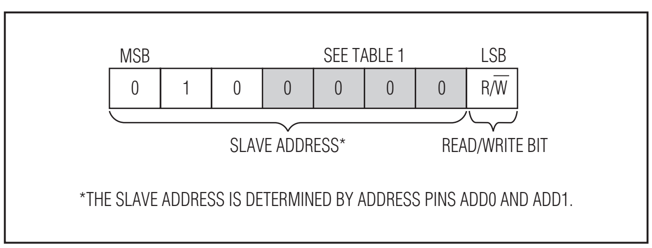


Figure 7. MAX31790 Slave Address Byte Example

Memory Description

The device's control registers are organized in rows of 8 bytes. The I²C master can read or write individual bytes, or can read or write multiple bytes. When writing consecutive bytes, all writes are to the same row. When the final byte in the row is reached, the next byte written is the row's first byte. For example, a write that starts with 02h (Fan 1 Configuration) can write to 02h, 03h, 04h, 05h, 06h, and 07h. If writes continue, the next byte written is 00h, and so on.

Consecutive reads are not subject to the single-row limitation. A read can start at any address and can continue through FFh. If reads continue past FFh, they wrap around to 00h.

"User Bytes" are general-purpose R/W bytes. X denotes the input state at POR.

Register Map

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00h	0010 0XX0b	Global Configuration	$\overline{\text{Run}}$/Standby 0 = Run 1 = Standby	Reset: 0 = Normal 1 = Reset	$\overline{\text{Bus Timeout}}$ 0 = Enabled	RESERVED	OSC: 0 = Internal oscillator 1 = External crystal	I²C Watchdog: 00b = Disabled 01b = 5s 10b = 10s 11b = 30s		I²C Watchdog Status 1 = Watchdog fault detected
R/W	01h	FREQ_START	PWM Frequency	PWM4-PWM6 Frequency: 0000b = 25Hz 0001b = 30Hz 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz				PWM1-PWM3 Frequency: 0000b = 25Hz 0001b = 30Hz 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz			
R/W	02h	0XX0 0000b	Fan 1 Configuration	Mode: 0 = PWM 1 = RPM	Spin-Up 00b = No Spin-up 01b = 2 TACH counts or 0.5s 10b = 2 TACH counts or 1s 11b = 2 TACH counts or 2s		$\overline{\text{Control}}$/Monitor 0 = Control 1 = Monitor only	TACH Input Enable 1 = Enabled	$\overline{\text{TACH}}$/Locked Rotor 0 = TACH 1 = Locked Rotor	Locked Rotor Polarity 0 = Low 1 = High	$\overline{\text{PWM}}$/TACH 0 = PWM 1 = TACH
R/W	03h	0XX0 0000b	Fan 2 Configuration	Same as Fan 1 Configuration							
R/W	04h	0XX0 0000b	Fan 3 Configuration	Same as Fan 1 Configuration							

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	0XX0 0000b	Fan 4 Configuration	Same as Fan 1 Configuration							
R/W	06h	0XX0 0000b	Fan 5 Configuration	Same as Fan 1 Configuration							
R/W	07h	0XX0 0000b	Fan 6 Configuration	Same as Fan 1 Configuration							
R/W	08h	0100 1100b	Fan 1 Dynamics	Speed Range (TACH Periods Counted) 000b = 1 001b = 2 010b = 4 (default) 011b = 8 100b = 16 101b = 32 110b = 32 111b = 32			PWM Rate-of-Change: 000b = 0ms per LSB (PWM) 000b = 0.9765ms per LSB (RPM) 001b = 1.953125ms per LSB 010b = 3.90625ms per LSB 011b = 7.8125ms per LSB (default) 100b = 15.625ms per LSB 101b = 31.25ms per LSB 110b = 62.5ms per LSB 111b = 125ms per LSB			Asymmetric Rate of Change 1 = Enabled	RESERVED
R/W	09h	0100 1100b	Fan 2 Dynamics	Same as Fan 1 Dynamics							
R/W	0Ah	0100 1100b	Fan 3 Dynamics	Same as Fan 1 Dynamics							
R/W	0Bh	0100 1100b	Fan 4 Dynamics	Same as Fan 1 Dynamics							
R/W	0Ch	0100 1100b	Fan 5 Dynamics	Same as Fan 1 Dynamics							
R/W	0Dh	0100 1100b	Fan 6 Dynamics	Same as Fan 1 Dynamics							
R/W	0Eh	0000 0000b	User Byte	—							
R/W	0Fh	0000 0000b	User Byte	—							
R/W	10h	0000 0000b	Fan Fault Status 2	RESERVED	RESERVED	Fan 12 Fault 1 = Fault	Fan 11 Fault 1 = Fault	Fan 10 Fault 1 = Fault	Fan 9 Fault 1 = Fault	Fan 8 Fault 1 = Fault	Fan 7 Fault 1 = Fault
R/W	11h	0000 0000b	Fan Fault Status 1	RESERVED	RESERVED	Fan 6 Fault 1 = Fault	Fan 5 Fault 1 = Fault	Fan 4 Fault 1 = Fault	Fan 3 Fault 1 = Fault	Fan 2 Fault 1 = Fault	Fan 1 Fault 1 = Fault
R/W	12h	0011 1111b	Fan Fault Mask 2	RESERVED	RESERVED	Fan 12 Mask 1 = Masked	Fan 11 Mask 1 = Masked	Fan 10 Mask 1 = Masked	Fan 9 Mask 1 = Masked	Fan 8 Mask 1 = Masked	Fan 7 Mask 1 = Masked
R/W	13h	0011 1111b	Fan Fault Mask 1	RESERVED	RESERVED	Fan 6 Mask 1 = Masked	Fan 5 Mask 1 = Masked	Fan 4 Mask 1 = Masked	Fan 3 Mask 1 = Masked	Fan 2 Mask 1 = Masked	Fan 1 Mask 1 = Masked

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	0100 0101b	Failed Fan Options/ Sequential Start	Sequential Start Delay 000b = 0s 001b = 250ms 010b = 500ms 011b = 1s 100b = 2s 101b, 110b, 111b = 4s			RESERVED	Failed Fan Options 00b = duty cycle = 0% on fail 01b = Continue PWM or RPM mode operation on fail. 10b = duty cycle = 100% on fail 11b = All fans to 100% on any unmasked fan failure.		Fan Faut Queue 00b = 1 fault 01b = 2 faults 10b = 4 faults 11b = 6 faults	
R/W	15h	0000 0000b	User Byte	—							
R/W	16h	0000 0000b	User Byte	—							
R/W	17h	0000 0000b	User Byte	—							
R	18h	1111 1111b	TACH 1 Count MSB	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}
R	19h	1110 0000b	TACH 1 Count LSB	2^{2}	2^{1}	2^{0}	0	0	0	0	0
R	1Ah	1111 1111b	TACH 2 Count MSB	Same as TACH 1 Count							
R	1Bh	1110 0000b	TACH 2 Count LSB								
R	1Ch	1111 1111b	TACH 3 Count MSB	Same as TACH 1 Count							
R	1Dh	1110 0000b	TACH 3 Count LSB								
R	1Eh	1111 1111b	TACH 4 Count MSB	Same as TACH 1 Count							
R	1Fh	1110 0000b	TACH 4 Count LSB								
R	20h	1111 1111b	TACH 5 Count MSB	Same as TACH 1 Count							
R	21h	1110 0000b	TACH 5 Count LSB								
R	22h	1111 1111b	TACH 6 Count MSB	Same as TACH 1 Count							
R	23h	1110 0000b	TACH 6 Count LSB								
R	24h	1111 1111b	TACH 7 Count MSB	Same as TACH 1 Count							
R	25h	1110 0000b	TACH 7 Count LSB								

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R	26h	1111 1111b	TACH 8 Count MSB	Same as TACH 1 Count							
R	27h	1110 0000b	TACH 8 Count LSB								
R	28h	1111 1111b	TACH 9 Count MSB	Same as TACH 1 Count							
R	29h	1110 0000b	TACH 9 Count LSB								
R	2Ah	1111 1111b	TACH 10 Count MSB	Same as TACH 1 Count							
R	2Bh	1110 0000b	TACH 10 Count LSB								
R	2Ch	1111 1111b	TACH 11 Count MSB	Same as TACH 1 Count							
R	2Dh	1110 0000b	TACH 11 Count LSB								
R	2Eh	1111 1111b	TACH 12 Count MSB	Same as TACH 1 Count							
R	2Fh	1110 0000b	TACH 12 Count LSB								
R	30h	0000 0000b	PWMOUT 1 Duty Cycle MSB	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1
R	31h	0000 0000b	PWMOUT 1 Duty Cycle LSB	2^0	0	0	0	0	0	0	0
R	32h	0000 0000b	PWMOUT 2 Duty Cycle MSB	Same as PWMOUT 1 Duty Cycle							
R	33h	0000 0000b	PWMOUT 2 Duty Cycle LSB								
R	34h	0000 0000b	PWMOUT 3 Duty Cycle MSB	Same as PWMOUT 1 Duty Cycle							
R	35h	0000 0000b	PWMOUT 3 Duty Cycle LSB								

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R	36h	0000 0000b	PWMOUT 4 Duty Cycle MSB	Same as PWMOUT 1 Duty Cycle							
R	37h	0000 0000b	PWMOUT 4 Duty Cycle LSB								
R	38h	0000 0000b	PWMOUT 5 Duty Cycle MSB	Same as PWMOUT 1 Duty Cycle							
R	39h	0000 0000b	PWMOUT 5 Duty Cycle LSB								
R	3Ah	0000 0000b	PWMOUT 6 Duty Cycle MSB	Same as PWMOUT 1 Duty Cycle							
R	3Bh	0000 0000b	PWMOUT 6 Duty Cycle LSB								
R	3Ch	0000 0000b	RESERVED	0	0	0	0	0	0	0	0
R	3Dh	0000 0000b	RESERVED	0	0	0	0	0	0	0	0
R	3Eh	0000 0000b	RESERVED	0	0	0	0	0	0	0	0
R	3Fh	0000 0000b	RESERVED	0	0	0	0	0	0	0	0
R/W	40h	PWM_START	PWMOUT1 Target Duty Cycle MSB	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1
R/W	41h	PWM_START	PWMOUT1 Target Duty Cycle LSB	2^0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W	42h	PWM_START	PWMOUT2 Target Duty Cycle MSB	Same as PWMOUT 1 Target Duty Cycle							
R/W	43h	PWM_START	PWMOUT2 Target Duty Cycle LSB								
R/W	44h	PWM_START	PWMOUT3 Target Duty Cycle MSB	Same as PWMOUT 1 Target Duty Cycle							
R/W	45h	PWM_START	PWMOUT3 Target Duty Cycle LSB								

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	46h	PWM_START	PWMOUT4 Target Duty Cycle MSB	Same as PWMOUT 1 Target Duty Cycle							
R/W	47h	PWM_START	PWMOUT4 Target Duty Cycle LSB								
R/W	48h	PWM_START	PWMOUT5 Target Duty Cycle MSB	Same as PWMOUT 1 Target Duty Cycle							
R/W	49h	PWM_START	PWMOUT5 Target Duty Cycle LSB								
R/W	4Ah	PWM_START	PWMOUT6 Target Duty Cycle MSB	Same as PWMOUT 1 Target Duty Cycle							
R/W	4Bh	PWM_START	PWMOUT6 Target Duty Cycle LSB								
R/W	4Ch	0000 0000b	User Byte	—							
R/W	4Dh	0000 0000b	User Byte	—							
R/W	4Eh	0000 0000b	User Byte	—							
R/W	4Fh	0000 0000b	User Byte	—							
R/W	50h	0011 1100b	TACH 1 Target Count MSB	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3
R/W	51h	0000 0000b	TACH 1 Target Count LSB	2^2	2^1	2^0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W	52h	0011 1100b	TACH 2 Target Count MSB	Same as TACH 1 Target Count							
R/W	53h	0000 0000b	TACH 2 Target Count LSB								
R/W	54h	0011 1100b	TACH 3 Target Count MSB	Same as TACH 1 Target Count							
R/W	55h	0000 0000b	TACH 3 Target Count LSB								

Register Map (continued)

R/W	REGISTER	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	56h	0011 1100b	TACH 4 Target Count MSB	Same as TACH 1 Target Count							
R/W	57h	0000 0000b	TACH 4 Target Count LSB								
R/W	58h	0011 1100b	TACH 5 Target Count MSB	Same as TACH 1 Target Count							
R/W	59h	0000 0000b	TACH 5 Target Count LSB								
R/W	5Ah	0011 1100b	TACH 6 Target Count MSB	Same as TACH 1 Target Count							
R/W	5Bh	0000 0000b	TACH 6 Target Count LSB								
R/W	5Ch	0000 0000b	User Byte	—							
R/W	5Dh	0000 0000b	User Byte	—							
R/W	5Eh	0000 0000b	User Byte	—							
R/W	5Fh	0000 0000b	User Byte	—							
R/W	60h	0000 0000b	Window 1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
R/W	61h	0000 0000b	Window 2	Same as Window 1							
R/W	62h	0000 0000b	Window 3	Same as Window 1							
R/W	63h	0000 0000b	Window 4	Same as Window 1							
R/W	64h	0000 0000b	Window 5	Same as Window 1							
R/W	65h	0000 0000b	Window 6	Same as Window 1							
R/W	66h	0000 0000b	User Byte	—							
R/W	67h	0000 0000b	User Byte	—							

X = Input state at POR.

Register Descriptions

X = Input state at POR.

Global Configuration Register (00h)

Power-On Value	0010 0XX0b
Read Access	All
Write Access	All
Memory Type	Volatile

	BIT 7						BIT 0
00h	$\overline{\text{Run}}$/ Standby	Reset	Bus Timeout	RESERVED	OSC	I^2C Watchdog	I^2C Watchdog Status

BIT 7	**$\overline{\text{Run}}$/Standby:** Places the device in standby mode. 0 = Run 1 = Standby Entering standby mode sets all PWM duty cycles to 0 and stops fan failure detection. However, driving the $\overline{\text{FULL\_SPEED}}$ input low forces all enabled PWMOUT outputs high (100% duty cycle) regardless of the state of the $\overline{\text{Run}}$ bit.
BIT 6	**Reset:** 0 = Normal operation 1 = Reset all registers to POR value This bit automatically resets itself and always returns a 0 when read.
BIT 5	**$\overline{\text{Bus Timeout}}$:** I^2C bus timeout. 0 = Enabled 1 = Disabled The I^2C interface resets if SDA is low for more than 35ms.
BIT 4	**RESERVED**
BIT 3	**Oscillator Selection:** 0 = Internal oscillator (default at power-on) 1 = External 32.768kHz crystal Selects on-chip oscillator or external 32.768kHz crystal/ceramic resonator for TACH count and source for CLKOUT pin. Use crystal or ceramic resonator if higher accuracy is required. When switching from the internal oscillator to an external crystal, the device operates from the internal oscillator until the crystal oscillator has started up. If the crystal is damaged or the oscillator fails to start, the device continues to operate from the internal oscillator.

<table>
<tr><td rowspan="6">BITS 2:1</td><td colspan="3">I^{2}C Watchdog: When active, the watchdog monitors SDA and SCL for valid I^{2}C transactions. If there are no valid transactions between the master and the device within the watchdog period, all fan PWM outputs go to 100%. If the watchdog times out and valid I^{2}C transactions begin to occur again, operation resumes with the previous PWM value. The master can then program the PWM outputs, target TACH counts, or other functions in the normal manner. When the watchdog function is active, ensure that the master communicates to the device periodically, for example, reading a status register. The POR state is set by the state of the WD_START pin at power-up.</td></tr>
<tr><td>BITS 2:1</td><td>I^{2}C WATCHDOG PERIOD (s)</td><td>POR CONDITION</td></tr>
<tr><td>00b</td><td>Inactive (no watchdog)</td><td>WD_START = GND</td></tr>
<tr><td>01b</td><td>5</td><td>—</td></tr>
<tr><td>10b</td><td>10</td><td>—</td></tr>
<tr><td>11b</td><td>30</td><td>WD_START = V_{CC}</td></tr>
<tr><td>BIT 0</td><td colspan="3">I^{2}C Watchdog Status:
0 = I^{2}C transactions occurred within watchdog period
1 = Time between I^{2}C transaction exceeds watchdog period
Clear this bit by writing a 0 to it.</td></tr>
</table>

PWM Frequency Register (01h)

Power-On Value	XXXX XXXXb
Read Access	All
Write Access	All
Memory Type	Volatile

01h	PWM4-PWM6 Frequency	PWM1-PWM3 Frequency
	BIT 7	BIT 0

BITS 7:4

PWM4-PWM6 Frequency: These bits select the PWM OUT frequency for PWMOUT4, PWMOUT5, and PWMOUT6 according to the following:

BITS 7:4	PWM OUPUT FREQUENCY	POR CONDITION
0000b	25Hz	—
0001b	30Hz	FREQ_START = GND
0010b	35Hz	—
0011b	100Hz	—
0100b	125Hz	—
0101b	149.7Hz	—
0110b	1.25kHz	—
0111b	1.47kHz	FREQ_START = Unconnected
1000b	3.57kHz	—
1001b	5kHz	—
1010b	12.5kHz	—
1011b	25kHz	FREQ_START = V_{CC}

The POR state is set by the state of the FREQ_START pin at power-up as shown.

BITS 3:0

PWM1-PWM3 Frequency: These bits select the PWM OUT frequency for PWMOUT1, PWMOUT2, and PWMOUT3 according to the following:

BITS 7:4	PWM OUPUT FREQUENCY	POR CONDITION
0000b	25Hz	—
0001b	30Hz	FREQ_START = GND
0010b	35Hz	—
0011b	100Hz	—
0100b	125Hz	—
0101b	149.7Hz	—
0110b	1.25kHz	—
0111b	1.47kHz	FREQ_START = Unconnected
1000b	3.57kHz	—
1001b	5kHz	—
1010b	12.5kHz	—
1011b	25kHz	FREQ_START = V_{CC}

The POR state is set by the state of the FREQ_START pin at power-up as shown.

Fan 1 Configuration Register (02h)
Fan 2 Configuration Register (03h)
Fan 3 Configuration Register (04h)
Fan 4 Configuration Register (05h)
Fan 5 Configuration Register (06h)
Fan 6 Configuration Register (07h)

Power-On Value	0XX0 0000b
Read Access	All
Write Access	All
Memory Type	Volatile

02h, 03h, 04h, 05h, 06h, 07h	Mode	Spin-Up	$\overline{\text{Control}}$/ Monitor	TACH Input Enable	$\overline{\text{TACH}}$/ Locked Rotor	Locked Rotor Polarity	$\overline{\text{PWM}}$/ TACH
	BIT 7						BIT 0

BIT 7	**Mode:** RPM/PWM mode select. 0 = PWM mode. PWM duty cycle is set by the value in the associated PWMOUT Target Duty Cycle register. 1 = RPM mode. The PWM duty cycle is adjusted to produce the TACH count value in the associated TACH Target Count register. When changing from PWM to RPM mode, if the current RPM value is different from the value selected in the TACH Target Count register, the PWM duty cycle starts from the current value and increment/decrements toward the desired value at the selected duty cycle rate-of-change.
BITS 6:5	**Spin-Up:** When spin-up is selected and the fan is started with a target PWM duty cycle less than 100%, the device produces 100% duty cycle until two tachometer pulses have been detected. A maximum spin-up time is also selectable to ensure that the spin-up time is not excessive. After two tachometer pulses have been detected, or the spin-up has timed out, the duty cycle goes to the value in the PWMOUT Target Duty Cycle register. The POR state is set by the state of the SPIN_START pin at power-up.
BIT 4	**$\overline{\text{Control}}$/Monitor:** 0 = Control fan speed. 1 = Monitor only. Associated duty cycle = 0% regardless of other settings; monitor associated TACH or locked rotor if enabled by bit 3.

BITS 6:5	SPIN-UP BEHAVIOR	POR CONDITION
00b	No spin-up	SPIN_START = GND
01b	Spin-up until two tachometer pulses or 0.5s (max)	SPIN_START = Unconnected
10b	Spin-up until two tachometer pulses or 1s (max)	SPIN_START = VCC
11b	Spin-up until two tachometer pulses or 2s (max)	—