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MAX32650–MAX32652

Ultra-Low Power Arm Cortex-M4 with FPU-Based Microcontroller for Battery-Powered Applications

General Description

DARWIN is a new breed of low-power microcontrollers built to thrive in the rapidly evolving Internet of Things (IoT). They are smart, with the biggest memories in their class and a massively scalable memory architecture. They run forever, thanks to wearable-grade power technology. They are also tough enough to withstand the most advanced cyberattacks. DARWIN microcontrollers are designed to run any application imaginable—in places where you would not dream of sending other microcontrollers.

Generation UP microcontrollers are designed to handle the increasingly complex applications demanded by today's advanced battery-powered devices and wireless sensors. The MAX32650–MAX32652 are ultra-low power memory-scalable microcontrollers designed specifically for high-performance, battery-powered applications. They are based on Arm® Cortex®-M4 with FPU CPU with 3MB flash and 1MB SRAM. Memory scalability is supported with multiple memory-expansion interfaces, including a HyperBus™/Xccela™ DDR interface and two SPI execute in place (SPIX) interfaces. A secure digital interface supports external high-speed memory cards, including SD, SDIO, MMC, SDHC, and microSD™.

Power management features provide five low power modes for clock, peripheral, and voltage control. Individual SRAM banks of 32KB, 96KB, or 1024KB (full retention) can be retained with reduced power consumption. A SmartDMA performs complex background processing while the CPU is off to dramatically reduces overall power consumption.

The MAX32651 is a secure version with a trust protection unit (TPU) that provides a modular arithmetic accelerator (MAA) for fast ECDSA, an AES engine, TRNG, SHA-256 hash, and secure bootloader. A memory decryption integrity unit (MDIU) provides on-the-fly data decryption (plain or executable) stored in external flash.

The MAX32652 is a high-density, 0.35mm pitch, 140-bump WLP package targeted for tiny form factor products that require high I/O counts.

Applications

- Sports Watches, Fitness Monitors
- Wearable Medical Patches, Portable Medical Devices
- Industrial Sensors, IoT

Benefits and Features

- Ultra-Efficient Microcontroller for Battery-Powered Applications
  - 120MHz Arm Cortex-M4 with FPU
  - SmartDMA Provides Background Memory Transfers with Programmable Data Processing
  - 120MHz High-Speed and 40MHz Low-Power Oscillators
  - 7.3728MHz Low-Power Oscillators
  - 32.768kHz and RTC Clock (Requires External Crystal)
  - 8kHz Always-On Ultra-Low Power Oscillator
  - 3MB Internal Flash, 1MB Internal SRAM
  - 104µW/MHz Executing from Cache at 1.1V
  - Five Low Power Modes: Active, Sleep, Background, Deep-Sleep, and Backup
  - 1.8V and 3.3V I/O with No Level Translators
- Scalable Cached External Memory Interfaces:
  - 120MB/s HyperBus/Xccela DDR Interface
  - SPIXF/SPIXR for External Flash/RAM Expansion
  - 240Mbps SDHC/eMMC/SDIO/microSD Interface
- Optimal Peripheral Mix Provides Platform Scalability
  - 16-Channel DMA
  - Three SPI Master (60MHz)/Slave (48MHz)
  - One QuadSPI Master (60MHz)/Slave (48MHz)
  - Up to Three 4Mbaud UARTs with Flow Control
  - Two 1MHz I^2C Master/Slave
  - I^2S Slave
  - Four-Channel 7.8ksps 10-Bit Delta-Sigma ADC
  - USB 2.0 Hi-Speed Device Interface with PHY
  - 16 Pulse Train Generators
  - Six 32-Bit Timers with 8mA High Drive
  - 1-Wire Master
- Trust Protection Unit (TPU) for IP/Data Security
  - Modular Arithmetic Accelerator (MAA), True Random Number Generator (TRNG)
  - Secure Nonvolatile Key Storage, SHA-256, AES-128/192/256
  - Memory Decryption Integrity Unit, Secure Boot ROM

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HyperBus is a trademark of Spansion.

Xccela is a trademark of Micron Technology, Inc.

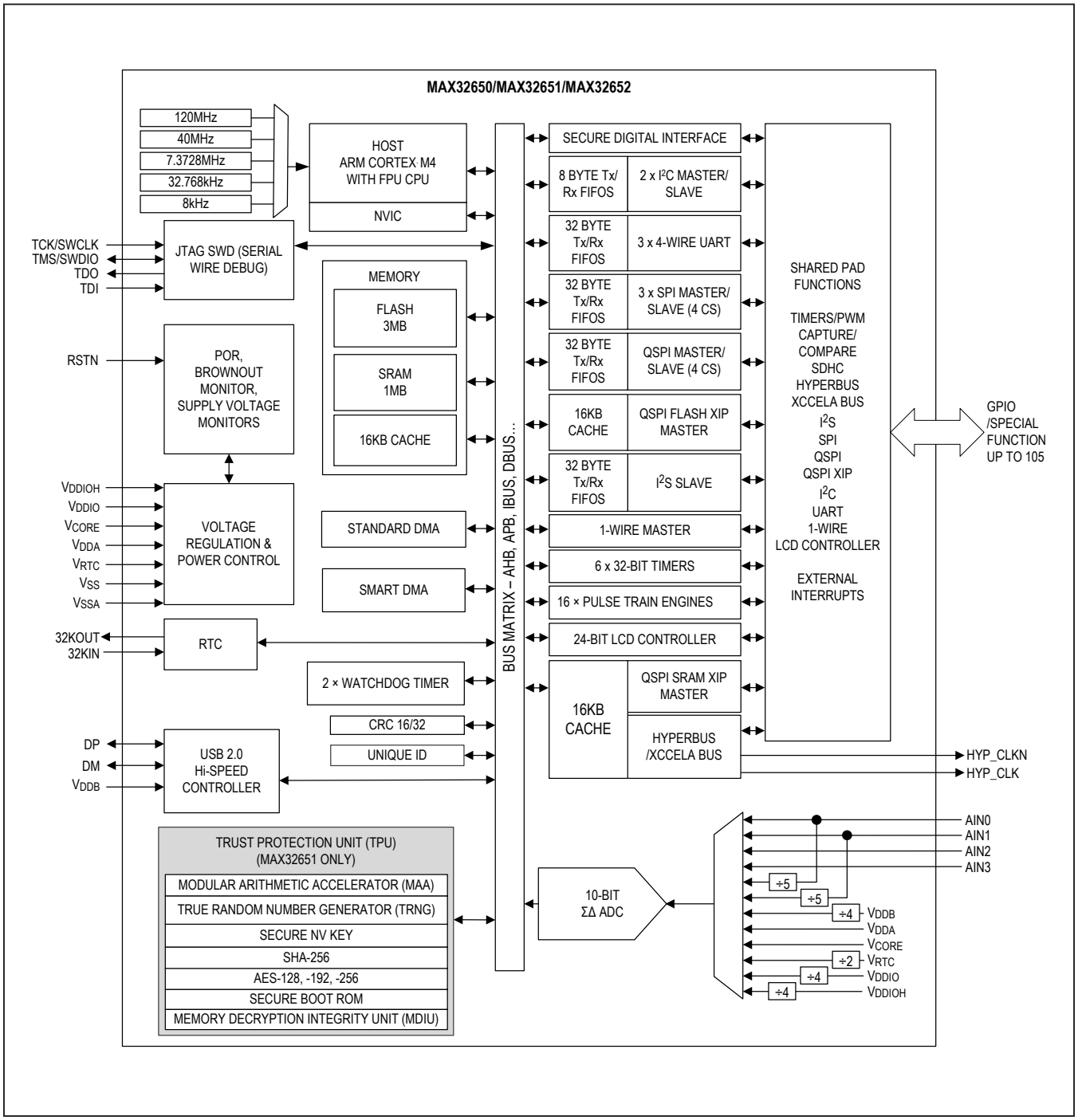
MicroSD is a trademark of SD-3C, LLC.

Ordering Information *appears at end of data sheet.*

19-100220; Rev 1; 3/18

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.)

V_{CORE} ..... -0.3V to 1.21V
V_{DDA} ..... -0.3V to 1.98V
V_{DDIO} ..... -0.3V to 1.98V
V_{DDIOH} ..... -0.3V to 3.6V
V_{RTC} ..... -0.3V to 1.98V
RSTN, GPIO (V_{DDIO}) ..... -0.3V to V_{DDIO} + 0.5V
GPIO (V_{DDIOH}) ..... -0.3V to V_{DDIOH} + 0.5V
32KIN, 32KOUT ..... -0.3V to V_{RTC} + 0.2V
AIN[1:0] ..... -0.3V to 5.5V
AIN[3:2] ..... -0.3V to V_{DDA} + 0.2V
V_{DDB} ..... -0.3V to 3.6V
DM, DP ..... -0.3V to 3.6V
HYP_CLK, HYP_CLKN, P1.[21:18], P1.[16:11], P3.0 ..... -0.3V to 1.98V
V_{DDIO} pins (sink) 100mA
V_{DDIOH} pins (sink) 100mA
V_{SSA} 100mA
V_{SS} 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
Continuous Package Power Dissipation TQFP (multilayer board) T_A = +70°C (derate 45.5mW/°C above +70°C) 2857.10mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

140 WLP

PACKAGE CODE	W1404A4+1
Outline Number	21-100219
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35.13°C/W
Junction to Case (θ_{JC})	N/A

96 WLP

PACKAGE CODE	W964A4+1
Outline Number	21-100240
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33.61°C/W
Junction to Case (θ_{JC})	N/A

144 TQFP

PACKAGE CODE	C144+1
Outline Number	21-0087
Land Pattern Number	90-0144
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage, Core	V_{CORE}	f_{SYS_CLK} = 120MHz	0.99	1.1	1.21	V
Supply Voltage, Analog	V_{DDA}		1.71	1.8	1.89	V
Supply Voltage, RTC	V_{RTC}		1.71	1.8	1.89	V
Supply Voltage, GPIO	V_{DDIO}		1.71	1.8	1.89	V
Supply Voltage, GPIO (High)	V_{DDIOH}		1.71	1.8	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{CORE}		0.835		V
		Monitors V_{DDA}		1.67		
		Monitors V_{RTC}		1.67		
		Monitors V_{DDIO}		1.67		
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDB}		2.95		V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDIOH}		1.67		V
Power-On Reset Voltage	V_{POR}	Monitors V_{CORE}		0.594		V
		Monitors V_{DDA}		1.52		
		Monitors V_{RTC}		1.17		
RAM Data Retention Voltage	V_{DRV}			0.81		V
V_{CORE} Dynamic Current, Active Mode	I_{CORE_DACT}	Total current into V_{CORE} pins, f_{SYS_CLK} = 120MHz, V_{CORE} = 1.1V, CPU in Active mode, executing from cache, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		95		µA/MHz
V_{CORE} Fixed Current, Active Mode	I_{CORE_FACT}	120MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		1020		µA
		7.3728MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		356		
V_{DDA} Fixed Current, Active Mode	I_{DDA_FACT}	120MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA , V_{CORE} and V_{DDA} voltage monitors enabled		348		µA
		7.3728MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA , V_{CORE} and V_{DDA} voltage monitors enabled		39		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CORE} Dynamic Current, Sleep Mode	I_{CORE_DSLP}	Total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active		114		µA/MHz
V_{CORE} Fixed Current, Sleep Mode	I_{CORE_FSLP}	f_{SYS_CLK} = 120MHz, total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active		1020		µA
		f_{SYS_CLK} = 7.3728MHz, total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active		356		
V_{DDA} Fixed Current, Sleep Mode	I_{DDA_FSLP}	f_{SYS_CLK} = 120MHz, total current into V_{DDA} pins, CPU in Sleep mode, Standard DMA with two channels active		348		µA
		f_{SYS_CLK} = 7.3728MHz, total current into V_{DDA} pins, CPU in Sleep mode, standard DMA with two channels active		49		
V_{CORE} Dynamic Current, Background Mode	I_{CORE_DBKG}	f_{SYS_CLK} = 7.3728MHz, total current into V_{CORE} pins, CPU in Deep-sleep mode, SmartDMA active		66		µA/MHz
V_{CORE} Fixed Current, Background Mode	I_{CORE_FBGD}	7.3728MHz oscillator enabled, total current into V_{CORE} pins, CPU in Deep-sleep mode, SmartDMA active		162		µA
V_{CORE} Fixed Current, Deep-Sleep Mode	I_{CORE_FDSL}	Standby state with full data retention		70		µA
V_{DDA} Fixed Current, Deep-Sleep Mode	I_{DDA_FDSL}	Standby state with full data retention, V_{CORE} and V_{DDA} voltage monitors enabled		132		nA
V_{RTC} Fixed Current, Deep-Sleep Mode	I_{DDRTC_FDSL}	Standby state with full data retention, V_{RTC} = 1.8V, RTC enabled		540		nA
V_{CORE} Fixed Current, Backup Mode	I_{CORE_FBKU}	No SRAM retention (0KB)		30		nA
V_{DDA} Fixed Current, Backup Mode	I_{DDA_FBKU}	V_{DDA} voltage monitor enabled		132		nA
V_{RTC} Fixed Current, Backup Mode	I_{DDRTC_FBKU}	RTC enabled, retention regulator off		540		nA
		RTC enabled, 32KB SRAM retained, retention regulator on		720		
		RTC disabled, retention regulator off		156		
Sleep Mode Resume Time	t_{SLP_ON}			575		ns
Deep-Sleep Mode Resume Time	t_{DSL_ON}	Wake to 40MHz		9		µs
		Wake to 120MHz		18		
Backup Mode Resume Time	t_{BKU_ON}			5		ms

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB						
USB Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
D+, D- Pin Capacitance	C_{IN_USB}	Pin to V_{SS}		8		pF
Driver Output Resistance	R_{DRV}	Steady state drive		45 ±10%		Ω
USB/FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.0			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.6	V
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5 kΩ from DP and DM to V_{SS}, I_{OH} = -4mA	V_{DDB} - 0.4		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5 kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.4	V
Differential Input Sensitivity	V_{DI}	|DP to DM|	0.2			V
Common Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Transition Time (Rise/Fall) D+, D- (Note 11)	t_{RF}	C_L = 50pF	4		20	ns
Pullup Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ
USB/HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High Level Output Voltage	V_{HSOH}			400 ± 40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ±200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ±200		mV

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.256		120,000	kHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		ns
High-Speed Oscillator Frequency	f_{HSCLK}	Measured at +25°C, 120MHz		120 ±1		MHz
Low-Power Oscillator Frequency	f_{LPCLK}			40		MHz
7MHz Oscillator Frequency	f_{7MCLK}			7.3728		MHz
Nano-Ring Oscillator Frequency	f_{NANO}			8		KHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, C_L = 6pF, ESR < 70kΩ		32.768		kHz
RTC Operating Current	I_{RTC_ACTSLP}	Sleep or Active mode		0.39		µA
RTC Power Up Time	t_{RTC_ON}			250		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}				0.3 × V_{DDIO}	V
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.75 × V_{DDIO}			V
Input High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.75 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}		0.75 x V_{DDIO}			V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All GPIO	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-1000		+1000	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-1000		+1000	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor TMS, TCK, TDI	R_{PU_T}			25		kΩ
Input Pullup Resistor RSTN	R_{PU_R}			1		MΩ

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup/Pulldown Resistor for All GPIO	R_{PU1}	Normal resistance		25		kΩ
	R_{PU2}	Highest resistance		1		MΩ
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time Per Word	t_{PROG}			60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years
ADC (DELTA-SIGMA)						
Resolution				10		Bits
ADC Clock Rate	f_{ACLK}		0.1		8	MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_CHSEL = 0-3, ADC_REFSEL = 1	V_{SSA} + 0.05		$V_{BG}/2$	V
		AIN[3:0], ADC_CHSEL = 0-3, ADC_REFSEL = 0	V_{SSA} + 0.05		V_{BG}	
		AIN[1:0], ADC_CHSEL = 4-5, ADC_REFSEL = 0	V_{SSA} + 0.05		5.5	
Input Impedance	R_{AIN}	AIN[1:0], ADC_CHSEL = 4-5, ADC active		40		kΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		1		pF
		Dynamically switched capacitance		250		fF
Integral Nonlinearity	INL		-2		+2	LSb
Differential Nonlinearity	DNL		-1		+2	LSb
Offset Error	V_{OS}			±1		LSb
Gain Error	GE			±2		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		210		µA
ADC Setup Time	t_{ADC_SU}	Any powerup of: ADC clock or ADC bias to CpuAdcStart			10	µs
ADC Output Latency	t_{ADC}			1025		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.01		nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.01		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/ gain error.		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	From +25ºC to +105ºC		15		ppm

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	$f_{MCK(MAX)} = f_{SYS\_CLK}/2$			60	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs

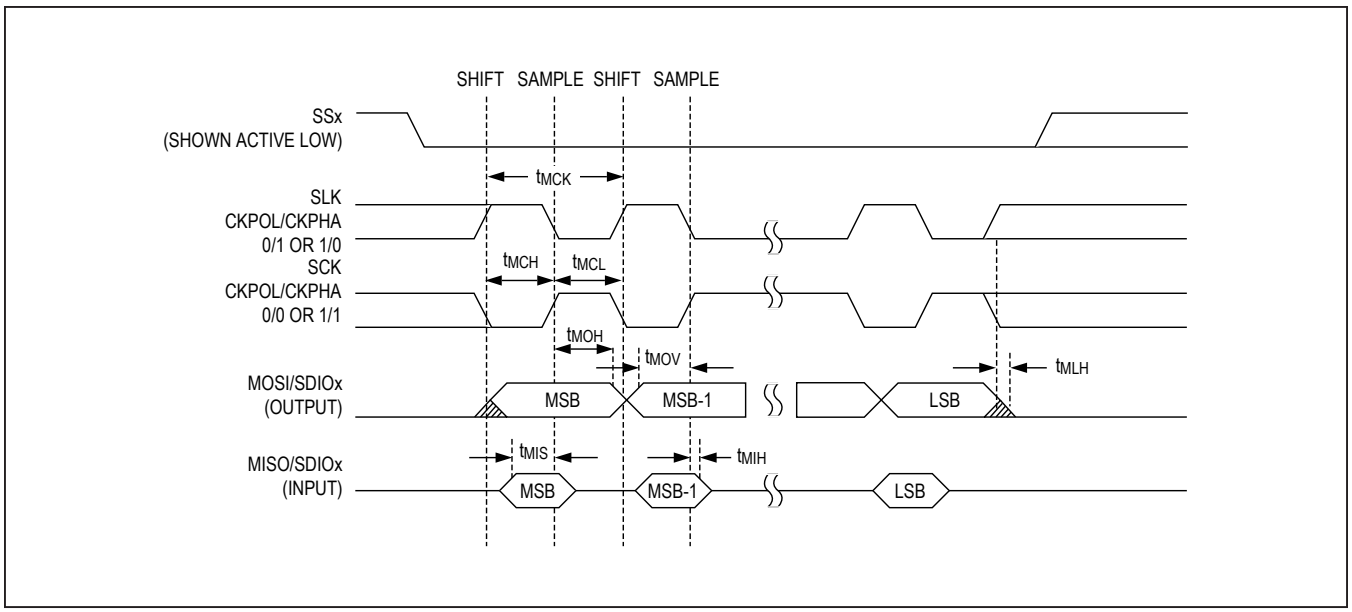


Figure 1. SPI Master Mode Timing Diagram

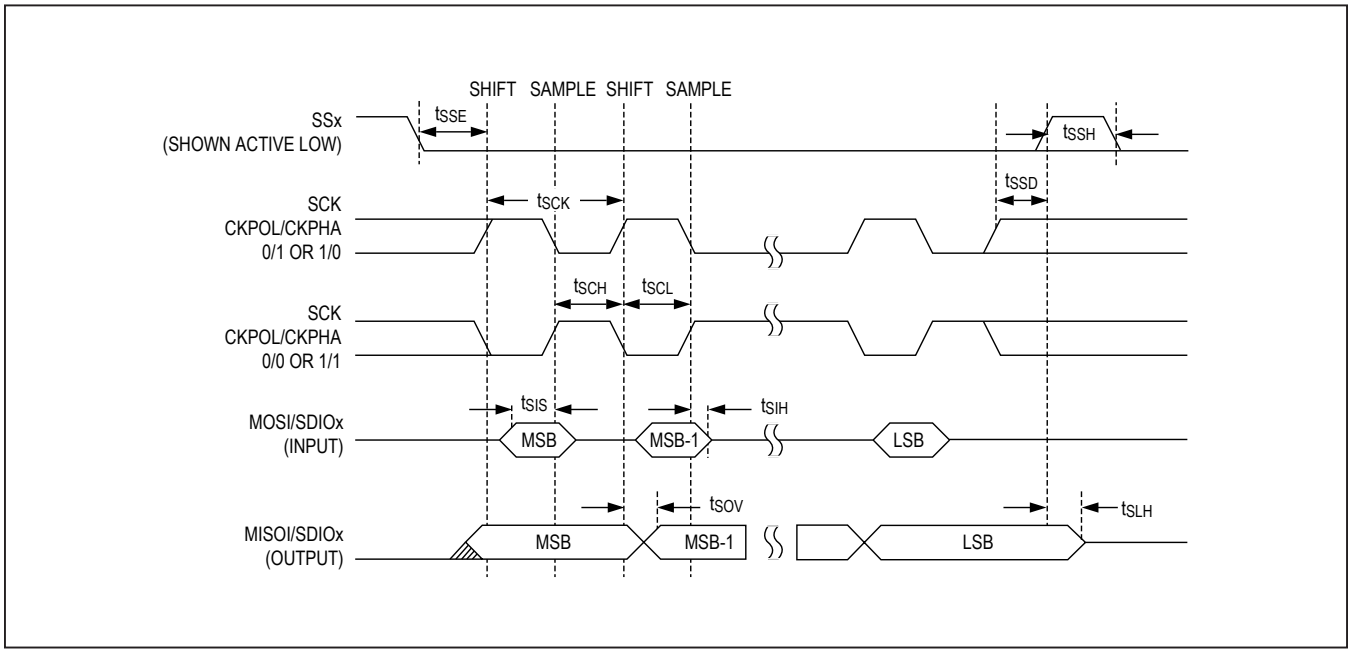


Figure 2. SPI Slave Mode Timing Diagram

Electrical Characteristics—I²C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

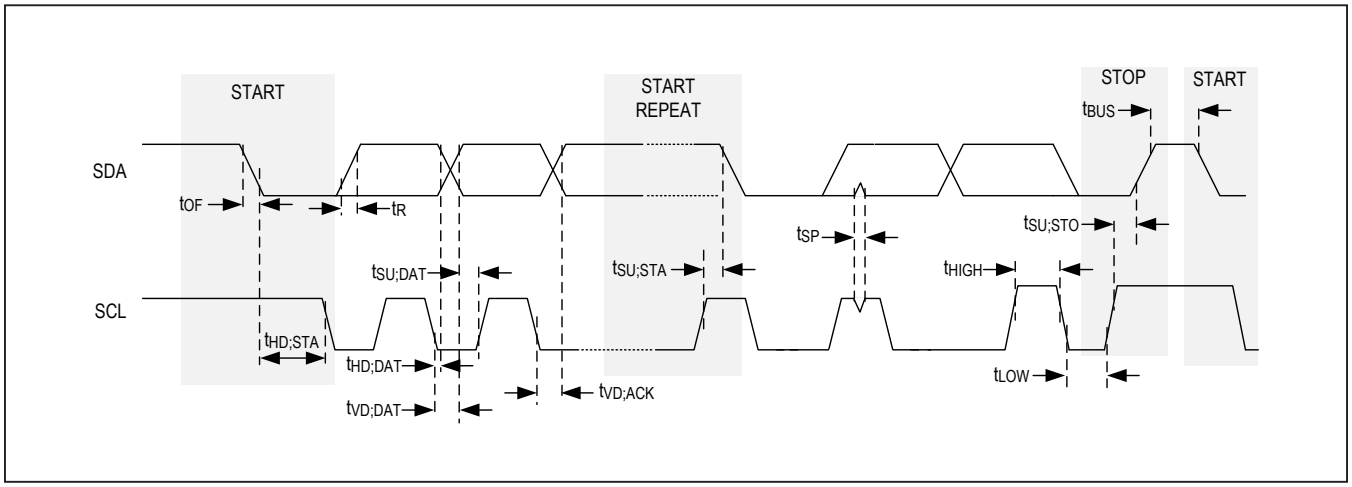


Figure 3. I²C Timing Diagram

Electrical Characteristics—I²C Slave

(Timing specifications are guaranteed by design and not production tested, T_A = -40°C to +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

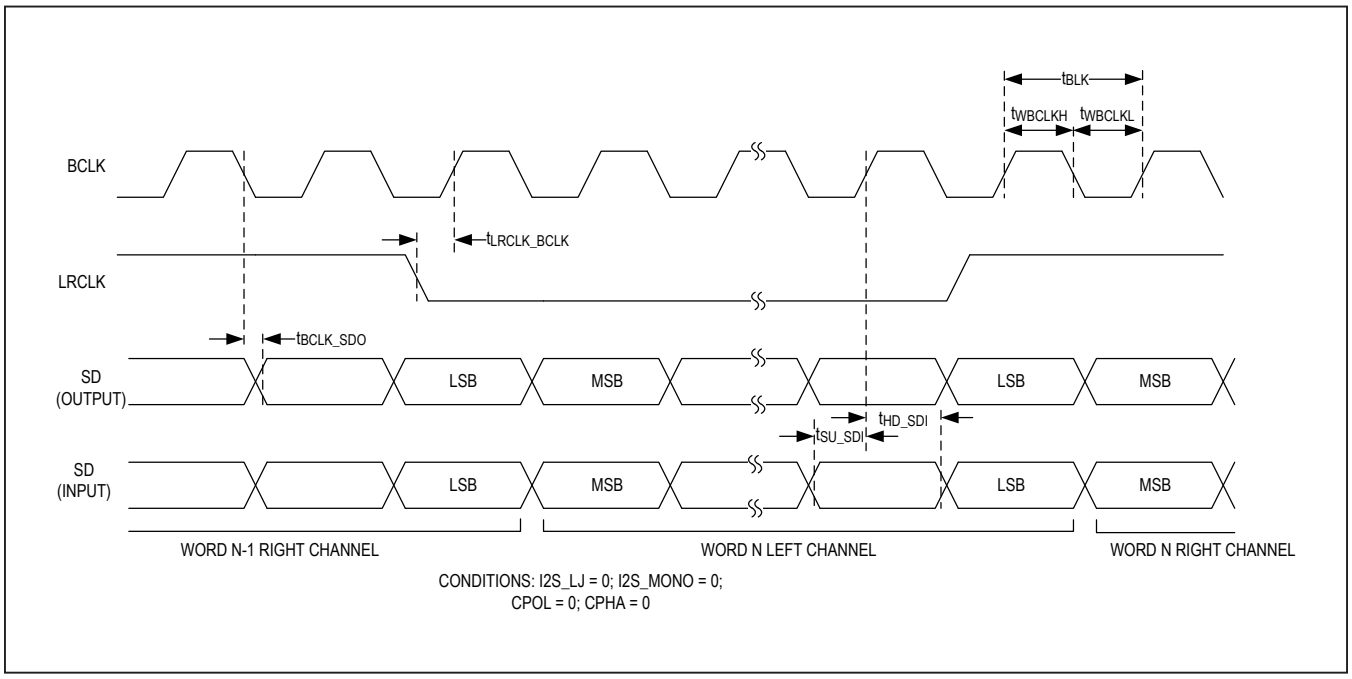


Figure 4. I²S Timing Diagram

Electrical Characteristics—SD/SDIO/SDHC/MMC

(T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	f_{SDHC_CLK}		0		$f_{HSCLK}/2$	MHz
Clock Period	t_{CLK}			$1/f_{SDHC\_CLK}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHLD}			1		ns
Output Valid Time	t_{OVLD}			5		ns
Output Hold Time	t_{OHLD}			6		ns

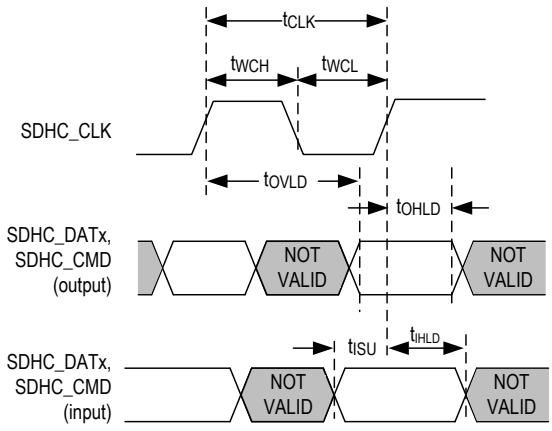


Figure 5. SD/SDIO/SDHC/MMC Timing Diagram

Electrical Characteristics—HyperBus

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HYP_CLK, HYP_CLKN Frequency	f_{HYP_CLK}				60	MHz
HYP_CLK, HYP_CLKN Period	t_{HYP_CLK}		$1/f_{HYP\_CLK}$			ns
HYP_CLK, HYP_CLKN High Time	t_{WHCKH}			7		ns
HYP_CLK, HYP_CLKN Low Time	t_{WHCKL}			7		ns
CS Setup to RWDS	t_{CSSU}			6		ns
RWDS Setup to CK	t_{RWDS_CK}			10		ns
Dx Output Setup	t_{OSU}			5		ns
Dx Output Hold	t_{OH}			3		ns
CS Hold After CK Falling Edge	t_{CSH}			5		ns
CS High Between Transactions	t_{CHSI}			15		ns
Dx Input Setup to RWDS	t_{ISU}			4		ns
Dx Input Hold	t_{IHD}			2		ns

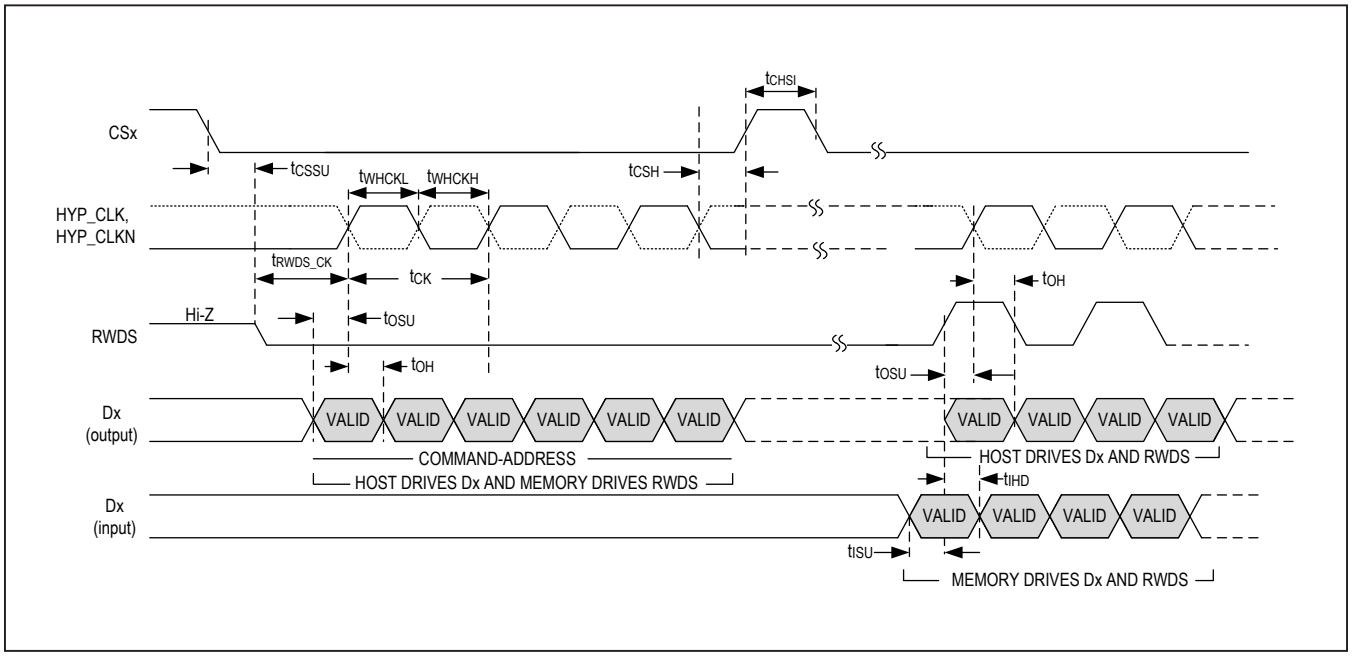


Figure 6. HyperBus/Xccela Bus Timing Diagram

Electrical Characteristics—One Wire Master

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

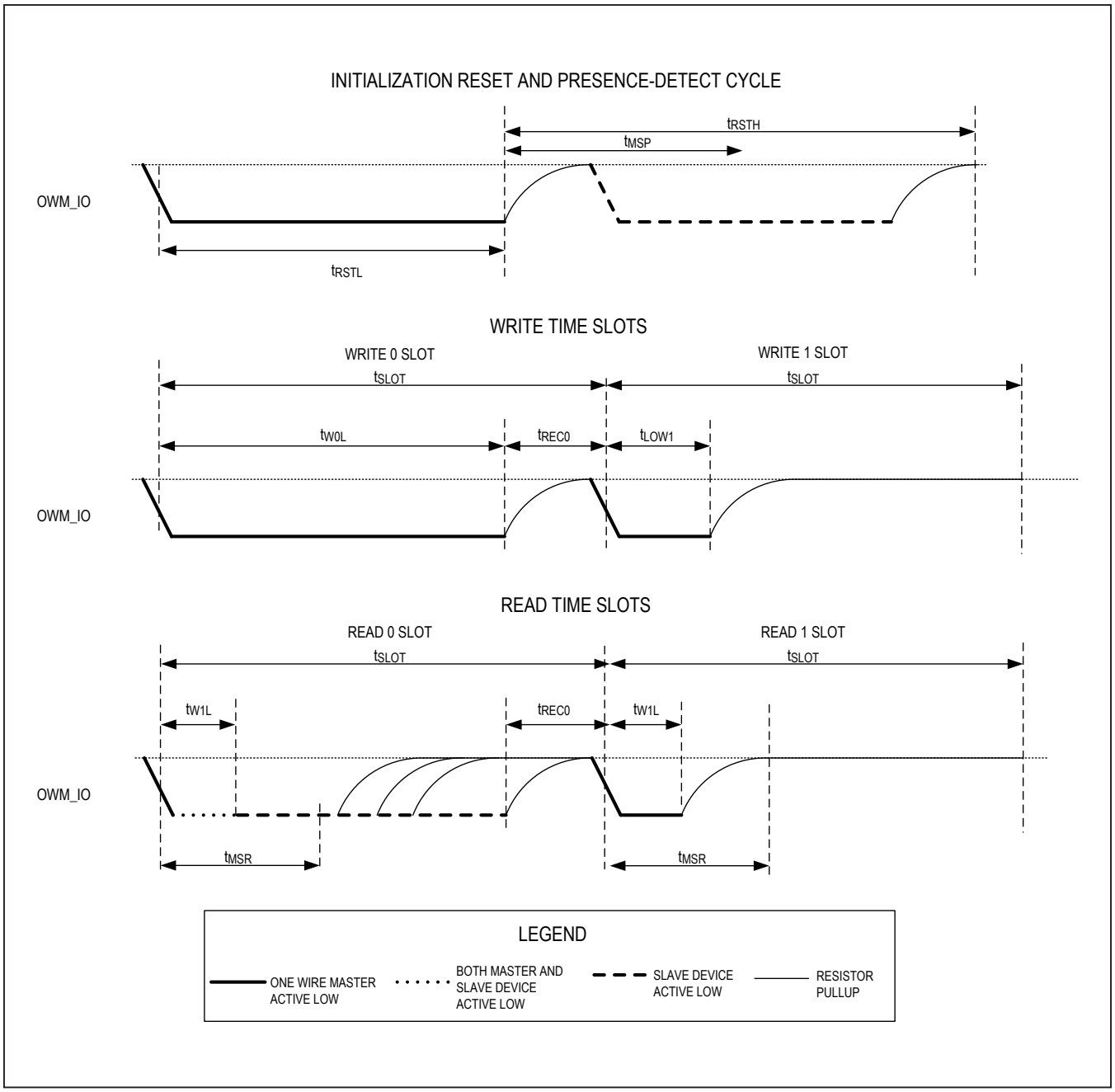
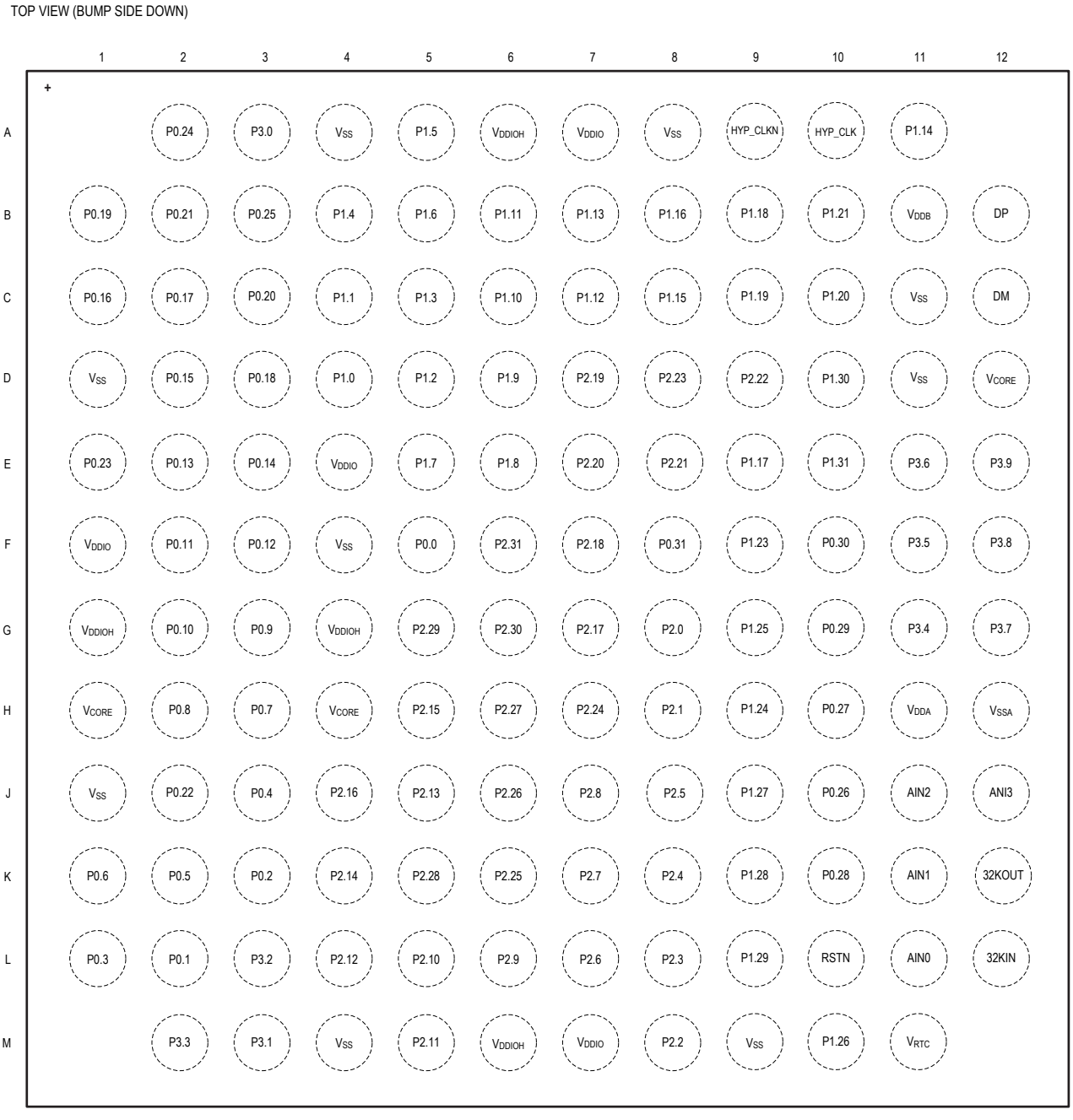


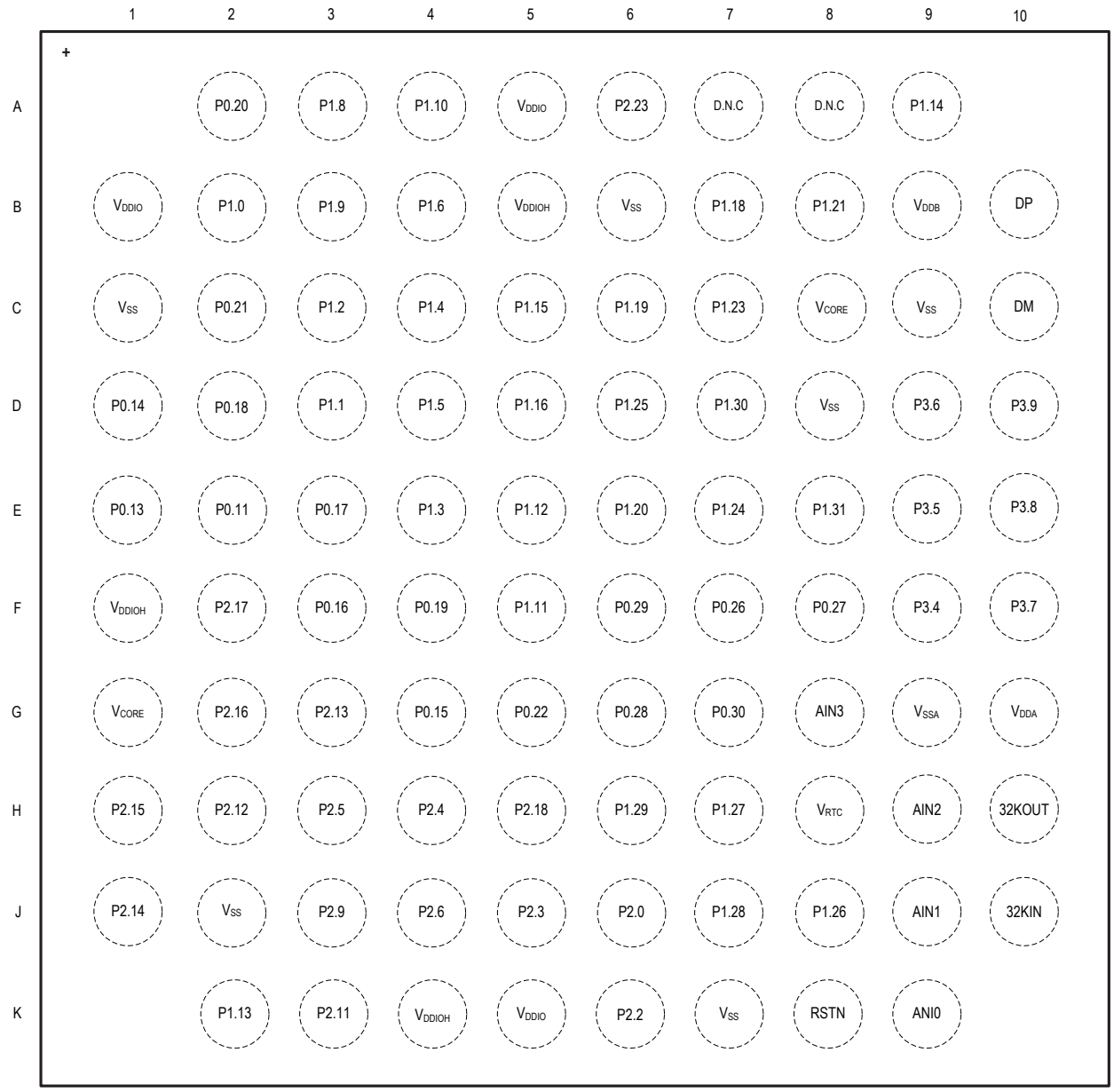
Figure 7. One-Wire Master Data Timing Diagram

Pin Configurations



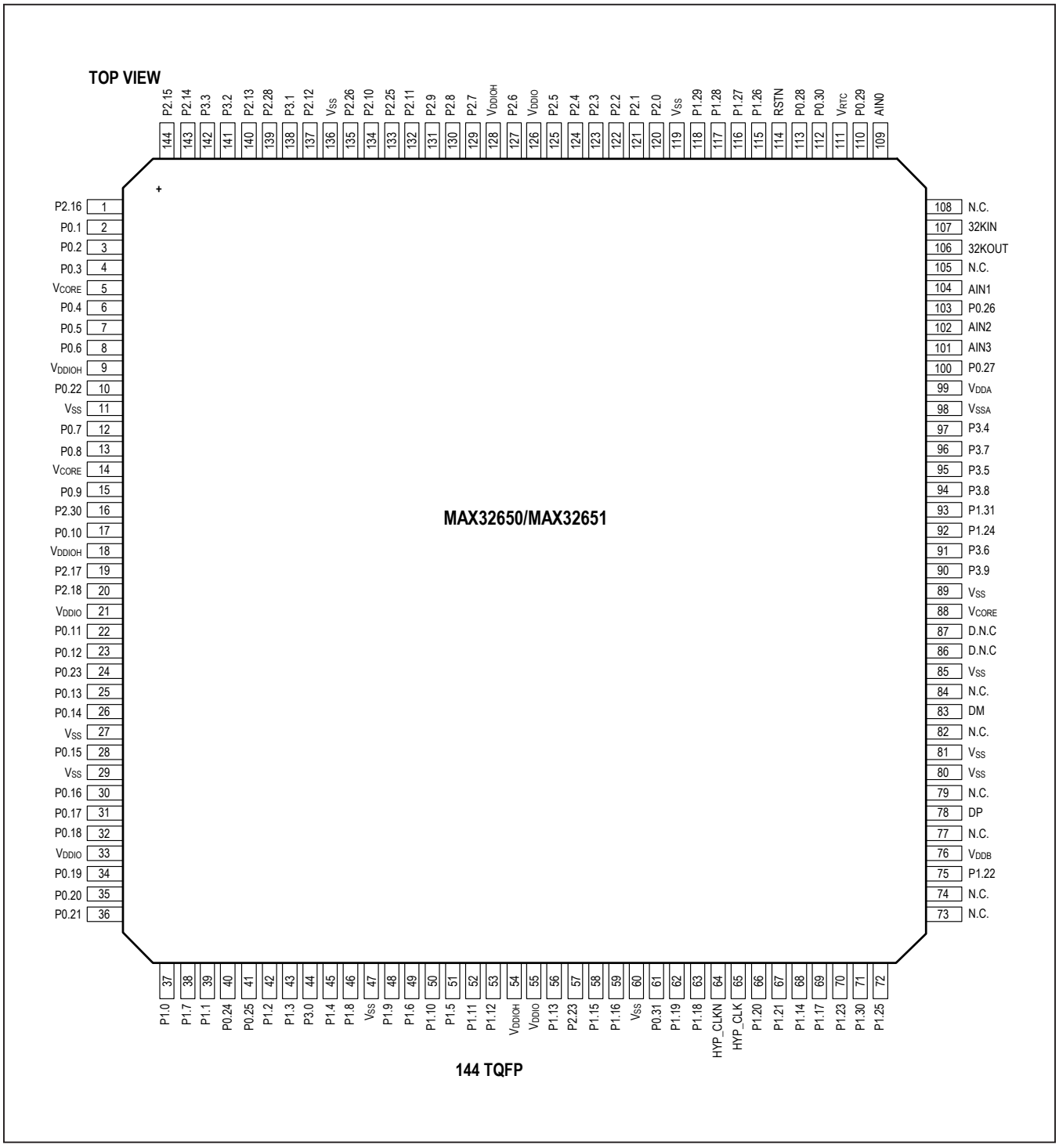
Pin Configurations (continued)

TOP VIEW (BUMP SIDE DOWN)



96 WLP

Pin Configurations (continued)



Pin Description

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
POWER				
H1, H4, D12	G1, C8	5, 14, 88	V_{CORE}	Core Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
H11	G10	99	V_{DDA}	1.8V Analog Supply Voltage. This pin must be bypassed to V_{SSA} with 1.0µF and 0.01µF capacitors as close as possible to the package.
B11	B9	76	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A7	A5	21	V_{DDIO}	GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
E4, F1	B1, K5	33, 55		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF and a 0.01µF capacitor as close as possible to the package.
M7	—	126		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
A6	B5	9	V_{DDIOH}	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitorx as close as possible to the package.
G1, G4, M6	F1, K4	18, 54, 128		GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
M11	H8	111	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A4, A8, C11, D1, D11, F4, J1, M4, M9	B6, C1, C9, D8, K7, J2	11, 27, 29, 47, 60, 80, 81, 85, 89, 119, 136	V_{SS}	Digital Ground
H12	G9	98	V_{SSA}	Analog Ground
RESET				
L10	K8	114	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
CLOCK				
L12	J10	107	32KIN	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected.
K12	H10	106	32KOUT	32kHz Crystal Oscillator Output
GPIO AND ALTERNATE FUNCTIONS				
F5	—	—	P0.0	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
L2	—	2	P0.1	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
K3	—	3	P0.2	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
L1	—	4	P0.3	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J3	—	6	P0.4	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K2	—	7	P0.5	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K1	—	8	P0.6	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H3	—	12	P0.7	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H2	—	13	P0.8	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G3	—	15	P0.9	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G2	—	17	P0.10	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F2	E2	22	P0.11	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F3	—	23	P0.12	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E2	E1	25	P0.13	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E3	D1	26	P0.14	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D2	G4	28	P0.15	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C1	F3	30	P0.16	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
C2	E3	31	P0.17	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D3	D2	32	P0.18	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B1	F4	34	P0.19	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C3	A2	35	P0.20	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B2	C2	36	P0.21	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J2	G5	10	P0.22	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E1	—	24	P0.23	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A2	—	40	P0.24	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B3	—	41	P0.25	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J10	F7	103	P0.26	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H10	F8	100	P0.27	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K10	G6	113	P0.28	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G10	F6	110	P0.29	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F10	G7	112	P0.30	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F8	—	61	P0.31	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
D4	B2	37	P1.0	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C4	D3	39	P1.1	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D5	C3	42	P1.2	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C5	E4	43	P1.3	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B4	C4	45	P1.4	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A5	D4	51	P1.5	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B5	B4	49	P1.6	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E5	—	38	P1.7	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E6	A3	46	P1.8	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D6	B3	48	P1.9	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C6	A4	50	P1.10	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B6	F5	52	P1.11	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C7	E5	53	P1.12	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B7	K2	56	P1.13	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A11	A9	68	P1.14	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.