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19-2845; Rev 1; 10/03

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

General Description

The MAX3353E I2C-compatible USB On-the-Go (OTG) regulated charge pump with switchable pullup/pulldown resistors allows peripherals and mobile devices such as PDAs, cellular phones, and digital cameras to be interconnected without a host PC.

The MAX3353E enables a system with an integrated USB dual-role transceiver to function as a USB OTG dual-role device. The charge pump in the MAX3353E supplies V_{BUS} power and signaling that is required by the transceiver as defined in *On-the-Go Supplement: USB 2.0, Revision 1.0*. The MAX3353E provides the switchable pullup and pulldown resistors on D+ and D- required for a dual-role device.

The MAX3353E integrates a regulated charge pump, switchable pullup/pulldown resistors, and an I2C-compatible 2-wire serial interface. The device provides a detector to monitor ID status and operates with logic supply voltages (V_L) between +1.65V and V_{CC} and charge-pump supply voltages (V_{CC}) from +2.6V to +5.5V. The charge pump supplies an OTG-compatible output on V_{BUS} while sourcing 8mA output current.

The MAX3353E enables USB OTG communication between digital logic parts that cannot supply or tolerate the +5V V_{BUS} levels that USB OTG requires. By controlling and measuring V_{BUS} using internal comparators, this device supports USB OTG session request protocol (SRP) and host negotiation protocol (HNP).

The MAX3353E has built-in ±15kV ESD protection circuitry to guard V_{BUS}, ID_IN, D+, and D-. The MAX3353E is available in a 5 x 4 chip-scale package (UCSP™) and 16-pin TSSOP package.

Applications

Mobile Phones
PDAs
Digital Cameras
MP3 Players
Photo Printers

Pin Configurations appear at end of data sheet.

Typical Applications Circuit appears at end of data sheet.

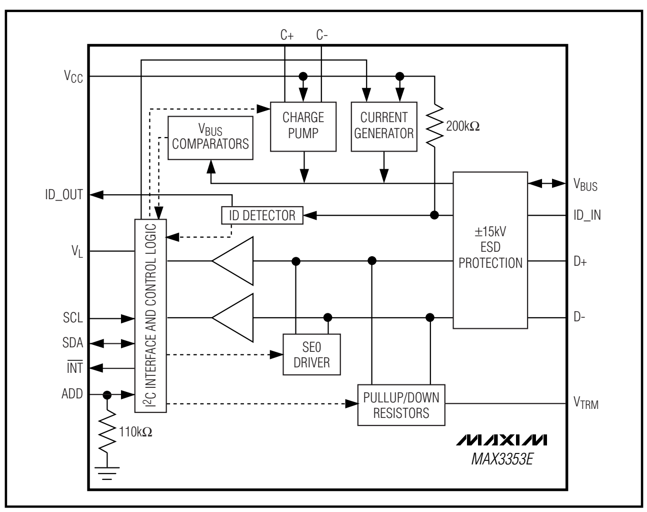
Features

- ♦ **Ideal for Enabling USB Dual-Role Components for USB OTG Protocol**
- ♦ **Charge Pump for V_{BUS} Signaling and Operation Down to +2.6V**
- ♦ **Level Translators Allow Low-Voltage System Interface**
- ♦ **Internal V_{BUS} Comparators and ID Detector**
- ♦ **Internal Switchable Pullup and Pulldown Resistors for Host/Peripheral Functionality**
- ♦ **I2C-Compatible Bus Interface with Command and Status Registers**
- ♦ **Interrupt Features**
- ♦ **±15kV ESD Protection on ID_IN, V_{BUS}, D+, and D-**
- ♦ **Supports SRP and HNP**
- ♦ **Available in 5 x 4 UCSP and 16-Pin TSSOP**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3353EEUE	-40°C to +85°C	16 TSSOP	—
MAX3353EEBP-T	-40°C to +85°C	5 x 4 UCSP	B20-4

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, V_L, V_{TRM} ....-0.3V to +6V
D+, D-, ID_IN (Note 1)..-0.3V to +6V
V_{BUS} (Notes 1, 2) ....-0.3V to +6V
C+..(V_{CC} - 0.3V) to +6V
C-...-0.3V to (V_{CC} + 0.3V)
$\overline{\text{INT}}$, ID_OUT..-0.3V to (V_L + 0.3V)
SDA, SCL, ADD ....-0.3V to +6V
V_{BUS} Output Short Circuit to Ground .... Continuous
Output Current (all other pins) ....±15mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
5 x 4 UCSP (derate 7.8mW/°C above +70°C) 625mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature...+150°C
Lead Temperature (soldering 10s) ....+300°C
Bump Temperature (soldering)
Infrared (15s) ....+200°C
Vapor Phase (20s) ....+215°C

Note 1: 15kV ESD protected.
Note 2: V_{BUS} can be backdriven to +6V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground; V_{TRM} and V_L decoupled with 0.1µF capacitor to ground; C_{VBUS} = 1µF (min), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V, and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.6		5.5	V
Logic Supply Voltage	V_L		1.65		V_{CC}	V
V_{TRM} Supply Voltage	V_{TRM}		3.0		3.6	V
V_{CC} Operating Supply Current	I_{CC}	ID_IN floating, V_{BUS_CHG1} = 0, V_{BUS_CHG2} = 0, V_{BUS_DRV} = 0, BDISC_ACONN = 0		73	100	µA
		V_{BUS_DRV} = 1, V_{BUS_CHG1}= 0, V_{BUS_CHG2} = 0, I_{VBUS} = 8mA		18	25	mA
V_{CC} Shutdown Supply Current	$I_{CC(SHDN)}$	No activity on I²C serial bus		0.4	2	µA
V_{TRM} Supply Current	I_{VTRM}	DP_PULLDWN = 1, DP_PULLUP = 0, DM_PULLDWN = 1, DM_PULLUP = 0 no activity on USB serial bus			1	µA
V_L Input Current	I_{VL}	No activity on I²C serial bus			1	µA
ID_OUT, $\overline{\text{INT}}$ Output Voltage High	V_{OH}	$\overline{\text{INT}}$ configured to push/pull; source current I_{LOAD} = +1mA	V_L - 0.4			V
SDA, $\overline{\text{INT}}$, ID_OUT Output Voltage Low	V_{OL}	Sink current I_{LOAD} = -1mA			0.4	V
SDA, SCL, ADD Input Voltage High	V_{IH}		0.67 x V_L			V
SDA, SCL, ADD Input Voltage Low	V_{IL}				0.4	V
Input/Three-State Output Leakage Current (SDA, SCL, $\overline{\text{INT}}$)		$\overline{\text{INT}}$ configured to open drain			±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground; V_{TRM} and V_L decoupled with 0.1µF capacitor to ground; C_{VBUS} = 1µF (min), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V, and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ADD Pulldown Resistor				110		kΩ
ESD PROTECTION (V_{BUS}, ID_IN, D+, D-)						
ESD Protection		Human Body Model		±15		kV
		IEC1000-4-2 Air-Gap Discharge		±11		
		IEC1000-4-2 Contact Discharge		±6		
V_{BUS}/CHARGE-PUMP SPECIFICATIONS (V_{BUS_DRV} = 1, V_{BUS_DISCHG} = 0, V_{BUS_CHG1} = 0, V_{BUS_CHG2} = 0, unless otherwise noted.)						
V_{BUS} Output Voltage	V_{BUS}	I_{VBUS} = 0 to 8mA, C_{VBUS} = 1µF	4.63		5.25	V
V_{BUS} Output Current	I_{VBUS}		8			mA
V_{BUS} Short-Circuit Current		V_{BUS} shorted to GND		140	250	mA
Output Ripple		I_{VBUS} = 8mA, C_{VBUS} = 1µF		100		mV
Efficiency		V_{CC} = 2.6V, I_{VBUS} = 8mA		80		%
Switching Frequency	f			600		kHz
V_{BUS} Voltage in Three-State Mode		V_{BUS_DRV} = 0			0.2	V
V_{BUS} Pulldown Resistance		V_{BUS_DRV} = 0, V_{BUS_DISCHG} = 1	3.2	5.1	6.5	kΩ
V_{BUS} Input Impedance		V_{BUS_DRV} = 0	40		100	kΩ
V_{BUS} AND CURRENT SOURCE SPECIFICATIONS (V_{BUS_CHG1} = 1, V_{BUS_CHG2} = 0, V_{BUS_DRV} = 0, V_{BUS_DISCHG} = 0)						
V_{BUS} Output Voltage	V_{BUS}	C_{LOAD} = 15µF	2.1			V
		C_{LOAD} = 95µF			1.9	
V_{BUS} Current Source		(Note 5)	450	600	850	µA
V_{BUS} Current Gate Time		V_{BUS_CHG1} = 1, V_{BUS_CHG2} = 0 (Note 5)	56	105	155	ms
COMPARATOR SPECIFICATIONS						
V_{BUS_VALID} Comparator Threshold			4.40	4.55	4.63	V
V_{BUS_VALID} Comparator Hysteresis				20		mV
SESSION_VALID Comparator Threshold			1.0	1.4	1.8	V
SESSION_VALID Comparator Hysteresis				20		mV
B_SESSION_END Comparator Threshold			0.4	0.5	0.6	V
B_SESSION_END Comparator Hysteresis				35		mV
SINGLE-ENDED RECEIVERS AND SE0 SPECIFICATIONS (D+, D-)						
Low-Level Input Threshold					0.8	V
High-Level Input Threshold			2.0			V

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground; V_{TRM} and V_L decoupled with 0.1µF capacitor to ground; C_{VBUS} = 1µF (min), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V, and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Hysteresis Voltage	V_{HYST}			0.2		V
Output Voltage Low (D+ and D- in SE0 state)		I_{SINK} = -2.4mA			0.3	V
PULLUP/PULLDOWN RESISTOR SPECIFICATIONS (D+, D-, ID_IN)						
Pulldown Resistor on D+		DP_PULLDWN = 1, DP_PULLUP = 0, BDISC_ACONN = 0	14.25		15.75	kΩ
Pulldown Resistor on D-		DM_PULLDWN = 1, DM_PULLUP = 0, BDISC_ACONN = 0	14.25		15.75	kΩ
Pullup Resistor on D+		DP_PULLDWN = 0, DP_PULLUP = 1, BDISC_ACONN = 0	1.425		1.575	kΩ
Pullup Resistor on D-		DM_PULLDWN = 0, DM_PULLUP = 1, DP_PULLUP = 0, BDISC_ACONN = 0	1.425		1.575	kΩ
D- Leakage Current		DM_PULLDWN = 0, DM_PULLUP = 0, BDISC_ACONN = 0			±1	µA
D+ Leakage Current		DP_PULLDWN = 0, DP_PULLUP = 0, BDISC_ACONN = 0			±1	µA
Input Impedance on D+/D-		DP_PULLUP = 0, DP_PULLDWN = 0, DM_PULLUP = 0, DM_PULLDWN = 0, BDISC_ACONN = 0	300			kΩ
ID_IN Pullup Resistor			140	200	270	kΩ
ID_IN Input Voltage Low					0.33 x V_{CC}	V
ID_IN Input Voltage High			0.67 x V_{CC}			V

TIMING CHARACTERISTICS

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground. V_{TRM} and V_L decoupled with 0.1µF capacitor to ground. C_{VBUS} = 1µF (min), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Time to Assert D+ Pullup		BDISC_ACONN = 1, ID_IN = GND (A Device)			1	ms
Time to Assert SE0		BDISC_ACONN = 1, ID_IN = floating (B Device)	0.025	0.061	1	ms
Interrupt Propagation Delay		(Note 6)			1	µs
V_{BUS} Rise Time		From 0 to 4.4V; C_{LOAD} = 1µF; I_{VBUS} = 8mA; V_{BUS_DRV} = 1			100	ms
$\overline{INT}$ Out Rise Time		$\overline{INT}$ out push/pull configured, C_{LOAD} = 50pF		20		ns

TIMING CHARACTERISTICS (continued)

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground. V_{TRM} and V_L decoupled with 0.1µF capacitor to ground. C_{VBUS} = 1µF (min), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
$\overline{INT}$ Out Fall Time		C_{LOAD} = 50pF		20		ns
ID_OUT Rise Time		C_{LOAD} = 50pF		30		ns
ID_OUT Fall Time		C_{LOAD} = 50pF		10		ns
Time to Exit Shutdown				500		µs
Time to Enter Shutdown				1000		µs

I²C/SMBUS-COMPATIBLE TIMING SPECIFICATIONS

(V_{CC} = +2.6V to +5.5V, V_L = +1.65V to V_{CC}, V_{TRM} = +3V to +3.6V, C_{FLYING} = 0.1µF, V_{CC} decoupled with 1µF capacitor to ground. V_{TRM} and V_L decoupled with 0.1µF capacitor to ground. C_{VBUS} = 1µF (min). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +4V, V_L = +1.8V, V_{TRM} = +3.3V, and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Start Condition Hold Time	$t_{HD:STA}$		0.6			µs
Stop Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	(Note 7)	0		0.9	µs
Maximum Receive SCL/SDA Rise Time	t_R	(Note 8)		300		ns
Minimum Receive SCL/SDA Rise Time	t_R	(Note 8)		20 + 0.1C_B		ns
Maximum Receive SCL/SDA Fall Time	t_F	(Note 8)		300		ns
Minimum Receive SCL/SDA Fall Time	t_F	(Note 8)		20 + 0.1C_B		ns
Transmit SDA Fall Time (Note 4)	t_F	C_B = 400pF, I_{SDA} = 3mA, $V_L \geq 2.5V$	20 + 0.1C_B		250	ns
	t_F	C_B = 50pF, I_{SDA} = 3mA, V_L < 2.5	20 + 0.1C_B		250	
Pulse Width of Suppressed Spike	t_{SP}	(Note 9)		50		ns

Note 3: All currents into the device are negative; currents out of the device are positive. All voltages are referenced to device ground unless otherwise specified.

Note 4: Parameters are 100% production tested at +25°C, limits over temperature are guaranteed by design.

Note 5: The V_{BUS} current source and current gate time vary together with process and temperature such that the resulting V_{BUS} pulse is guaranteed to drive a <13µF load to a voltage >2.0V, and to drive a >96µF load to a volatge <2.2V. See the *SRP V_{BUS} Pulsing* section for an explanation of this self-timed pulse.

Note 6: Guaranteed by design, not production tested.

Note 7: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.

Note 8: C_B is total capacitance of one bus line in pF. Tested with C_B = 400pF.

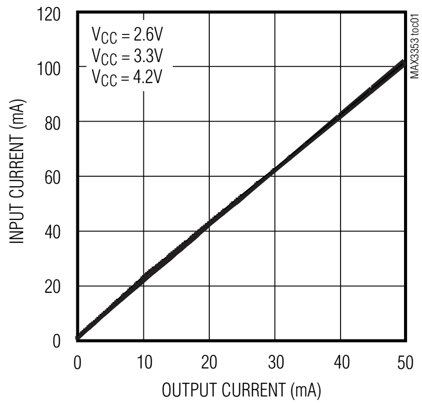
Note 9: Input filters on SDA, SCL, and ADD suppress noise spikes less than 50ns.

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

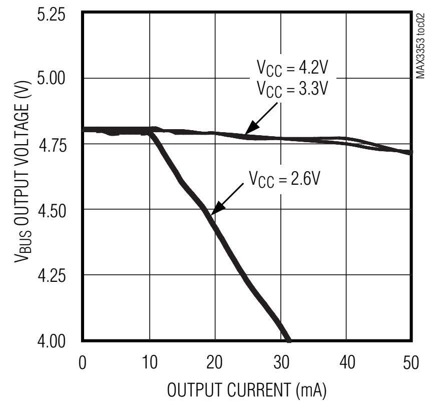
Typical Operating Characteristics

(V_{CC} = +3V, V_L = +2.5V, C_{FLYING} = 0.1µF, C_{VBUS} = 1µF (ESR_{CVBUS} = 0.1Ω), T_A = +25°C.)

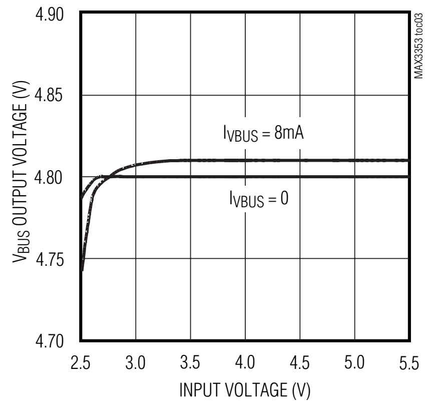
INPUT CURRENT vs. OUTPUT CURRENT



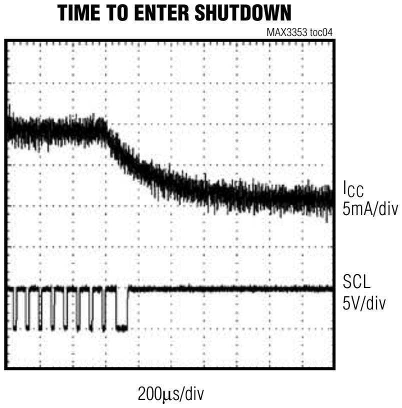
V_{BUS} OUTPUT VOLTAGE vs. V_{BUS} OUTPUT CURRENT



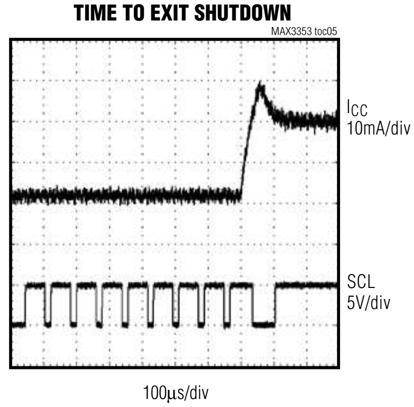
V_{BUS} OUTPUT VOLTAGE vs. INPUT VOLTAGE



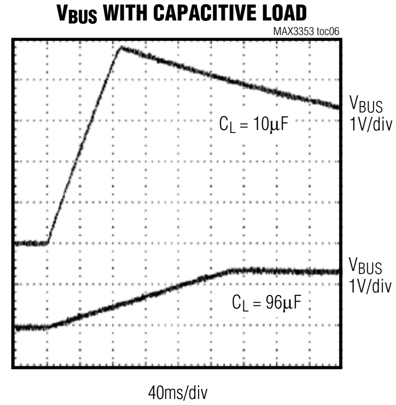
TIME TO ENTER SHUTDOWN



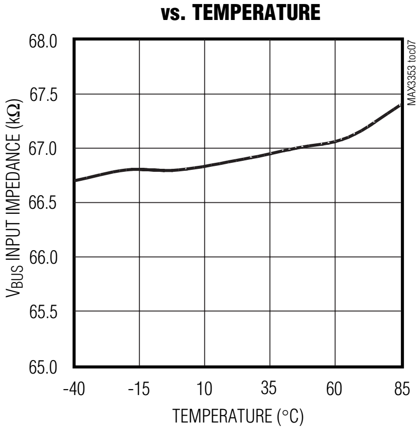
TIME TO EXIT SHUTDOWN



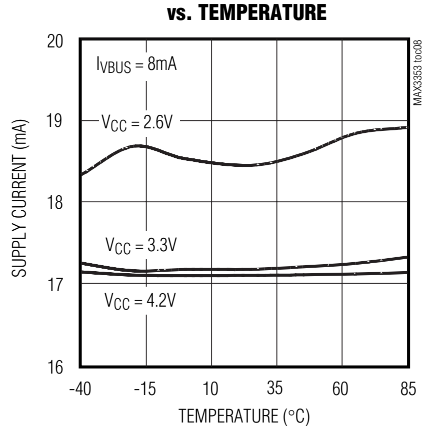
V_{BUS} WITH CAPACITIVE LOAD



V_{BUS} INPUT IMPEDANCE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	C5	V_{CC}	Power-Supply Input. V_{CC} input range is +2.6V to +5.5V. Bypass V_{CC} to GND with a 1µF capacitor.
2	D5	V_L	Logic Supply. V_L sets the logic output high voltage and logic input high threshold for SDA, SCL, $\overline{\text{INT}}$, and ID_OUT. V_L can range from +1.65V to V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
3	D4	SDA	Serial Data Input/Output. I^2C bus serial data input/open-drain output can be driven above V_L.
4	C3	ADD	Address Select Input. Address selection for the I^2C-compatible interface. ADD has an internal 110kΩ pulldown resistor (see the *2-Wire I^2C Compatible Serial Interface* section for details).
5	D3	SCL	Serial Clock Input. I^2C bus serial clock input. Can be driven above V_L.
6	D2	$\overline{\text{INT}}$	Interrupt Output. $\overline{\text{INT}}$ is an active-low output and can be set either open-drain or push/pull output through control register 1 (default = open drain).
7	D1	ID_OUT	Device ID Output. Output of ID_IN level translated to V_L.
8	C1	V_{TRM}	Termination Supply Input. Connect +3V to +3.6V supply voltage for internal USB pullup resistors. Bypass V_{TRM} to GND with a 0.1µF capacitor.
9	B1	D-	USB D- (±15kV ESD Protected)
10	A1	D+	USB D+ (±15kV ESD Protected)
11	A2	ID_IN	Device ID Input. Internally pulled up to V_{CC}. ID_IN logic state is V_L level translated to ID_OUT and can be read through the I^2C interface (±15kV ESD protected).
12	—	N.C.	No Connection. Not internally connected.
13	A3	GND	Ground
14	A4	C-	Charge-Pump Capacitor Negative Connection
15	A5	C+	Charge-Pump Capacitor Positive Connection
16	B5	V_{BUS}	OTG Bus Supply. Provides power to the bus. V_{BUS} can be back-driven to +6V. Bypass V_{BUS} to GND with a 1µF capacitor.

Detailed Description

The MAX3353E integrates a regulated charge pump, switchable pullup/pulldown resistors, and an I^2C-compatible 2-wire serial interface. The internal level shifter allows the device to operate with logic supply voltages (V_L) between +1.65V and V_{CC}. The MAX3353E's OTG-compliant charge pump operates with input supply voltages (V_{CC}) from +2.6V to +5.5V and supplies an OTG-compatible output on V_{BUS} while sourcing 8mA output current.

The MAX3353E level-detector comparators monitor important V_{BUS} voltages needed to support SRP and HNP and provides an interrupt output signal for OTG events that require action. The V_{BUS} power-control block performs the various switching functions required by an OTG dual-role device and is programmable by system logic.

For OTG operation, D+ and D- are connected to switchable pulldown resistors (host) and switchable pullup resistors (peripheral) controlled by internal registers.

Charge Pump

The MAX3353E's OTG-compliant charge-pump operates with input supply voltages (V_{CC}) from +2.6V to +5.5V and supplies an OTG-compatible output on V_{BUS} with the capability of sourcing 8mA (min) output current. When V_{BUS} is not providing power, an input impedance of no more than 100kΩ and no less than 40kΩ to GND is present on V_{BUS}. When V_{BUS} provides power, the rise time on V_{BUS} from 0 to 4.4V is no longer than 100ms when driving a constant current load of 8mA and an external load capacitance of 13µF.

During a continuous short circuit on V_{BUS}, the charge-pump output is current limited to 140mA (typ). Thermal-shutdown circuitry turns off the charge pump if the die temperature exceeds +150°C and restarts when the die cools to 140°C.

Level Shifters

Internal level shifters allow the system-side interface to run at logic supply voltages as low as 1.65V. Interface logic signals are referenced to the voltage applied to V_L.

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

V_{BUS} Level-Detection Comparators

Comparators drive status register bits 0, 1, and 2 to indicate these important USB OTG V_{BUS} voltage levels:

- V_{BUS} is valid (V_{BUS} > 4.6V)
- A USB session is valid (V_{BUS} > 1.4V)
- A USB session is ended (V_{BUS} < 0.5V)

The 4.6V comparator sets bit 0 in status register V_{BUS_VALID} to 1 if V_{BUS} > 4.6V. The A Device uses the V_{BUS} valid status bit (V_{BUS_VALID}) to determine if the B Device is sinking too much current (i.e., is not supported). The interrupt can be associated to either a positive or a negative transition. The 1.4V comparator sets bit 1 of status register SESSION_VALID to 1 if V_{BUS} > 1.4V. This status bit indicates that a data transfer session is valid and the interrupt can be associated to either a positive or a negative transition. The session-end comparator sets bit 2 in the status register SESSION_END to a 1 when V_{BUS} < 0.5V, and generates an interrupt when V_{BUS} falls below 0.5V. Figure 1 shows the level-detector comparators.

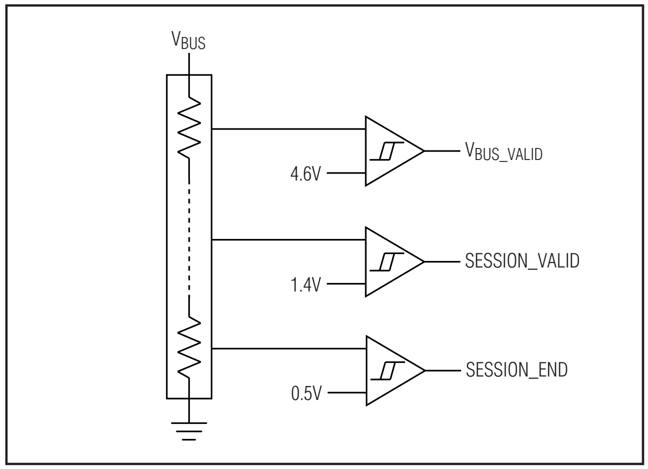


Figure 1. Comparator Network Diagram

Interrupt Logic

When OTG events require action, the MAX3353E provides an interrupt output signal on $\overline{INT}$. An interrupt is triggered ($\overline{INT}$ goes low) when one of the conditions specified by the interrupt-mask register and interrupt-edge register is verified. $\overline{INT}$ stays active until the interrupt is cleared by reading the interrupt latch register.

Shutdown

In shutdown mode, the MAX3353E's quiescent current is reduced to less than 2µA. Bit 0 in control register 2 controls the shutdown feature. Setting bit 0 = 1 places the device in shutdown mode (Figure 2, Table 5). When in shutdown, the MAX3353E's charge-pump current generator and V_{BUS} detection comparators are turned off. During shutdown, the I^2C serial interface is fully functional and registers can be read from or written to. ID_IN and ID_OUT are both functional in shutdown.

V_{BUS} Power Control

V_{BUS} is a dual-function I/O that can supply USB OTG-compliant voltage to the USB. The V_{BUS} power-control block performs the various switching functions required by an OTG dual-role device. This action is programmed by the system logic using internal register control bits in control register 2.

- Discharge V_{BUS} through a resistor to ensure a session is not in progress.
- Charge V_{BUS} through an internal current generator to initiate SRP (session request protocol).
- Connect the charge pump to V_{BUS} to provide power on V_{BUS}.

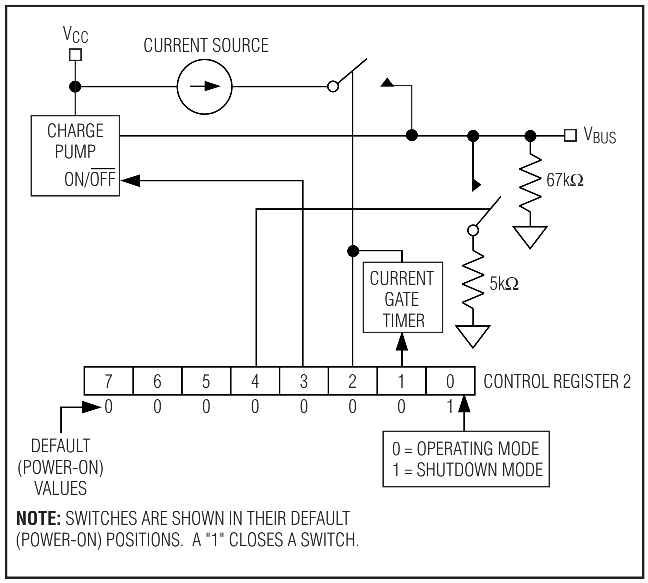


Figure 2. Power-Control Block Diagram

Bit 0 (SDWN) in control register 2 is used to place the MAX3353E in normal operation or shutdown mode. Setting bit 1 (V_{BUS_CHG1}) issues a timed pulse on V_{BUS} suitable for implementing the session request protocol (see the *SRP V_{BUS} Pulsing* section). The pulse is created by turning a current source – supplied by V_{CC} and connected to V_{BUS} – on and off. Setting control register bit 2 (V_{BUS_CHG2}) to 1 charges VBUS through the current source continuously. Setting V_{BUS_CHG2} to zero disconnects the current source. Bit 3 (V_{BUS_DRV}) turns the charge pump on and off to power V_{BUS}. Bit 4 in control register 2 (V_{BUS_DISCHG}) is used to discharge V_{BUS} through a 5kΩ resistor. Figure 2 and Table 2 show power control.

Autoconnect and Autoresponse

USB OTG defines the HNP, where the default host (A Device) can pass the host responsibilities off to the default peripheral (B Device). This protocol can be handled entirely by the firmware and controlling logic that drives the OTG transceiver. The MAX3353E has the option to automatically perform some of the required signaling for some of the timing-critical events in the HNP process. The automatic signaling used by the A Device, when it transfers host control to the B Device, is defined by the OTG transceiver supplement and is known as autoconnect. Autoconnect allows the transceiver to automatically connect the A Device's D+ pullup resistor during HNP. Autoconnect is enabled when the MAX3353E is configured as an A Device (ID_IN = 0) and the BDISC_ACONN control bit is set.

The MAX3353E also has the capability to automate the signaling used by the B Device when it assumes host control from the A Device. This autoresponse is not specified by the OTG-transceiver supplement. Autoresponse causes the B Device to automatically assert a bus reset by driving a single-ended zero (SE0: both D+ and D- driven low) onto USB in response to the A Device connecting its D+ pullup resistor. Autoresponse is enabled when the MAX3353E is configured as a B Device and the BDISC_ACONN control bit is set.

Note: In a system, D+ and D- are also driven by a transceiver in an ASIC or other device. The autoresponse mode should not be used unless the system designer can ensure that there is no bus conflict between the transceiver and the MAX3353E driving USB to SE0.

Autoconnect Details

When the MAX3353E is configured as an A Device (ID_IN = GND), it can enable autodetect by setting BDISC_ACONN to one. This should be done after the USB is in the suspend state (>3ms with no traffic). The MAX3353E monitors D+/D- for an SE0. The presence of the SE0 indicates that the B Device has disconnected its pullup resistor, the first step in HNP. When SE0 is detected, the MAX3353E automatically turns on its internal pullup resistor to the D+ line within 3ms. There are two ways for firmware to ascertain that the MAX3353E has automatically turned on its D+ pullup during HNP:

1) The A_HNP status bit goes high when the D+ pullup is automatically connected during HNP
2) The A_HNP_EN control bit is set, and an interrupt is issued as the D+ pullup is connected (see also the *Interrupt Logic* section).

By clearing BDISC_ACONN bit, the D+ pullup is disconnected. After a successful autoconnect operation, the firmware should set the DP_PULLUP control bit before clearing the BDISC_ACONN bit; this ensures that the D+ pullup remains connected.

Note: The autoconnect works only if MAX3353E is not in shutdown.

Autoresponse Details

When the MAX3353E is configured as a B Device (ID_IN = open), setting the BDISC_ACONN control bit enables the autoresponse feature. Using this feature, the MAX3353E automatically issues a USB bus reset when the A Device becomes a peripheral. Firmware can take advantage of the autoresponse feature of the MAX3353E by doing the following:

- Ensure that the system transceiver is in USB-suspend mode. Wait until the USB-suspend conditions are met (no USB activity for >3ms). Enable autoresponse. Set the BDISC_ACONN control bit. Signal a USB disconnect. Firmware clears the DP_PULLUP control bit, which disconnects the D+ pullup resistor. At this point, the MAX3353E waits at least 25µs before enabling its internal USB line monitor to detect if the A Device has attached its D+ pullup; this ensures that the D+ line is not high due to the residual effect of the B Device pullup. When the A Device has connected its D+ pullup, the MAX3353E issues a bus reset (SE0) and the B_HNP status bit goes high.
- Wait for B_HNP to go high; output SE0 from the ASIC or other device on D+/D-. Disable autoresponse. By clearing BDISC_ACONN bit, the SE0 generator is turned off. The SE0 is maintained by the system USB transceiver.

Note: The autoresponse works only if the MAX3353E is not in shutdown.

SRP V_{BUS} Pulsing

Session request protocol (SRP) is designed to allow the A Device (default host) to conserve power by turning off V_{BUS} when there is no USB traffic. The B Device (default peripheral) can request the A Device to turn V_{BUS} on and initiate a new session through SRP.

The B Device must initiate SRP in two ways: data-line and V_{BUS} pulsing. Firmware is responsible for turning on and off the pullup resistor on D+ to implement data-line pulsing. Firmware can also be used to turn on and off a current source to implement V_{BUS} pulsing.

The MAX3353E also has a special feature that allows it to control the timing of the V_{BUS} pulse.

Since an OTG device could be plugged into a PC, the V_{BUS} pulse must be particularly well controlled to prevent damage to a PC host. For this reason, V_{BUS} pulsing is done by turning on and off a current source. The V_{BUS} pulse must be timed so it drives a 13µF load (when it is connected to the A Device) to a voltage greater than 2.1V, and it drives a >96µF load (when it is connected to a standard PC) to a voltage less than 2.0V.

Firmware can control the current source and the timing of the V_{BUS} pulse through the V_{BUS_CHG2} control bit. The MAX3353E also has the capability to time the pulse itself. Firmware initiates the self-timed V_{BUS} pulse by setting the V_{BUS_CHG1} control bit to 1.

The internal timer and current generator guarantee that the V_{BUS} voltage goes above 2.1V if $C_{VBUS} \leq$ 13µF within 90ms and stands below 2.0V if $C_{VBUS} \geq$ 96µF. Once the time has elapsed, if another V_{BUS} pulse is required, it is necessary to clear the V_{BUS_CHG1} bit and then set it again.

Note: SRP V_{BUS} pulsing and its associated current generator work only if the MAX3353E is not in shutdown.

Data-Line Pullup and Pulldown Resistance

For OTG operation, D+ and D- are connected to switchable pulldown resistors (host) and switchable pullup resistors (peripheral). Data-line pullup/pulldown resistors are individually controlled through data bits 4 through 7 in control register 1. Two 15kΩ pulldown resistors allow the device to be set as a host and are asserted by bits 6 and 7. The 1.5kΩ pullup resistor is applied to the data lines through SW1 and SW2, which are controlled by bits 4 and 5. D+ pullup has higher priority to avoid direct connection of D+ and D-. Each of the control bits controls a designated switch; therefore, pullup and pulldown switches can be asserted at the same time. A simplified schematic of the switching network is shown in Figure 3.

The bidirectional D+ and D- lines are ESD protected to ±15kV, reducing external components in many applications.

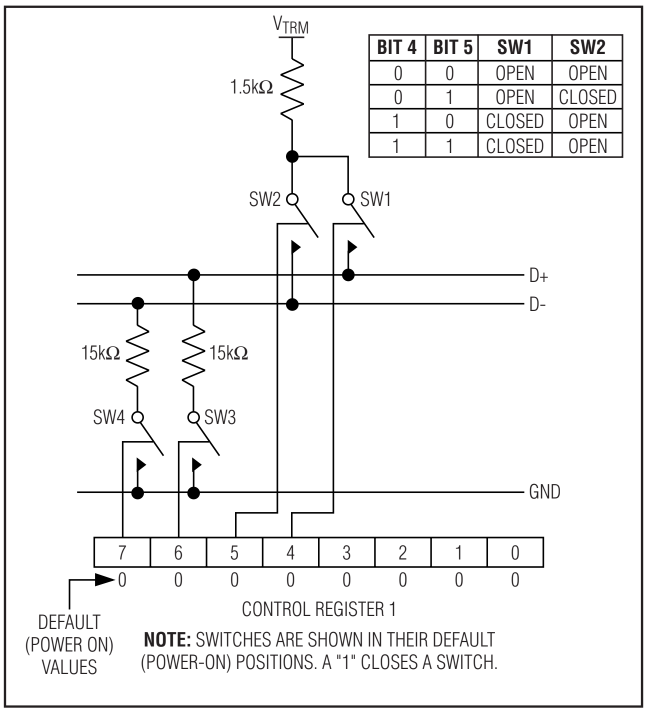


Figure 3. Pullup and Pulldown Resistors Network

Applications Information

2-Wire I²C-Compatible Serial Interface

A register file that interfaces to the control logic uses a simple 2-wire interface operating up to 400kHz to control the various switches and modes.

Serial Addressing

The MAX3353E operates as a slave that sends and receives control and status signals through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve

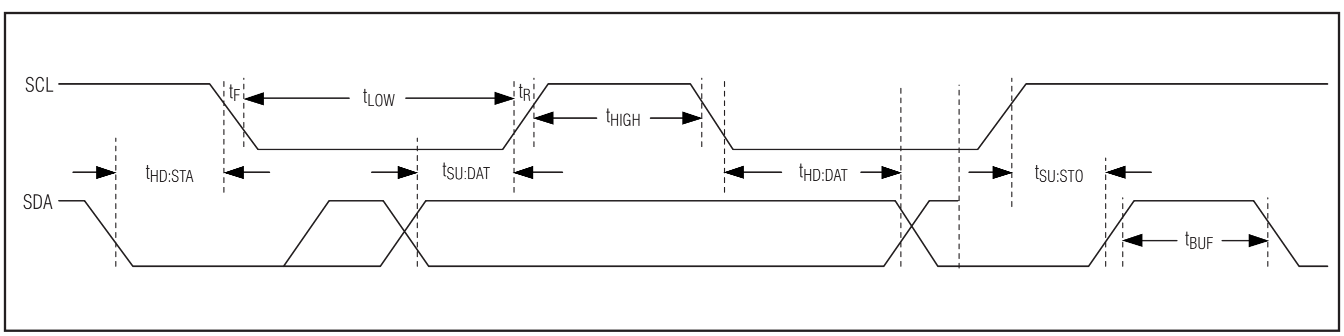


Figure 4. 2-Wire Serial Interface Timing Details

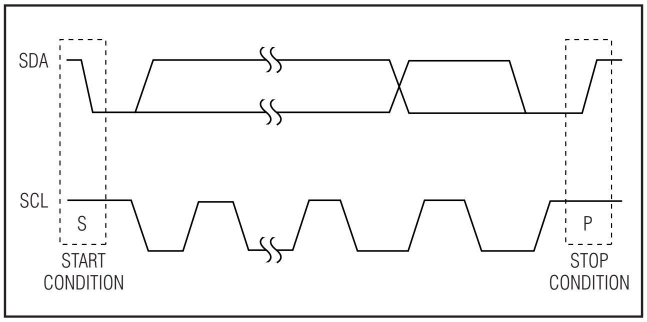


Figure 5. Start and Stop Conditions

bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX3353E and generates the SCL clock that synchronizes the data transfer (Figure 4).

The MAX3353E SDA line operates as both an input and an open-drain output. A pullup resistor (4.7kΩ typ) is required on SDA. The MAX3353E SCL line operates only as an input. A pullup resistor (4.7kΩ typ) is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 5) sent by a master, followed by the MAX3353E 7-bit slave address plus R/$\overline{W}$ bit (Figure 6), a register address byte, one or more data bytes, and finally a STOP condition (Figure 5).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 5).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 7).

Acknowledge

The acknowledge bit is the clocked ninth bit that the recipient uses to handshake receipt of each byte of data (Figure 8). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX3353E, the MAX3353E generates the acknowledge bit because it is the recipient. When the MAX3353E is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX3353E has a 7-bit-long slave address. The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, high for a read command. The first 6 bits (MSBs) of the MAX3353E slave address are always 010110. Select slave address bit A0 by connecting the address input ADD to V_L, GND, or leave floating (ADD is internally pulled to GND through a 110kΩ resistor). The MAX3353E has two possible slave addresses (Table 1). As a result, only two MAX3353E devices can share the same interface.

Write Byte Format

A write to the MAX3353E comprises the transmission of the MAX3353E's slave address with the R/$\overline{W}$ bit set to zero, followed by 2 bytes of information. The first byte of information is the command byte that determines which register of the MAX3353E is to be written by the second byte. The second byte is the data that goes into the register that is set by the first byte. Figure 9 shows the typical write byte format.

Read Byte Format

A read from the MAX3353E comprises the transmission of the MAX3353E's slave address (from the master) with the R/$\overline{W}$ bit set to zero, followed by one byte containing the address of the register, from which the master is going to read data, and then followed by MAX3353E's slave address again with the R/$\overline{W}$ bit set to one. After that one byte of data is being read by the master. Figure 10 shows the read byte format that must be used. To read many contiguous registers, multiple accesses are required.

Registers

Control Registers (10h, 11h)

There are two read/write control registers. Control register 1 is used to set D+, D- pullup or pulldown, and to set interrupt output to open-drain or push-pull. Control register 2 is the bus control register used to control the bus operation and put the device into shutdown mode. (Tables 3, 4, and 5.)

Status Register (13h)

The status register is a read-only register for determining valid bus and session comparator thresholds, ID_IN status, and HNP success. Tables 6 and 7 show status register address map, bit configuration, and description.

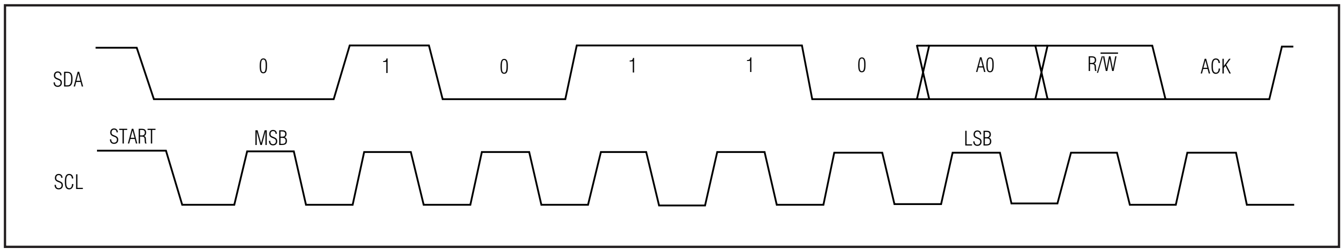


Figure 6. Slave Address

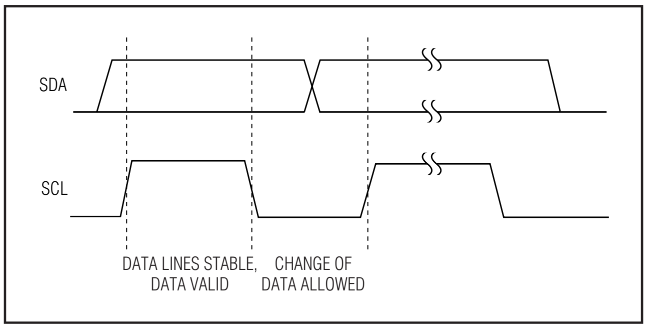


Figure 7. Bit Transfer

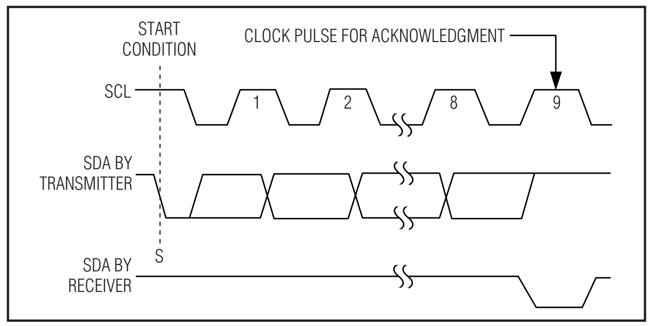


Figure 8. Acknowledge

S	**PART ADDRESS**							**R/W̄**	**ACK**	**REGISTER ADDRESS**								**ACK**
	A_6	A_5	A_4	A_3	A_2	A_1	A_0	0										
	7 bits							W		8 bits								

DATA								**ACK**	**P**
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
8 bits									

Where:

Slave address: Part address
Register address: Selecting which register to write to
Data: Data byte being read by the master
R/W: Read/Write (R/W = 1: Read; R/W = 0: Write)
S: Start condition
P: Stop condition
ACK: Acknowledge bit from the slave
NACK: Not acknowledged bit from the master
Blank: Master transmission
Shaded: Slave transmisstion

Figure 9. Write Byte Format

S	**PART ADDRESS**							**R/W̄**	**ACK**	**REGISTER ADDRESS**								**ACK**
	A_6	A_5	A_4	A_3	A_2	A_1	A_0	0	0									0
	7 bits									8 bits								

RS	**PART ADDRESS**							**R/W̄**	**ACK**	**DATA**								**NACK**	**P**
	A_6	A_5	A_4	A_3	A_2	A_1	A_0	1	0									1	
	7 bits									8 bits									

Where:

Slave address: Part address
Register address: Selecting which register to write to
Data: Data byte being read by the master
R/W̄: Read/Write (R/W̄ = 1: Read; R/W̄ = 0: Write)
S: Start condition
P: Stop condition
ACK: Acknowledge bit from the slave
NACK: Not acknowledged bit from the master
Blank: Master transmission
Shaded: Slave transmisstion

Figure 10. Read Byte Format

Table 1. MAX3353E Address Map

ADD PIN	ADDRESS BITS						
	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Float or GND	0	1	0	1	1	0	0
V_L	0	1	0	1	1	0	1

Table 2. Register Address Map

NAME	ADD	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Manufacturer Register 0	00h	0	1	1	0	1	0	1	0
Manufacturer Register 1	01h	0	0	0	0	1	0	1	1
Manufacturer Register 2	02h	0	1	0	1	0	0	1	1
Manufacturer Register 3	03h	0	0	1	1	0	0	1	1
Product ID Register 0	04h	0	1	0	0	1	0	0	0
Product ID Register 1	05h	0	1	0	1	1	0	1	0
Product ID Register 2	06h	0	1	0	0	0	0	1	0
Product ID Register 3	07h	0	0	0	0	0	0	0	1
Reserved	08h-0Fh	—	—	—	—	—	—	—	—
Control Register 1	10h	DM_ PULLDWN	DP_ PULLDWN	DM_ PULLUP	DP_ PULLUP	—	BDISC_ ACONN	IRQ_MODE	—
Control Register 2	11h	—	—	—	V_{BUS_DISCHG}	V_{BUS_DRV}	V_{BUS_CHG2}	V_{BUS_CHG1}	SDWN
Reserved	12h	—	—	—	—	—	—	—	—
Status Register	13h	—	B_HNP	A_HNP	ID_FLOAT	ID_GND	SESSION_ END	SESSION_ VALID	V_{BUS_VALID}
Interrupt Mask	14h	—	—	A_HNP_EN	ID_ FLOAT_EN	ID_ GND_EN	SESSION_ END_EN	SESSION_ VALID_EN	$V_{BUS\_VALID\_EN}$
Interrupt Edge	15h	—	—	—	—	—	—	SESSION_ VALID_ED	$V_{BUS\_VALID\_ED}$
Interrupt Latch	16h	A_HNP_RQ	ID_ FLOAT_RQ	ID_ GND_RQ	SESSION_ END_RQ	SESSION_ VALID_RN	$V_{BUS\_VALID\_RN}$	SESSION_ VALID_RP	$V_{BUS\_VALID\_RP}$
Reserved	17h -Ffh	—	—	—	—	—	—	—	—

Interrupt Registers (14h, 15h, 16h)

There are three interrupt registers. Interrupt mask register is a read/write register used to enable interrupts and read status of interrupts. Interrupt edge register is a read/write register for setting and determining interrupts for positive and negative edges. Interrupt latch register is a read only register to check and validate interrupt requests. Table 8 shows the interrupt mask, interrupt edge, and interrupt latch address maps. Bit configuration is shown in Tables 9, 10, and 11.

Manufacturer and ID Register Address Map

The manufacturer and ID registers are read-only registers (Table 12).

External Capacitors

Five external capacitors are recommended for proper operation. Bypass V_L and V_{TRM} to GND with a 0.1µF ceramic capacitor. Bypass V_{BUS} and V_{CC} to GND with a 1µF low-ESR ceramic capacitor. For the internal charge pump, use a 0.1µF ceramic capacitor between C+ and C-.

Table 3. Control Register Address Map

REGISTER	ADDRESS	POWER-UP REGISTER STATUS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Control 1	10h	0	0	0	0	0	0	0	0
Control 2	11h	0	0	0	0	0	0	0	1

Table 4. Control Register 1 (10h)

BIT NUMBER	SYMBOL	OPERATION
0	—	Not used
1	IRQ_MODE	Interrupt pin open-drain/push-pull: 0 = open drain 1 = push/pull
2	BDISC_ ACONN	0 = disable 1 = enable
3	—	Not used
4	DP_PULLUP	D+ pullup (high priority) 0 = D+ pullup unconnected 1 = D+ pullup connected
5	DM_PULLUP	D- pullup: 0 = D- pullup unconnected 1 = D- pullup connected
6	DP_ PULLDWN	D+ pulldown: 0 = D+ pulldown unconnected 1 = D+ pulldown connected
7	DM_ PULLDWN	D- pulldown: 0 = D- pulldown unconnected 1 = D- pulldown connected

Table 5. Control Register 2 (11h)

BIT NUMBER	SYMBOL	OPERATION
0	SDWN	Puts part in shutdown mode: 0 = operating 1 = shutdown mode
1	V_{BUS_CHG1}	Charge V_{BUS} through a current generator for 105ms: 0 = current generator OFF 1 = current generator ON (automatically turned off after 105ms)
2	V_{BUS_CHG2}	Charge V_{BUS} through a current generator: 0 = current generator OFF 1 = current generator ON
3	V_{BUS_DRV}	Drive V_{BUS} through charge pump 0 = V_{BUS} not driven 1 = V_{BUS} connected to the charge pump
4	V_{BUS_DISCHG}	Discharge V_{BUS} through a resistor: 0 = Resistor disconnected 1 = Resistor connected
5	—	Not used
6	—	Not used
7	—	Not used

Table 6. Status Register Address Map

REGISTER	ADDRESS	POWER-UP REGISTER STATUS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Status	13h	0	0	0	—	—	—	—	—

(—) = don't know

Table 7. Status Register (13h)

BIT NUMBER	SYMBOL	CONTENTS
0	V_{BUS_VALID}	Device A V_{BUS} valid comparator, threshold = 4.55V: 0 = V_{BUS} lower than threshold 1 = V_{BUS} higher than threshold
1	SESSION_ VALID	Session-valid comparator, threshold = 1.4V: 0 = V_{BUS} lower than threshold 1 = V_{BUS} higher than threshold
2	SESSION_END	V_{BUS} session-end comparator, threshold = 0.5V: 0 = V_{BUS} higher than threshold 1 = V_{BUS} lower than threshold
3	ID_GND	ID_IN grounded: 0 = not grounded 1 = grounded
4	ID_FLOAT	ID_IN floating: 0 = not floating 1 = floating
5	A_HNP	Set when Device A is configured, BDISC_ACONN is enabled and has attached pullup during HNP; cleared by resetting BDISC_ACONN bit in control register 1.
6	B_HNP	Set when Device B is configured, BDISC_ACONN is enabled and has asserted an SE0 during HNP; cleared by resetting BDISC_ACONN bit in control register 1.
7	—	Not used

Table 8. Interrupt Register Address Map

REGISTER	ADDRESS	POWER-UP REGISTER STATUS							
		BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Interrupt Mask	14h	0	0	0	0	0	0	0	0
Interrupt Edge	15h	0	0	0	0	0	0	0	0
Interrupt Latch	16h	0	0	0	0	0	0	0	0

Table 9. Interrupt Mask Register (14h)

BIT NUMBER	SYMBOL	OPERATION
0	$V_{BUS\_VALID\_EN}$	Enables V_{BUS_VALID} interrupt
1	SESSION_ VALID_EN	Enables SESSION_VALID interrupt
2	SESSION_ END_EN	Enables SESSION_END interrupt
3	ID_GND_EN	Enables ID_GND interrupt
4	ID_FLOAT_EN	Enables ID_FLOAT interrupt
5	A_HNP_EN	Enables A_HNP interrupt
6	—	Not used
7	—	Not used

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

Table 10. Interrupt Edge Register (15h)

BIT NUMBER	SYMBOL	OPERATION
0	$V_{BUS\_}$ VALID_ED	V_{BUS_VALID} interrupt on positive/negative edge: 0 = detected on negative edge 1 = detected on positive edge
1	SESSION_ VALID_ED	SESSION_VALID interrupt on positive/negative edge: 0 = detected on negative edge 1 = detected on positive edge
2	—	Not used
3	—	Not used
4	—	Not used
5	—	Not used
6	—	Not used
7	—	Not used

Table 11. Interrupt Latch Register (16h)

BIT NUMBER	SYMBOL	OPERATION
0	$V_{BUS\_VALID\_RP}$	V_{BUS_VALID} positive edge interrupt request: 0 = not asserted 1 = asserted
1	SESSION_ VALID _RP	SESSION_ VALID positive edge interrupt request: 0 = not asserted 1 = asserted
2	VBUS_ VALID _RN	V_{BUS_VALID} negative edge interrupt request: 0 = not asserted 1 = asserted
3	SESSION_ VALID _RN	SESSION_ VALID negative edge interrupt request: 0 = not asserted 1 = asserted
4	SESSION_END_ RQ	SESSION_END interrupt request: 0 = not asserted 1 = asserted
5	ID_GND_RQ	ID_GND interrupt request: 0 = not asserted 1 = asserted
6	ID_FLOAT_RQ	ID_FLOAT interrupt request: 0 = not asserted 1 = asserted
7	A_HNP_RQ	DP_SRP interrupt request: 0 = not asserted 1 = asserted

Table 12. Manufacturer and ID Register Address Map

REGISTER	ADD	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	hex
Manufacturer Register 0	00h	0	1	1	0	1	0	1	0	6A
Manufacturer Register 1	01h	0	0	0	0	1	0	1	1	0B
Manufacturer Register 2	02h	0	1	0	1	0	0	1	1	53
Manufacturer Register 3	03h	0	0	1	1	0	0	1	1	33
Product ID Register 0	04h	0	1	0	0	1	0	0	0	48
Product ID Register 1	05h	0	1	0	1	1	0	1	0	5A
Product ID Register 2	06h	0	1	0	0	0	0	1	0	42
Product ID Register 3	07h	0	0	0	0	0	0	0	1	01

Connect all capacitors as close to the device as possible. V_{BUS} and V_{CC} bypass capacitors should have trace lengths as short as possible

±15kV ESD Protection

To protect the MAX3353E against ESD, D+, D-, ID_IN, and V_{BUS}, have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states—normal operation, shutdown, and powered down. In order for the 15kV ESD structures to work correctly, a 1µF or greater capacitor must be connected from V_{BUS} to GND. ESD protection can be tested in various ways; D+, D-, ID_IN, and V_{BUS} are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±6kV using the IEC 1000-4-2 Contact Discharge method
3) ±11kV using the IEC 1000-4-2 Air-Gap Discharge method

ESD Test Conditions: ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the Human Body Model and Figure 12 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 13 shows the IEC 1000-4-2 model. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized. Figure 14 shows the IEC 1000-4-2 current waveform.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing. The Machine Model is less relevant to I/O ports after PC board assembly.

Layout Considerations

The MAX3353E high oscillator frequency makes proper layout important to ensure stability and maintain the output voltage under all loads. For best performance, minimize the distance between the capacitors and the MAX3353E.

UCSP Reliability

For the latest application details on UCSP construction, dimensions, tape-carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile as well as the latest information on reliability testing results, refer to Maxim Application Note: *UCSP – A Wafer-Level Chip Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

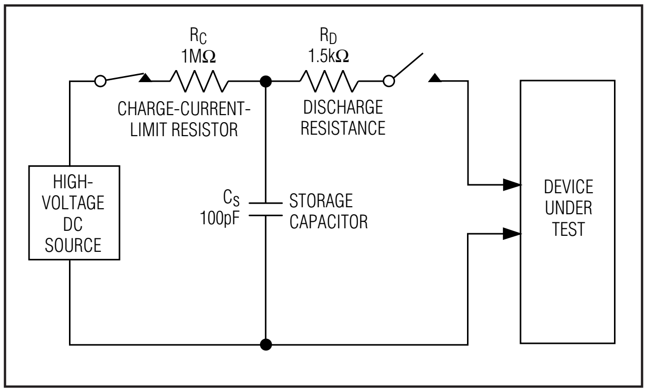


Figure 11. Human Body ESD Test Models

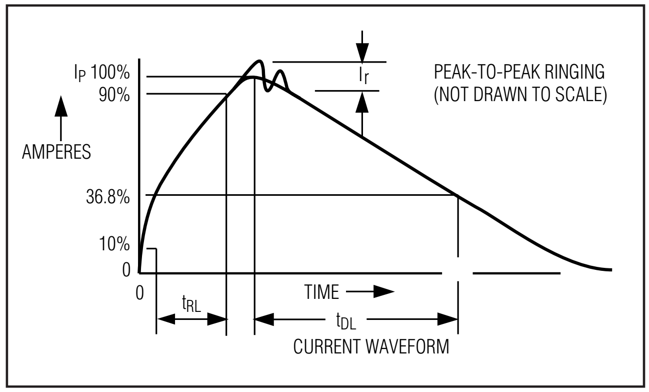


Figure 12. Human Body Model Current Waveform

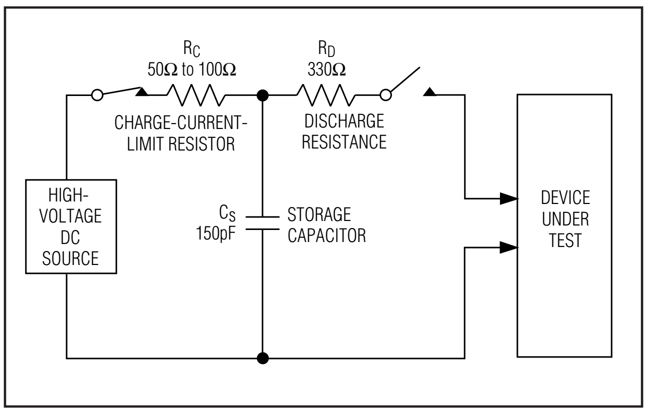


Figure 13. IEC 1000-4-2 ESD Test Model

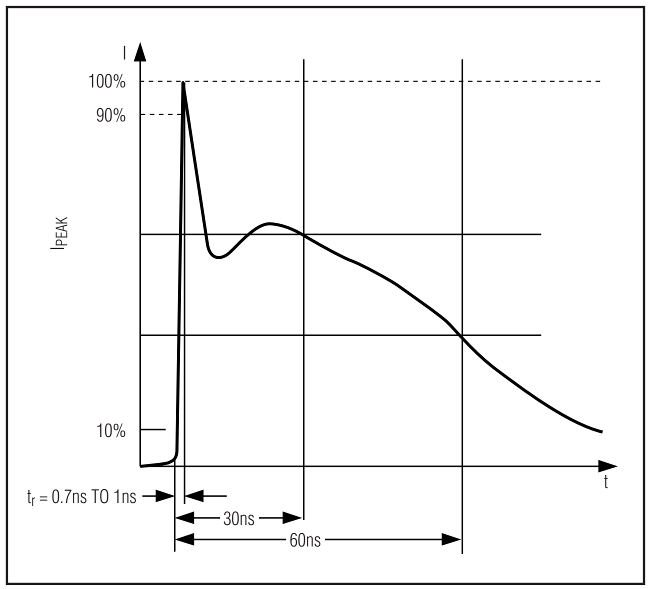
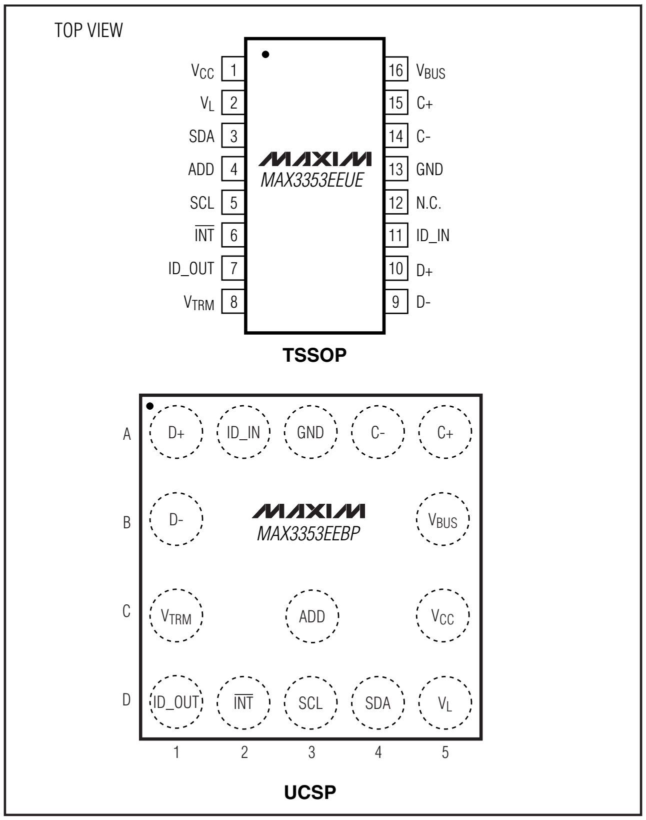
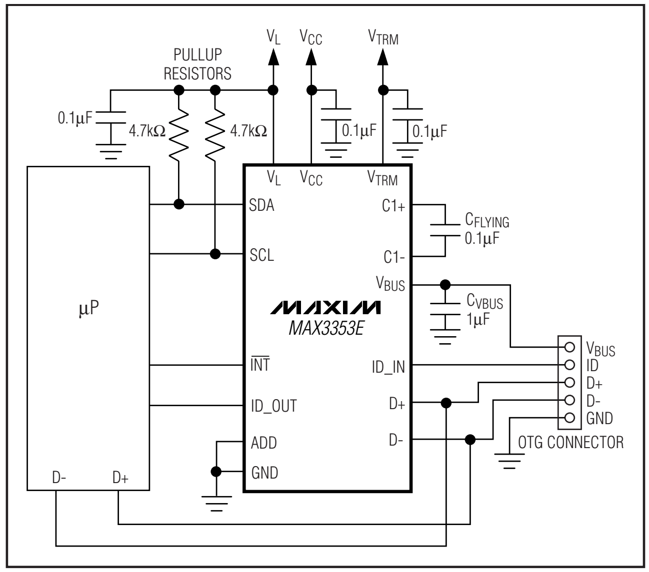


Figure 14. IEC 1000-4-2 Current Waveform

Pin Configurations



Typical Applications Circuit



Chip Information

TRANSISTOR COUNT: 9394

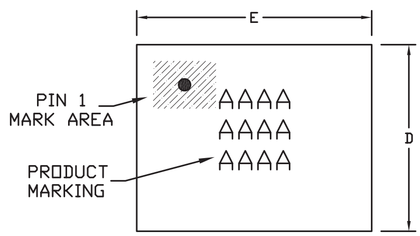
PROCESS: BiCMOS

USB On-the-Go Charge Pump with Switchable Pullup/Pulldown Resistors

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

5x4 UCSP.EPS

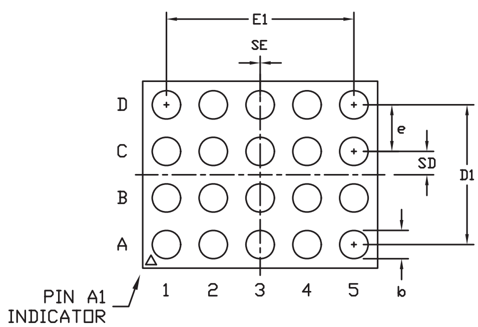


TOP VIEW

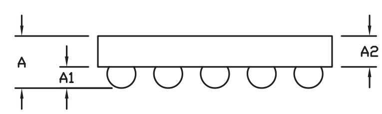
COMMON DIMENSIONS	
A	0.62+0.05−0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4
B20-7	2.03±0.08	2.54±0.08	B3, C3
B20-8	2.03±0.08	2.54±0.08	B2, B4, C2, C4

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

−DRAWING NOT TO SCALE−

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 5x4 UCSP

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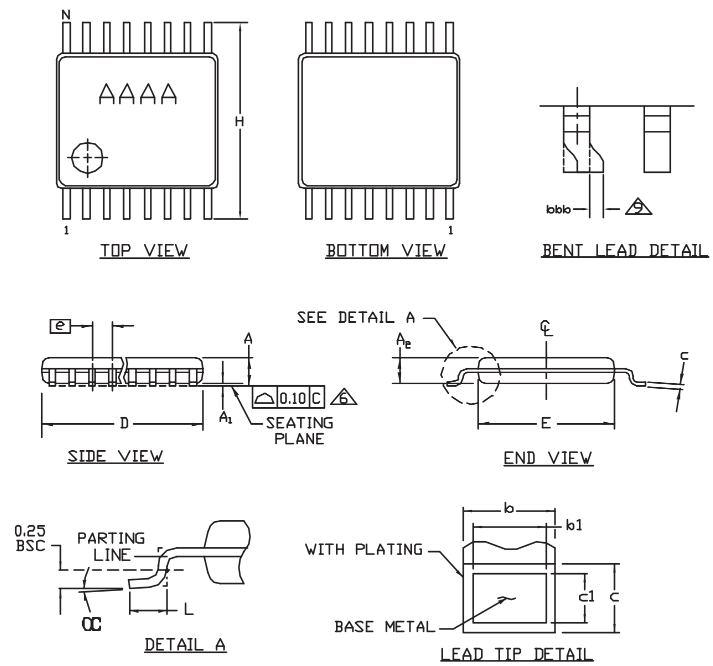
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

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