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19-5488; Rev 1; 1/12

PMBus 5-Channel Power-Supply Manager and Intelligent Fan Controller

General Description

The MAX34441 is a complex system monitor that can manage up to five power supplies and a fan. The power-supply manager monitors the power-supply output voltage and constantly checks for user-programmable overvoltage and undervoltage thresholds. It can also margin the power-supply output voltage up or down to a user-programmable level. The margining is performed in a closed-loop arrangement whereby the device automatically adjusts a pulse-width-modulated (PWM) output and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down. With the addition of an external current-sense amplifier, the device can also monitor currents.

The device also contains closed-loop fan-speed control. Based on user-programmable settings for fan-control PWM duty cycles or RPM speeds at particular temperature breakpoints, the device automatically adjusts the fan speed in a manner to reduce audible noise and power consumption.

Applications

Network Switches/Routers

Base Stations

Servers

Smart Grid Network Systems

Industrial Controls

Features

- ♦ 5 Channels of Power-Supply Management
  - Voltage Measurement/Monitoring
    - Differential 12-Bit 1% Accurate ADC
    - Min/Max Threshold Excursion Detection
  - Supports Current Monitoring with External Current-Sense Amplifier
  - Automatic Closed-Loop Margining
  - Programmable Up and Down Sequencing
  - Power-Good Output
- ♦ 1 Channel of Fan Control
  - Supports 3-Wire and 4-Wire Fans
  - Automatic Closed-Loop Fan-Speed Control
  - Support for Dual Tachometer Fans
  - Fan-Fault Detection
- ♦ Supports Up to Six Temperature Sensors
  - External Thermal Diode Interface with Automatic Series Resistance Cancellation
  - One Internal Temperature Sensor
  - Support for Up to Four Additional I^2C Digital Temp Sensor ICs
  - Fault Detection on All Temp Sensors
- ♦ PMBus™-Compliant Command Interface
- ♦ I^2C/SMBus-Compatible Serial Bus with Bus Timeout Function
- ♦ On-Board Nonvolatile Fault Logging and Default Configuration Setting
- ♦ No External Clocking Required
- ♦ +3.3V Supply Voltage

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX34441ETL+	-40°C to +85°C	40 TQFN-EP*
MAX34441ETL+T	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

PMBus is a trademark of SMIF, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* **www.maxim-ic.com/errata**.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} ....-0.3V to +5.5V
RS- to V_{SS} ....-0.3V to +0.3V
All Other Pins Except REG18 and
REG25 Relative to V_{SS} ....-0.3V to (V_{DD} + 0.3V)*
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 35.7mW/°C above +70°C)..............2857.1mW

Operating Temperature Range....................-40°C to +85°C
Storage Temperature Range....................-55°C to +125°C
Lead Temperature (soldering, 10s)....................+300°C
Soldering Temperature (reflow)....................+260°C

**Subject to not exceeding +5.5V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage Range	V_{DD}	(Note 1)	2.7		5.5	V
Input Logic 1	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic 0	V_{IL}		0		0.3 x V_{DD}	V
Input Logic-High: SCL, SDA, MSCL, MSDA	V_{I2C_IH}	2.7V ≤ V_{DD} ≤ 3.6V (Note 1)	2.1		V_{DD} + 0.3	V
Input Logic-Low: SCL, SDA, MSCL, MSDA	V_{I2C_IL}	2.7V ≤ V_{DD} ≤ 3.6V (Note 1)	0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CPU}	(Note 2)		2.5		mA
	$I_{PROGRAM}$			8		
Brownout Voltage	V_{BO}	Monitors V_{DD} (Note 1)	2.40	2.46	2.55	V
Brownout Hysteresis	V_{BOH}	Monitors V_{DD} (Note 1)		30		mV
Internal System Clock	f_{MOSC}			4.0		MHz
System Clock Error (Note 3)	$f_{ERR:MOSC}$	+25°C ≤ T_A ≤ +85°C	-3		+2	%
		-40°C ≤ T_A ≤ +25°C	-6.5		+1.6	
Output Logic-Low	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V
Output Logic-High	V_{OH1}	I_{OH} = -2mA (Note 1)	V_{DD} - 0.5			V
PWM, PSEN Pullup Current	I_{PU}	V_{PIN} = V_{SS}, V_{DD} = 3.3V	38	55	107	µA
ADC Internal Reference				1.225		V
ADC Voltage Measurement Error	V_{ERR}		-1		+1	%
ADC Internal Reference Temperature Drift			-0.5		+0.5	%

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Internal Reference Initial Accuracy (+25°C)			-1		+1	mV
ADC Full-Scale Input Voltage	V_{FS}		1.213	1.225	1.237	V
ADC Measurement Resolution	V_{LSB}			300		µV
ADC Bit Resolution			12			Bits
RS+ Input Resistance	R_{IN}		15			MΩ
ADC Integral Nonlinearity	INL	(Note 4)			±8	LSB
ADC Offset	V_{OFFSET}			±2		LSB
Internal Temperature Measurement Error		T_A = -40°C to +85°C	-3		+3	°C
Remote Temperature Measurement Error (MAX34441 Error Only)		T_A = 0°C to +60°C, T_{DIODE} = +60°C to +120°C	-1.5		+1.5	°C
		T_A = 0°C to +60°C, T_{DIODE} = -45°C to +120°C	-1.75		+1.75	
		T_A = -40°C to +85°C, T_{DIODE} = +60°C to +120°C	-2.75		+2.75	
		T_A = -40°C to +85°C, T_{DIODE} = -45°C to +120°C	-3.0		+3.0	
Store Default All Time				37		ms
Nonvolatile Log Write Time				12		ms
Nonvolatile Log Delete Time				200		ms
Flash Endurance	N_{FLASH}	T_A = +50°C	20,000			Write Cycles
Data Retention		T_A = +50°C	100			Years
Voltage Sample Rate				5		ms
Current Sample Rate				200		ms
RPM Sample Rate				1000		ms
Temperature Sample Rate				1000		ms
Device Startup Time		Measured from POR until monitoring begins		12		ms
PWM Frequency		Power supply		62.5		kHz
		Fan	30		25,000	Hz
PWM Resolution		Power supply		6		Bits
		Fan		7		

PMBus 5-Channel Power-Supply Manager and Intelligent Fan Controller

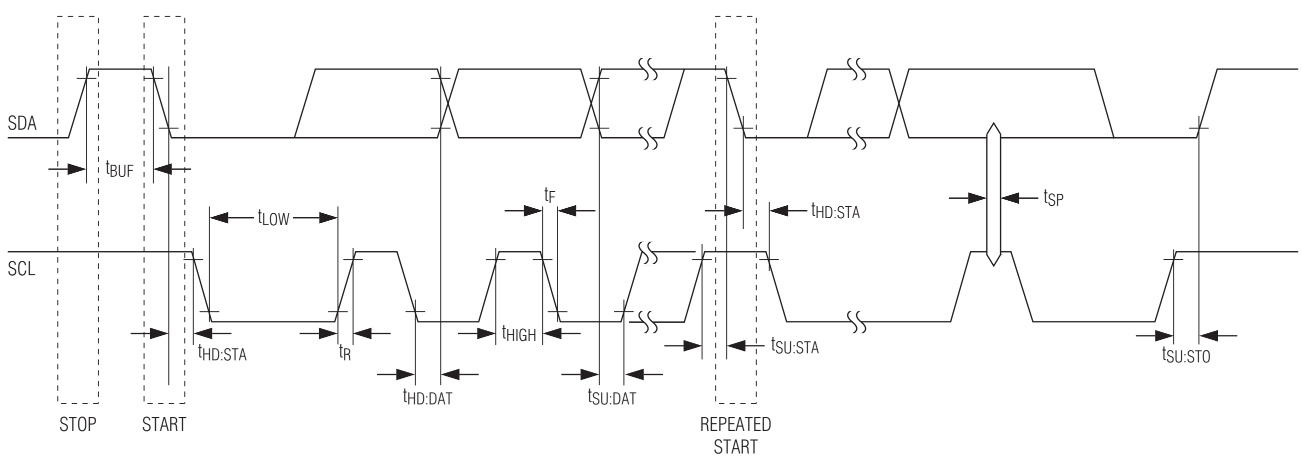
I²C/SMBus INTERFACE ELECTRICAL SPECIFICATIONS

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		100	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		4.7			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0			µs
Low Period of SCL	t_{LOW}		4.7			µs
High Period of SCL	t_{HIGH}		4.0			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		4.7			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
STOP Setup Time	$t_{SU:STO}$		4.0			µs
Clock Low Timeout	t_{TO}		25		35	ms

Note 1: All voltages are referenced to ground (V_{SS}). Currents entering the IC are specified as positive, and currents exiting the IC are negative.
Note 2: This does not include pin input/output currents.
Note 3: Guaranteed by design.
Note 4: ADC has no missing codes.

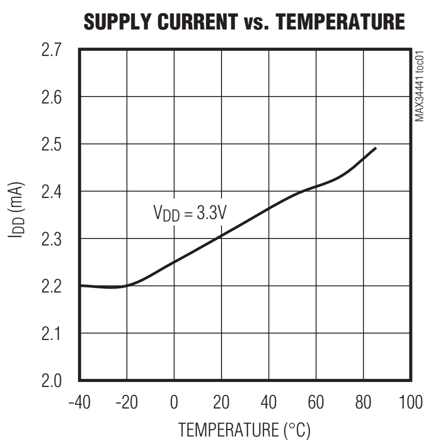
I²C/SMBus Timing

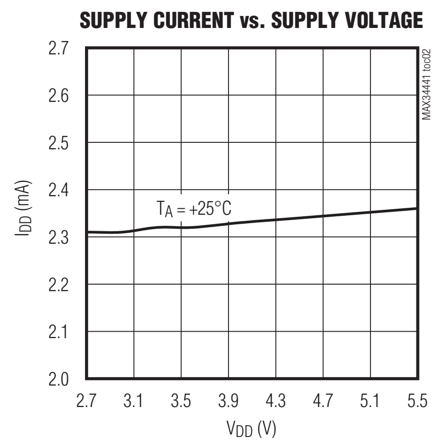


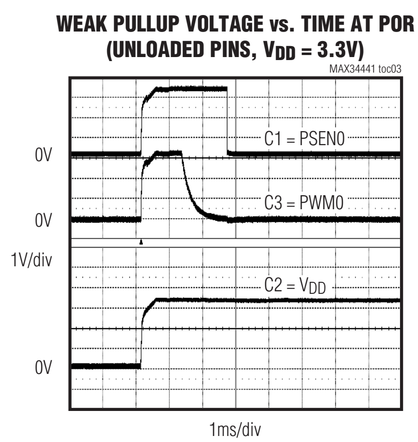
NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

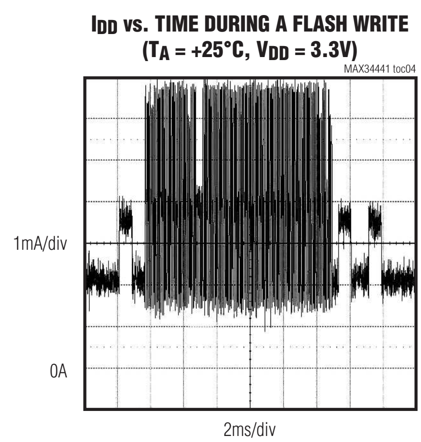
Typical Operating Characteristics

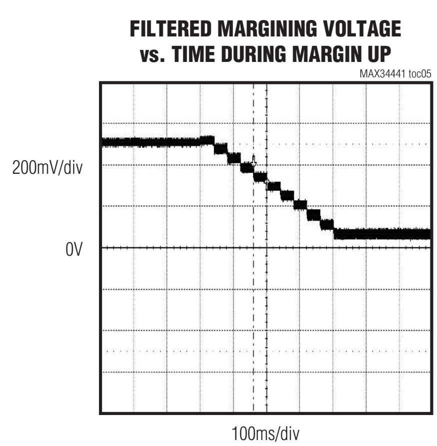
(T_A = +25°C, unless otherwise noted.)





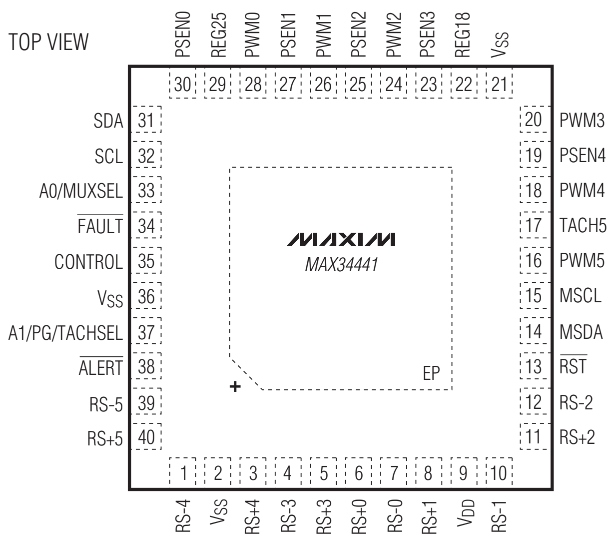






PMBus 5-Channel Power-Supply Manager and Intelligent Fan Controller

Pin Configuration



TQFN
(6mm × 6mm × 0.75mm)

Pin Description

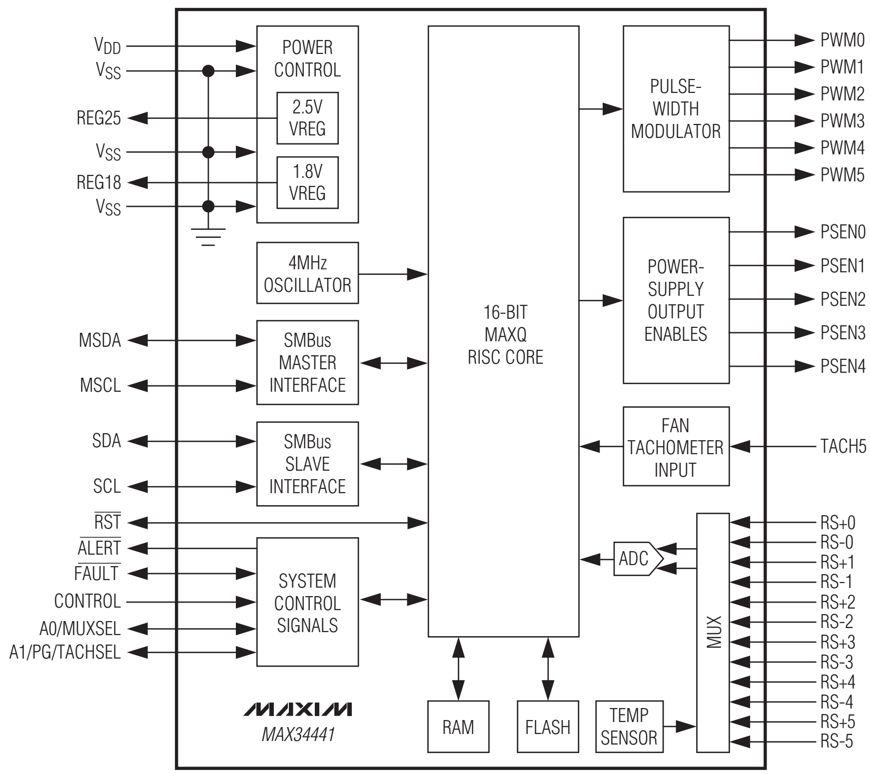
PIN	NAME	FUNCTION
1	RS-4	Ground Reference for ADC4 Voltage Measurement
2, 21, 36	V_{SS}	Digital-Supply Return Node (Ground)
3	RS+4	Power-Supply ADC Voltage-Sense Input, Measurement Relative to RS-4
4	RS-3	Ground Reference for ADC3 Voltage Measurement
5	RS+3	Power-Supply ADC Voltage-Sense Input, Measurement Relative to RS-3
6	RS+0	Power-Supply ADC Voltage-Sense Input, Measurement Relative to RS-0
7	RS-0	Ground Reference for ADC0 Voltage Measurement
8	RS+1	Power-Supply ADC Voltage-Sense Input, Measurement Relative to RS-1
9	V_{DD}	Supply Voltage. Bypass V_{DD} to V_{SS} with a 0.1µF capacitor.
10	RS-1	Ground Reference for ADC1 Voltage Measurement
11	RS+2	Power-Supply ADC Voltage-Sense Input, Measurement Relative to RS-2
12	RS-2	Ground Reference for ADC2 Voltage Measurement
13	$\overline{RST}$	Reset Active-Low Input
14	MSDA	Master I^2C Data Input/Output. Open-drain output.
15	MSCL	Master I^2C Clock Output. Open-drain output.
16	PWM5	Fan PWM Output #5. CMOS push-pull output. Low when the fan is disabled. A 100% duty cycle implies this pin is continuously high.
17	TACH5	Fan Tachometer Input
18	PWM4	PWM Margin Output #4. High impedance when the margining is disabled. A 100% duty cycle implies this pin is continuously high.
19	PSEN4	Power-Supply Enable Output #4. Programmable through MFR_MODE for either active high or active low and either open drain or CMOS push-pull.

Pin Description (continued)

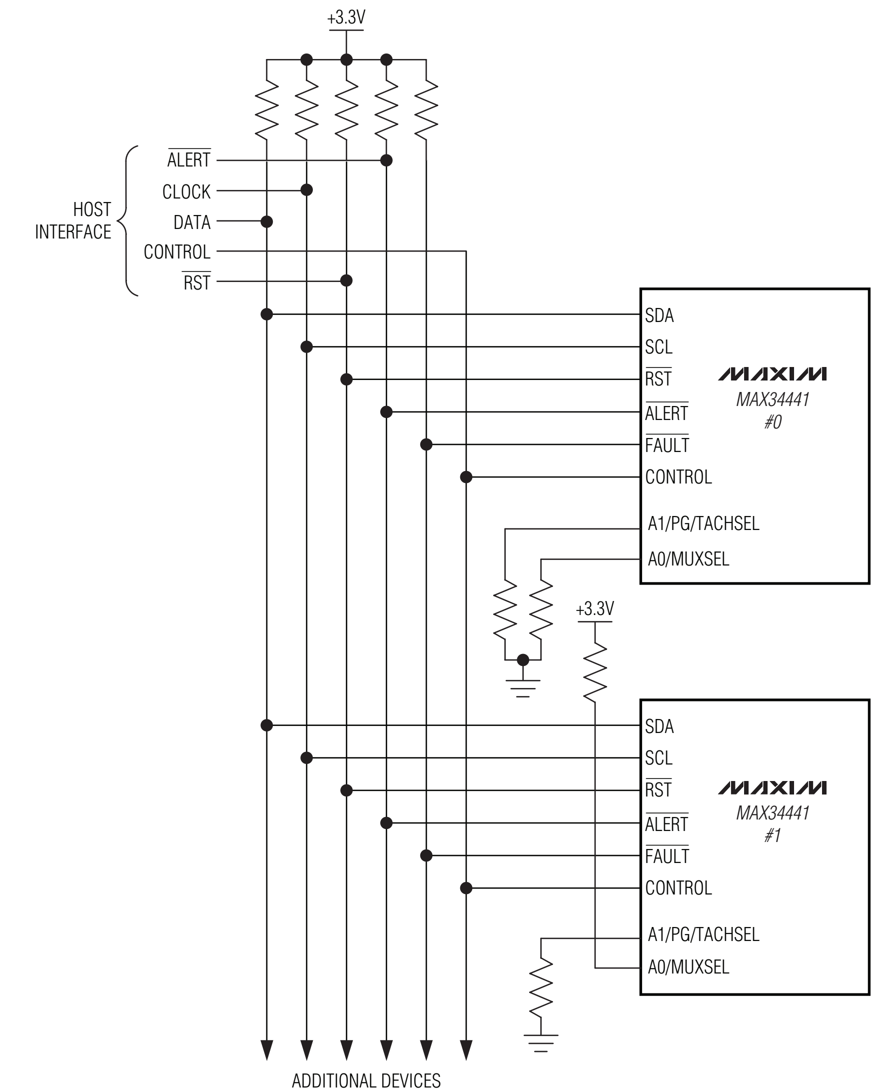
PIN	NAME	FUNCTION
20	PWM3	PWM Margin Output #3. High impedance when the margining is disabled. A 100% duty cycle implies this pin is continuously high.
22	REG18	Regulator for Low-Voltage Digital Circuitry. Bypass REG18 to V_{SS} with 1µF and 10nF capacitors. Do not connect other circuitry to this pin.
23	PSEN3	Power-Supply Enable Output #3. Programmable through MFR_MODE for either active high or active low and either open drain or CMOS push-pull.
24	PWM2	PWM Margin Output #2. High impedance when the margining is disabled. A 100% duty cycle implies this pin is continuously high.
25	PSEN2	Power-Supply Enable Output #2. Programmable through MFR_MODE for either active high or active low and either open drain or CMOS push-pull.
26	PWM1	PWM Margin Output #1. High impedance when the margining is disabled. A 100% duty cycle implies this pin is continuously high.
27	PSEN1	Power-Supply Enable Output #1. Programmable through MFR_MODE for either active high or active low and either open drain or CMOS push-pull.
28	PWM0	PWM Margin Output #0. High impedance when the margining is disabled. A 100% duty cycle implies this pin is continuously high.
29	REG25	Regulator for Analog Circuitry. Bypass REG25 to V_{SS} with 1µF and 10nF capacitors. Do not connect other circuitry to this pin.
30	PSEN0	Power-Supply Enable Output #0. Programmable through MFR_MODE for either active high or active low and either open drain or CMOS push-pull.
31	SDA	I^2C/SMBus-Compatible Input/Output
32	SCL	I^2C/SMBus-Compatible Clock Input
33	A0/MUXSEL	SMBus Address 0 Input/Multiplexer Control Output. This dual-function pin is sampled on device power-up to determine the SMBus address; connect a 100kΩ resistor from this pin to either V_{SS} or V_{DD} to set the address. After device power-up, this pin becomes an output that acts as voltage/current selector for an external analog multiplexer. MUXSEL is low for voltage measurements and high for current measurements.
34	$\overline{FAULT}$	Active-Low, Open-Drain Fault Input/Output. This pin is asserted when one or more of the power supplies in a global group are shut down due to a fault condition. Also, this pin is monitored and, when it is asserted, all power supplies in a global group are shut down. This pin is used to provide hardware control for power supplies in a global group across multiple devices. This output is unconditionally deasserted when $\overline{RST}$ is asserted or the device is power cycled. This pin has a 50µs deglitch filter.
35	CONTROL	Device Enable. Option through ON_OFF_CONFIG for active-low or active-high power-supply control. This pin has a 50µs deglitch filter.
37	A1/PG/ TACHSEL	SMBus Address 1 Input/Power-Good Output. This triple-function pin is sampled on device power-up to determine the SMBus address; connect a 100kΩ resistor from this pin to either V_{SS} or V_{DD} to set the address. After device power-up, this pin becomes an output that transitions high when all the enabled power supplies are above their associated POWER_GOOD_ON thresholds. Alternately, this pin can be programmed through MFR_MODE to select between two tachometers in dual-fan applications.
38	$\overline{ALERT}$	Active-Low, Open-Drain Alert Output
39	RS-5	Thermal Diode ADC Voltage Negative-Sense Input, Measurement Relative to RS+5
40	RS+5	Thermal Diode ADC Voltage Positive-Sense Input, Measurement Relative to RS-5
—	EP	Exposed Pad (Bottom Side of Package). Connect EP to V_{SS}.

Note: *All pins except V_{DD}, V_{SS}, REG18, REG25, ADC, and the EP are high impedance with a 50µA pullup during device power-up and reset. After device reset, the weak pullup is removed, and the pin is configured as input or output.*

Block Diagram



Multiple Device Connection Diagram



PMBus 5-Channel Power-Supply Manager and Intelligent Fan Controller

Detailed Description

The MAX34441 is a highly integrated system monitor based upon a 4MHz, 16-bit, MAXQ® microcontroller with factory-programmed functionality to monitor up to five power supplies and a system cooling fan. The device provides power-supply closed-loop control, fan-speed monitoring, and local/remote thermal-sensing facilities.

The power-supply manager monitors the power-supply output voltage and constantly checks for user-programmable overvoltage and undervoltage thresholds. It also can margin the power-supply output voltage up or down by a user-programmable level. The margining is performed in a closed-loop arrangement, whereby the device automatically adjusts a pulse-width-modulated (PWM) output and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down. With the addition of an external current-sense amplifier, the device can also monitor currents.

Thermal monitoring can be accomplished using up to six temperature sensors, including an on-chip thermal sensor, four DS75LV digital thermometers, and a remote thermal diode. Temperature offset can be added to individual sensors to compensate for thermal differences in a system. Communication with the DS75LV temperature sensor is conducted through a dedicated I^2C/SMBus interface.

The device also contains closed-loop fan-speed control. Based on user-programmable settings for fan-control PWM duty cycles or for fan RPM speeds at particular temperature breakpoints, the device automatically adjusts the fan speed in a manner to reduce audible noise and power consumption.

The device provides $\overline{ALERT}$ and $\overline{FAULT}$ output signals. Host communications are conducted through a PMBus-compatible communications port. Address input connections are also provided to allow up to four MAX34441 devices to reside on the system's I/O bus.

Table 1. PMBus Command Codes

CODE	COMMAND NAME	TYPE	PAGE 0–4 (NOTE 1)	PAGE 5 (NOTE 1)	PAGE 6–11 (NOTE 1)	PAGE 255 (NOTE 1)	NO. OF BYTES	FLASH STORED (NOTE 2)	DEFAULT VALUE (NOTE 2)
00h	PAGE	R/W Byte	R/W	R/W	R/W	R/W	1	N	00h
01h	OPERATION	R/W Byte	R/W	—	—	W	1	N	00h
02h	ON_OFF_CONFIG	R/W Byte	R/W	R/W	R/W	R/W	1	Y	1Ah
03h	CLEAR_FAULTS	Send Byte	W	W	W	W	0	N	—
10h	WRITE_PROTECT	R/W Byte	R/W	R/W	R/W	R/W	1	N	00h
11h	STORE_DEFAULT_ALL	Send Byte	W	W	W	W	0	N	—
12h	RESTORE_DEFAULT_ALL	Send Byte	W	W	W	W	0	N	—
19h	CAPABILITY	Read Byte	R	R	R	R	1	N	00h/10h
20h	VOUT_MODE	Read Byte	R	R	R	R	1	FIXED	40h
25h	VOUT_MARGIN_HIGH	R/W Word	R/W	—	—	—	2	Y	0000h
26h	VOUT_MARGIN_LOW	R/W Word	R/W	—	—	—	2	Y	0000h
2Ah	VOUT_SCALE_MONITOR	R/W Word	R/W	—	—	—	2	Y	7FFFh
38h	IOUT_CAL_GAIN	R/W Word	R/W	—	—	—	2	Y	0000h
3Ah	FAN_CONFIG_1_2	R/W Byte	—	R/W	—	—	1	Y	00h
3Bh	FAN_COMMAND_1	R/W Word	—	R/W	—	—	2	Y	FFFFh
40h	VOUT_OV_FAULT_LIMIT	R/W Word	R/W	—	—	—	2	Y	7FFFh
42h	VOUT_OV_WARN_LIMIT	R/W Word	R/W	—	—	—	2	Y	7FFFh
43h	VOUT_UV_WARN_LIMIT	R/W Word	R/W	—	—	—	2	Y	0000h
44h	VOUT_UV_FAULT_LIMIT	R/W Word	R/W	—	—	—	2	Y	0000h
46h	IOUT_OC_WARN_LIMIT	R/W Word	R/W	—	—	—	2	Y	7FFFh
4Ah	IOUT_OC_FAULT_LIMIT	R/W Word	R/W	—	—	—	2	Y	0000h
4Fh	OT_FAULT_LIMIT	R/W Word	—	—	R/W	—	2	Y	7FFFh

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Table 1. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE 0–4 (NOTE 1)	PAGE 5 (NOTE 1)	PAGE 6–11 (NOTE 1)	PAGE 255 (NOTE 1)	NO. OF BYTES	FLASH STORED (NOTE 2)	DEFAULT VALUE (NOTE 2)
51h	OT_WARN_LIMIT	R/W Word	—	—	R/W	—	2	Y	7FFFh
5Eh	POWER_GOOD_ON	R/W Word	R/W	—	—	—	2	Y	0000h
5Fh	POWER_GOOD_OFF	R/W Word	R/W	—	—	—	2	Y	0000h
60h	TON_DELAY	R/W Word	R/W	—	—	—	2	Y	0000h
62h	TON_MAX_FAULT_LIMIT	R/W Word	R/W	—	—	—	2	Y	0000h
64h	TOFF_DELAY	R/W Word	R/W	—	—	—	2	Y	0000h
78h	STATUS_BYTE	Read Byte	R	R	R	R	1	N	00h
79h	STATUS_WORD	Read Word	R	R	R	R	2	N	0000h
7Ah	STATUS_VOUT	Read Byte	R	—	—	—	1	N	00h
7Eh	STATUS_CML	Read Byte	R	R	R	R	1	N	00h
80h	STATUS_MFR_SPECIFIC	Read Byte	R	—	R	—	1	N	00h
81h	STATUS_FANS_1_2	Read Byte	—	R	—	—	1	N	00h
8Bh	READ_VOUT	Read Word	R	—	—	—	2	N	0000h
8Ch	READ_IOUT	Read Word	R	—	—	—	2	N	0000h
8Dh	READ_TEMPERATURE_1	Read Word	—	—	R	—	2	N	0000h
90h	READ_FAN_SPEED_1	Read Word	—	R	—	—	2	N	0000h
98h	PMBUS_REVISION	Read Byte	R	R	R	R	1	FIXED	11h
99h	MFR_ID	Read Byte	R	R	R	R	1	FIXED	4Dh
9Ah	MFR_MODEL	Read Byte	R	R	R	R	1	FIXED	52h
9Bh	MFR_REVISION	Read Word	R	R	R	R	2	FIXED	3031h
9Ch	MFR_LOCATION	Block R/W	R/W	R/W	R/W	R/W	8	Y	(Note 3)
9Dh	MFR_DATE	Block R/W	R/W	R/W	R/W	R/W	8	Y	(Note 3)
9Eh	MFR_SERIAL	Block R/W	R/W	R/W	R/W	R/W	8	Y	(Note 3)
D1h	MFR_MODE	R/W Word	R/W	R/W	R/W	R/W	2	Y	0000h
D4h	MFR_VOUT_PEAK	R/W Word	R/W	—	—	—	2	N	0000h
D5h	MFR_IOUT_PEAK	R/W Word	R/W	—	—	—	2	N	0000h
D6h	MFR_TEMPERATURE_PEAK	R/W Word	—	—	R/W	—	2	N	8000h
D7h	MFR_VOUT_MIN	R/W Word	R/W	—	—	—	2	N	7FFFh
D9h	MFR_FAULT_RESPONSE	R/W Word	R/W	—	—	—	2	Y	0000h
DAh	MFR_FAULT_RETRY	R/W Word	R/W	R/W	R/W	R/W	2	Y	0000h
DCh	MFR_NV_FAULT_LOG	Block Read	R	R	R	R	255	Y	(Note 4)
DDh	MFR_TIME_COUNT	Block Read	R	R	R	R	4	N	(Note 5)
E0h	MFR_MARGIN_CONFIG	R/W Word	R/W	—	—	—	2	Y	0000h
F0h	MFR_TEMP_SENSOR_CONFIG	R/W Word	—	—	R/W	—	2	Y	0000h
F1h	MFR_FAN_CONFIG	R/W Word	—	R/W	—	—	2	Y	0000h
F2h	MFR_FAN_LUT	Block R/W	—	R/W	—	—	32	Y	(Note 6)
F3h	MFR_READ_FAN_PWM	Read Word	—	R	—	—	2	N	0000h
F5h	MFR_FAN_FAULT_LIMIT	R/W Word	—	R/W	—	—	2	Y	0000h
F6h	MFR_FAN_WARN_LIMIT	R/W Word	—	R/W	—	—	2	Y	0000h

Note 1: Common commands are shaded. Access through any page results in the same device response.

Note 2: In the **Flash Stored** column, an "N" indicates that this parameter is not stored in flash memory when the STORE_DEFAULT_ALL command is executed and the value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. A "Y" in the **Flash Stored** column indicates that the currently loaded value in this parameter is stored in flash memory when the STORE_DEFAULT_ALL command is executed and is automatically

Table 1. PMBus Command Codes (continued)

loaded upon power-on reset or when the $\overline{RST}$ pin is asserted and the value shown in the **Default Value** column is the value when shipped from the factory. “FIXED” in the **Flash Stored** column means this value is fixed at the factory and cannot be changed.

Note 3: The factory-set default value for this 8-byte block is 3130313031303130h.
Note 4: The factory-set default value for the complete block of the MFR_NV_FAULT_LOG is FFh.
Note 5: The power-on reset value for this 4-byte block is 00000000h.
Note 6: The factory-set default value for the complete block of the MFR_FAN_LUT is 00h.

Table 2. PMBus/SMBus Serial-Port Address

A1	A0	7-BIT SLAVE ADDRESS
100kΩ to V_{SS}	100kΩ to V_{SS}	1101 010 (D4h)
	100kΩ to V_{DD}	1101 011 (D6h)
100kΩ to V_{DD}	100kΩ to V_{SS}	1101 100 (D8h)
	100kΩ to V_{DD}	1101 101 (DAh)

Address Select

On device power-up, the device samples the A0 and A1 pins to determine the PMBus/SMBus serial-port address.

SMBus/PMBus Operation

The device implements the PMBus command structure using the SMBus format. The structure of the data flow between the host and the slave is shown below for several different types of transactions. All transactions begin with a host sending a command code that is immediately preceded with a 7-bit slave address (R/$\overline{W}$ = 0). Data is sent most significant bit (MSB) first.

SMBus/PMBus Communication Examples

READ WORD FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE LOW	A	DATA BYTE HIGH	NA	P

READ BYTE FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE	NA	P

WRITE WORD FORMAT

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

WRITE BYTE FORMAT

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE	A	P

SEND BYTE FORMAT

1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	P

KEY:
S = START
Sr = REPEATED START
P = STOP
W = WRITE BIT (0)
R = READ BIT (1)
A = ACKNOWLEDGE (0)
NA = NOT ACKNOWLEDGE (1)
SHADED BLOCK = SLAVE TRANSACTION

Group Command

The device supports the group command. With the group command, a host can write different data to multiple devices on the same serial bus with one long continuous data stream. All the devices addressed during this transaction wait for the host to issue a STOP before beginning to respond to the command.

Group Command Write Format

SLAVE ADDRESS, COMMAND BYTE, AND DATA WORD FOR DEVICE 1

1	7	1	1	8	1	8	1	8	1	
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	• • •

SLAVE ADDRESS, COMMAND BYTE, AND DATA BYTE FOR DEVICE 2

1	7	1	1	8	1	8	1	
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE	A	• • •

SLAVE ADDRESS AND SEND BYTE FOR DEVICE 3

1	7	1	1	8	1	
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	• • •

• • •

SLAVE ADDRESS, COMMAND BYTE, AND DATA WORD FOR DEVICE N

1	7	1	1	8	1	8	1	8	1	1
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

KEY:

S = START
Sr = REPEATED START
P = STOP
W = WRITE BIT (0)
A = ACKNOWLEDGE (0)
SHADED BLOCK = SLAVE TRANSACTION

Addressing

The device responds to receiving its fixed slave address by asserting an acknowledge (ACK) on the bus. The device does not respond to a general call address; it only responds when it receives its fixed slave address. The only exception to this operation is if the $\overline{\text{ALERT}}$ output is enabled (ALERT bit = 1 in MFR_MODE) and $\overline{\text{ALERT}}$ has been asserted. When this condition occurs, the device only recognizes the alert response address (0001 100, 18h). See the *ALERT and Alert Response Address (ARA)* section for more details.

ALERT and Alert Response Address (ARA)

If the $\overline{\text{ALERT}}$ output is enabled (ALERT bit = 1 in MFR_MODE), when a fault occurs the device asserts the $\overline{\text{ALERT}}$ signal and then waits for the host to send the alert response address (ARA) as shown in the *Alert Response Address (ARA) Byte Format* section. **While waiting for the ARA, the device does not respond to its fixed slave address.**

When the ARA is received and the device is asserting $\overline{\text{ALERT}}$, the device ACKs it and then attempts to place its fixed slave address on the bus by arbitrating the bus, since another device could also try to respond to the ARA. The rules of arbitration state that the lowest address device wins. If the device wins the arbitration, it deasserts $\overline{\text{ALERT}}$ and begins to respond to its fixed slave address. If the device loses arbitration, it keeps $\overline{\text{ALERT}}$ asserted and waits for the host to once again send the ARA.

Alert Response Address (ARA) Byte Format

1	7	1	1	8	1	1
S	ARA 0001100	R	A	DEVICE SLAVE ADDRESS WITH LSB = 0	NA	P

Host Sends or Reads Too Few Bits

If for any reason the host does not complete writing a full byte or reading a full byte from the device before a START or STOP is received, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends or Reads Too Few Bytes

For each supported command, the device expects a fixed number of bytes to be written or read from the device. If for any reason fewer than the expected number of bytes is written to or read from the device, the device completely ignores the command and takes no action.

Host Sends Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be written to the device. If for any reason more than the expected number of bytes or bits is written to the device, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be read from the device. If for any reason more than the expected number of bytes or bits is read from the device, the device does the following:

1) Sends all ones (FFh) as long as the host keeps acknowledging.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends Improperly Set Read Bit in the Slave Address Byte

If the device receives the R/$\overline{\text{W}}$ bit in the slave address set to one immediately preceding the command code, the device does the following (note this does not apply to ARA):

1) ACKs the address byte.
2) Sends all ones (FFh) as long as the host keeps acknowledging.
3) Sets the CML bit in STATUS_BYTE.
4) Sets the CML bit in STATUS_WORD.
5) Sets the DATA_FAULT bit in STATUS_CML.
6) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Unsupported Command Code Received

If the host sends the device a command code that it does not support, or if the host sends a command code that is not supported by the current PAGE setting, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the COMM_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Invalid Data Received

The device checks the PAGE, OPERATION, and WRITE_PROTECT command codes for valid data. If the host writes a data value that is invalid, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads from a Write-Only Command

When a read request is issued to a write-only command (CLEAR_FAULTS, STORE_DEFAULT_ALL, RESTORE_DEFAULT_ALL), the device does the following:

1) ACKs the address byte.
2) Ignores the command.
3) Sends all ones (FFh) as long as the host keeps acknowledging.
4) Sets the CML bit in STATUS_BYTE.
5) Sets the CML bit in STATUS_WORD.
6) Sets the DATA_FAULT bit in STATUS_CML.
7) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Writes to a Read-Only Command

When a write request is issued to a read-only command, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_BYTE.
3) Sets the CML bit in STATUS_WORD.
4) Sets the COMM_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

SMBus Timeout

If during an active SMBus communication sequence the SCL signal is held low for greater than the timeout duration (nominally 30ms), the device terminates the sequence and resets the serial bus. It takes no other action. No status bits are set.

PMBus Operation

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. A PMBus 1.1-compliant device uses the SMBus version 1.1 for transport protocol and responds to the SMBus slave address. In this data sheet, the term SMBus is used to refer to the electrical characteristics of the PMBus communication using the SMBus physical layer. The term PMBus is used to refer to the PMBus command protocol. The device employs a number of standard SMBus protocols such as Write Word, Read Word, Write Byte, Read Byte, Send Byte, and so on to program output voltage and warning/faults thresholds, read monitored data, and provide access to all manufacturer-specific commands.

The device supports the group command. The group command is used to send commands to more than one PMBus device. It is not required that all the devices receive the same command. However, no more than one command can be sent to any one device in one group command packet. The group command must not be used with commands that require receiving devices to respond with data, such as the STATUS_BYTE command. When the device receives a command through this protocol, it immediately begins execution of the received command after detecting the STOP condition.

The device supports the PAGE command and uses it to select which individual channel to access. When a data word is transmitted, the lower order byte is sent first and the higher order byte is sent last. Within any byte, the most significant bit (MSB) is sent first and the least significant bit (LSB) is sent last.

PMBus Protocol Support

The device supports a subset of the commands defined in the *PMBus™ Power System Management Protocol Specification Part II - Command Language, Revision 1.1*. For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at www.PMBus.org. The supported PMBus commands and the corresponding device behavior are described in this document. All data values are represented in DIRECT format, unless otherwise stated. Whenever the PMBus specification refers to the PMBus device, it is referring to the MAX34441 operating in conjunction with a power supply or fan. While the command can call for turning on or turning off the PMBus device, the MAX34441 always remains on to continue communicating with the PMBus master, and the MAX34441 transfers the command to the power supply accordingly.

Data Format

Voltage data for commanding or reading the output voltage or related parameters (such as the overvoltage threshold) is presented in DIRECT format. DIRECT format data is a 2-byte, two's complement binary value. DIRECT format data can be used with any command that sends or reads a parametric value. The DIRECT format uses an equation and defined coefficients to calculate the desired values. Table 3 shows the coefficients used by the device.

PMBus 5-Channel Power-Supply Manager and Intelligent Fan Controller

Table 3. PMBus Command Code Coefficients

PARAMETER	COMMANDS	UNITS	RESOLUTION	MAX	m	b	R
Voltage	VOUT_MARGIN_HIGH VOUT_MARGIN_LOW VOUT_OV_FAULT_LIMIT VOUT_OV_WARN_LIMIT VOUT_UV_WARN_LIMIT VOUT_UV_FAULT_LIMIT POWER_GOOD_ON POWER_GOOD_OFF READ_VOUT MFR_VOUT_PEAK MFR_VOUT_MIN	mV	1	32,767	1	0	0
Voltage Scaling	VOUT_SCALE_MONITOR	—	1/32,767	1	32,767	0	0
Current	IOUT_OC_WARN_LIMIT IOUT_OC_FAULT_LIMIT READ_IOUT MFR_IOUT_PEAK	mA	1	32,767	1	0	0
Current Scaling	IOUT_CAL_GAIN	mΩ	0.1	3276.7	1	0	1
Temperature	OT_FAULT_LIMIT OT_WARN_LIMIT READ_TEMPERATURE_1 MFR_TEMPERATURE_PEAK	°C	0.01	327.67	1	0	2
Fan Speed	READ_FAN_SPEED_1 FAN_COMMAND_1 MFR_FAN_FAULT_LIMIT MFR_FAN_WARN_LIMIT	RPM	1	32,767	1	0	0
	FAN_COMMAND_1 MFR_READ_FAN_PWM MFR_FAN_FAULT_LIMIT MFR_FAN_WARN_LIMIT	%	0.01	327.67	1	0	2
Timing	TON_DELAY TON_MAX_FAULT_LIMIT TOFF_DELAY MFR_FAULT_RETRY	ms	1	32,767	1	0	0

Interpreting Received DIRECT Format Values

The host system uses the following equation to convert the value received from the PMBus device—in this case, the MAX34441—into a reading of volts, degrees Celsius, or other units as appropriate:

$$X = (1/m) \times (Y \times 10^{-R} - b)$$

where X is the calculated, real world value in the appropriate units (V, °C, etc.); m is the slope coefficient; Y is the 2-byte, two's complement integer received from the PMBus device; b is the offset; and R is the exponent.

Sending a DIRECT Format Value

To send a value, the host must use the below equation to solve for Y:

$$Y = (mX + b) \times 10^{R}$$

where Y is the 2-byte, two's complement integer to be sent to the unit; m is the slope coefficient; X is the real world value, in units such as volts, to be converted for transmission; b is the offset; and R is the exponent.

The following example demonstrates how the host can send and retrieve values from the device. Table 4 shows the coefficients used in the following parameters.

Table 4. Coefficients for DIRECT Format Value

COMMAND CODE	COMMAND NAME	m	b	R
25h	VOUT_MARGIN_HIGH	1	0	0
8Bh	READ_VOUT	1	0	0

If a host wants to set the device to change the power-supply output voltage to 3.465V (or 3465mV), the corresponding VOUT_MARGIN_HIGH value is:

$$Y = (1 \times 3465 + 0) \times 10^{0} = 3465 \text{ (decimal)} = \text{0D89h (hex)}$$

Conversely, if the host received a value of 0D89h on a READ_VOUT command, this is equivalent to:

$$X = (1/1) \times (\text{0D89h} \times 10^{-(-0)} - 0) = 3465\text{mV} = 3.465\text{V}$$

Power supplies and power converters generally have no way of knowing how their outputs are connected to ground. Within the power supply, all output voltages are most commonly treated as positive. Accordingly, all output voltages and output voltage-related parameters of PMBus devices are commanded and reported as positive values. It is up to the system to know that a particular output is negative if that is of interest to the system. All output-voltage-related commands use 2 data bytes.

Fault Management and Reporting

For reporting faults/warnings to the host on a real-time basis, the device asserts the open-drain ALERT pin (if enabled in MFR_MODE) and sets the appropriate bit in the various status registers. On recognition of the ALERT assertion, the host or system manager is expected to poll the I^2C bus to determine the device asserting ALERT. The host sends the SMBus ARA (0001 100). The device ACKs the SMBus ARA, transmits its slave address, and deasserts ALERT. The system controller then communicates with PMBus commands to retrieve the fault/warning status information from the device.

See the individual command sections for more details. Faults and warnings that are latched in the status registers are cleared when any one of the following conditions occurs:

- A CLEAR_FAULTS command is received.
- The RST pin is toggled.
- Bias power to the device is removed and then reapplied.

One or more latched-off power supplies is only restarted when one of the following occurs:

- The output is commanded through the CONTROL pin, the OPERATION command, to turn off and then turn back on.
- The RST pin is toggled.
- Bias power to the device is removed and then reapplied.

A power supply is not allowed to turn on if any faults the supply responds to are detected. Only after the faults clear is the power supply allowed to turn on. When global supplies are being sequenced on, a fault on any of the supplies keeps all supplies from being turned on.

A system-wide power-up (OPERATION command is received to turn the supplies on when PAGE is 255 or the CONTROL pin is toggled to turn on the supplies) allows all enabled power supplies to power-up. If any faults are detected once the supplies start to turn on, the response of MFR_FAULT_RESPONSE is performed.

The device responds to fault conditions according to the manufacturer fault response command (MFR_FAULT_RESPONSE). This command byte determines how the device should respond to each

Table 5. Device Parametric Monitoring States

PARAMETER	REQUIRED CONDITIONS FOR ACTIVE MONITORING	ACTION DURING A FAULT
Overvoltage	Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 0000h)	Continue monitoring
Undervoltage	• Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 0000h) • PSEN output is active • Channel's VOUT must have exceeded VOUT_UV_FAULT during channel power-up	Stop monitoring while the power supply is off
Overcurrent	• Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 0000h) • Current monitoring enabled (IOUT_OC_FAULT_LIMIT ≠ 0000h)	Continue monitoring
Power-Up Time	Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 0000h)	Monitor only during power-on
Overtemperature	Temp sensor enabled (ENABLE in MFR_TEMP_SENSOR_CONFIG = 1)	Continue monitoring
Fan Speed	Fan enabled (bit 7 in FAN_CONFIG_1_2 = 1)	Continue monitoring

particular fault. Table 5 illustrates the required conditions and fault actions for specific parameters.

System Watchdog Timer

The device uses an internal watchdog timer that is internally reset every 5ms. In the event that the device is locked up and this watchdog reset does not occur after 500ms, the device automatically resets. After the reset occurs, the device reloads all configuration values that were stored to flash and begins normal operation. After the reset, the device also does the following:

1) Sets the NONE OF THE ABOVE bit in STATUS_BYTE.
2) Sets the NONE OF THE ABOVE and MFR bits in STATUS_WORD.
3) Sets the WATCHDOG bit in STATUS_MFR_SPECIFIC.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

Temperature Sensor Operation

The device can monitor up to six different temperature sensors. It can monitor up to four remote I²C-based temperature sensors plus a remote diode and its own internal temperature sensor. Each of the enabled temperature sensors is measured once a second. The remote diode and internal temperature sensors are averaged four times to reduce the affect of noise. Each time the device attempts to read a temperature sensor it checks for faults. For the remote diode, a fault is defined as reading greater than +160°C or less than -60°C. For the internal temperature sensor, a fault is defined as reading greater than +130°C or less than -60°C. For the I²C temperature sensors, a fault is defined as a communication access failure. Temperature sensor faults are reported by setting the temperature reading to 7FFFh. A temperature sensor fault results in the setting of the TEMPERATURE bit in STATUS_BYTE and STATUS_WORD and $\overline{\text{ALERT}}$ is asserted (if enabled in MFR_MODE). No bits are set in STATUS_MFR_SPECIFIC.

The temperatures do not have to be used to control the fan speed. They can be enabled and used for temperature monitoring only. Reading disabled temperature sensors returns a fixed value of 0000h.

The remote diode temperature sensor can support either npn or pnp transistors. The device automatically cancels the series resistance that can affect remote diodes that are located far from the device.

The device can control up to four DS75LV digital temperature sensors. The A0, A1, and A2 pins on the DS75LV should be configured as shown in Table 6. The thermostat function on the DS75LV is not used and thus the O.S. output should be left open circuit.

Table 6. DS75LV Address Pin Configurations

PAGE	MAX34441 I²C TEMP SENSOR	DS75LV ADDRESS PIN CONFIGURATION		
		A2	A1	A0
7	TEMP SENSOR I²C 0	0	0	0
8	TEMP SENSOR I²C 1	0	0	1
9	TEMP SENSOR I²C 2	0	1	0
10	TEMP SENSOR I²C 3	0	1	1

Fan Control Operation

Fan control has four operational modes. The mode is determined by the combination of FAN_COMMAND_1 and bit 6 of FAN_CONFIG_1_2 (see Table 7). Fan control can be disabled by setting bit 7 in FAN_CONFIG_1_2 to zero.

Dual Fan Applications

In dual fan applications operating in RPM mode, the tachometer selected when TACHSEL = 0 is close-loop-controlled to the target RPM. Once PWM ramping is complete, TACHSEL toggles between the two tachometers every 500ms for monitoring purposes. The slower of the two tachometer signals is reported by READ_FAN_SPEED_1 and is used as a comparison for fan faults and warning. In dual fan applications operating in PWM mode, TACHSEL always switches every 500ms. If one of the two tachometer signals operate at a slower speed, it is recommended that the slower tachometer be presented to the TACH input when TACHSEL = 0.

Automatic Fan Control Operation

In the automatic mode, the fan is controlled in a closed loop based on the controlling temperature (the highest postnormalized temperature reading) and the associated fan control PWM duty cycle (in %) or fan speed (in RPM). These parameters are assigned in the fan lookup table (LUT). See the MFR_FAN_LUT description for configuration details. When a controlling temperature exceeds the temperature level programmed in the LUT, the device outputs a PWM duty cycle or adjusts the fan speed, associated with that temperature. See Figure 1 for an example.

Table 7. Fan Control Operation Modes

FAN CONTROL MODE	FAN OPERATIONAL DETAILS	BIT 6 OF FAN_CONFIG_1_2	VALUE IN FAN_COMMAND_1
Manual PWM	External host controls the fan speed by directly setting the fan PWM duty cycle values.	0	0000h to 7FFFh
Manual RPM	External host controls the fan speed by setting target fan speed values. The device reads the actual fan speed, and close loop adjusts the output fan PWM to match the target fan speed.	1	0000h to 7FFFh
Automatic PWM	The device sets the output PWM based on the fan LUT that maps the temperature sensor readings to the required fan PWM duty-cycle values.	0	8000h to FFFFh
Automatic RPM	The device reads the actual fan speed and close loop adjusts the output fan PWM to match the target fan speed based on the fan LUT that maps the temperature sensor readings to the required fan speed.	1	8000h to FFFFh

Note: *The RPM modes should only be used with fans that provide a tachometer output.*

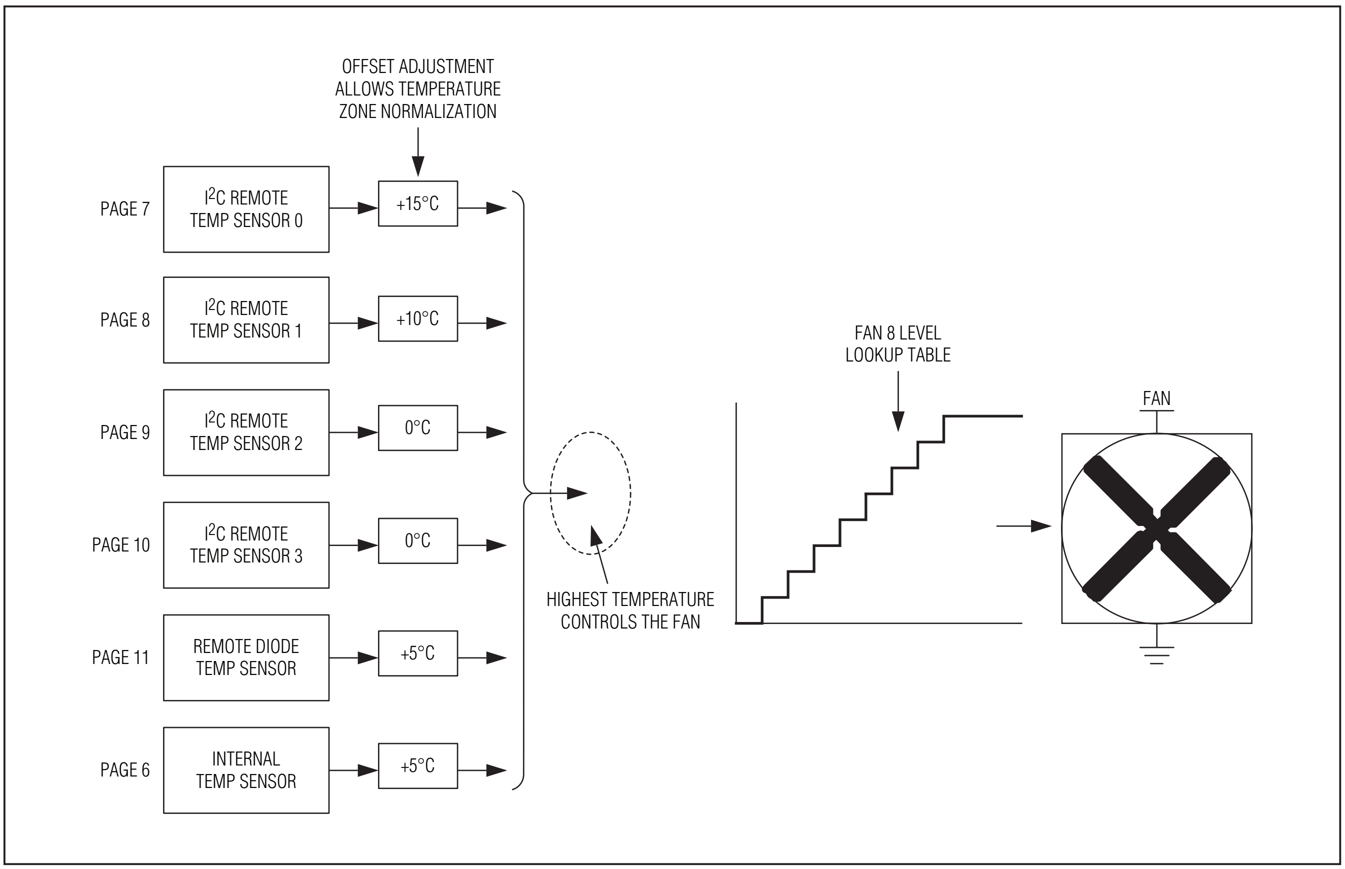


Figure 1. Automatic Fan Control

One or all of the six available temperature sensors can be used to control the fan speed. Each temperature sensor has an offset adjustment that allows monitoring specific temperature zones with different thermal characteristics. In Figure 1, I^2C temperature sensor 0 is monitoring a zone that is 15°C more sensitive than the zone that the I^2C temperature sensor 3 is measuring. To keep the audible noise and fan power consumption as low as possible, the device allows each temperature sensor to have a temperature offset added. This allows temperature zones with different thermal profiles to control the fan at the lowest possible speed to maintain the required temperature.

If no temperature sensors are assigned to control the fan, the output fan PWM signal is ramped to 100% duty cycle.

In Figure 2, at temperature sample 1, the required fan speed is at the level associated with temperature level 2 and since temperature sample 1 is above temperature level 3, the fan PWM duty cycle needs to be increased to increase the fan speed. The device increases the fan PWM duty cycle at a rate controlled by the RAMP bits in the MFR_FAN_CONFIG command code. If the PWM duty cycle has not reached the target value before the temperature sample detects that a new PWM target value is needed, the device stops moving toward the old target and starts moving to the new target according to the programmed ramp rate.

At temperature sample 2, the temperature has increased to greater than temperature level 4 so again the PWM duty cycle must be increased. At temperature sample 3, the temperature has dropped but not below the thermal hysteresis level (which is set by the HYS bits in the MFR_FAN_CONFIG command code), so the fan speed remains at level 4. At temperature sample 4, the temperature has dropped below the hysteresis point so the PWM duty cycle is decreased.

Pulse Stretching

In some 3-wire fan applications, when the supply power is interrupted to control fan speed, the tachometer signal is not available. Some fan controllers periodically stretch the PWM signal to allow the tachometer to be accurately detected. Pulse stretching can create audible noise. **This device does not implement pulse stretching.** Hence, the RPM fan modes that require a reliable tachometer signal to be available at all times should not be used in applications that switch power to the fan to control the speed of the fan. For example, low-side switching of a 3-wire fan should not use either of the RPM fan modes.

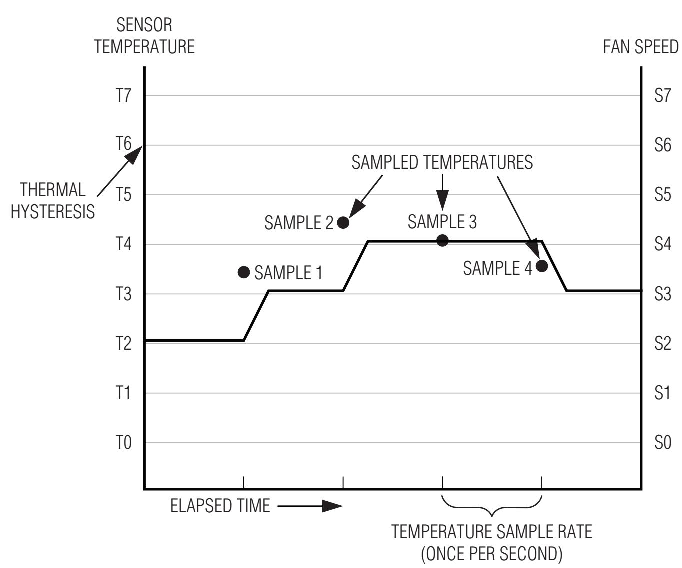


Figure 2. Fan Speed Example

Fan Spin-Up

Figure 3 shows the fan spin-up process. When the fan is spinning up, the number of revolutions is checked every 200ms for up to 2s. When the number of cumulated revolutions is greater than or equal to the spin-up relaxation criteria, the fan passes spin-up. If the fan has a locked rotor output, fan spin-up passes when the locked rotor signal is no longer asserted.

When spin-up passes, the device forces the fan PWM with a 40% duty cycle. The 40% duty cycle is maintained until the next temperature conversion is completed, which occurs once a second. After the temperature conversion, the device enters either manual mode operation or automatic operation using MFR_FAN_LUT.

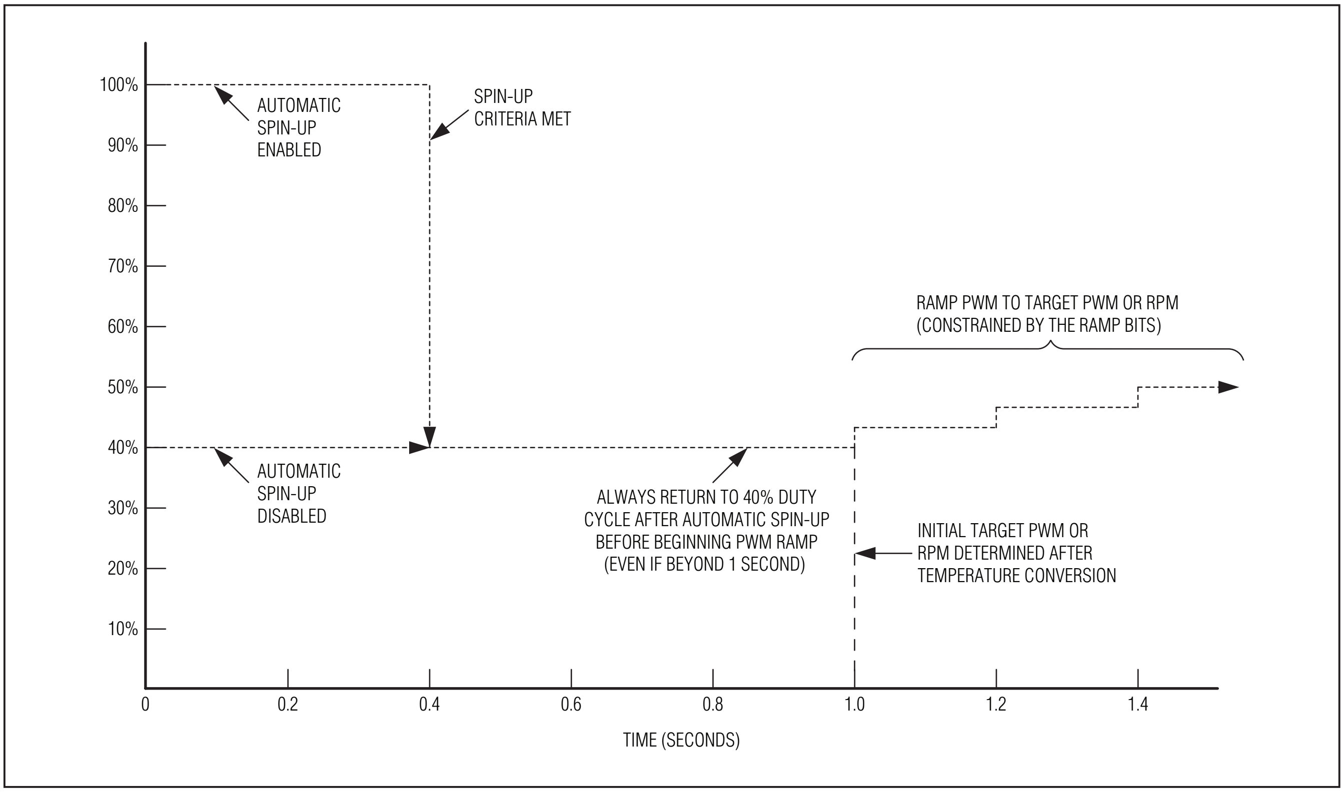


Figure 3. Fan Spin-Up