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MAX34451

PMBus 16-Channel V/I Monitor and 12-Channel Sequencer/Marginer

General Description

The MAX34451 is a power-supply system manager that is capable of monitoring up to 16 different voltage rails or currents and is also capable of sequencing and margining up to 12 power supplies. The system manager monitors the power-supply output voltages and currents and constantly checks them for user programmable over and under threshold limits. If a fault is detected, the device automatically shuts down the system in an orderly fashion. The device can sequence the supplies in any order at both power-up and power-down. The device has the ability to close-loop margin the power-supply output voltages up or down to a user-programmable level. The device contains an internal temperature sensor and can support up to four external remote temperature sensors. Once configured, the device can operate autonomously without any host intervention.

Applications

- Network Switches/Routers
- Base Stations
- Servers
- Smart Grid Network Systems

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX34451ETN+	-40°C to +85°C	56 TQFN-EP*
MAX34451ETN+T	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

***Typical Operating Circuit* apears at end of data sheet.**

Benefits and Features

- Integration Enables Management of Multiple Power Supplies to Maximize System Performance
  - 16 Channels of Voltage or Current Monitoring
  - 12 Channels of Sequencing and Margining (8 PWM, 4 External Current DACs (1 x DS4424), and Sequencing
  - Expandable Channel Operation with Parallel Devices
  - Remote Ground Sensing Improves Measurement Accuracy
  - Programmable Up and Down Time-Based or Event-Based Sequencing
  - Dual Sequencing Loops
  - Configurable Combinatorial Logic Supporting Up to 16 GPIs and 20 GPOs
  - Automatic Closed-Loop Margining
  - No External Clocking Required
  - PMBus™-Compliant Command Interface
- Fast, Reliable Control and Fault Detection Improves System Reliability
  - Fast Minimum/Maximum Threshold Excursion Detection
  - Supports Up to 5 Temperature Sensors (1 Internal and 4 Remote)
  - Fault Detection on All Temperature Sensors
  - Reports Peak, Minimum, and Average Levels for a Number of Parameters
  - Programmable Alarm Outputs
  - On-Board Nonvolatile Black Box Fault Logging and Default Configuration Setting
- I2C-/SMBus-Compatible Serial Bus with Bus Time-Out Function Simplifies Additional Temperature Sensors and DACs to the MAX34451
- +3.0V to +3.6V Supply Voltage

PMBus is a trademark of SMIF, Inc.

19-6642; Rev 2; 5/15

maxim integrated™

Absolute Maximum Ratings

V_{DD} and V_{DDA} to V_{SS} .....-0.3V to +4.0V
RSG0 and RSG1 to V_{SS}.....-0.3V to +0.3V
All Other Pins Except REG18
Relative to V_{SS}.....-0.3V to (V_{DD} + 0.3V)*
REG18 to V_{SS}.....-0.3V to +2.0V

**Subject to not exceeding +4.0V.*

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C).....2222.2mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage Range	V_{DD}	(Note 1)	3.0		3.6	V
Input Logic 1 (Except I²C and GPIn Pins)	V_{IH1}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic 0 (Except I²C and GPIn Pins)	V_{IL1}		-0.3		+0.3 x V_{DD}	V
Input Logic 1: SCL, SDA, MSCL, MSDA	V_{IH2}		2.1		V_{DD} + 0.3	V
Input Logic 0: SCL, SDA, MSCL, MSDA	V_{IL2}		-0.3		+0.8	V
Input Logic 1 (GPIn Pins)	V_{IH3}	Minimum pulse width 5ms	1.5		V_{DD} + 0.3	V
Input Logic 0 (GPIn Pins)	V_{IL3}	Minimum pulse width 5ms	-0.3		+1.0	V
Source Impedance to RSn		ADC_TIME[1:0] = 00			1	kΩ
		ADC_TIME[1:0] = 01			5	
		ADC_TIME[1:0] = 10			10	
		ADC_TIME[1:0] = 11			20	
V_{DD} Rise Time		From 0V to 3.0V			4	ms
V_{DD} Source Impedance					10	Ω

ELECTRICAL CHARACTERISTICS

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Current	I_{CPU}	(Note 3)		12		mA
	$I_{PROGRAM}$			18		
System Clock Error	$f_{ERR:MOSC}$	+25°C < T_A < +85°C	-3		+3	%
		-40°C < T_A < +25°C	-4		+4	
Output Logic-Low (Except I²C Pins)	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-High (Except I²C Pins)	V_{OH1}	I_{OH} = -2mA (Note 1)	V_{DD} - 0.5			V
Output Logic-Low: SCL, SDA, MSCL, MSDA	V_{OL2}	I_{OL} = 4mA (Note 1)			0.4	V
SCL, SDA, MSCL, MSDA Leakage	IL_{I2C}	V_{DD} = 0V or unconnected			±5	µA
CONTROL0 Threshold				2.048		V
CONTROL0 Hysteresis				50		mV
ADC						
ADC Bit Resolution				12		Bits
ADC Conversion Time		ADC_TIME[1:0] = 00		1000		ns
ADC Full Scale	V_{FS}	T_A = 0°C to +85°C	2.032	2.048	2.064	V
ADC Measurement Resolution	V_{LSB}			500		µV
RSn Input Capacitance	C_{RS}			15		pF
RSn Input Leakage	IL_{RS}	0V < V_{RSn} < 2.1V		±0.25		µA
ADC Integral Nonlinearity	INL			±1		LSB
ADC Differential Nonlinearity	DNL			±1		LSB
TEMPERATURE SENSOR						
Internal Temperature-Measurement Error		T_A = -40°C to +85°C		±2		°C
FLASH						
Flash Endurance	N_{FLASH}	Note 3	20,000			Write Cycles
Data Retention		T_A = +50°C (Note 4)	100			Years
STORE_DEFAULT_ALL, MFR_STORE_ALL Write Time				80		ms
RESTORE_DEFAULT_ALL		With MFR_STORE_SINGLE data		105		ms
RESTORE_DEFAULT_ALL or MFR_RESTORE_ALL		Without MFR_STORE_SINGLE data		500		µs
MFR_STORE_SINGLE Write Time				310		µs
MFR_NV_FAULT_LOG Write Time		Writing 1 fault log		11		ms
MFR_NV_FAULT_LOG Delete Time		Deleting all fault logs		200		ms
MFR_NV_FAULT_LOG Overwrite Time				40		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING OPERATING CHARACTERISTICS						
Round-Robin Voltage and Current Sample Rate		Threshold excursion (Note 5)		64		µs
		Data collection		5		ms
Temperature Sample Rate				1000		ms
Device Startup Time		With MFR_STORE_SINGLE data		170		ms
		Without MFR_STORE_SINGLE data		90		
PWM Frequency		PWM power-supply margining		312.5		kHz
PWM Resolution		PWM power-supply margining		8		Bits

Note 1: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and chacterization.

Note 3: This does not include pin input/output currents.

Note 4: Guaranteed by design.

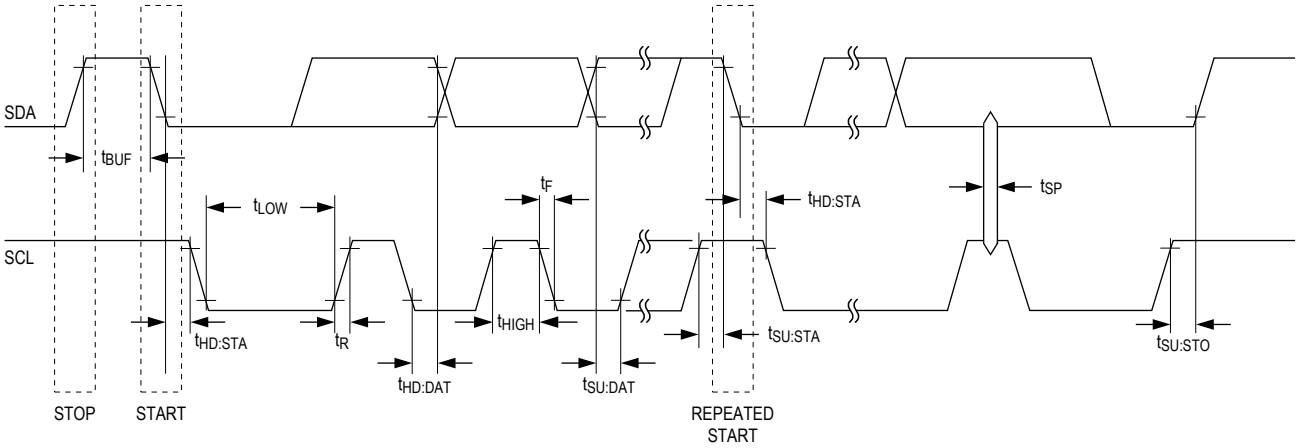
Note 5: The round-robin threshold excursion rate can be changed with the ADC_AVERAGE and ADC_TIME bits in MFR_MODE from 16µs (no averaging and 1µs conversion) to 1024µs (8x averaging and 8µs conversion).

I²C/SMBus INTERFACE ELECTRICAL SPECIFICATIONS

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		400	kHz
MSCL Clock Frequency	f_{MSCL}			100		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Timeout	t_{TO}		25	27	35	ms

I²C/SMBus Timing

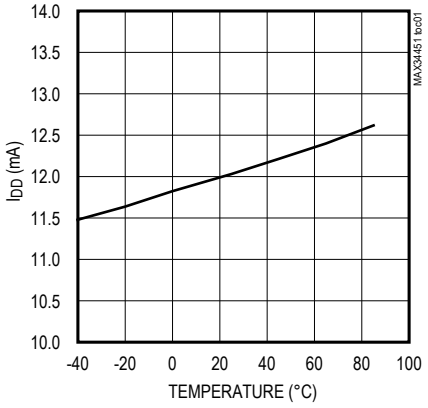


NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

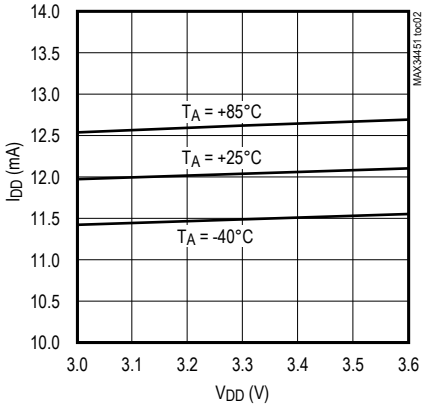
Typical Operating Characteristics

(V_{DD} = 3.3V and T_A = +25°C, without MFR_STORE_SINGLE data, unless otherwise noted.)

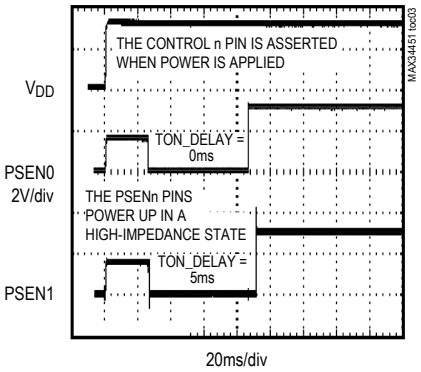
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



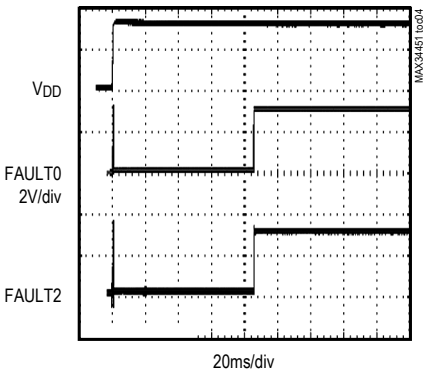
PSENn OUTPUTS DURING POWER-UP



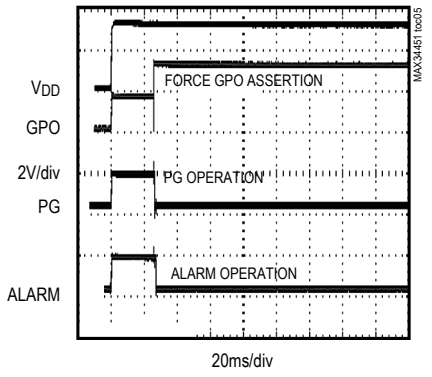
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V and T_A = +25°C, without MFR_STORE_SINGLE data, unless otherwise noted.)

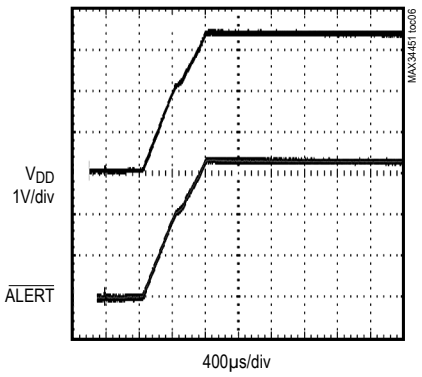
FAULT PINS DURING POWER-UP



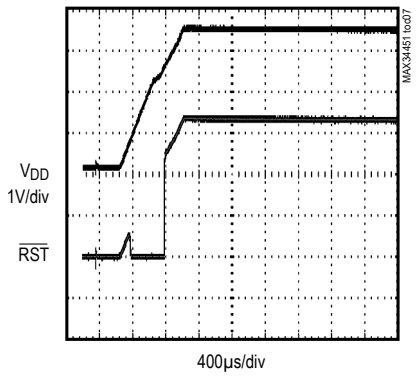
GPOn OUTPUT PINS CONFIGURED DURING POWER-UP (ALL PINS CONFIGURED TO BE PUSH-PULL ACTIVE-HIGH)



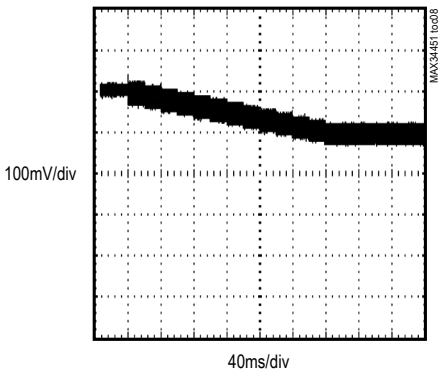
ALERT PIN DURING POWER-UP



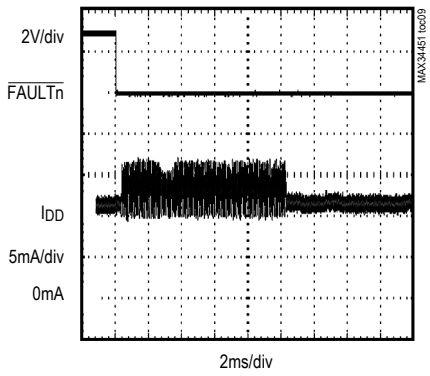
RST PIN DURING POWER-UP



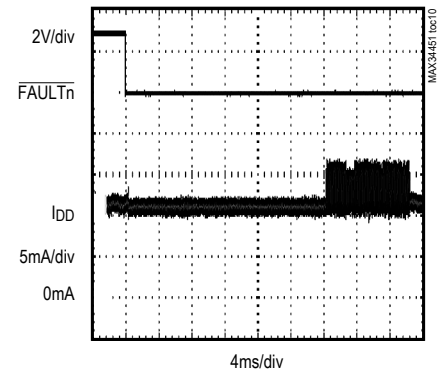
FILTERED MARGINING VOLTAGE vs. TIME



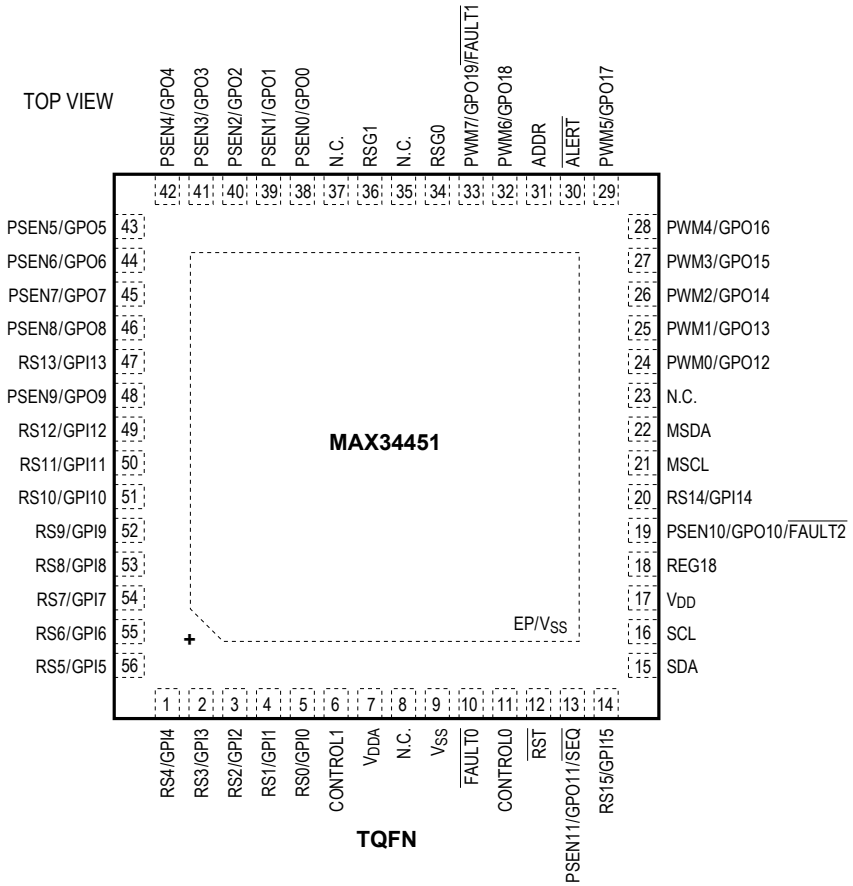
IDD vs. TIME DURING A NONVOLATILE LOG WRITE



IDD vs. TIME DURING A NONVOLATILE LOG WRITE WITH OVERWRITE ENABLED



Pin Configuration



Pin Description

PIN*	NAME	TYPE**	FUNCTION
1	RS4	AI	ADC Voltage-Sense Input 4. Connect to V_{SS} if unused.
	GPI4	AI	General-Purpose Input 4. Connect to V_{SS} if unused.
2	RS3	AI	ADC Voltage-Sense Input 3. Connect to V_{SS} if unused.
	GPI3	AI	General-Purpose Input 3. Connect to V_{SS} if unused.
3	RS2	AI	ADC Voltage-Sense Input 2. Connect to V_{SS} if unused.
	GPI2	AI	General-Purpose Input 2. Connect to V_{SS} if unused.
4	RS1	AI	ADC Voltage-Sense Input 1. Connect to V_{SS} if unused.
	GPI1	AI	General-Purpose Input 1. Connect to V_{SS} if unused.
5	RS0	AI	ADC Voltage-Sense Input 0. Connect to V_{SS} if unused.
	GPI0	AI	General-Purpose Input 0. Connect to V_{SS} if unused.
6	CONTROL1	DI	Power-Supply Master On/Off Control Input 1. Active low or active high based on ON_OFF_CONFIG command. Connect to V_{SS} if unused.

Pin Description (continued)

PIN*	NAME	TYPE**	FUNCTION
7	V_{DDA}	Power	Analog Supply Voltage. Bypass V_{DDA} to V_{SS} with 0.1µF. Connect to V_{DD}.
8	N.C.	—	No Connection. Do not connect any signal to this pin.
9	V_{SS}	Power	Ground Reference. Must be connected to EP (exposed pad).
10	$\overline{FAULT0}$	DIO	Fault Input/Output 0. Open-drain, active-low I/O. See the *Expanded Pin Description* section for more details.
11	CONTROL0	AI	Power-Supply Master On/Off Control Input 0. Active low or active high based on ON_OFF_CONFIG command. Connect to V_{SS} if unused.
12	$\overline{RST}$	DIO	Active-Low Reset Input/Output. Contains an internal pullup.
13	PSEN11	DO	Power-Supply Enable 11. See the *Expanded Pin Description* section for more details.
	GPO11	DO	General-Purpose Output 11
	$\overline{SEQ}$	DIO	Sequencing Input/Output. Open-drain, active-low I/O. This pin is used as a handshake signal to coordinate sequencing in systems using multiple devices.
14	RS15	AI	ADC Voltage-Sense Input 15. Connect to V_{SS} if unused.
	GPI15	AI	General-Purpose Input 15. Connect to V_{SS} if unused.
15	SDA	DIO	I^2C/SMBus-Compatible Input/Output. Open-drain output.
16	SCL	DIO	I^2C/SMBus-Compatible Clock Input/Output. Open-drain output.
17	V_{DD}	Power	Digital Supply Voltage. Bypass V_{DD} to V_{SS} with 0.1µF. Connect to V_{DDA}.
18	REG18	Power	Regulator for Digital Circuitry. Bypass to V_{SS} with 1µF and 10nF (500mΩ maximum ESR). Do not connect other circuitry to this pin.
19	PSEN10	DO	Power-Supply Enable 10. See the *Expanded Pin Description* section for more details.
	GPO10	DO	General-Purpose Output 10
	$\overline{FAULT2}$	DIO	Fault Input/Output 2. Open-drain, active-low I/O. See the *Expanded Pin Description* section for more details.
20	RS14	AI	ADC Voltage-Sense Input 14. Connect to V_{SS} if unused.
	GPI14	AI	General-Purpose Input 14. Connect to V_{SS} if unused.
21	MSCL	DIO	Master I^2C Clock Input/Output. Open-drain output.
22	MSDA	DIO	Master I^2C Data Input/Output. Open-drain output.
23	N.C.	—	No Internal Connection
24	PWM0	DO	PWM Margin Output 0. See the *Expanded Pin Description* section for more details.
	GPO12	DO	General-Purpose Output 12
25	PWM1	DO	PWM Margin Output 1. See the *Expanded Pin Description* section for more details.
	GPO13	DO	General-Purpose Output 13
26	PWM2	DO	PWM Margin Output 2. See the *Expanded Pin Description* section for more details.
	GPO14	DO	General-Purpose Output 14
27	PWM3	DO	PWM Margin Output 3. See the *Expanded Pin Description* section for more details.
	GPO15	DO	General-Purpose Output 15
28	PWM4	DO	PWM Margin Output 4. See the *Expanded Pin Description* section for more details.
	GPO16	DO	General-Purpose Output 16

Pin Description (continued)

PIN*	NAME	TYPE**	FUNCTION
29	PWM5	DO	PWM Margin Output 5. See the *Expanded Pin Description* section for more details.
	GPO17	DO	General-Purpose Output 17
30	$\overline{\text{ALERT}}$	DO	Alert Output. Open-drain, active-low output.
31	ADDR	DI	SMBus Slave Address Select. This pin is sampled on device power-up to determine the SMBus address. See the *PMBus/SMBus Address Select* section for details on how to strap this pin to select the proper slave address.
32	PWM6	DO	PWM Margin Output 6. See the *Expanded Pin Description* section for more details.
	GPO18	DO	General-Purpose Output 18
33	PWM7	DO	PWM Margin Output 7. See the *Expanded Pin Description* section for more details.
	GPO19	DO	General-Purpose Output 19
	$\overline{\text{FAULT1}}$	DIO	Fault Input/Output 1. Open-drain, active-low I/O. See the *Expanded Pin Description* section for more details.
34	RSG0	AI	Remote-Sense Ground for RS0/GPI0 to RS3/GPI3 and RS12/GPI12 to RS15/GPI15.
35	N.C.	—	No Internal Connection
36	RSG1	AI	Remote-Sense Ground for RS4/GPI4 to RS11/GPI11.
37	N.C.	—	No Internal Connection
38	PSEN0	DO	Power-Supply Enable 0. See the *Expanded Pin Description* section for more details.
	GPO0	DO	General-Purpose Output 0
39	PSEN1	DO	Power-Supply Enable 1. See the *Expanded Pin Description* section for more details.
	GPO1	DO	General-Purpose Output 1
40	PSEN2	DO	Power-Supply Enable 2. See the *Expanded Pin Description* section for more details.
	GPO2	DO	General-Purpose Output 2
41	PSEN3	DO	Power-Supply Enable 3. See the *Expanded Pin Description* section for more details.
	GPO3	DO	General-Purpose Output 3
42	PSEN4	DO	Power-Supply Enable 4. See the *Expanded Pin Description* section for more details.
	GPO4	DO	General-Purpose Output 4
43	PSEN5	DO	Power-Supply Enable 5. See the *Expanded Pin Description* section for more details.
	GPO5	DO	General-Purpose Output 5
44	PSEN6	DO	Power-Supply Enable 6. See the *Expanded Pin Description* section for more details.
	GPO6	DO	General-Purpose Output 6
45	PSEN7	DO	Power-Supply Enable 7. See the *Expanded Pin Description* section for more details.
	GPO7	DO	General-Purpose Output 7
46	PSEN8	DO	Power-Supply Enable 8. See the *Expanded Pin Description* section for more details.
	GPO8	DO	General-Purpose Output 8
47	RS13	AI	ADC Voltage-Sense Input 13. Connect to V_{SS} if unused.
	GPI13	AI	General-Purpose Input 13. Connect to V_{SS} if unused.
48	PSEN9	DO	Power-Supply Enable 9. See the *Expanded Pin Description* section for more details.
	GPO9	DO	General-Purpose Output 9

Pin Description (continued)

PIN*	NAME	TYPE**	FUNCTION
49	RS12	AI	ADC Voltage-Sense Input 12. Connect to V_{SS} if unused.
	GPI12	AI	General-Purpose Input 12. Connect to V_{SS} if unused.
50	RS11	AI	ADC Voltage-Sense Input 11. Connect to V_{SS} if unused.
	GPI11	AI	General-Purpose Input 11. Connect to V_{SS} if unused.
51	RS10	AI	ADC Voltage-Sense Input 10. Connect to V_{SS} if unused.
	GPI10	AI	General-Purpose Input 10. Connect to V_{SS} if unused.
52	RS9	AI	ADC Voltage-Sense Input 9. Connect to V_{SS} if unused.
	GPI9	AI	General-Purpose Input 9. Connect to V_{SS} if unused.
53	RS8	AI	ADC Voltage-Sense Input 8. Connect to V_{SS} if unused.
	GPI8	AI	General-Purpose Input 8. Connect to V_{SS} if unused.
54	RS7	AI	ADC Voltage-Sense Input 7. Connect to V_{SS} if unused.
	GPI7	AI	General-Purpose Input 7. Connect to V_{SS} if unused.
55	RS6	AI	ADC Voltage-Sense Input 6. Connect to V_{SS} if unused.
	GPI6	AI	General-Purpose Input 6. Connect to V_{SS} if unused.
56	RS5	AI	ADC Voltage-Sense Input 5. Connect to V_{SS} if unused.
	GPI5	AI	General-Purpose Input 5. Connect to V_{SS} if unused.
—	EP/V_{SS}	Power	Exposed Pad (Bottom Side of Package). Must be connected to local ground. The exposed pad is the ground reference (V_{SS}) for the device.

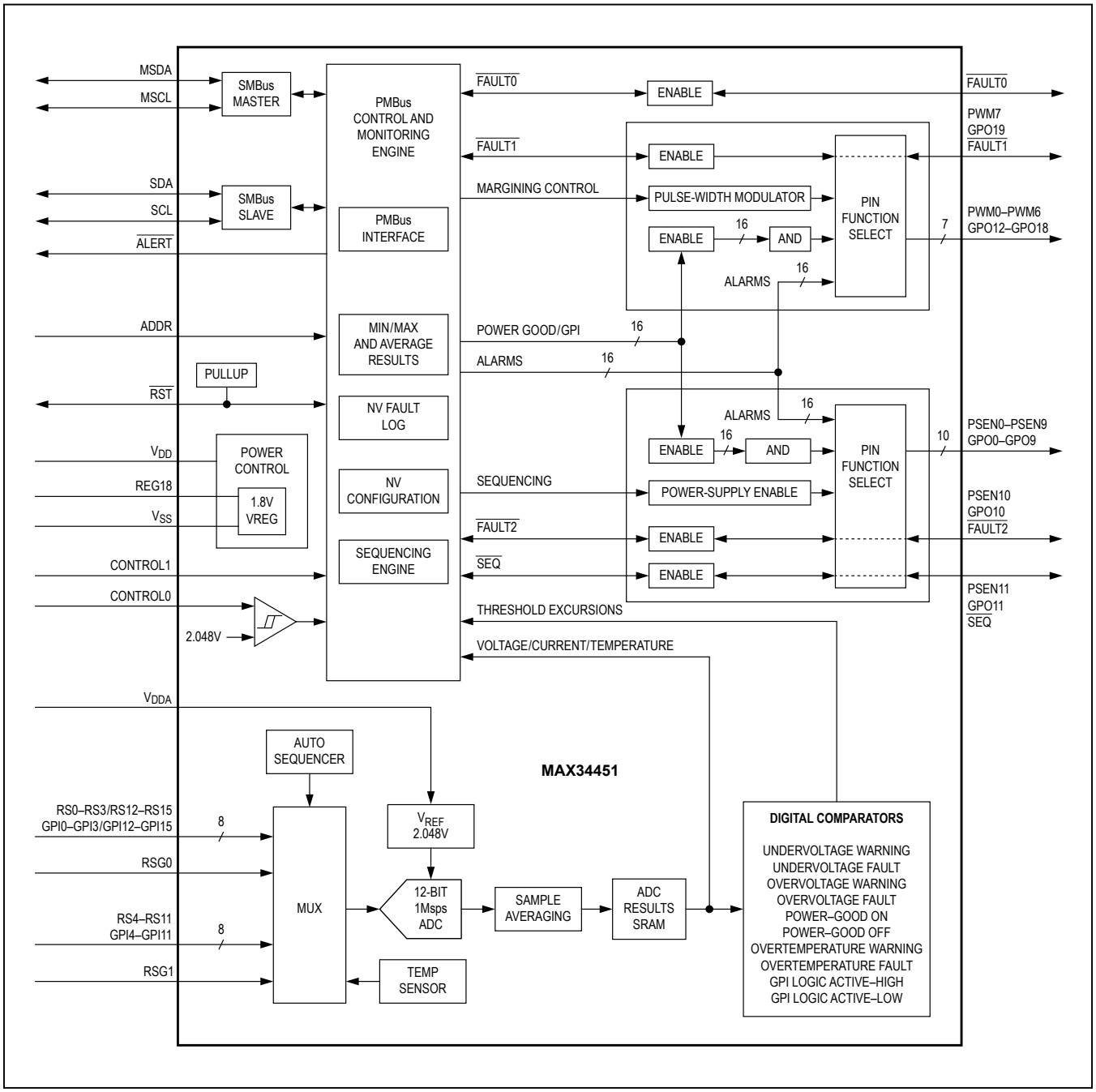
**All pins except the power pins, $\overline{ALERT}$, and ADDR are high impedance during device power-up and reset.*

***AI = Analog input, AO = Analog output, DI = Digital input, DIO = Digital input/output, and DO = Digital output.*

Expanded Pin Description

PIN	FUNCTION
PSEN0–PSEN11	The PSEN0–PSEN11 outputs are programmable with the MFR_PSEN_CONFIG command for either active-high or active-low operation and can be either open drain or push-pull. If not used for power-supply enables, these outputs can be repurposed as general-purpose outputs using the MFR_PSEN_CONFIG command. If these pins are used to enable power supplies, it is **highly recommended** that they have external pullups or pulldowns to force the supplies into an off state when the device is not active.
PWM0–PWM7	The PWM0–PWM7 outputs are high impedance when the margining is disabled. A 100% duty cycle implies the pins are continuously high. If not used for margining, these pins can be repurposed as general-purpose outputs with the MFR_PWM_CONFIG command.
$\overline{FAULT0}$–$\overline{FAULT2}$	The $\overline{FAULT0}$–$\overline{FAULT2}$ pins operate independently. Any global channel can be enabled with the MFR_FAULT_RESPONSE command to assert one or more of the $\overline{FAULTn}$ signals. Also, each global channel can be enabled to shut down when one or more of the $\overline{FAULTn}$ signals asserts. These pins are used to provide hardware control for power supplies across multiple devices. These outputs are unconditionally deasserted while $\overline{RST}$ is asserted or the device is power cycled. After device reset and upon device power-up, these outputs are pulled low immediately after program recall and held low until monitoring starts. Once monitoring starts, the $\overline{FAULTn}$ signals are released if no enabled faults are present.

Block Diagram



Detailed Description

The MAX34451 is a highly integrated system monitor with functionality to monitor up to 16 different voltages or currents and to sequence and close-loop margin up to 12 power supplies. It also supports local and remote thermal sensing.

The power-supply manager monitors the power-supply output voltage and current and constantly checks for user-programmable overvoltage, undervoltage, and overcurrent thresholds. It also has the ability to margin the power-supply output voltage up or down by a user-programmable level. The margining is performed in a closed-loop arrangement, whereby the device automatically adjusts a PWM signal or an external current DAC output and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down.

Thermal monitoring can be accomplished using up to five temperature sensors including an on-chip temperature sensor and up to four external remote DS75LV digital temperature sensors. Communications with the DS75LV temperature sensors is conducted through a dedicated I^2C/SMBus interface.

The device provides $\overline{\text{ALERT}}$ and $\overline{\text{FAULTn}}$ output signals. Host communications are conducted through a PMBus-compatible communications port.

See Table 1 and Table 2 for more details on specific device operation.

Table 1. PMBus PAGE to Pin/Resource Mapping

PMBus PAGE	PIN NAME								
	RSn/GPIn (16 AVAILABLE)			PSENn/GPOn (12 AVAILABLE)			PWMn/GPOn (8 AVAILABLE)		
	VOLTAGE OR CURRENT MONITOR	GENERAL-PURPOSE INPUT (GPI)	PIN	POWER-SUPPLY ENABLE (PSEN)	GENERAL-PURPOSE OUTPUT (GPO)	PIN	PWM MARGIN OUTPUT (PWM)	GENERAL-PURPOSE OUTPUT (GPO)	PIN
0	RS0	GPI0	5	PSEN0	GPO0	38	PWM0	GPO12	24
1	RS1	GPI1	4	PSEN1	GPO1	39	PWM1	GPO13	25
2	RS2	GPI2	3	PSEN2	GPO2	40	PWM2	GPO14	26
3	RS3	GPI3	2	PSEN3	GPO3	41	PWM3	GPO15	27
4	RS4	GPI4	1	PSEN4	GPO4	42	PWM4	GPO16	28
5	RS5	GPI5	56	PSEN5	GPO5	43	PWM5	GPO17	29
6	RS6	GPI6	55	PSEN6	GPO6	44	PWM6	GPO18	32
7	RS7	GPI7	54	PSEN7	GPO7	45	PWM7	GPO19	33
8	RS8	GPI8	53	PSEN8	GPO8	46	Margin capability provided through the external DS4424		
9	RS9	GPI9	52	PSEN9	GPO9	48			
10	RS10	GPI10	51	PSEN10	GPO10	19			
11	RS11	GPI11	50	PSEN11	GPO11	13			
12	RS12	GPI12	49	Can monitor voltage or current or be assigned as GPI					
13	RS13	GPI13	47						
14	RS14	GPI14	20						
15	RS15	GPI15	14						

Table 2. Device Channel Capabilities and Options

MAX34451 CHANNEL	PMBus COMMAND PAGE	CHANNEL CAPABILITIES
0–7	0–7	**Voltage Monitor/Sequence/Margin/GPO Option:** Pins RSn/GPIn, PSENn, and PWMn (where n = 0–7) have a one-to-one association for each channel that monitors for voltage (RSn) and can be used to sequence (PSENn) and margin (PWMn) the power supply. The voltage monitored on this channel can also be configured to determine a power-good state. If not required for either sequencing or margining, the associated PSENn and PWMn outputs can be repurposed as GPOn outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms. **Current Monitor/GPO Option:** If the RSn/GPIn input is used to monitor current, then the channel is not used to sequence or margin. The associated PSENn and PWMn outputs can be repurposed as GPOn outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms. **GPI/GPO Option:** If the RSn/GPIn input is configured as a general-purpose input (GPI), it can be used as a term in a logic combination to determine a power-good (PG) state and assert a GPOn output or act as a condition to allow a power supply to be enabled. The associated PSENn and PWMn outputs can be repurposed as GPOn outputs that can indicate power-good (PG) states or report alarms.
8–11	8–11	**Same as Channels 0–7 Except No PWM Outputs:** Pins RSn/GPIn, and PSENn (where n = 8–11) are the same as channels 0–7, except the PWMn outputs for these channels do not exist and instead the device uses an external DS4424 current DAC (connected to the master I^2C local bus) to margin the power supplies. These channels can also be used to monitor current or be used as GPIn inputs just like channels 0–7.
12–15	12–15	Pins RSn/GPIn (where n = 12–15) cannot be used to control sequencing or for margining. **Voltage Monitor Option:** Monitor voltage including channel power-good (PG) and can also be configured to shut down one or more power supplies if a fault occurs. **Current Monitor Option:** Monitor current and can be configured to shut down one or more power supplies if a fault occurs. **GPI Option:** As a general-purpose input (GPI), can be used as a term in a logic combination to determine a power-good (PG) state and assert a GPOn output or act as a condition to allow a power supply to be enabled.

Table 3. PMBus Command Codes

CODE	COMMAND NAME	TYPE	PAGE				NO. OF BYTES	FLASH STORED/ LOCKED (NOTE 2)	DEFAULT VALUE (NOTE 2)
			0–11	12–15	16–20	255			
			(NOTE 1)						
00h	PAGE	R/W byte	R/W	R/W	R/W	R/W	1	N/N	00h
01h	OPERATION	R/W byte	R/W			W	1	N/N	00h
02h	ON_OFF_CONFIG	R/W byte	R/W	R/W	R/W	R/W	1	Y/Y	1Ah
03h	CLEAR_FAULTS	Send byte	W	W	W	W	0	N/N	—
10h	WRITE_PROTECT	R/W byte	R/W	R/W	R/W	R/W	1	N/Y	00h
11h	STORE_DEFAULT_ALL	Send byte	W	W	W	W	0	N/Y	—
12h	RESTORE_DEFAULT_ALL	Send byte	W	W	W	W	0	N/Y	—
19h	CAPABILITY	Read byte	R	R	R	R	1	N/N	20h/30h
20h	VOUT_MODE	Read byte	R	R	R	R	1	FIXED/N	40h
25h	VOUT_MARGIN_HIGH	R/W word	R/W	—	—	—	2	Y/Y	0000h
26h	VOUT_MARGIN_LOW	R/W word	R/W	—	—	—	2	Y/Y	0000h
2Ah	VOUT_SCALE_MONITOR	R/W word	R/W	R/W	—	—	2	Y/Y	7FFFh
38h	IOUT_CAL_GAIN	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
40h	VOUT_OV_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	7FFFh
42h	VOUT_OV_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	7FFFh
43h	VOUT_UV_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
44h	VOUT_UV_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
46h	IOUT_OC_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	7FFFh
4Ah	IOUT_OC_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	7FFFh
4Fh	OT_FAULT_LIMIT	R/W word	—	—	R/W	—	2	Y/Y	7FFFh
51h	OT_WARN_LIMIT	R/W word	—	—	R/W	—	2	Y/Y	7FFFh
5Eh	POWER_GOOD_ON	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
5Fh	POWER_GOOD_OFF	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
60h	TON_DELAY	R/W word	R/W	—	—	—	2	Y/Y	0000h
62h	TON_MAX_FAULT_LIMIT	R/W word	R/W	—	—	—	2	Y/Y	FFFFh
64h	TOFF_DELAY	R/W word	R/W	—	—	—	2	Y/Y	0000h
79h	STATUS_WORD	Read word	R	R	R	R	2	N/N	0000h
7Ah	STATUS_VOUT	Read byte	R	R	—	—	1	N/N	00h
7Bh	STATUS_IOUT	Read byte	R	R	—	—	1	N/N	00h

Table 3. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE				NO. OF BYTES	FLASH STORED/ LOCKED (NOTE 2)	DEFAULT VALUE (NOTE 2)
			0–11	12–15	16–20	255			
			(NOTE 1)						
7Dh	STATUS_TEMPERATURE	Read byte	—	—	R	—	1	N/N	00h
7Eh	STATUS_CML	Read byte	R	R	R	R	1	N/N	00h
80h	STATUS_MFR_SPECIFIC	Read byte	R	R	—	R	1	N/N	00h
8Bh	READ_VOUT	Read word	R	R	—	—	2	N/N	0000h
8Ch	READ_IOUT	Read word	R	R	—	—	2	N/N	0000h
8Dh	READ_TEMPERATURE_1	Read word	—	—	R	—	2	N/N	0000h
98h	PMBUS_REVISION	Read byte	R	R	R	R	1	FIXED/N	11h
99h	MFR_ID	Read byte	R	R	R	R	1	FIXED/N	4Dh
9Ah	MFR_MODEL	Read byte	R	R	R	R	1	FIXED/N	59h
9Bh	MFR_REVISION	Read word	R	R	R	R	2	FIXED/N	(Note 3)
9Ch	MFR_LOCATION	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Dh	MFR_DATE	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Eh	MFR_SERIAL	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
D1h	MFR_MODE	Block R/W	R/W	R/W	R/W	R/W	2	Y/Y	0020h
D2h	MFR_PSEN_CONFIG	Block R/W	R/W	—	—	—	4	Y/Y	(Note 5)
D4h	MFR_VOUT_PEAK	R/W word	R/W	R/W	—	—	2	N/Y	0000h
D5h	MFR_IOUT_PEAK	R/W word	R/W	R/W	—	—	2	N/Y	0000h
D6h	MFR_TEMPERATURE_PEAK	R/W word	—	—	R/W	—	2	N/Y	8000h
D7h	MFR_VOUT_MIN	R/W word	R/W	R/W	—	—	2	N/Y	7FFFh
D8h	MFR_NV_LOG_CONFIG	R/W word	R/W	R/W	R/W	R/W	2	Y/Y	0000h
D9h	MFR_FAULT_RESPONSE	Block R/W	R/W	R/W			4	Y/Y	(Note 5)
DAh	MFR_FAULT_RETRY	R/W word	R/W	R/W	R/W	R/W	2	Y/Y	0000h
DCh	MFR_NV_FAULT_LOG	Block read	R	R	R	R	255	Y/Y	(Note 6)
DDh	MFR_TIME_COUNT	Block R/W	R/W	R/W	R/W	R/W	4	N/Y	(Note 5)
DFh	MFR_MARGIN_CONFIG	R/W word	R/W	—	—	—	2	Y/Y	0000h
E2h	MFR_IOUT_AVG	R/W word	R	R	—	—	2	N/Y	0000h
E4h	MFR_CHANNEL_CONFIG	R/W word	R/W	R/W	—	—	2	Y/Y	0000h
E6h	MFR_TON_SEQ_MAX	R/W word	R/W	—	—	—	2	Y/Y	0000h
E7h	MFR_PWM_CONFIG (Note 7)	Block R/W	R/W	—	—	—	4	Y/Y	(Note 5)

Table 3. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE				NO. OF BYTES	FLASH STORED/ LOCKED (NOTE 2)	DEFAULT VALUE (NOTE 2)
			0–11	12–15	16–20	255			
			(NOTE 1)						
E8h	MFR_SEQ_CONFIG	Block R/W	R/W	—	—	—	4	Y/Y	(Note 5)
EEh	MFR_STORE_ALL	Write byte	W	W	W	W	1	N/Y	—
EFh	MFR_RESTORE_ALL	Write byte	W	W	W	W	1	N/Y	—
F0h	MFR_TEMP_SENSOR_CONFIG	R/W word	—	—	R/W	—	2	Y/Y	0000h
FCh	MFR_STORE_SINGLE	R/W word	R/W	R/W	R/W	R/W	2	N/Y	0000h
FEh	MFR_CRC	R/W word	R/W	R/W	R/W	R/W	2	N/Y	FFFFh

Note 1: Common commands are shaded; access through any page results in the same device response.

Note 2: In the **Flash Stored/Locked** column, the "N" on the left indicates that this parameter is not stored in flash memory when the STORE_DEFAULT_ALL or MFR_STORE_ALL command is executed; the value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. The "Y" on the left in the **Flash Stored/Locked** column indicates that the currently loaded value in this parameter is stored in flash memory when the STORE_DEFAULT_ALL or MFR_STORE_ALL command is executed and is automatically loaded upon power-on reset or when the RST pin is asserted; the value shown in the **Default Value** column is the value when shipped from the factory. "FIXED" in the **Flash Stored** column means that the value is fixed at the factory and cannot be changed. The value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. The right-side Y/N indicates that when the device is locked, only the commands listed with "N" can be accessed. All other commands are ignored if written and return FFh if read. Only the PAGE, CLEAR_FAULTS, OPERATION, and MFR_SERIAL commands can be written to. The device unlocks if the upper 4 bytes of MFR_SERIAL match the data written to the device.

Note 3: The factory-set value is dependent on the device hardware and firmware revision.

Note 4: The factory-set default value for this 8-byte block is 3130313031303130h.

Note 5: The factory-set default value for this 4-byte block is 00000000h.

Note 6: The factory-set default value for the complete block of the MFR_NV_FAULT_LOG is FFh.

Note 7: MFR_PWM_CONFIG is only available for PAGES 0–7.

PMBus/SMBus Address Select

On device power-up, the device samples the ADDR pin to determine the PMBus/SMBus serial-port address. The combination of the components shown in Figure 1 determines the serial-port address (also see Table 4).

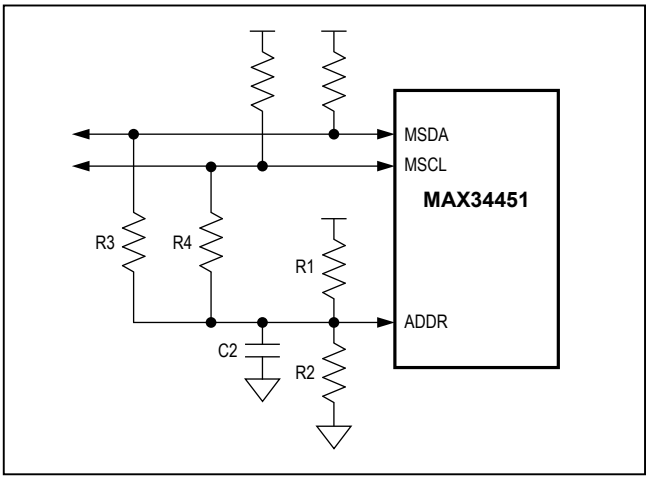


Figure 1. PMBus/SMBus Address Select

SMBus/PMBus Operation

The device implements the PMBus command structure using the SMBus format. The structure of the data flow between the host and the slave is shown below for several different types of transactions. All transactions begin with a host sending a command code that is immediately preceded with a 7-bit slave address (R/$\overline{W}$ = 0). Data is sent MSB first.

Table 4. PMBus/SMBus Serial-Port Address

R1	R2	R3	R4	C2	7-BIT SLAVE ADDRESS
—	220kΩ	—	—	—	1110 100 (E8h)
220kΩ	—	—	—	—	1110 101 (EAh)
220kΩ	—	—	—	100nF	0010 010 (24h)
22kΩ	—	—	—	100nF	0010 011 (26h)
—	—	0kΩ	—	—	1001 100 (98h)
—	—	220kΩ	—	—	1001 101 (9Ah)
—	—	—	0kΩ	—	1011 000 (B0h)
—	—	—	220kΩ	—	1011 001 (B2h)
—	0kΩ	—	—	—	1001 110 (9Ch)

Note: *The device also responds to a slave address of 34h (this is the factory programming address); the device should not share the same I^2C bus with other devices that use this slave address.*

SMBus/PMBus Operation Examples

READ WORD FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE LOW	A	DATA BYTE HIGH	NA	P

READ BYTE FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE	NA	P

WRITE WORD FORMAT

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

WRITE BYTE FORMAT

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE	A	P

SEND BYTE FORMAT

1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	P

KEY:

S = START
Sr = REPEATED START
P = STOP
W = WRITE BIT (0)
R = READ BIT (1)
A = ACKNOWLEDGE (0)
NA = NOT ACKNOWLEDGE (1)
SHADED BLOCK = SLAVE TRANSACTION

Group Command

The device supports the group command. With the group command, a host can write different data to multiple devices on the same serial bus with one long continuous data stream. All the devices addressed during this transaction wait for the host to issue a STOP before beginning to respond to the command.

Group Command Write Format

SLAVE ADDRESS, COMMAND BYTE, AND DATA WORD FOR DEVICE 1

1	7	1	1	8	1	8	1	8	1	
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	• • •

SLAVE ADDRESS, COMMAND BYTE, AND DATA BYTE FOR DEVICE 2

1	7	1	1	8	1	8	1	
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE	A	• • •

SLAVE ADDRESS AND SEND BYTE FOR DEVICE 3

1	7	1	1	8	1	
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	• • •

• • •

SLAVE ADDRESS, COMMAND BYTE, AND DATA WORD FOR DEVICE N

1	7	1	1	8	1	8	1	8	1	1
Sr	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

KEY:

S = START

Sr = REPEATED START

P = STOP

W = WRITE BIT (0)

R = READ BIT (1)

A = ACKNOWLEDGE (0)

NA = NOT ACKNOWLEDGE (1)

SHADED BLOCK = SLAVE TRANSACTION

Addressing

The device responds to receiving its fixed slave address by asserting an acknowledge (ACK) on the bus. The device does not respond to a general call address; it only responds when it receives its fixed slave address or the alert response address. See the *ALERT and Alert Response Address (ARA)* section for more details.

ALERT and Alert Response Address (ARA)

If the $\overline{\text{ALERT}}$ output is enabled (ALERT bit = 1 in MFR_MODE) when a fault occurs, the device asserts the $\overline{\text{ALERT}}$ signal and then waits for the host to send an ARA, as shown in the *Alert Response Address (ARA) Byte Format* section.

Alert Response Address (ARA) Byte Format

1	7	1	1	8	1	1
S	ARA 0001100	R	A	DEVICE SLAVE ADDRESS WITH LSB = 0	NA	P

When the ARA is received and the device is asserting $\overline{\text{ALERT}}$, the device ACKs it and then attempts to place its fixed slave address on the bus by arbitrating the bus, since another device could also try to respond to the ARA. The rules of arbitration state that the lowest address device wins. If the device wins the arbitration, it deasserts $\overline{\text{ALERT}}$. If the device loses arbitration, it keeps $\overline{\text{ALERT}}$ asserted and waits for the host to once again send the ARA.

Host Sends or Reads Too Few Bits

If, for any reason, the host does not complete writing a full byte or reading a full byte from the device before a START or STOP is received, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends or Reads Too Few Bytes

For each supported command, the device expects a fixed number of bytes to be written to or read from the device. If, for any reason, less than the expected number of bytes are written to or read from the device, the device completely ignores the command and takes no action.

Host Sends Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be written to the device. If for any reason, more than the expected number of bytes or bits is written to the device, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be read from the device. If, for any reason, more than the expected number of bytes or bits is read from the device, the device does the following:

1) Sends all ones (FFh) as long as the host keeps acknowledging.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends Improperly Set Read Bit in the Slave Address Byte

If the device receives the R/$\overline{\text{W}}$ bit in the slave address set to a one immediately preceding the command code, the device does the following (this does not apply to the ARA):

1) ACKs the address byte.
2) Sends all ones (FFh) as long as the host keeps acknowledging.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Unsupported Command Code Received/Host Writes to a Read-Only Command

If the host sends the device a command code that it does not support, or if the host sends a command code that is not supported by the current PAGE setting, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the COMM_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Invalid Data Received

The device checks the PAGE, OPERATION, and WRITE_PROTECT command codes for valid data. If the host writes a data value that is invalid, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads from a Write-Only Command

When a read request is issued to a write-only command (CLEAR_FAULTS, STORE_DEFAULT_ALL, RESTORE_DEFAULT_ALL, MFR_STORE_ALL, MFR_RESTORE_ALL, OPERATION with PAGE = 255), the device does the following:

1) ACKs the address byte.
2) Ignores the command.
3) Sends all ones (FFh) as long as the host keeps acknowledging.
4) Sets the CML bit in STATUS_WORD.
5) Sets the DATA_FAULT bit in STATUS_CML.
6) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

SMBus Timeout

If, during an active SMBus communication sequence, the SCL signal is held low for greater than the timeout duration (nominally 27ms), the device terminates the sequence and resets the serial bus. It takes no other action. No status bits are set.

PMBus Operation

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. A PMBus 1.1-compliant device uses the SMBus version 1.1 for transport protocol and responds to the SMBus slave address. In this data sheet, the term SMBus is used to refer to the electrical characteristics of the PMBus communication using the SMBus physical layer. The term PMBus is used to refer to the PMBus command protocol. The device employs a number of standard SMBus protocols (e.g., Write Word, Read Word, Write Byte, Read Byte, Send Byte, etc.) to program output voltage and warning/fault thresholds, read monitored data, and provide access to all manufacturer-specific commands.

The device supports the group command. The group command is used to send commands to more than one PMBus device. It is not required that all the devices receive the same command. However, no more than one command can be sent to any one device in one group command packet. The group command must not be used with commands that require receiving devices to respond with data, such as the STATUS_WORD command. When the device receives a command through this protocol, it immediately begins execution of the received command after detecting the STOP condition.

The device supports the PAGE command and uses it to select which individual channel to access. When a data word is transmitted, the lower order byte is sent first and the higher order byte is sent last. Within any byte, the most-significant bit (MSB) is sent first and the least-significant bit (LSB) is sent last.

PMBus Protocol Support

The device supports a subset of the commands defined in the PMBus Power System Management Protocol Specification Part II - Command Language Revision 1.1.

For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at **www.PMBus.org**. The supported PMBus commands and the corresponding device behavior are described in this document. All data values are represented in DIRECT format, unless otherwise stated. Whenever the PMBus specification refers to the PMBus device, it is referring to the device operating in conjunction with a power supply. While the command can call for turning on or off the PMBus device, the device always remains on to continue communicating with the PMBus master and transfers the command to the power supply accordingly.

Data Format

Voltage data for commanding or reading the output voltage or related parameters (such as the overvoltage threshold) are presented in DIRECT format. DIRECT format data is a 2-byte, two's complement binary value. DIRECT format data can be used with any command that sends or reads a parametric value. The DIRECT format uses an equation and defined coefficients to calculate the desired values. Table 5 lists coefficients used by the device.

Interpreting Received DIRECT Format Values

The host system uses the following equation to convert the value received from the PMBus device—in this case the MAX34451—into a reading of volts, degrees Celsius, or other units as appropriate:

$$X = (1/m) \times (Y \times 10^{-R} - b)$$

where X is the calculated real-world value in the appropriate units (V, °C, etc.); m is the slope coefficient; Y is the 2-byte, two's complement integer received from the PMBus device; b is the offset; and R is the exponent.

Table 5. PMBus Command Code Coefficients

PARAMETER	COMMANDS	UNITS	RESOLUTION	MAXIMUM	m	b	R
Voltage	VOUT_MARGIN_HIGH VOUT_MARGIN_LOW VOUT_OV_FAULT_LIMIT VOUT_OV_WARN_LIMIT VOUT_UV_WARN_LIMIT VOUT_UV_FAULT_LIMIT POWER_GOOD_ON POWER_GOOD_OFF READ_VOUT MFR_VOUT_PEAK MFR_VOUT_MIN	mV	1	32767	1	0	0
Voltage Scaling	VOUT_SCALE_MONITOR	—	1/32767	1	32767	0	0
Current	IOUT_OC_FAULT_LIMIT IOUT_OC_WARN_LIMIT READ_IOUT MFR_IOUT_PEAK MFR_IOUT_AVG	A	0.01	327.67	1	0	2
Current Scaling	IOUT_CAL_GAIN	mΩ	0.1	3276.7	1	0	1
Temperature	OT_FAULT_LIMIT OT_WARN_LIMIT READ_TEMPERATURE_1 MFR_TEMPERATURE_PEAK	°C	0.01	327.67	1	0	2
Timing	TON_DELAY TON_MAX_FAULT_LIMIT TOFF_DELAY MFR_FAULT_RETRY MFR_TON_SEQ_MAX	ms	0.2	6553.4	5	0	0

Sending a DIRECT Format Value

To send a value, the host must use the following equation to solve for Y:

$$Y = (mX + b) \times 10^{R}$$

where Y is the 2-byte, two's complement integer to be sent to the unit; m is the slope coefficient; X is the real-world value, in units such as volts, to be converted for transmission; b is the offset; and R is the exponent.

The following example demonstrates how the host can send and retrieve values from the device. Table 6 lists the coefficients used in the following parameters.

Table 6. Coefficients for DIRECT Format Value

COMMAND CODE	COMMAND NAME	m	b	R
25h	VOUT_MARGIN_HIGH	1	0	0
8Bh	READ_VOUT	1	0	0

If a host wants to set the device to change the power-supply output voltage to 3.465V (or 3465mV), the corresponding VOUT_MARGIN_HIGH value is:

$$Y = (1 \times 3465 + 0) \times 10^{0} = 3465 \text{ (decimal)}$$
$$= 0D89h \text{ (hex)}$$

Conversely, if the host received a value of 0D89h on a READ_VOUT command, this is equivalent to:

$$X = (1/1) \times (0D89h \times 10^{-(-0)} - 0) = 3465mV = 3.465V$$

Power supplies and power converters generally have no way of knowing how their outputs are connected to ground. Within the power supply, all output voltages are most commonly treated as positive. Accordingly, all output voltages and output-voltage-related parameters of PMBus devices are commanded and reported as positive values. It is up to the system to know that a particular output is negative if that is of interest to the system. All output-voltage-related commands use 2 data bytes.

Fault Management and Reporting

For reporting faults/warnings to the host on a real-time basis, the device asserts the open-drain $\overline{ALERT}$ pin (if enabled in MFR_MODE) and sets the appropriate bit in the various status registers. On recognition of the $\overline{ALERT}$ assertion, the host or system manager is expected to poll the I^2C bus to determine the device asserting $\overline{ALERT}$. The host sends the SMBus ARA (0001 100). The device ACKs the SMBus ARA, transmits its slave address, and deasserts $\overline{ALERT}$. The system controller then communicates with PMBus commands to retrieve the fault/warning status information from the device.

See the individual command sections for more details. Faults and warnings that are latched in the status registers are cleared when any one of the following conditions occur:

- A CLEAR_FAULTS command is received.
- The $\overline{RST}$ pin is toggled or a soft-reset is issued.
- Bias power to the device is removed and then reapplied.

One or more latched-off power supplies are only restarted when one of the following occurs:

- OPERATION commands are received that turn off and turn on the power supplies, or the CONTROLn pins are toggled to turn off and then turn on the power supplies.
- The $\overline{RST}$ pin is toggled or a soft-reset is issued.
- Bias power to the device is removed and then reapplied.

The device responds to fault conditions according to the configuration of the MFR_FAULT_RESPONSE command. This command determines how the device should respond to each particular fault and whether it should assert one or more of the $\overline{FAULTn}$ pins when a fault occurs.

The MFR_FAULT_RESPONSE command also determines whether a channel should power up if a fault is present. With the RESPONSE bits in MFR_FAULT_RESPONSE, each channel can be independently configured to either respond or not respond to each possible fault. Before any power-supply channel is enabled, or the $\overline{FAULTn}$ outputs deasserted, the device checks for overvoltage, overcurrent, and temperature faults (but not for undervoltage) if the channel is configured for a fault response to either latchoff (RESPONSE[1:0] = 01) or retry (RESPONSE[1:0] = 10) in the MFR_FAULT_RESPONSE command. Only after the faults clear is the channel allowed to turn on. See Table 7 for fault-monitoring states.

Table 7. Fault-Monitoring States

FAULT	REQUIRED DEVICE CONFIGURATION FOR ACTIVE MONITORING	WHEN MONITORED
Overvoltage	• Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)	Continuous monitoring.
Undervoltage	• Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)	Stop monitoring while the power supply is off; start monitoring when voltage exceeds the POWER_GOOD_ON level.
Overcurrent	• Current monitoring enabled (SELECT[5:0] = 22h in MFR_CHANNEL_CONFIG)	Continuous monitoring.
Power-Up Time	• Sequencing enabled (SELECT[5:0] = 10h in MFR_CHANNEL_CONFIG)	Monitored only during power-on sequence.
Overtemperature	• Temperature sensor enabled (ENABLE = 1 in MFR_TEMP_SENSOR_CONFIG)	Continuous monitoring.

Note: *Device response to faults is determined by the configuration of MFR_FAULT_RESPONSE.*

Password Protection

The device can be password protected by using the LOCK bit in the MFR_MODE command. Once the device is locked, only certain PMBus commands can be accessed with the serial port. See Table 3 for a complete list of PMBus commands. Commands that have password protection return all ones (FFh), with the proper number of data bytes, when read. When the device is locked, only the PAGE, OPERATION, CLEAR_FAULTS, and MFR_SERIAL commands can be written; all other written commands are ignored. When MFR_SERIAL is written and the upper 4 bytes match the internally flash-stored value, the device unlocks and remains unlocked until the LOCK bit in MFR_MODE is activated once again. The LOCK status bit in STATUS_MFR_SPECIFIC is always available to indicate whether the device is locked or unlocked.

Power-Supply Sequencing

Sequencing control for each of the 12 power-supply channels on the device is configured using the MFR_SEQ_CONFIG and ON_OFF_CONFIG commands. See the descriptions of these commands for details on the exact device configuration required. Power supplies can be powered up and down in any order (even across multiple devices). See the command descriptions and Figure 2 for specifics on sequencing control.

Dual-Loop Sequencing

The device contains two independent sequencing groups, SEQUENCE0 and SEQUENCE1. Both groups do not need to be used, but every channel is assigned to one of the two groups with the SEQ_SELECT bit in the MFR_SEQ_CONFIG command. The two sequencing groups operate independently. SEQUENCE0 is always associated with CONTROL0 and SEQUENCE1 is always associated with CONTROL1. The two sequencing groups can also be independently controlled with the OPERATION command. With the ON_OFF_CONFIG command, the device is configured to respond to the CONTROLn pins or the OPERATION command (or both). When the OPERATION command is sent to the device (when the PAGE is set to 255), both sequence groups are controlled, as shown in Table 8.

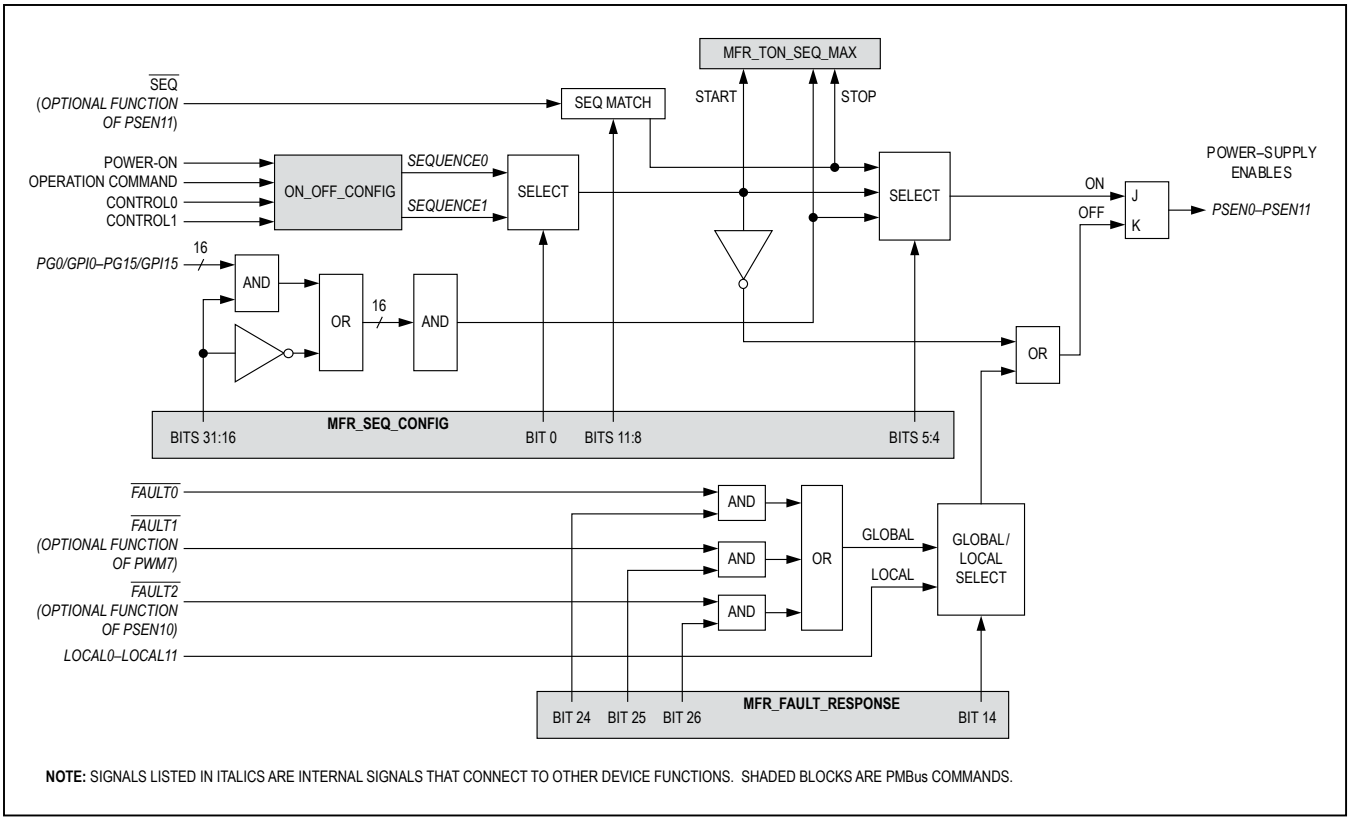


Figure 2. Sequence Control Logic

Table 8. OPERATION Command Sequence Control Options

GROUP	OPERATION COMMAND (PAGE = 255)		
	ON	SOFT-OFF	IMMEDIATE OFF
SEQUENCE0	80h or 81h	40h or 41h	00h or 01h
SEQUENCE1	80h or 82h	40h or 42h	00h or 02h

Power-On Sequencing

The activation of all power-supply channels (even across multiple devices) is initiated from a common START signal that can either be the CONTROL0 or CONTROL1 pin, or the OPERATION command. Each power-supply channel on the device can be sequenced on by one of the following methods:

- Power is applied to the device.
- The CONTROL0 pin goes active.
- The CONTROL1 pin goes active.
- The OPERATION command is received.
- The logic combination of power goods and GPI is valid.
- The $\overline{SEQ}$ pin signal is matched.

Each enabled PSENn output goes active (either active high or active low, as defined in MFR_PSEN_CONFIG) after the associated delay time programmed in TON_DELAY. The power supplies can be sequenced on in any order. Each channel can be sequenced on with either time-based or event-based conditions. The output voltage of each power supply is monitored to ensure that the supply crosses the power-good-on level (as configured in the POWER_GOOD_ON command) within a programmable time limit, as configured in the TON_MAX_FAULT_LIMIT command. This power-up time limit can be disabled by configuring TON_MAX_FAULT_LIMIT to 0000h. For channels using event-based sequencing, the MFR_TON_SEQ_MAX command determines the maximum time limit for the sequence-on event to occur. Like the TON_MAX_FAULT_LIMIT, this limit can be disabled by configuring MFR_TON_SEQ_MAX to 0000h. There is a one-to-one correspondence between the RSn inputs and the PSENn outputs. For example, RS6 monitors the power supply controlled by PSEN6. All power-on sequencing is gated by detected faults. Before any power-supply channel is enabled (or the $\overline{FAULTn}$ output deasserted) the device checks for overvoltage, overcurrent, and temperature faults that are enabled (but not for undervoltage since the supply is off).

Power-Off Sequencing

The order in which the supplies are disabled is determined with the TOFF_DELAY configuration. Alternatively, all the power supplies can be switched off immediately, as configured in the ON_OFF_CONFIG command or with the OPERATION command.

As configured with the ON_OFF_CONFIG command, either the CONTROL0 or CONTROL1 pin or the OPERATION command is the master off switch. When either the CONTROL0 or CONTROL1 pin goes inactive, or the OPERATION off command is received (or one of the enabled $\overline{FAULTn}$ pins asserted), the power supplies are sequenced off. Neither the power-good (PG) or GPI logic combinations, nor the $\overline{SEQ}$ pin, can be used to turn off the power supplies.

Sequencing Example

As an example, Figure 3 details a simple sequencing scheme consisting of four power supplies using a mixture of time-based and event-based sequencing. Channels 0 and 2 use time-based sequencing and channels 1 and 5 use event-based sequencing. When either the CONTROL0 or CONTROL1 pin goes active, or the OPERATION command is received (as defined by the ON_OFF_CONFIG command), PSEN0 is asserted after the delay time configured in TON_DELAY. RS0 is monitored to ensure that the PSEN0 supply crosses the power-good-on level (as configured in POWER_GOOD_ON) within a programmable time limit (as configured in TON_MAX_FAULT_LIMIT). PSEN2 operates in a similar fashion as PSEN0, but with a different TON_DELAY and a different TON_MAX_FAULT_LIMIT. Since the power-up of channels 0 and 2 are based solely on their TON_DELAY values, these channels are time-based.

When RS2 crosses its power-good-on level, PSEN5 is asserted after its configured TON_DELAY and similarly, PSEN1 asserts when RS5 crosses its power-good-on level. Since the power-up of channels 5 and 1 are based on the power-good states of other channels, these channels are event-based. The MFR_TON_SEQ_MAX command can be used to ensure that these events occur and the power-up sequence does not hang waiting for an event to transpire. When RS1 crosses its power-good-on level, it has been configured to generate a $\overline{SEQ}$ pin signal to communicate to another device to turn on one or more of its power supplies.

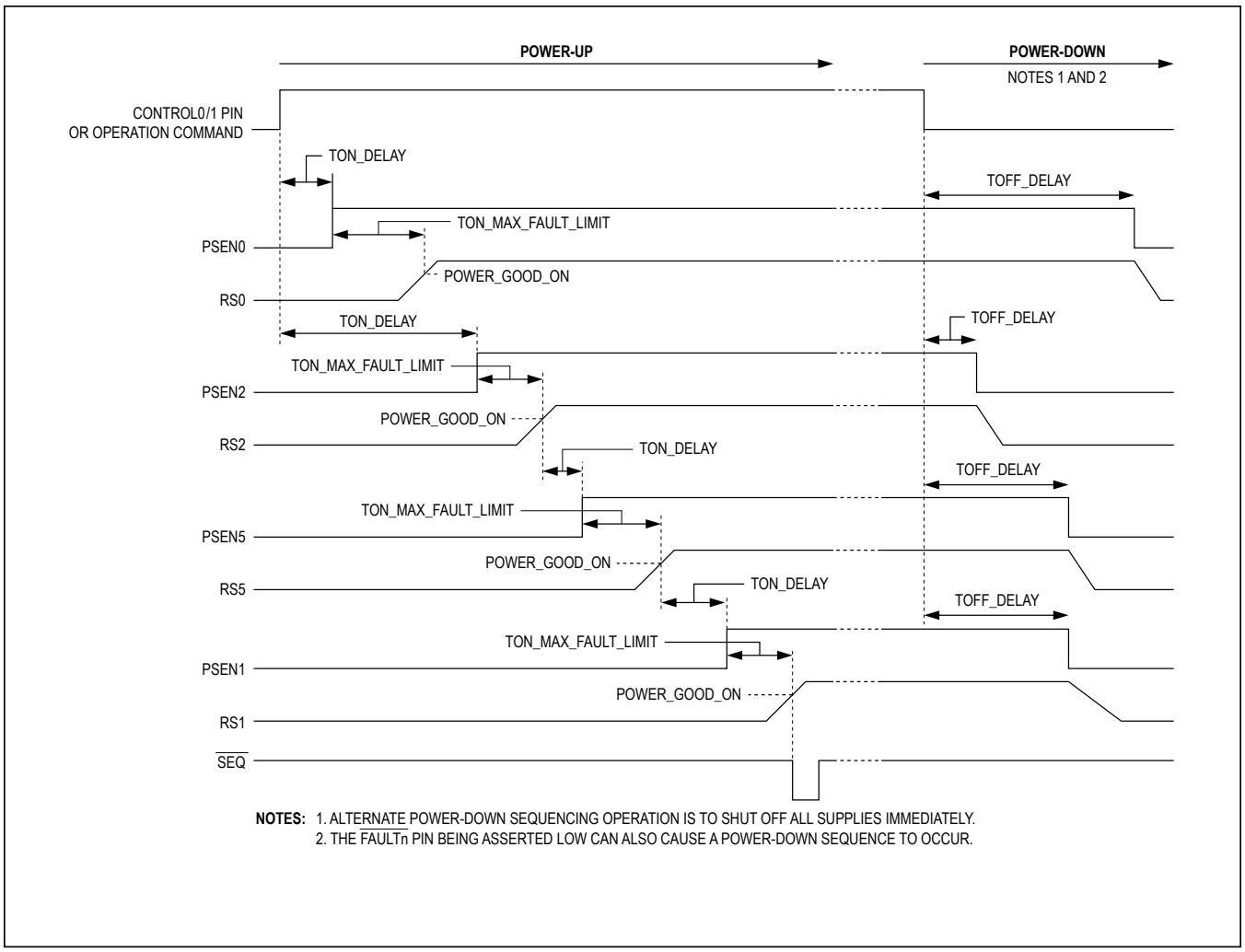


Figure 3. Sequencing Example

Multiple Device Connections

Multiple MAX34451 devices can be connected together to increase the system channel count. Figure 4 details the recommended connection scheme.

All the paralleled devices share the same CONTROLn, FAULTn, SEQ, and SMBus signals. The devices all use a common signal (either the CONTROL0 or CONTROL1 pin, or the OPERATION command) to enable/disable all the power supplies. Any of the monitored power supplies can be configured with the MFR_FAULT_RESPONSE command to activate one or more of the FAULTn signals and shut down all the other supplies enabled to respond to one or more of the FAULTn signals. The FAULT0 signal is always available, whereas FAULT1 and FAULT2 are optional signals. When they are enabled, the PWM7 and PSEN10 outputs (respectively) are disabled. The use of multiple fault signals allows more flexibility in controlling which power supplies need to shut down during a fault.

USER NOTE:

- All devices must be configured with the same ON_OFF_CONFIG configuration.
- All devices must be powered up and reset at the same time.