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MAX34462

PMBus 16-Channel Monitor/Sequencer with Differential Inputs and Margining DACs

General Description

The MAX34462 is a system monitor that can manage up to 16 power supplies. The power-supply manager monitors the power-supply output voltages and constantly checks for user-programmable overvoltage and undervoltage thresholds. If a fault is detected, the device automatically shuts down the system in an orderly fashion. The device can sequence the supplies in any order at both power-up and power-down. The device contains 16 independent voltages DACs, which the device uses to close-loop margin the power-supply output voltages up or down to a user-programmable level. The device contains an internal temperature sensor and can support up to four external remote temperature sensors. Once configured, the device can operate autonomously without any host intervention.

Applications

- Network Switches/Routers
- Base Stations
- Servers
- Smart Grid Network Systems

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX34462.related.

Benefits and Features

- 16 Channels of Power-Supply Management
- Power-Supply Voltage or Current Measurement and Monitoring
- Fast Minimum/Maximum Threshold Excursion Detection
- Differential Input Sensing Improves Measurement Accuracy
- 16 Independent Voltage DACs for Power-Supply Margining
- Automatic Closed-Loop Margining
- Programmable Up and Down Sequencing
- Up to Four Independent Sequencing Loops
- 5V Tolerant Power-Supply Output Enables
- Internal Temperature Sensor
- Reports Peak and Average Levels for a Number of Parameters
- PMBus™-Compliant Command Interface
- I²C/SMBus-Compatible Serial Bus with Bus Timeout Function
- On-Board Nonvolatile Black Box Fault Logging and Default Configuration Setting
- Expandable Channel Operation with Parallel Devices
- Sequencing Can be Timing Synchronized Across Multiple Devices
- Configurable Combinatorial Logic Supporting Up to 16 GPIs and 36 GPOs
- No External Clocking Required
- +3.0 to +3.6V Supply Voltage

19-6785; Rev 0; 9/13

maxim integrated™

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Absolute Maximum Ratings

DVDD/AVDD to DVSS/AVSS .....-0.3V to +4.0V
RSN/GPIN to AVSS.....-0.3V to +0.3V
PSEN to DVSS.....-0.3V to +5.5V
All Other Pins (except REG18 and REG18A)
Relative to DVSS/AVSS ..... -0.3V to (V_{DVDD}/V_{AVDD} + 0.3V)*
REG18 and REG18A to AVSS .....-0.3V to +2.0V

Continuous Power Dissipation (T_A = +70ºC)
CSBGA (derate 40mW/ºC above +70ºC) 2200mW
Operating Temperature Range.....-40ºC to +95ºC
Storage Temperature Range.....-55ºC to +125ºC
Soldering Temperature (reflow) ..... +260ºC

**Subject to not exceeding +4.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = -40ºC to +95ºC, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DVDD}, V_{AVDD}	(Note 1)	3.0		3.6	V
V_{DD} Rise Time		From 0 to 2.5V			4	ms
V_{DD} Source Impedance					10	Ω
Input Logic 1 (except I^2C and GPI Pins)	V_{IH1}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic 0 (except I^2C and GPI Pins)	V_{IL1}		-0.3		+0.3 x V_{DD}	V
Input Logic 1: SCL, SDA, MSCL, MSDA	V_{IH2}		2.1		V_{DD} + 0.3	V
Input Logic 0: SCL, SDA, MSCL, MSDA	V_{IL2}		-0.3		+0.8	V
Input Logic 1 (GPI Pins)	V_{IH3}	Minimum pulse width = 5ms	1.5		V_{DD} + 0.3	V
Input Logic 0 (GPI Pins)	V_{IL3}	Minimum pulse width = 5ms	-0.3		+1.0	V
Source Impedance to RS		ADC_TIME[1:0] = 00			1	kΩ
		ADC_TIME[1:0] = 01			5	
		ADC_TIME[1:0] = 10			10	
		ADC_TIME[1:0] = 11			20	
DAC Output Capacitance Load		In series with > 5kΩ			50	nF

Electrical Characteristics

(V_{DVDD} and V_{AVDD} = 3.0V to 3.6V, T_A = -40ºC to +95ºC, unless otherwise noted. Typical values are at V_{DVDD}/V_{AVDD} = 3.3V, T_A = +25ºC.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Current	I_{CPU}	(Note 2)		13		mA
	$I_{PROGRAM}$			16		
System Clock Error	$f_{ERR:MOSC}$	+25°C < T_A < +95°C	-3		+3	%
		-40°C < T_A < 25°C	-4		+4	
Output Logic-Low (except I^2C Pins)	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V
Output Logic-High (except I^2C Pins)	V_{OH1}	I_{OH} = -2mA (Note 1)	V_{DVDD} - 0.5			V
Output Logic-Low: SCL, SDA, MSCL, MSDA	V_{OL2}	I_{OL} = 4mA (Note 1)			0.4	V
SCL, SDA, MSCL, MSDA Leakage	IL_{I2C}	V_{DVDD} = 0V or float			±5	µA
CONTROL0 Threshold				2.048		V
CONTROL0 Hysteresis				50		mV
ADC						
ADC Bit Resolution				12		Bits
ADC Conversion Time		ADC_TIME[1:0] = 00		1000		ns
ADC Full Scale	V_{FS}	T_A = 0°C to +95°C	2.032	2.048	2.064	V
ADC Measurement Resolution	V_{LSB}			500		µV
RS Input Capacitance	C_{RS}			15		pF
RS Input Leakage	IL_{RS}	0V < V_{RS} < V_{AVDD}		±0.25		µA
ADC Integral Nonlinearity	INL			±1		LSB
ADC Differential Nonlinearity	DNL			±1		LSB
DAC						
DAC Resolution				8		Bits
DAC Full-Scale Accuracy		0°C ≤ T_A ≤ +95°C	2.0	2.048	2.1	V
DAC Integral Nonlinearity					±2	LSB
DAC Differential Nonlinearity					±1	LSB
DAC Offset Error					±25	mV
DAC Load Regulation	$DAC_{LDREG500}$	V_{DACOUT} > 200mV, 500µA sink and source	-8		+8	mV
	$DAC_{LDREG200}$	V_{DACOUT} > 100mV, 200µA sink and source	-5		+5	
Output Short Circuit				5		mA
Output Leakage		Output disabled			±1	µA

Electrical Characteristics (continued)

(V_{DVDD} and V_{AVDD} = 3.0V to 3.6V, T_A = -40ºC to +95ºC, unless otherwise noted. Typical values are at V_{DVDD}/V_{AVDD} = 3.3V, T_A = +25ºC.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE SENSOR						
Internal Temperature Measurement Error		T_A = -40°C to +95°C		±2		°C
FLASH						
Flash Endurance	N_{FLASH}	(Note 3)	20,000			Write Cycles
Data Retention		T_A = +50°C (Note 3)	100			Years
STORE_DEFAULT_ALL MFR_STORE_ALL Write Time				85		ms
MFR_STORE_SINGLE Write Time				310		µs
RESTORE_DEFAULT_ALL MFR_RESTORE_ALL Time		With MFR_STORE_SINGLE data		110		ms
		Without MFR_STORE_SINGLE data		1.2		
MFR_NV_FAULT_LOG Write Time		Writing one fault log		11		ms
MFR_NV_FAULT_LOG Delete Time		Deleting all fault logs		200		ms
MFR_NV_FAULT_LOG Overwrite Time				40		ms
TIMING OPERATING CHARACTERISTICS						
Round-Robin Voltage and Current Sample Rate		Threshold excursion (Note 4)		64		µs
		Data collection		5		ms
Temperature Sample Rate				1000		ms
Device Startup Time		With MFR_STORE_SINGLE data		170		ms
		Without MFR_STORE_SINGLE data		90		
SYNC Clock Frequency				20		kHz

Note 1: All voltages are reference to ground. Currents entering the IC are specified as positive and currents exiting the IC are negative.

Note 2: This does not include pin input/output currents.

Note 3: Guaranteed by design.

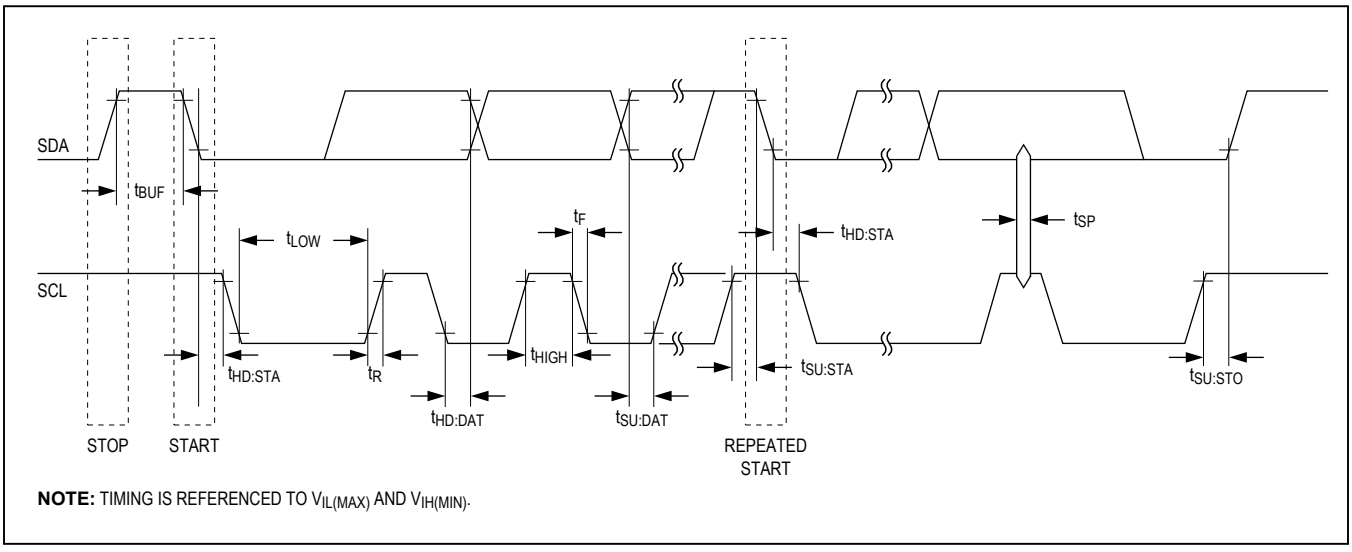
Note 4: The round-robin threshold excursion rate can be changed with the ADC_AVERAGE and ADC_TIME bits in MFR_MODE from 16µs (no averaging and 1µs conversion) to 1024µs (8x averaging and 8µs conversion).

I²C/SMBus Interface Electrical Specifications

(V_{DVDD} and V_{AVDD} = 3.0V to 3.6V, T_A = -40ºC to +95ºC, unless otherwise noted. Typical values are at V_{DVDD}/V_{AVDD} = 3.3V, T_A = +25ºC.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		400	kHz
MSCL Clock Frequency	f_{MSCL}			100		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Set-Up Time	$t_{SU:DAT}$		100			ns
START Set-Up Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
STOP Set-Up Time	$t_{SU:STO}$		0.6			µs
Clock Low Timeout	t_{TO}		25	27	35	ms

I²C/SMBus Timing

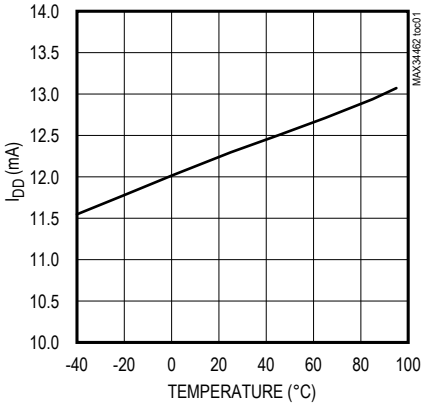


NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

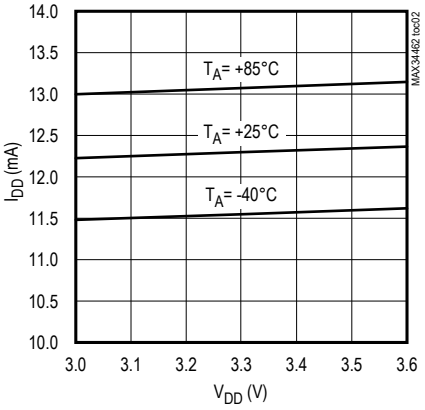
Typical Operating Characteristics

(V_{DVDD} and V_{AVDD} = 3.3V and T_A = +25°C, without MFR_STORE_SINGLE data, unless otherwise noted.)

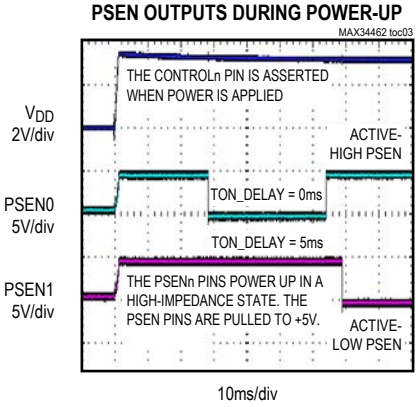
SUPPLY CURRENT vs. TEMPERATURE



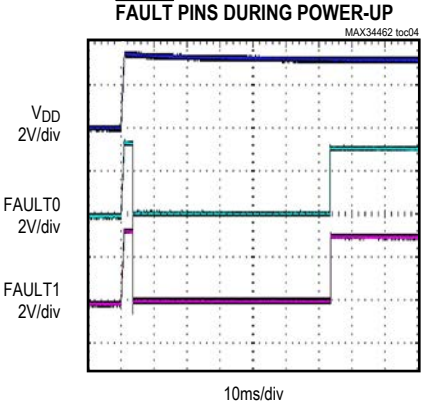
SUPPLY CURRENT vs. SUPPLY VOLTAGE



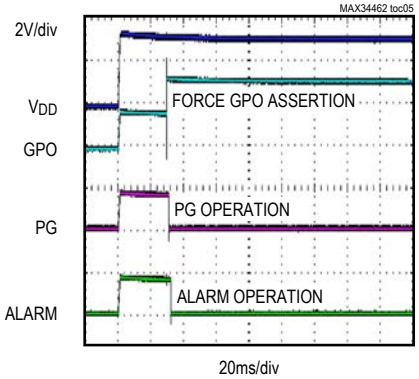
PSEN OUTPUTS DURING POWER-UP



$\overline{\text{FAULT}}$ PINS DURING POWER-UP



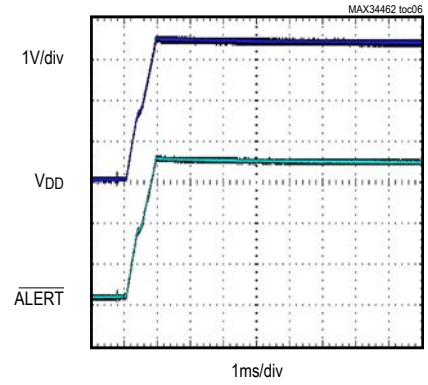
GPO OUTPUT PINS DURING POWER-UP ALL PIN CONFIGURED TO BE PUSH-PULL ACTIVE-HIGH



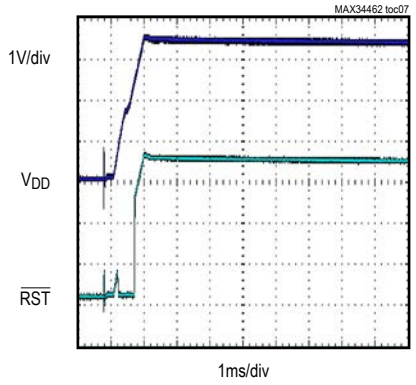
Typical Operating Characteristics (continued)

(V_{DVDD} and V_{AVDD} = 3.3V and T_A = +25°C, without MFR_STORE_SINGLE data, unless otherwise noted.)

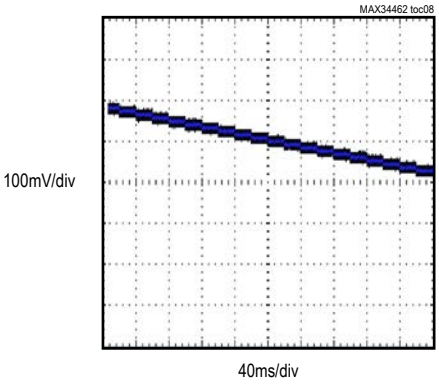
$\overline{ALERT}$ PIN DURING POWER-UP



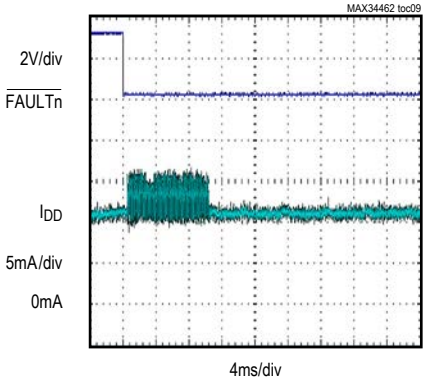
$\overline{RST}$ PIN DURING POWER-UP



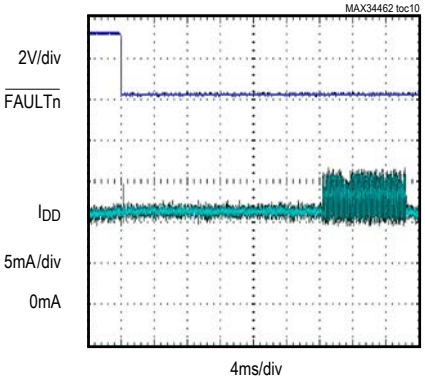
DAC MARGINING VOLTAGE vs. TIME



I_{DD} vs. TIME DURING A NONVOLATILE LOG WRITE



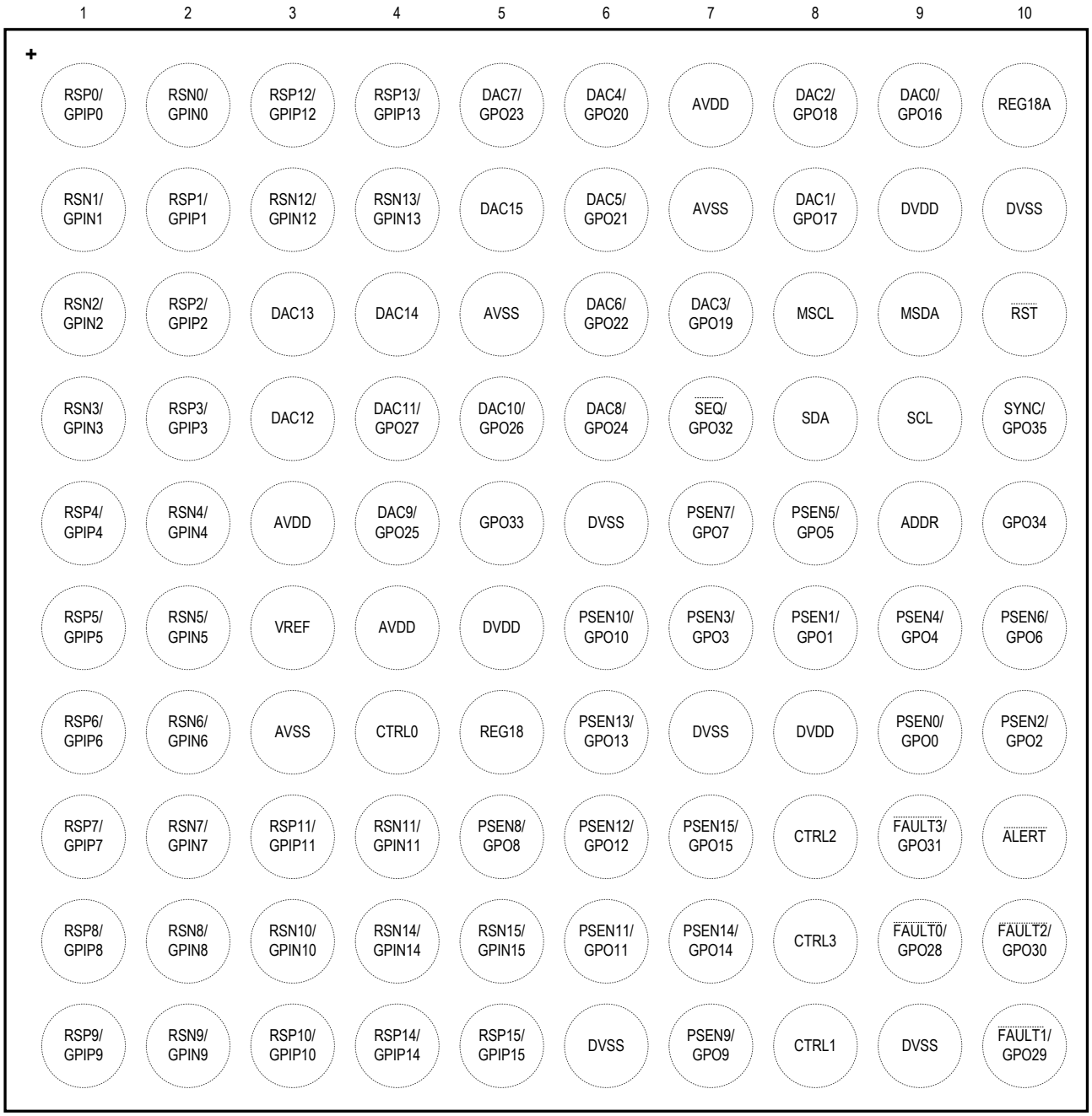
I_{DD} vs. TIME DURING A NONVOLATILE LOG WRITE WITH OVERWRITE ENABLED



Bump Configuration

TOP VIEW

MAX34462



CSBGA

Bump Description

BUMP	NAME	TYPE	FUNCTION
A1	RSP0	AI	ADC Voltage Sense Positive Input 0. Connect to AVSS if unused.
	GPIP0	AI	General-Purpose Positive Input 0. Connect to AVSS if unused.
A2	RSN0	AI	ADC Voltage Sense Negative Input 0. Connect to AVSS if unused.
	GPIN0	AI	General-Purpose Negative Input 0. Connect to AVSS if unused.
B2	RSP1	AI	ADC Voltage Sense Positive Input 1. Connect to AVSS if unused.
	GPIP1	AI	General-Purpose Positive Input 1. Connect to AVSS if unused.
B1	RSN1	AI	ADC Voltage Sense Negative Input 1. Connect to AVSS if unused.
	GPIN1	AI	General-Purpose Negative Input 1. Connect to AVSS if unused.
C2	RSP2	AI	ADC Voltage Sense Positive Input 2. Connect to AVSS if unused.
	GPIP2	AI	General-Purpose Positive Input 2. Connect to AVSS if unused.
C1	RSN2	AI	ADC Voltage Sense Negative Input 2. Connect to AVSS if unused.
	GPIN2	AI	General-Purpose Negative Input 2. Connect to AVSS if unused.
D2	RSP3	AI	ADC Voltage Sense Positive Input 3. Connect to AVSS if unused.
	GPIP3	AI	General-Purpose Positive Input 3. Connect to AVSS if unused.
D1	RSN3	AI	ADC Voltage Sense Negative Input 3. Connect to AVSS if unused.
	GPIN3	AI	General-Purpose Negative Input 3. Connect to AVSS if unused.
E1	RSP4	AI	ADC Voltage Sense Positive Input 4. Connect to AVSS if unused.
	GPIP4	AI	General-Purpose Positive Input 4. Connect to AVSS if unused.
E2	RSN4	AI	ADC Voltage Sense Negative Input 4. Connect to AVSS if unused.
	GPIN4	AI	General-Purpose Negative Input 4. Connect to AVSS if unused.
F1	RSP5	AI	ADC Voltage Sense Positive Input 5. Connect to AVSS if unused.
	GPIP5	AI	General-Purpose Positive Input 5. Connect to AVSS if unused.
F2	RSN5	AI	ADC Voltage Sense Negative Input 5. Connect to AVSS if unused.
	GPIN5	AI	General-Purpose Negative Input 5. Connect to AVSS if unused.
G1	RSP6	AI	ADC Voltage Sense Positive Input 6. Connect to AVSS if unused.
	GPIP6	AI	General-Purpose Positive Input 6. Connect to AVSS if unused.
G2	RSN6	AI	ADC Voltage Sense Negative Input 6. Connect to AVSS if unused.
	GPIN6	AI	General-Purpose Negative Input 6. Connect to AVSS if unused.
H1	RSP7	AI	ADC Voltage Sense Positive Input 7. Connect to AVSS if unused.
	GPIP7	AI	General-Purpose Positive Input 7. Connect to AVSS if unused.
H2	RSN7	AI	ADC Voltage Sense Negative Input 7. Connect to AVSS if unused.
	GPIN7	AI	General-Purpose Negative Input 7. Connect to AVSS if unused.
J1	RSP8	AI	ADC Voltage Sense Positive Input 8. Connect to AVSS if unused.
	GPIP8	AI	General-Purpose Positive Input 8. Connect to AVSS if unused.
J2	RSN8	AI	ADC Voltage Sense Negative Input 8. Connect to AVSS if unused.
	GPIN8	AI	General-Purpose Negative Input 8. Connect to AVSS if unused.
K1	RSP9	AI	ADC Voltage Sense Positive Input 9. Connect to AVSS if unused.
	GPIP9	AI	General-Purpose Positive Input 9. Connect to AVSS if unused.
K2	RSN9	AI	ADC Voltage Sense Negative Input 9. Connect to AVSS if unused.
	GPIN9	AI	General-Purpose Negative Input 9. Connect to AVSS if unused.
K3	RSP10	AI	ADC Voltage Sense Positive Input 10. Connect to AVSS if unused.
	GPIP10	AI	General-Purpose Positive Input 10. Connect to AVSS if unused.

Bump Description (continued)

BUMP	NAME	TYPE	FUNCTION
J3	RSN10	AI	ADC Voltage Sense Negative Input 10. Connect to AVSS if unused.
	GPIN10	AI	General-Purpose Negative Input 10. Connect to AVSS if unused.
H3	RSP11	AI	ADC Voltage Sense Positive Input 11. Connect to AVSS if unused.
	GPIP11	AI	General-Purpose Positive Input 11. Connect to AVSS if unused.
H4	RSN11	AI	ADC Voltage Sense Negative Input 11. Connect to AVSS if unused.
	GPIN11	AI	General-Purpose Negative Input 11. Connect to AVSS if unused.
A3	RSP12	AI	ADC Voltage Sense Positive Input 12. Connect to AVSS if unused.
	GPIP12	AI	General-Purpose Positive Input 12. Connect to AVSS if unused.
B3	RSN12	AI	ADC Voltage Sense Negative Input 12. Connect to AVSS if unused.
	GPIN12	AI	General-Purpose Negative Input 12. Connect to AVSS if unused.
A4	RSP13	AI	ADC Voltage Sense Positive Input 13. Connect to AVSS if unused.
	GPIP13	AI	General-Purpose Positive Input 13. Connect to AVSS if unused.
B4	RSN13	AI	ADC Voltage Sense Negative Input 13. Connect to AVSS if unused.
	GPIN13	AI	General-Purpose Negative Input 13. Connect to AVSS if unused.
K4	RSP14	AI	ADC Voltage Sense Positive Input 14. Connect to AVSS if unused.
	GPIP14	AI	General-Purpose Positive Input 14. Connect to AVSS if unused.
J4	RSN14	AI	ADC Voltage Sense Negative Input 14. Connect to AVSS if unused.
	GPIN14	AI	General-Purpose Negative Input 14. Connect to AVSS if unused.
K5	RSP15	AI	ADC Voltage Sense Positive Input 15. Connect to AVSS if unused.
	GPIP15	AI	General-Purpose Positive Input 15. Connect to AVSS if unused.
J5	RSN15	AI	ADC Voltage Sense Negative Input 15. Connect to AVSS if unused.
	GPIN15	AI	General-Purpose Negative Input 15. Connect to AVSS if unused.
C10	$\overline{\text{RST}}$	DIO	Reset Active-Low Input/Output. Contains an internal pullup.
G4	CONTROL0	AI	Power-Supply Master On/Off Control Input 0. Active-low or active-high based on ON_OFF_CONFIG command. Connect to AVSS if unused. A series 100Ω resistor is recommended if this input can be driven when the device is powered down.
K8	CONTROL1	DI	Power-Supply Master On/Off Control Input 1. Active-low or active-high based on ON_OFF_CONFIG command. Connect to DVSS if unused. A series 100Ω resistor is recommended if this input can be driven when the device is powered down.
H8	CONTROL2	DI	Power-Supply Master On/Off Control Input 2. Active-low or active-high based on ON_OFF_CONFIG command. Connect to DVSS if unused. A series 100Ω resistor is recommended if this input can be driven when the device is powered down.
J8	CONTROL3	DI	Power-Supply Master On/Off Control Input 3. Active-low or active-high based on ON_OFF_CONFIG command. Connect to DVSS if unused. A series 100Ω resistor is recommended if this input can be driven when the device is powered down.
E5	GPO33	DO	General-Purpose Output 33. Function is selected using the MFR_GPO_CONFIG command.
D7	$\overline{\text{SEQ}}$	DIO	Sequencing Input/Output. Open-drain, active low. This pin is used as handshake signal to coordinate event-based sequencing in systems using multiple devices.
	GPO32	DO	General-Purpose Output 32. Function is selected using the MFR_GPO_CONFIG command.
D8	SDA	DIO	I^2C/SMBus-Compatible Input/Output. Open-drain output.
D9	SCL	DIO	I^2C/SMBus-Compatible Clock Input/Output. Open-drain output.

Bump Description (continued)

BUMP	NAME	TYPE	FUNCTION
C8	MSCL	DIO	Master I2C Clock Input/Output. Open-drain output.
C9	MSDA	DIO	Master I2C Data Input/Output. Open-drain output.
H10	$\overline{\text{ALERT}}$	DO	Alert Output. Open-drain, active-low output.
E9	ADDR	DI	SMBus Slave Address Select. This pin is sampled on device power-up to determine the SMBus address. See the section on PMBus/SMBus address select for details on how to strap this pin to select the proper slave address.
E10	GPO34	DO	General-Purpose Output 34. Function is selected using the MFR_GPO_CONFIG command.
J9	$\overline{\text{FAULT0}}$	DIO	Fault Input/Output 0. Open-drain, active-low. See the *Expanded Bump Description* section for more details.
	GPO28	DO	General-Purpose Output 28. Function is selected using the MFR_GPO_CONFIG command.
K10	$\overline{\text{FAULT1}}$	DIO	Fault Input/Output 1. Open-drain, active-low. See the *Expanded Bump Description* section for more details.
	GPO29	DO	General-Purpose Output 29. Function is selected using the MFR_GPO_CONFIG command.
J10	$\overline{\text{FAULT2}}$	DIO	Fault Input/Output 2. Open-drain, active-low. See the *Expanded Bump Description* section for more details.
	GPO30	DO	General-Purpose Output 30. Function is selected using the MFR_GPO_CONFIG command.
H9	$\overline{\text{FAULT3}}$	DIO	Fault Input/Output 3. Open-drain, active-low. See the *Expanded Bump Description* for more details.
	GPO31	DO	General-Purpose Output 31. Function is selected using the MFR_GPO_CONFIG command.
G9	PSEN0	DO	Power-Supply Enable 0. See the *Expanded Bump Description* section for more details.
	GPO0	DO	General-Purpose Output 0
F8	PSEN1	DO	Power-Supply Enable 1. See the *Expanded Bump Description* section for more details.
	GPO1	DO	General-Purpose Output 1
G10	PSEN2	DO	Power-Supply Enable 2. See the *Expanded Bump Description* section for more details.
	GPO2	DO	General-Purpose Output 2
F7	PSEN3	DO	Power-Supply Enable 3. See the *Expanded Bump Description* section for more details.
	GPO3	DO	General-Purpose Output 3
F9	PSEN4	DO	Power-Supply Enable 4. See the *Expanded Bump Description* section for more details.
	GPO4	DO	General-Purpose Output 4
E8	PSEN5	DO	Power-Supply Enable 5. See the *Expanded Bump Description* section for more details.
	GPO5	DO	General-Purpose Output 5
F10	PSEN6	DO	Power-Supply Enable 6. See the *Expanded Bump Description* section for more details.
	GPO6	DO	General-Purpose Output 6
E7	PSEN7	DO	Power-Supply Enable 7. See the *Expanded Bump Description* section for more details.
	GPO7	DO	General-Purpose Output 7
H5	PSEN8	DO	Power-Supply Enable 8. See the *Expanded Bump Description* section for more details.
	GPO8	DO	General-Purpose Output 8

Bump Description (continued)

BUMP	NAME	TYPE	FUNCTION
K7	PSEN9	DO	Power-Supply Enable 9. See the *Expanded Bump Description* section for more details.
	GPO9	DO	General-Purpose Output 9
F6	PSEN10	DO	Power-Supply Enable 10. See the *Expanded Bump Description* section for more details.
	GPO10	DO	General-Purpose Output 10
J6	PSEN11	DO	Power-Supply Enable 11. See the *Expanded Bump Description* section for more details.
	GPO11	DO	General-Purpose Output 11
H6	PSEN12	DO	Power-Supply Enable 12. See the *Expanded Bump Description* section for more details.
	GPO12	DO	General-Purpose Output 12
G6	PSEN13	DO	Power-Supply Enable 13. See the *Expanded Bump Description* section for more details.
	GPO13	DO	General-Purpose Output 13
J7	PSEN14	DO	Power-Supply Enable 14. See the *Expanded Bump Description* section for more details.
	GPO14	DO	General-Purpose Output 14
H7	PSEN15	DO	Power-Supply Enable 15. See the *Expanded Bump Description* section for more details.
	GPO15	DO	General-Purpose Output 15
A9	DAC0	AO	Margining DAC Output 0. See the *Expanded Bump Description* section for more details.
	GPO16	DO	General-Purpose Output 16
B8	DAC1	AO	Margining DAC Output 1. See the *Expanded Bump Description* section for more details.
	GPO17	DO	General-Purpose Output 17
A8	DAC2	AO	Margining DAC Output 2. See the *Expanded Bump Description* section for more details.
	GPO18	DO	General-Purpose Output 18
C7	DAC3	AO	Margining DAC Output 3. See the *Expanded Bump Description* section for more details.
	GPO19	DO	General-Purpose Output 19
A6	DAC4	AO	Margining DAC Output 4. See the *Expanded Bump Description* section for more details.
	GPO20	DO	General-Purpose Output 20
B6	DAC5	AO	Margining DAC Output 5. See the *Expanded Bump Description* section for more details.
	GPO21	DO	General-Purpose Output 21
C6	DAC6	AO	Margining DAC Output 6. See the *Expanded Bump Description* section for more details.
	GPO22	DO	General-Purpose Output 22
A5	DAC7	AO	Margining DAC Output 7. See the *Expanded Bump Description* section for more details.
	GPO23	DO	General-Purpose Output 23
D6	DAC8	AO	Margining DAC Output 8. See the *Expanded Bump Description* section for more details.
	GPO24	DO	General-Purpose Output 24
E4	DAC9	AO	Margining DAC Output 9. See the *Expanded Bump Description* section for more details.
	GPO25	DO	General-Purpose Output 25
D5	DAC10	AO	Margining DAC Output 10. See the *Expanded Bump Description* section for more details.
	GPO26	DO	General-Purpose Output 26
D4	DAC11	AO	Margining DAC Output 11. See the *Expanded Bump Description* section for more details.
	GPO27	DO	General-Purpose Output 27
D3	DAC12	AO	Margining DAC Output 12. See the *Expanded Bump Description* section for more details.
C3	DAC13	AO	Margining DAC Output 13. See the *Expanded Bump Description* section for more details.
C4	DAC14	AO	Margining DAC Output 14. See the *Expanded Bump Description* section for more details.
B5	DAC15	AO	Margining DAC Output 15. See the *Expanded Bump Description* section for more details.

Bump Description (continued)

BUMP	NAME	TYPE	FUNCTION
D10	SYNC	DIO	Sequencing Synchronization Clock. This pin can be configured using the MFR_MODE command to be either an output (master mode) which provides a 20kHz clock or an input which accepts a 20kHz clock (slave mode) to share the same clock across multiple devices in order to synchronize the time base used for power-supply sequencing. A series 100Ω resistor is recommended to isolate outputs if two masters share the same bus. Leave open circuit if unused.
	GPO35	DO	General-Purpose Output 35. Function is selected using the MFR_GPO_CONFIG command.
F3	VREF	AO	Voltage Reference Output for Analog Circuitry. Bypass to AVSS with 22nF. Do not connect other circuitry to this pin.
B9	DVDD	Power	Digital Supply Voltage. Bypass to DVSS with 0.1µF. Connect all DVDD and AVDD pins together.
F5	DVDD	Power	Digital Supply Voltage. Bypass to DVSS with 0.1µF. Connect all DVDD and AVDD pins together.
G8	DVDD	Power	Digital Supply Voltage. Bypass to DVSS with 0.1µF. Connect all DVDD and AVDD pins together.
B10	DVSS	Power	Digital Supply Ground Reference. Connect all DVSS and AVSS pins together.
K9	DVSS	Power	Digital Supply Ground Reference. Connect all DVSS and AVSS pins together.
G7	DVSS	Power	Digital Supply Ground Reference. Connect all DVSS and AVSS pins together.
E6	DVSS	Power	Digital Supply Ground Reference. Connect all DVSS and AVSS pins together.
K6	DVSS	Power	Digital Supply Ground Reference. Connect all DVSS and AVSS pins together.
G5	REG18	Power	Regulator for Digital Circuitry. Bypass to AVSS with 1µF (500mΩ maximum ESR) and 10nF. Do not connect other circuitry to this pin.
A10	REG18A	Power	Supplemental Bypass for Regulator for Digital Circuitry. Bypass to AVSS with 0.1µF. Do not connect other circuitry to this pin.
B7	AVSS	Power	Analog Supply Ground Reference. Connect all DVSS and AVSS pins together.
C5	AVSS	Power	Analog Supply Ground Reference. Connect all DVSS and AVSS pins together.
G3	AVSS	Power	Analog Supply Ground Reference. Connect all DVSS and AVSS pins together.
F4	AVDD	Power	Analog Supply Voltage. Bypass to AVSS with 0.1µF. Connect all DVDD and AVDD pins together.
E3	AVDD	Power	Analog Supply Voltage. Bypass to AVSS with 0.1µF. Connect all DVDD and AVDD pins together.
A7	AVDD	Power	Analog Supply Voltage. Bypass to AVSS with 0.1µF. Connect all DVDD and AVDD pins together.

Note: *All pins except the power pins and ADDR and GPO34 are high impedance during device power-up and during device reset.*

DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output, AI = Analog Input, AO = Analog Output

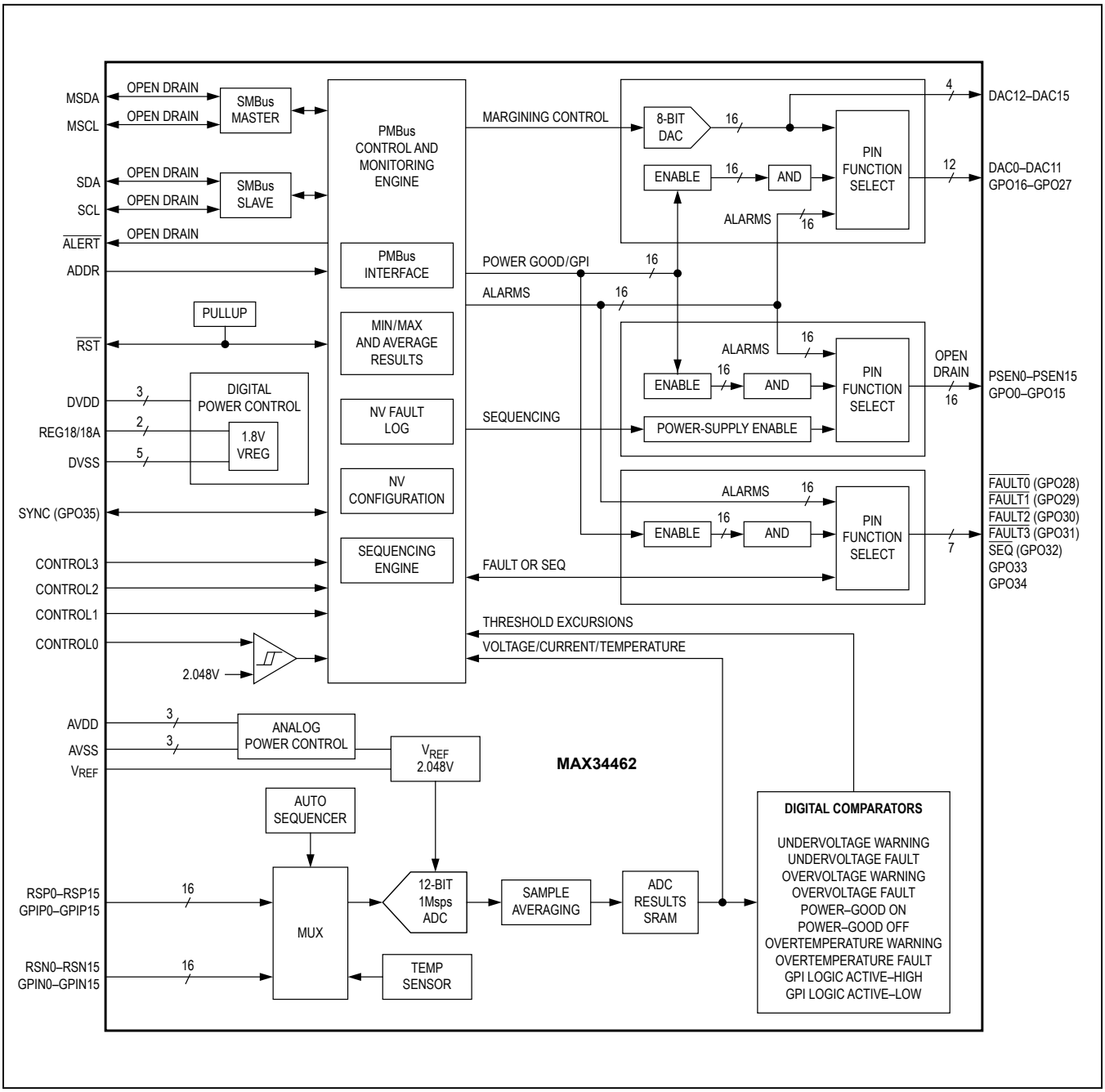
Expanded Bump Description

BUMP	EXPANDED DESCRIPTION
PSEN	The PSEN open-drain outputs are 5V tolerant and they are programmable with the MFR_PSEN_CONFIG command for either active-high or active-low operation. If not used for power-supply enables, these outputs can be repurposed as general purpose outputs (GPO) using the MFR_PSEN_CONFIG command. *If these pins are used to enable power supplies, it is **highly recommended** that these pins have external pullups or pulldowns to force the supplies into an off state when the device is not active.*
DAC	The DAC outputs are high-impedance when the margining is disabled. If DAC0 to DAC11 are not used for margining, these pins can be repurposed as a general purpose outputs (GPO) with the MFR_DAC_CONFIG command.
$\overline{\text{FAULT}}$	All $\overline{\text{FAULT}}$ pins operate independently. Any global channel can be enabled with the MFR_FAULT_RESPONSE command to assert one or more of the $\overline{\text{FAULT}}$ signals. Also each global channel can be enabled to shut down when one or more of the $\overline{\text{FAULT}}$ signals asserts. These pins are used to provide hardware control for power supplies across multiple devices. These outputs are unconditionally deasserted while $\overline{\text{RST}}$ is asserted or when the device is power cycled. After device reset and upon device power-up, these outputs are pulled low immediately after program recall and held low until monitoring starts. Once monitoring starts, the $\overline{\text{FAULT}}$ signals are released if no enabled faults are present.

CSBGA Bump Map

	1	2	3	4	5	6	7	8	9	10
A	RSP0	RSN0	RSP12	RSP13	DAC7	DAC4	AVDD	DAC2	DAC0	REG18A
B	RSN1	RSP1	RSN12	RSN13	DAC15	DAC5	AVSS	DAC1	DVDD	DVSS
C	RSN2	RSP2	DAC13	DAC14	AVSS	DAC6	DAC3	MSCL	MSDA	$\overline{\text{RST}}$
D	RSN3	RSP3	DAC12	DAC11	DAC10	DAC8	$\overline{\text{SEQ}}$	SDA	SCL	SYNC
E	RSP4	RSN4	AVDD	DAC9	GPO33	DVSS	PSEN7	PSEN5	ADDR	GPO34
F	RSP5	RSN5	VREF	AVDD	DVDD	PSEN10	PSEN3	PSEN1	PSEN4	PSEN6
G	RSP6	RSN6	AVSS	CONTROL0	REG18	PSEN13	DVSS	DVDD	PSEN0	PSEN2
H	RSP7	RSN7	RSP11	RSN11	PSEN8	PSEN12	PSEN15	CONTROL2	$\overline{\text{FAULT3}}$	$\overline{\text{ALERT}}$
J	RSP8	RSN8	RSN10	RSN14	RSN15	PSEN11	PSEN14	CONTROL3	$\overline{\text{FAULT0}}$	$\overline{\text{FAULT2}}$
K	RSP9	RSN9	RSP10	RSP14	RSP15	DVSS	PSEN9	CONTROL1	DVSS	$\overline{\text{FAULT1}}$

Block Diagram



Detailed Description

The MAX34462 is a highly-integrated system monitor with functionality to monitor up to 16 different voltages or currents and also to sequence and close-loop margin up to 16 power supplies. It also supports local and remote thermal sensing.

The power-supply manager monitors the power-supply output voltage and current and constantly checks for user-programmable overvoltage, undervoltage, and overcurrent thresholds. It can also margin the power-supply output voltage up or down by a user-programmable level. The margining is performed in a closed-loop arrangement, whereby the device automatically adjusts a DAC output voltage and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down.

Thermal monitoring can be accomplished using up to five temperature sensors including an on-chip temperature sensor and up to four external remote DS75LV digital temperature sensors. Communications with the DS75LV temperature sensors is conducted via a dedicated I^2C/SMBus interface.

The MAX34462 provides $\overline{\text{ALERT}}$ and multiple $\overline{\text{FAULT}}$ output signals. Host communications are conducted through a PMBus-compatible communications port.

See Table 1 and Table 2 for more details on specific device operation. Table 3 shows the PMBus command codes.

Table 1. PMBus PAGE to Pin/Resource Mapping

PIN NAME	RS/GPI (16 AVAILABLE)			PSEN/GPO (16 AVAILABLE)			DAC/GPO (16 AVAILABLE (12 GPO))		
PMBus PAGE	VOLTAGE OR CURRENT MONITOR	GENERAL-PURPOSE INPUT (GPI)	BALL	POWER-SUPPLY ENABLE (PSEN)	GENERAL-PURPOSE OUTPUT (GPO)	BALL	DAC MARGIN OUTPUT (DAC)	GENERAL-PURPOSE OUTPUT (GPO)	BALL
0	RS0	GPI0	A1/A2	PSEN0	GPO0	G9	DAC0	GPO16	A9
1	RS1	GPI1	B2/B1	PSEN1	GPO1	F8	DAC1	GPO17	B8
2	RS2	GPI2	C2/C1	PSEN2	GPO2	G10	DAC2	GPO18	A8
3	RS3	GPI3	D2/D1	PSEN3	GPO3	F7	DAC3	GPO19	C7
4	RS4	GPI4	E1/E2	PSEN4	GPO4	F9	DAC4	GPO20	A6
5	RS5	GPI5	F1/F2	PSEN5	GPO5	E8	DAC5	GPO21	B6
6	RS6	GPI6	G1/G2	PSEN6	GPO6	F10	DAC6	GPO22	C6
7	RS7	GPI7	H1/H2	PSEN7	GPO7	E7	DAC7	GPO23	A5
8	RS8	GPI8	J1/J2	PSEN8	GPO8	H5	DAC8	GPO24	D6
9	RS9	GPI9	K1/K2	PSEN9	GPO9	K7	DAC9	GPO25	E4
10	RS10	GPI10	K3/J3	PSEN10	GPO10	F6	DAC10	GPO26	D5
11	RS11	GPI11	H3/H4	PSEN11	GPO11	J6	DAC11	GPO27	D4
12	RS12	GPI12	A3/B3	PSEN12	GPO12	H6	DAC12	N/A	D3
13	RS13	GPI13	A4/B4	PSEN13	GPO13	G6	DAC13	N/A	C3
14	RS14	GPI14	K4/J4	PSEN14	GPO14	J7	DAC14	N/A	C4
15	RS15	GPI15	K5/J5	PSEN15	GPO15	H7	DAC15	N/A	B5

Table 2. Device Channel Capabilities and Options

MAX34462 CHANNEL	PMBus COMMAND PAGE	CHANNEL CAPABILITIES
0 to 15	0 to 15	**Voltage Monitor/Sequence/Margin/GPO Option** Pins RS/GPI, PSEN, and DAC (where n = 0 to 15) have a one-to-one association for each channel that monitors for voltage (RS) and can be used to sequence (PSEN) and margin (DAC) the power supply. The voltage monitored on this channel can also be configured to determine a power-good state. If not required for either sequencing or margining, the associated PSEN and DAC outputs (only for DAC channels 0 to 11) can be repurposed as GPO outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms. **Current Monitor/GPO Option** If the RS/GPI input is used to monitor current, then the channel is not used to sequence or margin. The associated PSEN and DAC outputs (only for DAC channels 0 to 11) can be repurposed as GPO outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms. **GPI/GPO Option** If the RS/GPI input is configured as a general-purpose input (GPI), then it can be used as a term in a logic combination to determine a power-good (PG) state and assert a GPO output or act as a condition to allow a power supply to be enabled. The associated PSEN and DAC outputs (only for DAC channels 0 to 11) can be repurposed as GPO outputs that can be indicate power-good (PG) states or report alarms.

Table 3. PMBus Command Codes

CODE	COMMAND NAME	TYPE	PAGE (Note 1)				# BYTE	FLASH STORED/ LOCKED (Note 2)	DEFAULT VALUE (Note 2)
			0-15	16-20	21-28	255			
00h	PAGE	R/W Byte	R/W	R/W	R/W	R/W	1	N/N	00h
01h	OPERATION	R/W Byte	R/W			W	1	N/N	00h
02h	ON_OFF_CONFIG	R/W Byte	R/W	R/W	R/W	R/W	1	Y/Y	1Ah
03h	CLEAR_FAULTS	Send Byte	W	W	W	W	0	N/N	—
10h	WRITE_PROTECT	R/W Byte	R/W	R/W	R/W	R/W	1	N/Y	00h
11h	STORE_DEFAULT_ALL	Send Byte	W	W	W	W	0	N/Y	—
12h	RESTORE_DEFAULT_ALL	Send Byte	W	W	W	W	0	N/Y	—
19h	CAPABILITY	Read Byte	R	R	R	R	1	N/N	20h/30h
20h	VOUT_MODE	Read Byte	R	R	R	R	1	FIXED/N	40h
21h	VOUT_COMMAND	R/W Word	R/W				2	Y/Y	0000h
25h	VOUT_MARGIN_HIGH	R/W Word	R/W				2	Y/Y	0000h
26h	VOUT_MARGIN_LOW	R/W Word	R/W				2	Y/Y	0000h
2Ah	VOUT_SCALE_MONITOR	R/W Word	R/W				2	Y/Y	7FFFh
38h	IOUT_CAL_GAIN	R/W Word	R/W				2	Y/Y	0000h
40h	VOUT_OV_FAULT_LIMIT	R/W Word	R/W				2	Y/Y	7FFFh
42h	VOUT_OV_WARN_LIMIT	R/W Word	R/W				2	Y/Y	7FFFh
43h	VOUT_UV_WARN_LIMIT	R/W Word	R/W				2	Y/Y	0000h

Table 3. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE (Note 1)				# BYTE	FLASH STORED/ LOCKED (Note 2)	DEFAULT VALUE (Note 2)
			0-15	16-20	21-28	255			
44h	VOUT_UV_FAULT_LIMIT	R/W Word	R/W				2	Y/Y	0000h
46h	IOUT_OC_WARN_LIMIT	R/W Word	R/W				2	Y/Y	7FFFh
4Ah	IOUT_OC_FAULT_LIMIT	R/W Word	R/W				2	Y/Y	7FFFh
4Fh	OT_FAULT_LIMIT	R/W Word		R/W			2	Y/Y	7FFFh
51h	OT_WARN_LIMIT	R/W Word		R/W			2	Y/Y	7FFFh
5Eh	POWER_GOOD_ON	R/W Word	R/W				2	Y/Y	0000h
5Fh	POWER_GOOD_OFF	R/W Word	R/W				2	Y/Y	0000h
60h	TON_DELAY	R/W Word	R/W				2	Y/Y	0000h
62h	TON_MAX_FAULT_LIMIT	R/W Word	R/W				2	Y/Y	FFFFh
64h	TOFF_DELAY	R/W Word	R/W				2	Y/Y	0000h
79h	STATUS_WORD	Read Word	R	R	R	R	2	N/N	0000h
7Ah	STATUS_VOUT	Read Byte	R				1	N/N	00h
7Bh	STATUS_IOUT	Read Byte	R				1	N/N	00h
7Dh	STATUS_TEMPERATURE	Read Byte		R			1	N/N	00h
7Eh	STATUS_CML	Read Byte	R	R	R	R	1	N/N	00h
80h	STATUS_MFR_SPECIFIC	Read Byte	R			R	1	N/N	00h
8Bh	READ_VOUT	Read Word	R				2	N/N	0000h
8Ch	READ_IOUT	Read Word	R				2	N/N	0000h
8Dh	READ_TEMPERATURE_1	Read Word		R			2	N/N	0000h
98h	PMBUS_REVISION	Read Byte	R	R	R	R	1	FIXED/N	11h
99h	MFR_ID	Read Byte	R	R	R	R	1	FIXED/N	4Dh
9Ah	MFR_MODEL	Read Byte	R	R	R	R	1	FIXED/N	5Ah
9Bh	MFR_REVISION	Read Word	R	R	R	R	2	FIXED/N	(Note 3)
9Ch	MFR_LOCATION	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Dh	MFR_DATE	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Eh	MFR_SERIAL	Block R/W	R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
D1h	MFR_MODE	Block R/W	R/W	R/W	R/W	R/W	2	Y/Y	0020h
D2h	MFR_PSEN_CONFIG	Block R/W	R/W				4	Y/Y	(Note 5)
D4h	MFR_VOUT_PEAK	R/W Word	R/W				2	N/Y	0000h
D5h	MFR_IOUT_PEAK	R/W Word	R/W				2	N/Y	0000h
D6h	MFR_TEMPERATURE_PEAK	R/W Word		R/W			2	N/Y	8000h
D7h	MFR_VOUT_MIN	R/W Word	R/W				2	N/Y	7FFFh
D8h	MFR_NV_LOG_CONFIG	R/W Word	R/W	R/W	R/W	R/W	2	Y/Y	0000h
D9h	MFR_FAULT_RESPONSE	Block R/W	R/W				4	Y/Y	(Note 5)
DAh	MFR_FAULT_RETRY	R/W Word	R/W	R/W	R/W	R/W	2	Y/Y	0000h
DCh	MFR_NV_FAULT_LOG	Block Read	R	R	R	R	255	Y/Y	(Note 6)
DDh	MFR_TIME_COUNT	Block R/W	R/W	R/W	R/W	R/W	4	N/Y	(Note 5)
DFh	MFR_MARGIN_CONFIG	R/W Word	R/W				2	Y/Y	0000h
E2h	MFR_IOUT_AVG	R/W Word	R				2	N/Y	0000h
E4h	MFR_CHANNEL_CONFIG	R/W Word	R/W				2	Y/Y	0000h

Table 3. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE (Note 1)				# BYTE	FLASH STORED/ LOCKED (Note 2)	DEFAULT VALUE (Note 2)
			0-15	16-20	21-28	255			
E6h	MFR_TON_SEQ_MAX	R/W Word	R/W				2	Y/Y	0000h
E8h	MFR_SEQ_CONFIG	Block R/W	R/W				4	Y/Y	(Note 5)
E9h	MFR_DAC_CONFIG (Note 7)	Block R/W	R/W				4	Y/Y	(Note 5)
EEh	MFR_STORE_ALL	Write Byte	W	W	W	W	1	N/Y	—
EFh	MFR_RESTORE_ALL	Write Byte	W	W	W	W	1	N/Y	—
F0h	MFR_TEMP_SENSOR_ CONFIG	R/W Word		R/W			2	Y/Y	0000h
F8h	MFR_GPO_CONFIG	Block R/W			R/W		4	Y/Y	(Note 5)
FCh	MFR_STORE_SINGLE	R/W Word	R/W	R/W	R/W	R/W	2	N/Y	0000h
FEh	MFR_CRC	R/W Word	R/W	R/W	R/W	R/W	2	N/Y	FFFFh

Note 1: Common commands are shaded. Access via any PAGE results in the same device response.

Note 2: In the **Flash Stored/Locked** column, the left “N” indicates that this parameter is not stored in flash memory when the STORE_DEFAULT_ALL or MFR_STORE_ALL command is executed and the value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. The left “Y” in the **Flash Stored/Locked** column indicates that the currently loaded value in this parameter is stored in flash memory when the STORE_DEFAULT_ALL or MFR_STORE_ALL command is executed and is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted and the value shown in the **Default Value** column is the value when shipped from the factory. “FIXED” in the **Flash Stored** column means this value is fixed at the factory and cannot be changed. The value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. The right side Y/N indicates that when the device is locked, only the commands listed with “N” can be accessed. All other commands are ignored if written and return FFh if read. Only the PAGE, CLEAR_FAULTS, OPERATION, and MFR_SERIAL commands can be written to. The device unlocks if the upper 4 bytes of MFR_SERIAL match the data written to the device.

Note 3: The factory-set value is dependent on the device hardware and firmware revision.

Note 4: The factory-set default value for this 8-byte block is 3130313031303130h.

Note 5: The factory-set default value for this 4-byte block is 00000000h.

Note 6: The factory-set default value for the complete block of the MFR_NV_FAULT_LOG is FFh.

Note 7: MFR_DAC_CONFIG is only available for PAGES 0 to 11.