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MAX35101 Time-to-Digital Converter with Analog Front-End

General Description

The MAX35101 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end (AFE) solution for the ultrasonic heat meter and flow meter markets.

With a time measurement accuracy of 20ps and automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements.

Multihit capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, an autozero amplifier/comparator, real-time clock (RTC), and programmable receiver sensitivity provide the analog interface and control for a minimal electrical bill of material solution. The RTC provides an event timing mode that is configurable and runs cyclic algorithms to minimize microprocessor interactivity and increase battery life.

Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access and thus minimize current consumption.

For temperature measurement, the MAX35101 supports up to four (4) 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

On-board 8KB user flash allows the MAX35101 to be nonvolatile-configurable and provide nonvolatile energy use data to be logged. Configuration can be recalled anytime with a SPI command.

Benefits and Features

- High Accuracy Flow Measurement for Billing and Leak Detection
  - Time-to-Digital Accuracy Down to 20ps
  - Measurement Range Up to 8ms
  - Two Channels: Single-Stop Channel
- High Accuracy Temperature Measurement for Precise Heat and Flow Calculations
  - Up to Four (4) 2-Wire Sensors
  - PT1000 and PT500 RTD Support
- Maximizes Battery Life with Low Device and Overall System Power
  - Low 10µA ToF measurement and < 125nA Duty-Cycled Temperature Measurement
  - Event Timing Mode Reduces Host µC
- Overhead to Minimize System Power Consumption
  - 2.3V to 3.6V Single-Supply Operation
- High-Integration Solution Minimizes Parts Count and Reduces BOM Cost
  - 8KB of Nonvolatile Flash Memory for Data Logging
  - Built-in Real Time Clock
  - Small, 5mm x 5mm, 32-Pin TQFP Package
  - -40°C to +85°C Operation

Applications

- Ultrasonic Heat Meters
- Ultrasonic Water Meters
- Ultrasonic Gas Meters

Ordering Information ***appears at end of data sheet.***

19-6830; Rev 1; 1/15

maxim integrated™

Absolute Maximum Ratings

(Voltages relative to ground.)
Voltage Range on V_{CC} Pins.....-0.5V to +4.0V
Voltage Range on All Other Pins
(not to exceed 4.0V).....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 27.80mW/ºC above +70°C).....2222.20mW

Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C
ESD Protection (All Pins, Human Body Model) .....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.0	3.6	V
Input Logic 1 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.3	V
Input Logic 0 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IL}		-0.3		V_{CC} x 0.3	V
Input Logic 1 (32KX1)	$V_{IH32KX1}$		V_{CC} x 0.85		V_{CC} + 0.3	V
Input Logic 0 (32KX1)	$V_{IL32KX1}$		-0.3		V_{CC} x 0.15	V

Electrical Characteristics

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (CSW, $\overline{RST}$, SCK, DIN, $\overline{CE}$)	I_L		-0.1		+0.1	µA
Output Leakage ($\overline{INT}$, $\overline{WDO}$, T1,T2,T3,T4)			-0.1		+0.1	µA
Output Voltage Low (32KOUT)	V_{OL32K}	2mA			0.2 x V_{CC}	V
Output Voltage High (32KOUT)	V_{OH32K}	-1mA	0.8 x V_{CC}			V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	V_{OH}	-4mA	0.8 x V_{CC}			V
Output Voltage High (TC)	V_{OHTC}	V_{CC} = 3.3V, I_{OUT} = -4mA	2.9	3.1		V

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High (Launch_UP, Launch_DN)	$V_{OHLAUCH}$	V_{CC} = 3.3V, I_{OUT} = -50mA	2.8	3.0		V
Output Voltage Low ($\overline{WDO}$, $\overline{INT}$, DOUT, CMP_OUT/UP_DN)	V_{OL}	4mA			0.2 x V_{CC}	V
Pulldown Resistance (TC)	R_{TC}		650	1000	1500	Ω
Input Voltage Low (TC)	V_{ILTC}			0.36 x V_{CC}		V
Output Voltage Low (Launch_UP, Launch_DN)	$V_{OLLAUCH}$	V_{CC} = 3.3V, I_{OUT} = 50mA		0.2	0.4	V
Resistance (T1, T2, T3, T4)	R_{ON}			1		Ω
Input Capacitance ($\overline{CE}$, SCK, DIN, $\overline{RST}$, CSW)	C_{IN}	Not tested		7		pF
$\overline{RST}$ Low Time	t_{RST}				100	ns
CURRENT						
Standby Current	I_{DDQ}	No oscillators running, T_A = +25°C		0.1	1	µA
32kHz OSC Current	I_{32KHZ}	32kHz oscillator only (Note 4)		0.5	0.9	µA
4MHz OSC Current	I_{4MHZ}	4MHz oscillator only (Note 4)		40	85	µA
LDO Bias Current	I_{CCLDO}	I_{CCCPU} = 0 (Note 4)		15	35	µA
Time Measurement Unit Current	I_{CCTMU}	(Note 4)		4.5	8	mA
Calculator Current	I_{CCCPU}			2.5	5	mA
Device Current Drain	I_{CC3}	TOF_DIFF = 2 per second (3 hits), temperature = 1 per 30s		10		µA
	I_{CC6}	TOF_DIFF = 2 per second (6 hits), temperature = 1 per 30s		13		
FLASH Erase Current	I_{FLASH}			0.5	1	mA
ANALOG RECEIVER						
Analog Input Voltage (STOP_UP, STOP_DN)	V_{ANA}		10	700	2 x V_{CC} x (3/8)	mV_{P-P}
Input Offset Step Size	V_{STEP}			1		mV
STOP_UP/STOP_DN Bias Voltage	V_{BIAS}			V_{CC} x (3/8)		V
Receiver Sensitivity	V_{ANA}	Stop hit detect level (Note 5)	10			mV_{P-P}
TIME MEASUREMENT UNIT						
Measurement Range	t_{MEAS}	Time of flight	8		8000	µs
Time Measurement Accuracy	t_{ACC}	Differential time measurement		20		ps
Time Measurement Resolution	t_{RES}			3.8		ps

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH						
Data Retention	D_R	T_A = +25°C	100			Years
Flash Endurance	N_{FLASH}	T_A = +25°C	20k			Cycles
Block Flash Erase Time	t_{ERASE}				50	ms
LDO Stabilization Time	t_{STABLE}			135		µs
Word Write Time	t_{WRITE}			72	100	µs
Transfer Configuration to Flash Command Time	t_{CONFIG}			35		ms
EXECUTION TIMES						
Power-On-Reset Time	t_{RESET}	Reset to POR INT		275		µs
INIT Command Time	t_{INIT}	Command received when INIT bit set		2.5		ms
Case Switch Time	t_{CSW}	CSW pin logic-high until CSWI bit set		20		ns
CAL Command Time	t_{CAL}	Command received when CAL bit set		1.25		ms
SERIAL PERIPHERAL INTERFACE						
DIN to SCK Setup	t_{DC}				20	ns
SCK to DIN Hold	t_{CDH}			2	20	ns
SCK to DOUT Delay	t_{CDD}			5	20	ns
SCK Low Time	t_{CL}	V_{CC} ≥ 3.0V	25	4		ns
		V_{CC} = 2.3V	50	30		
SCK High Time	t_{CH}		25	4		ns
SCK Frequency	t_{CLK}	V_{CC} ≥ 3.0V			20	MHz
		V_{CC} = 2.3V			10	
$\overline{CE}$ to SCK Setup	t_{CC}			5	40	ns
SCK to $\overline{CE}$ Hold	t_{CCH}				20	ns
$\overline{CE}$ Inactive Time	t_{CWH}			2	40	ns
$\overline{CE}$ to DOUT High Impedance	t_{CCZ}			5	20	ns

Recommended External Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f_{32K}			32.768		kHz
32kHz Frequency Tolerance	$\Delta f_{32K}/f_{32K}$	T_A = +25°C	-20		+20	ppm
32kHz Load Capacitance	C_{L32K}			12.5		pF
32kHz Series Resistance	R_{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	F_{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	$\Delta f_{4M}/f_{4M}$	T_A = +25°C	-30		+30	ppm
4MHz Crystal Load Capacitance	C_{L4M}			12.0		pF
4MHz Crystal Series Resistance	R_{S4M}				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		T_A = +25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF
4MHz Ceramic Series Resistance					30	Ω

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: Currents are specified as individual block currents. Total current for a point in time can be calculated by taking the standby current and adding any block currents that are active at that time.

Note 5: Receiver sensitivity includes performance degradation contributed by STOP_UP and STOP_DN device pin input offset voltage and common mode drift.

Timing Diagrams

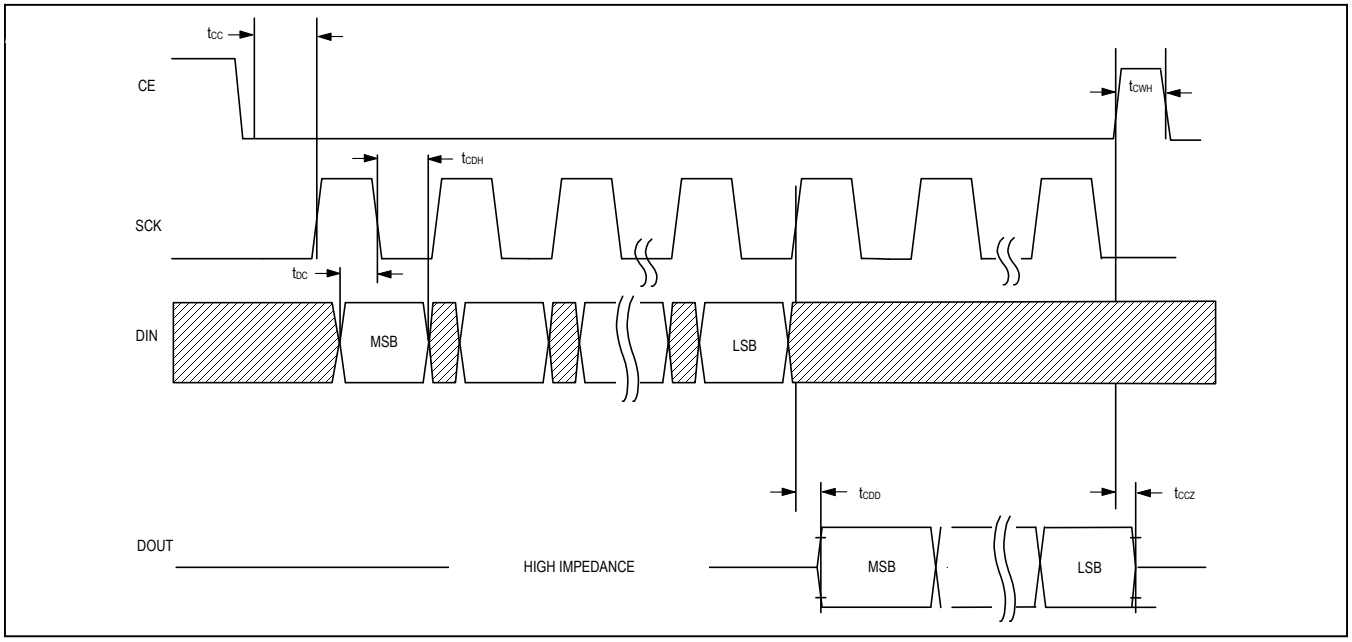


Figure 1. SPI Timing Diagram Read

Timing Diagrams (continued)

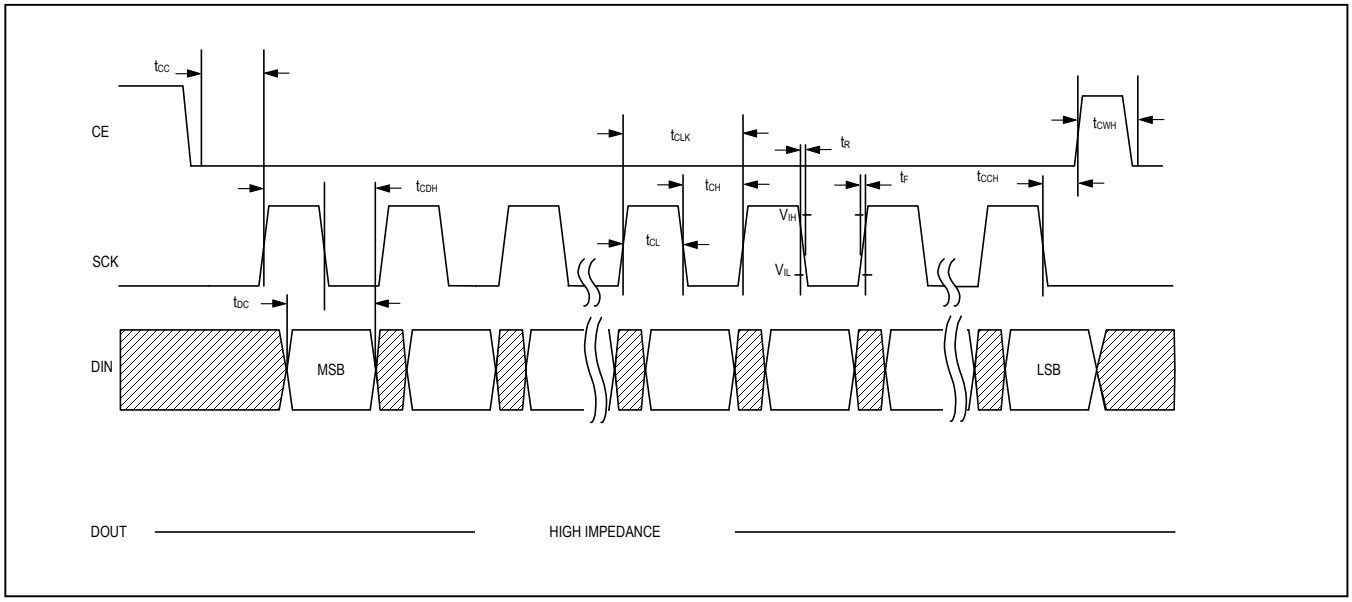
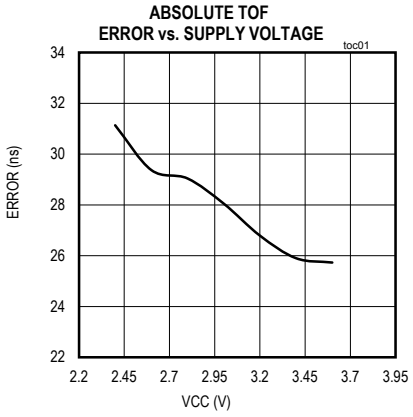
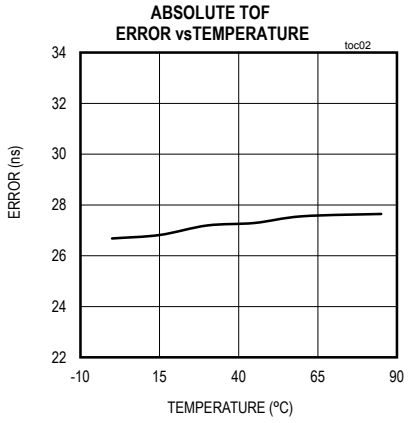


Figure 2. SPI Timing Diagram Write

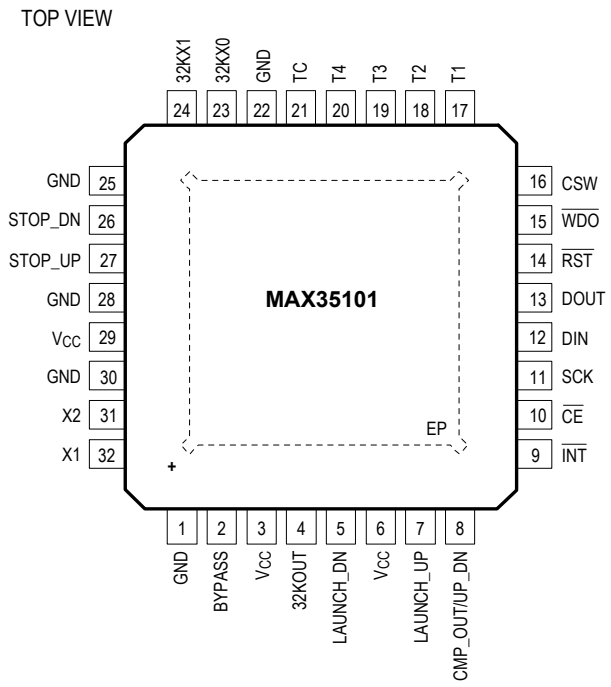
Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)





Pin Configuration



TQFP
(5mm x 5mm)

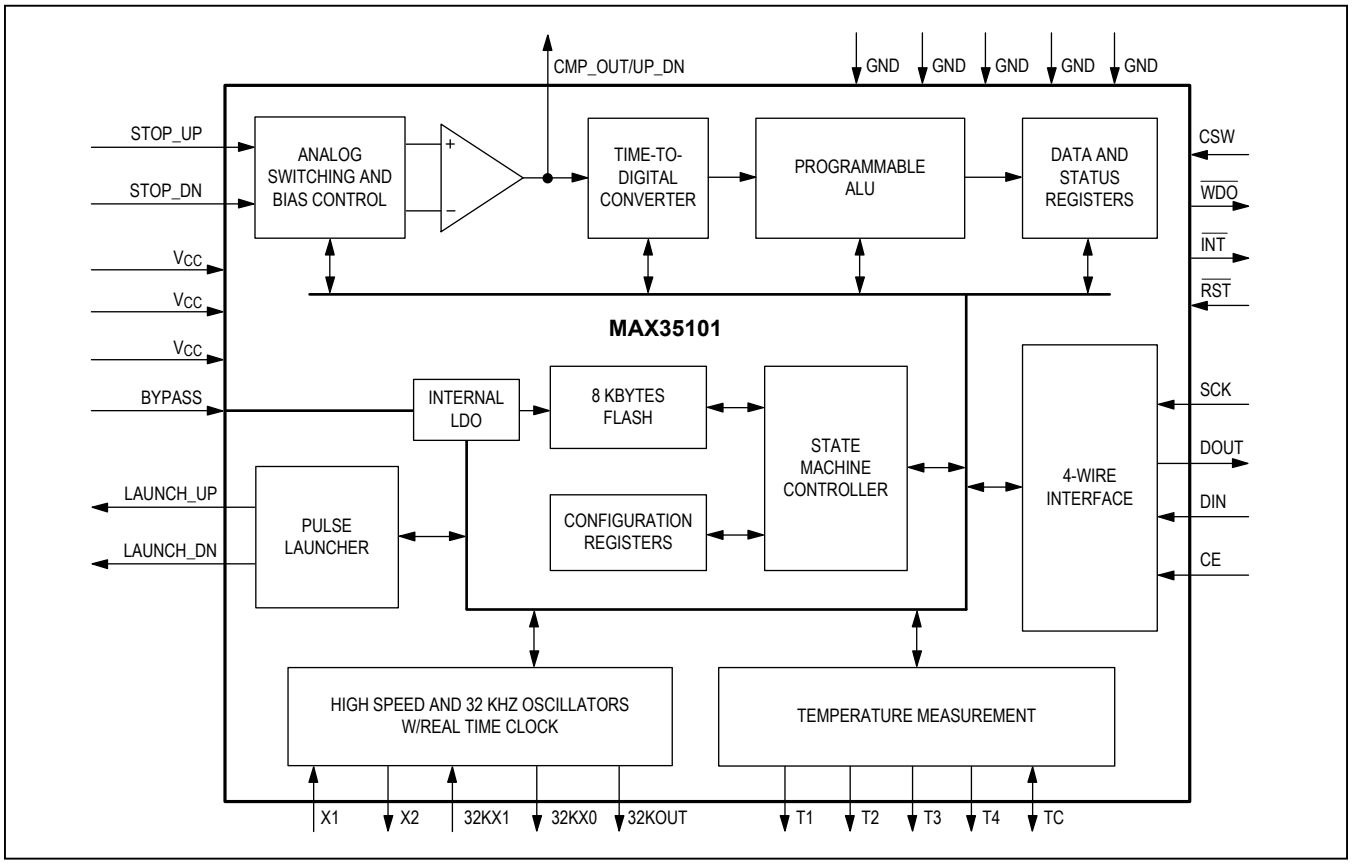
Pin Description

PIN	NAME	FUNCTION
1, 22, 25, 28, 30	GND	Device Ground
2	BYPASS	Connect this pin to ground with a capacitor (100nF) to provide stability for the on-board low-dropout regulator that is used to supply the flash circuitry. The effective series resistance of this capacitor needs to be in the 1Ω to 2Ω range.
3, 6, 29	V_{CC}	Main Supply. Typically sourced from a single lithium cell.
4	32KOUT	CMOS Output. Repeats the 32kHz crystal oscillator frequency.
5	LAUNCH_DN	CMOS Pulse Output Transmission in Downstream Direction of Water Flow
7	LAUNCH _UP	CMOS Pulse Output Transmission in Upstream Direction of Water Flow
8	CMP_OUT/UP_DN	CMOS Output. Indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output.
9	$\overline{INT}$	Active-Low Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
10	$\overline{CE}$	Active-Low CMOS Digital Input. Serial peripheral interface chip enable input.

Pin Description (continued)

PIN	NAME	FUNCTION
11	SCK	CMOS Digital Input. Serial peripheral interface clock input.
12	DIN	CMOS Digital Input. Serial peripheral interface data input.
13	DOUT	CMOS Output. Serial peripheral interface data output.
14	$\overline{RST}$	Active-Low CMOS Digital Reset Input
15	$\overline{WDO}$	Active-Low Open-Drain Watchdog Output
16	CSW	CMOS Digital Input. Case Switch. Active-high tamper detect input.
17	T1	Open-Drain Probe 1 Temperature Measurement
18	T2	Open-Drain Probe 2 Temperature Measurement
19	T3	Open-Drain Probe 3 Temperature Measurement
20	T4	Open-Drain Probe 4 Temperature Measurement
21	TC	Input/Output Temperature Measurement Capacitor Connection
23	32KX0	Connections for 32.768kHz Quartz Crystal. An external CMOS 32.768kHz oscillator can also drive the MAX35101. In this configuration, the 32KX1 pin is connected to the external oscillator signal and the 32KX0 pin is left unconnected.
24	32KX1	
26	STOP_DN	Downstream STOP Analog Input. Used for the signal that is received from the downstream transmission of a time-of-flight measurement.
27	STOP_UP	Upstream STOP Analog Input. Used for the signal that is received from the upstream transmission of a time-of-flight measurement.
31	X2	Connections for 4MHz Quartz Crystal. A ceramic resonator can also be used.
32	X1	
—	EP	Exposed Pad. Connect to GND.

Block Diagram



Detailed Description

The MAX35101 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end solution for the ultrasonic heat meter and flow meter markets.

With automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access.

For temperature measurement, the MAX35101 supports up to four (4) 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

The MAX35101 offers an event timing mode that is configurable and runs cyclic algorithms to minimize microprocessor interactivity and increase battery life.

The real-time clock (RTC) provides one programmable alarm and watchdog functionality.

A simple opcode based 4-Wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

On-board user flash allows the MAX35101 to be nonvolatile configurable and provides nonvolatile energy use data to be logged.

Time-of-Flight (TOF) Measurement Operations

TOF is measured by launching pulses from one piezoelectric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The MAX35101 contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The MAX35101 can measure two separate TOFs, which are defined as TOF up and TOF down.

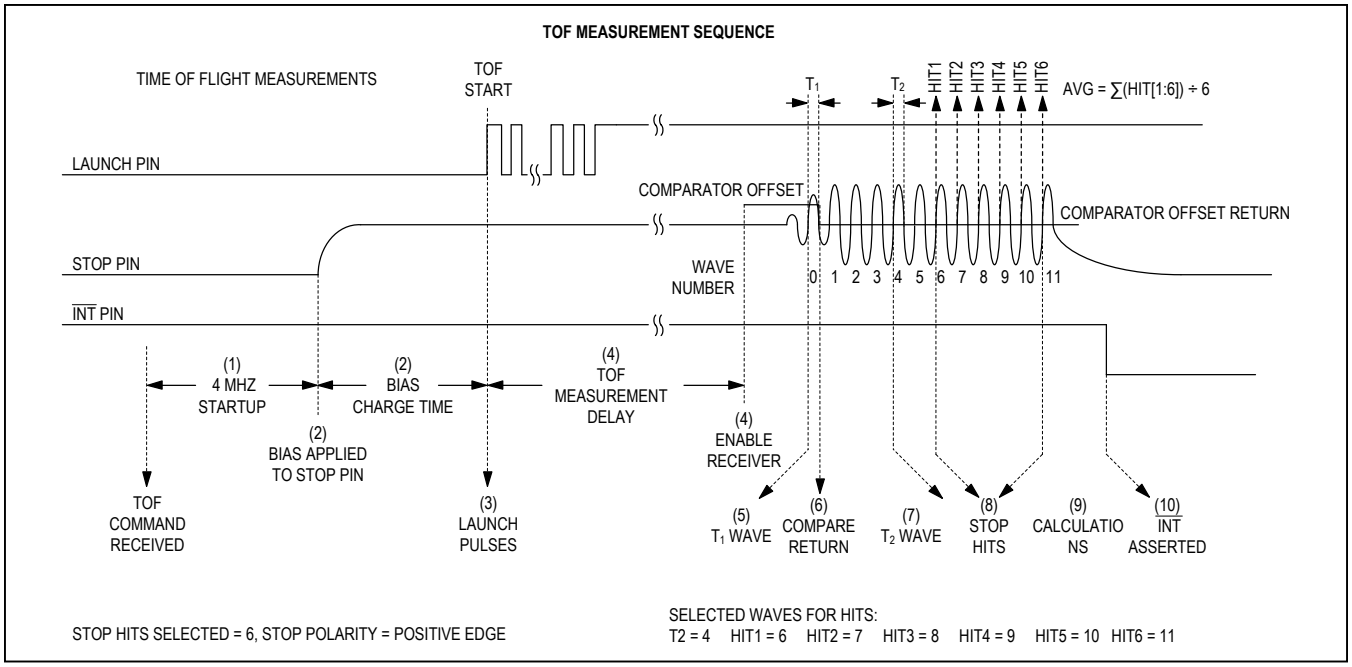


Figure 3. Time-of-Flight Sequence

A TOF up measurement has pulses launched from the LAUNCH_UP pin, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the STOP_UP pin. A TOF down measurement has pulses launched from the LAUNCH_DN pin, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the STOP_DN pin.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands. TOF_DIFF measurements can also be automatically executed using event timing mode commands EVTMG1 or EVTMG2.

The steps involved in a single TOF measurement are described here and shown in Figure 3.

1) The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
2) A common-mode bias is enabled on the STOP pin. This bias charge time is set by the CT[1:0] bits in the TOF1 register.
3) Once the bias charge time has expired, the pulse launcher drives the appropriate LAUNCH pin with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% duty-cycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses generates a start signal for the time-to-digital converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted by the start signal in the start/stop TDC timing (Figure 3).
4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate STOP pin are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
5) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the STOP pin according to the setting of the STOP_POL bit in the TOF1 register. The first stop hit is detected when a wave received at the STOP pin exceeds the comparator offset voltage, which is set in the TOF6 and TOF7 registers. This first detected wave is wave number 0. The width of the wave's pulse that exceeds the comparator offset voltage is measured and stored as the t1 time.
6) The offset of the comparator then automatically and immediately switches to the comparator return offset, which is set in the TOF6 and TOF7 registers.

7) The t_2 wave is detected and the width of the t_2 pulse is measured and stored as the t_2 time. The wave number for the measurement of the t_2 wave width is set by the T2WV[5:0] bits in the TOF2 register.

8) The preferred number of stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[2:0] bits in the TOF2 register. The wave number to measure for each stop hit is set by the HITx wave select bits in the TOF3, TOF4, and TOF5 registers.

9) After receiving all of the programmed hits, the MAX35101 calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t_1/t_2 and t_2/t_{ideal} are calculated and stored in the WVRUP or WVRDN register.

10) Once all of the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a read register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is 7FFFh or (2^{15}-1) x t_{4MHz} or ~ 8.19 ms. The maximum size of the fraction is: FFFFh or $\frac{2^{16}-1}{2^{16}} \times t_{4MHz}$. or ~ 249.9961 ns.

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTER VALUE		CONVERTER VALUE
TOF_DIFFInt (hex)	**TOF_DIFFFrac (hex)**	**TOF DIFF VALUE (ns)**
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

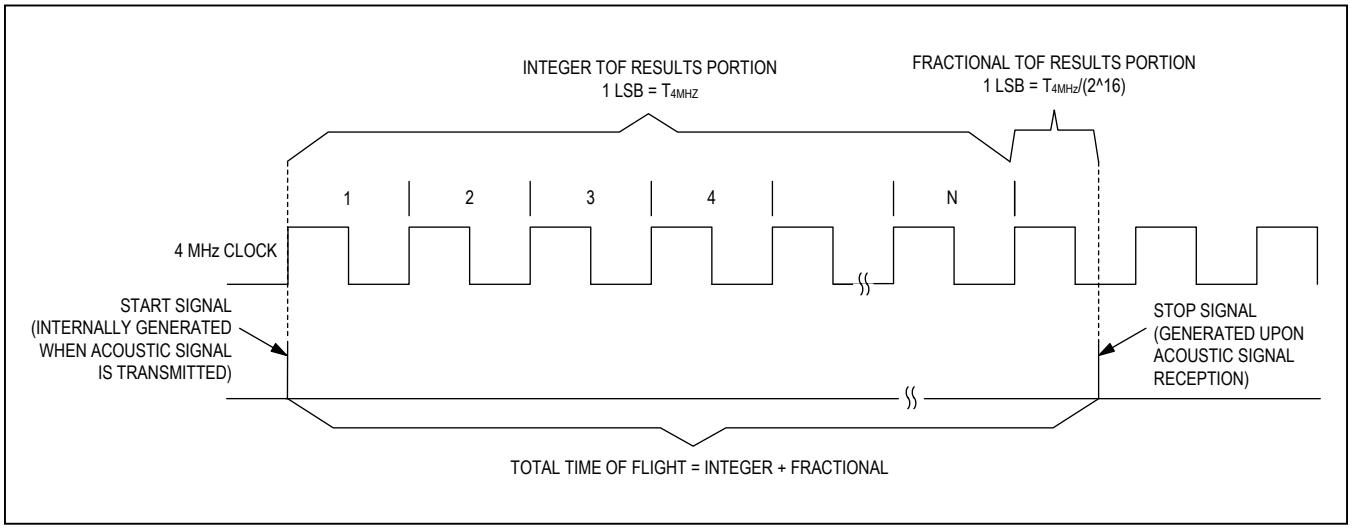


Figure 4.Start/Stop for Time-to-Digital Timing

Early Edge Detect

This early edge detect method of measuring the TOF of acoustic waves is used for all of the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the MAX35101 to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +127 LSBs if triggering on a positive edge and -127 LSBs if triggering on a negative edge, with 1 LSB = V_{CC}/3072. Separate input offset settings are available for the upstream received signal and the downstream received signal. The input offset for the upstream received signal is programmed using the C_OFFSETUP[6:0] bits in the TOF6 register. The input offset for the downstream received signal is programmed using the C_OFFSETDN[6:0] bits in the TOF7 register. Once the first hit is detected, the time t1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to a preprogrammed comparator offset value. This return offset value has a range of +127 LSBs to -128 LSBs in 1 LSB steps and is programmed into the C_OFFSETUPR[7:0] bits in the TOF6 register for the upstream received signal and programmed into the C_OFFSETDNR[7:0] bits in the TOF7 register. This preprogrammed comparator offset return value is provided to allow for common-mode shifts that can be present in the received acoustic wave.

The MAX35101 is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5, this is the 7th wave after the early edge detect wave. The selection of the t_2 wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{ideal} is calculated and registered for the user. For this calculation, t_{ideal} is1/2 the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all of the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. The TOF_DIFF_AVG Results registers do not include the error measurement. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

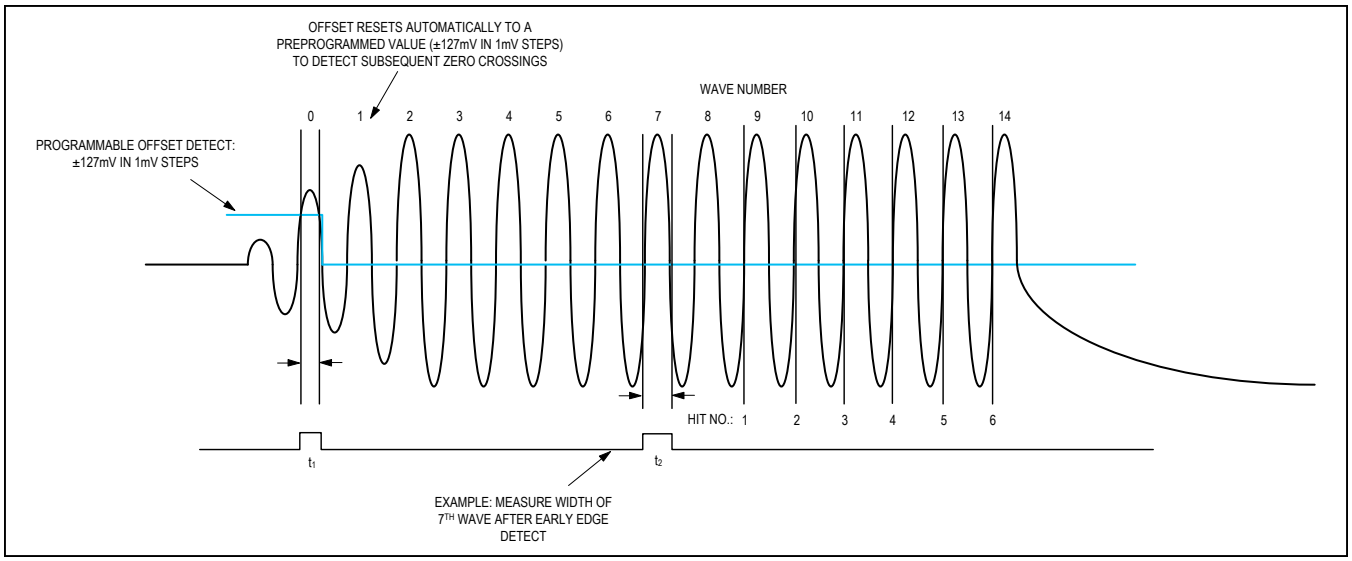


Figure 5. Early Edge Detect Received Wave Example

Temperature Measurement Operations

A temperature measurement is a time measurement of the RC circuit connected to the temperature port device pins T1 through T4 and TC. The TC device pin has a driver to charge the timing capacitor. The ports that are measured and the order in which the measurement is performed is selected with the TP[1:0] bits in the Event Timing 2 register.

Figure 6 depicts a 1000Ω platinum RTD with a 100nF NPO COG 30ppm/°C capacitor. It shows two dummy cycles with 4 temperature port evaluation measurements and 4 real temperature port measurements. This occurs when setting the TP[1:0] bits in the Event Timing 2 register to 11b.

The dummy 1 and dummy 2 cycles represent preamble measurements that are intended to eliminate the dielectric absorption of the temperature measurement capacitor. These dummy cycles are executed using a RTD Emulation resistor of 1000Ω internal to the MAX35101. This dummy path allows the dielectric absorption effects of the capacitor to be eliminated without causing any of the RTDs to be unduly self-heated. The number of dummy measurements to be taken ranges from 0 to 7. This parameter is configured by setting the PRECYC[2:0] bits in the Event Timing 2 register.

Following the dummy cycles, an evaluation, TXevaluate, is performed. This measurement allows the MAX35101 to maximize power efficiency by evaluating the temperature of the RTDs with a coarse measurement prior to a real measurement. The coarse measurement provides an approximation to the TDC converter. During the real measurement, the TDC can then optimize its measurement parameters to use power efficiently. These evaluate cycles are automatically inserted according to the order of ports selected with the of the Temperature Port bits. The time from the start of one port's temperature measurement to the next port's temperature measurement is set using with the PORTCYC[1:0] bits in the Event Timing 2 register.

Once all the temperature measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register is also set and the $\overline{INT}$ pin asserts (if enabled).

Actual temperature is determined by a ratiometric calculation. If T1 and T2 are connected to platinum RTDs and T3 and T4 are connected to the same reference resistor (as shown in the System Diagram), then the ratio of T1/T3 = R_{RTD1}/R_{REF} and T2/T4 = R_{RTD2}/R_{REF}. The ratios R_{RTD1}/R_{REF} and R_{RTD2}/R_{REF} can be determined by the host microprocessor and the temperature can be derived from a look-up table of Temperature vs. Resistance for each of the RTDs utilizing interpolation of table entries if required.

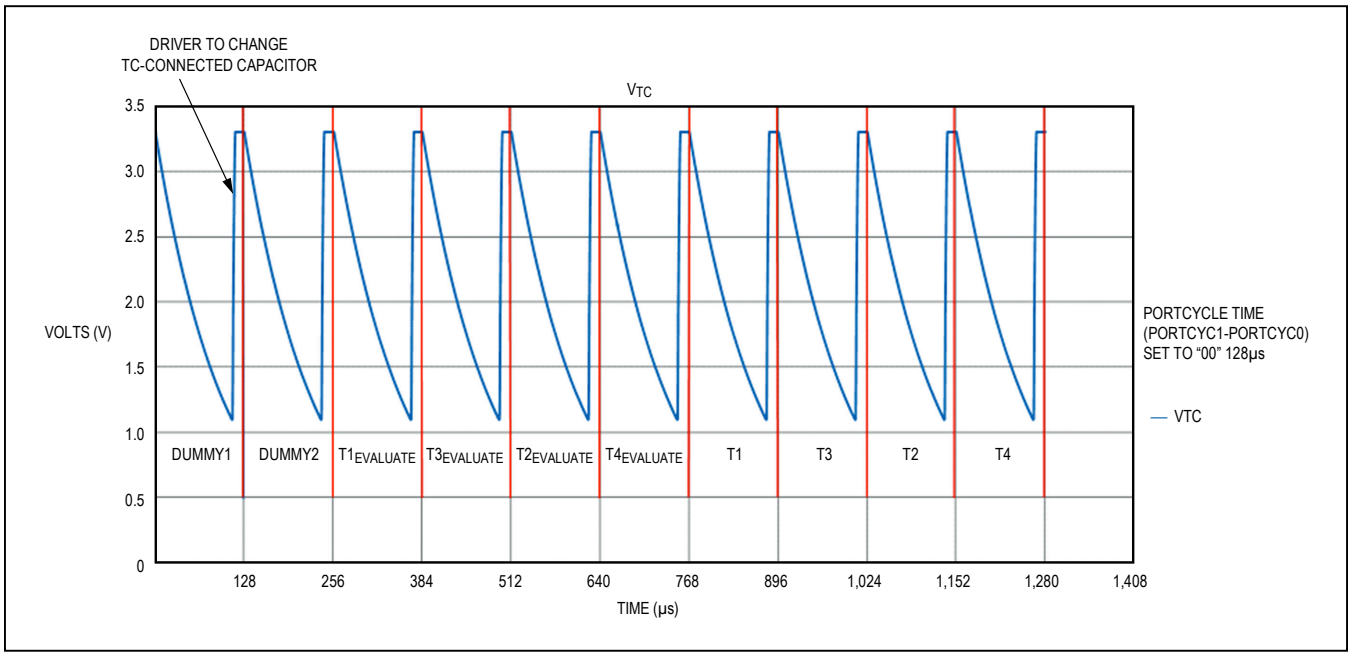


Figure 6. Temperature Command Execution Cycle Example

Temperature Error Handling

The temperature measurement unit can detect open and/or short-circuit temperature probes. If the resultant temperature reading in less than 8µs, then the MAX35101 writes a value of 0000h to the corresponding Results registers to indicate a short-circuit temperature probe. If the measurement process does not discharge the TC pin below the threshold of the internal temperature comparator within 2µs of the time set by the PORTCYC[1:0] bits in the Event Timing 2 register, then an open circuit temperature probe error is declared. The MAX35101 writes a value of FFFFh to the corresponding results registers to indicate an open circuit temperature probe, the TO bit in the Interrupt Status register is set, and the $\overline{INT}$ pin asserts (if enabled). If the temperature measurement error is caused by any other problems, then the MAX35101 writes a value of FFFFh to each of the temperature port results registers indicating that all of the temperature port measurements are invalid.

Event Timing Operation

The event timing mode of operation is an advanced feature that allows the user to configure the MAX35101 to perform automatic measurement cycles. This allows the host microcontroller to enter low-power mode and only awaken upon assertion of the MAX35101 $\overline{INT}$ pin (if enabled) when new measurement data is available. By using the TOF_DIFF and temperature commands and configuring the appropriate TOFx registers and the Event Timing registers, the event timing modes directs the MAX35101 to provide complete data for a sequence of measurements captured on a cyclical basis. There are three versions of the EVTMG commands.

- **EVTMG2:** Performs automatic TOF_DIFF measurements. The parameters and operation of the TOF measurement are described in the *Time-of-Flight (TOF) Measurement Operations* section.
- **EVTMG3:** Performs automatic Temperature measurements. The parameters and operation of the Temperature measurements are described in the *Temperature Measurement Operations* section.
- **EVTMG1:** Performs automatic TOF_DIFF and Temperature measurements.

Continuous Event Timing Operation

The MAX35101 can be configured to continue running event timing sequences at the completion of any sequence. If the ET_CONT bit in the Calibration and Control register is set, the currently executing EVTMGx command continues to execute until a HALT command is received by the MAX35101. If the ET_CONT bit is clear, automatic execution of event timing stops after the completion of a full sequence of measurements.

Continuous Interrupt Timing Operation

When operating in event timing mode, the $\overline{INT}$ pin can be asserted (if enabled) either after each TOF or temperature measurement, or at the completion of the sequence of measurements. If the CONT_INT bit in the Calibration and Control register is set to a 1, then the $\overline{INT}$ pin asserts (if enabled) at the completion of each TOF or temperature command. This allows the host microcontroller to interrogate the current event for accuracy of measurement. If the CONT_INT bit is set to a 0, then the $\overline{INT}$ pin only asserts (if enabled) at the completion of a sequence of measurements. This allows the host microcontroller to remain in a low-power sleep mode and only wake-up upon the assertion of the $\overline{INT}$ pin.

Error Handling During Event Timing Operation

During execution of event timing modes, any error that occurs during a TOF_DIFF or temperature measurement are handled as described in the corresponding error handling sections. Calibration can be executed during event timing operation, if programmed to do so with the calibration configuration bits in the Calibration and Control register. If a calibration error occurs, this is handled as described in the *Error Handling During Calibration* section. If any of these errors occur, the event timing operation does not terminate, but continues operation.

When making TOF measurements in event timing mode, the MAX35101 provides additional data in the TOF_Cycle_Count/TOF_Range register that can be used to check the validity of all of the TOF measurements. The TOF_Cycle_Count is the number of valid error-free TOF measurements that were recorded during an Event Timing Sequence. If a TOF error occurs, the TOF_Cycle_Count register will not be incremented. The TOF_Range is the range of all valid TOF measurements that were captured during a sequence.

When making temperature measurements in event timing mode, the MAX35101 provides additional data in the Temp_Cycle_Count register. This count increments after every valid error-free temperature measurement and can be used to check the validity of all of the temperature measurements. Also, the Temperature Average Results registers, TxAVG, are not updated with the error measurement if a temperature error occurs during event timing operation.

Event Timing Mode 2

The EVTMG2 command execution causes the TOF_DIFF command to be executed automatically with programmable repetition rates and programmable total counts as shown in Figure 7.

During execution of the EVTMG2 command, each TOF_DIFF command execution cycle causes the MAX35101 to compute a TOF_DIFF measurement (AVGUP register minus AVGDN register) as well as the running average of TOF_DIFF measurements (TOFF_DIFF_AVG register). The setting of the TDF[3:0] bits in the Event Timing 1 register selects the rate at which TOF_DIFF commands are executed. The setting of the TDM[4:0] bits in the Event Timing 1 register determines the number of TOF_DIFF measurements to be taken during the sequence.

Once all of the TOF_DIFF measurements in the sequence are captured, the TOF_DIFF_AVG register contains the average of the differences of the resultant AVGDN and AVGUP Results register content of each TOF_DIFF measurement. After the TOF_DIFF_AVG registers are updated, the TOF_EVTMG bit is set in the Interrupt Status register and the $\overline{INT}$ pin asserts (if enabled).

Event Timing Mode 3

The EVTMG3 command execution causes the temperature command to be executed automatically with programmable repetition rates and programmable total counts (Figure 9).

During execution of the EVTMG3 command, each Temperature command execution cycle computes the running average of the measurement of each temperature port. The results are provided in the Tx_AVGInt and TxAVGFrac Results registers.

The setting of the TMF[5:0] bits in the Event Timing 1 register selects the rate at which temperature commands are executed. The setting of the TMM[4:0] bits in the Event Timing 2 register determines the number of temperature measurements to be taken during the sequence.

Once all of the temperature measurements in the sequence are captured Tx_AVGInt and TxAVGFrac Results registers contains the average of all the temperature measurements in the sequence. After these registers are updated, the Temp_EVTMG bit is set in the Interrupt Status register and the $\overline{INT}$ pin asserts (if enabled).

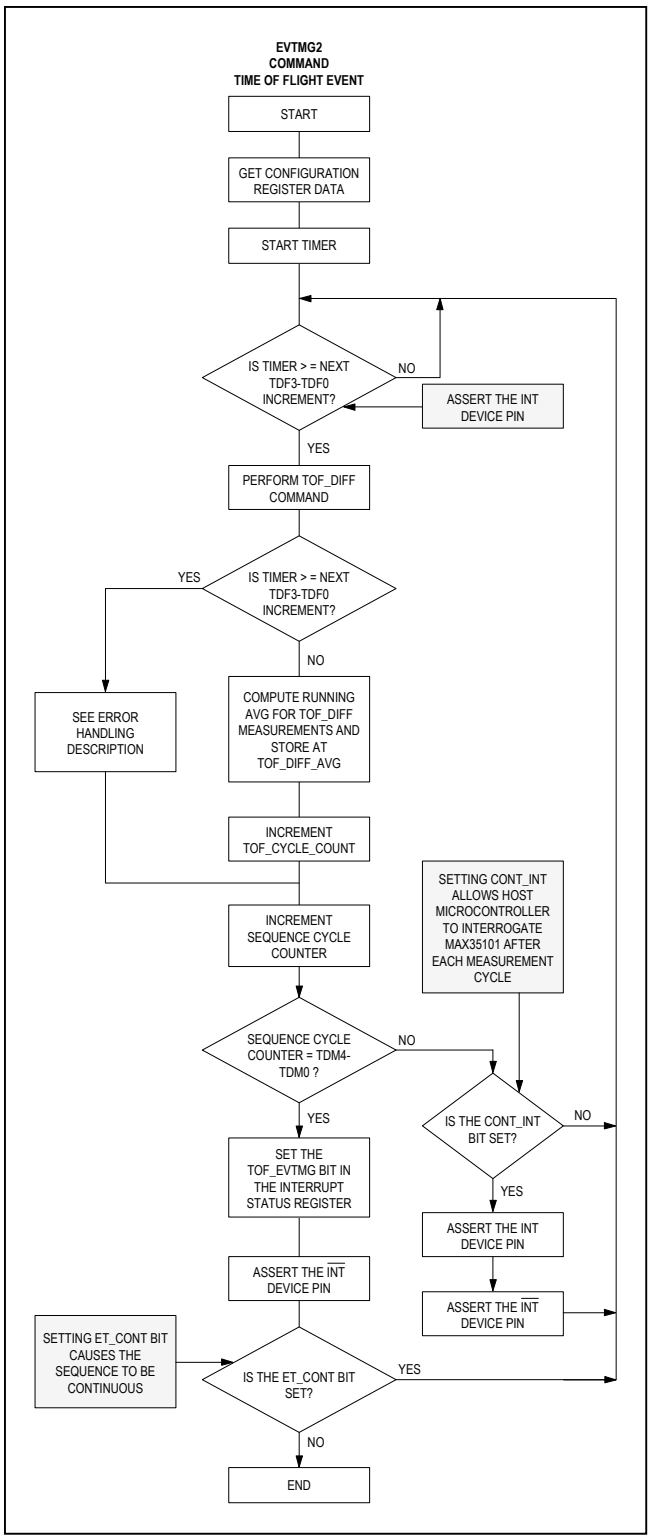


Figure 7. EVTMG2 Command

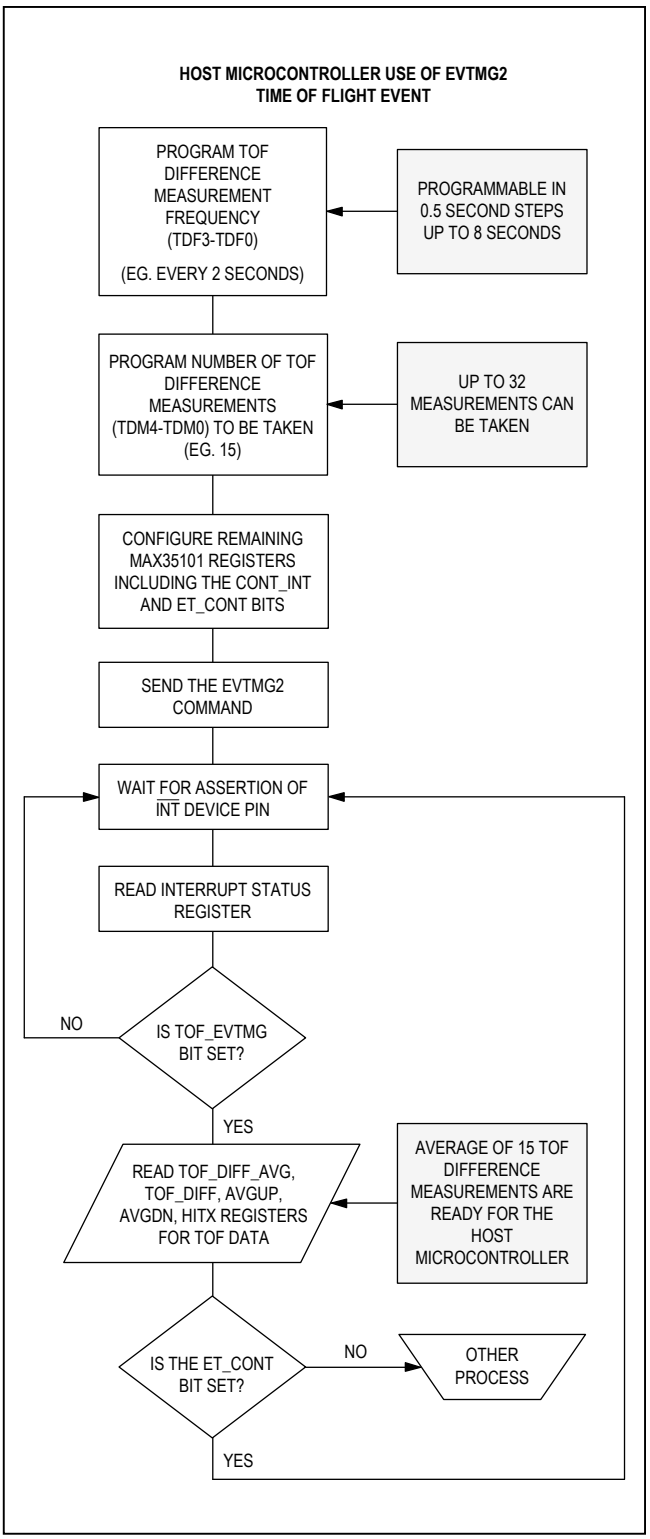


Figure 8. EVTMG2 Pseudo Code

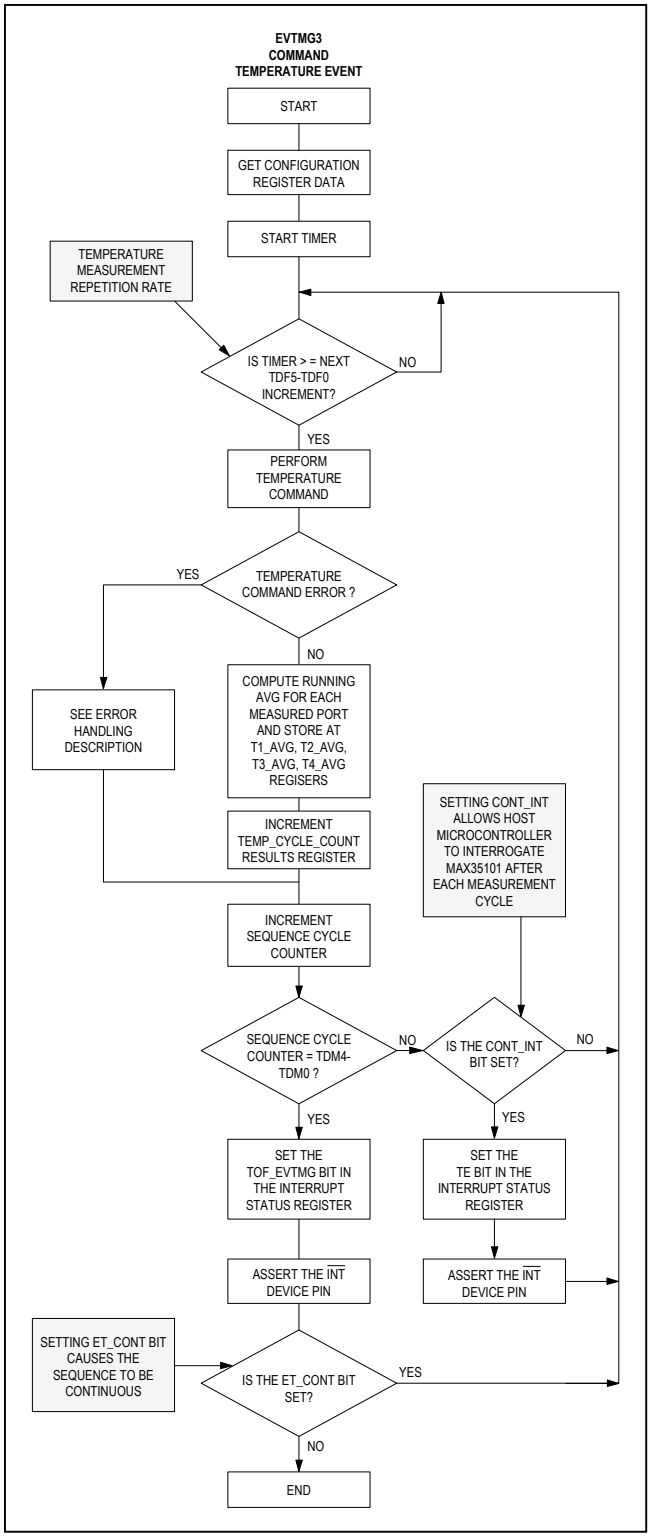


Figure 9. EVTMG3 Command

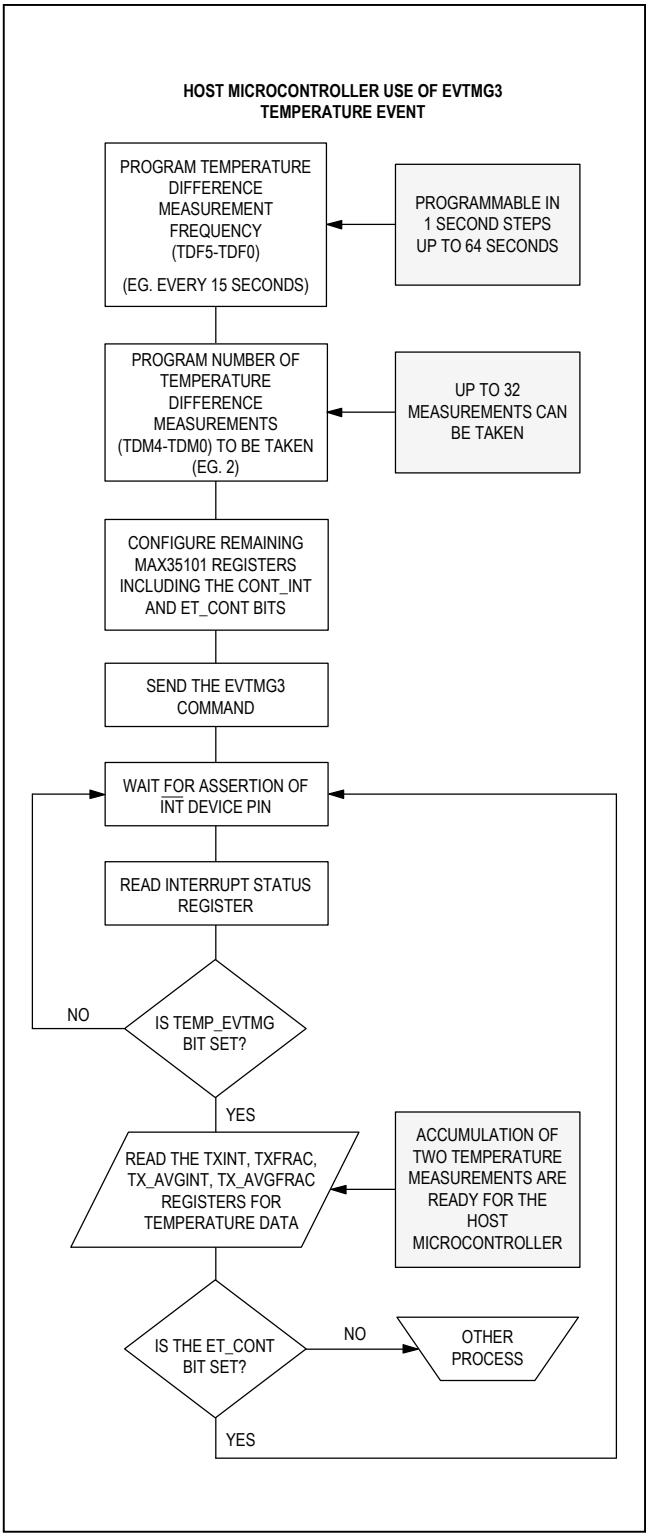


Figure 10. EVTMG3 Pseudo Code

Event Timing Mode 1

The EVTMG1 command execution causes the TOF_DIFF command and the temperature command to be executed automatically with programmable repetition rates and programmable total counts. In essence, both the EVTMG2 and EVTMG3 commands are simultaneously executed in a synchronous manner.

Setting up the TOF measurements for automatic execution in event timing mode 1 is identical to setting these up for execution with event timing mode 2. Likewise, setting up the temperature measurements is identical to setting these up for execution using event timing mode 3.

If the TOF_DIF command repetition rate and the temperature command repetition rate cause both measurements to be required at the same time, the TOFF_DIF command takes precedent. Upon completion of the TOFF_DIFF command, the pending temperature command is executed (Figure 12).

Once all of the TOF_DIFF measurements in the sequence are complete, the TOF_EVTMG bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled). Likewise, when all of the temperature measurements in the sequence are completed, the Temp_EVTMG bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled). It should be noted that depending upon the selected rates and number of cycles, the TOF_DIFF and temperature measurements can complete their sequences at different times. This causes the $\overline{INT}$ pin to assert (if enabled) before both sequences are complete.

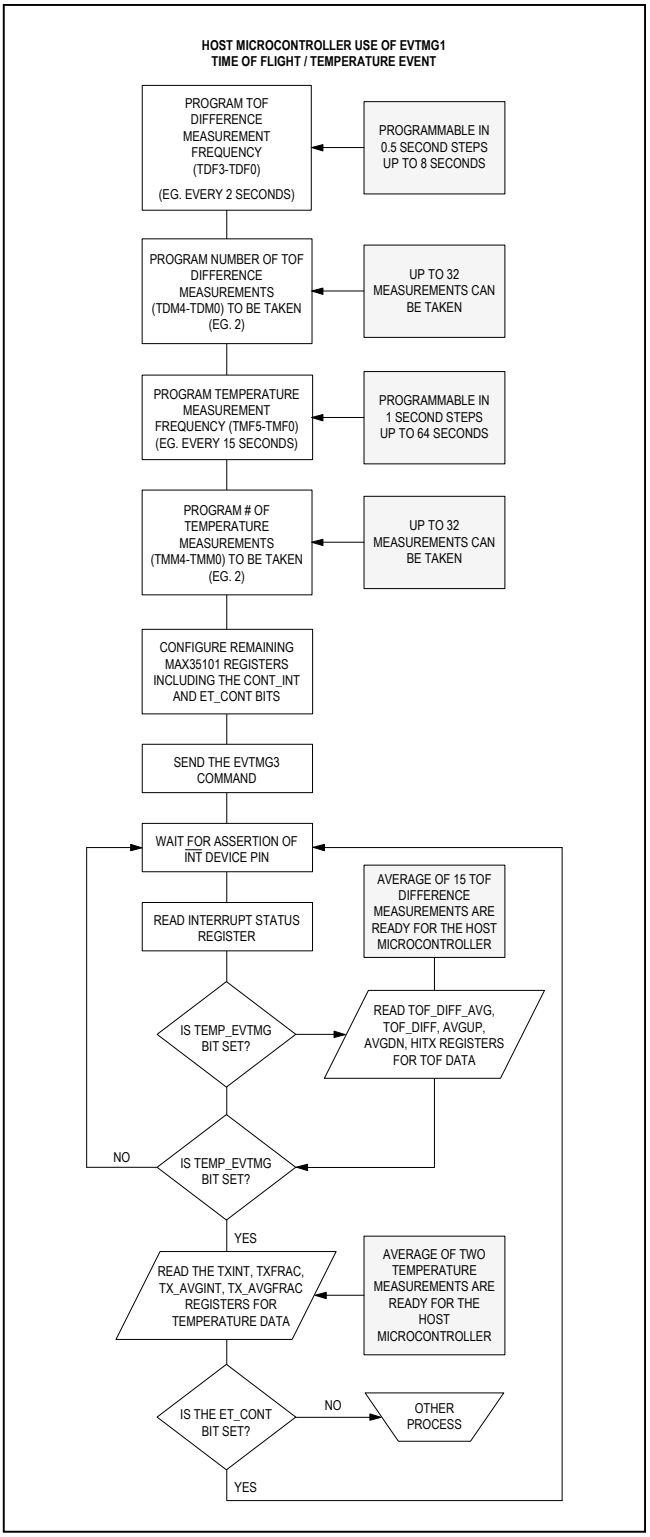


Figure 11. EVTMG1 Pseudo Code

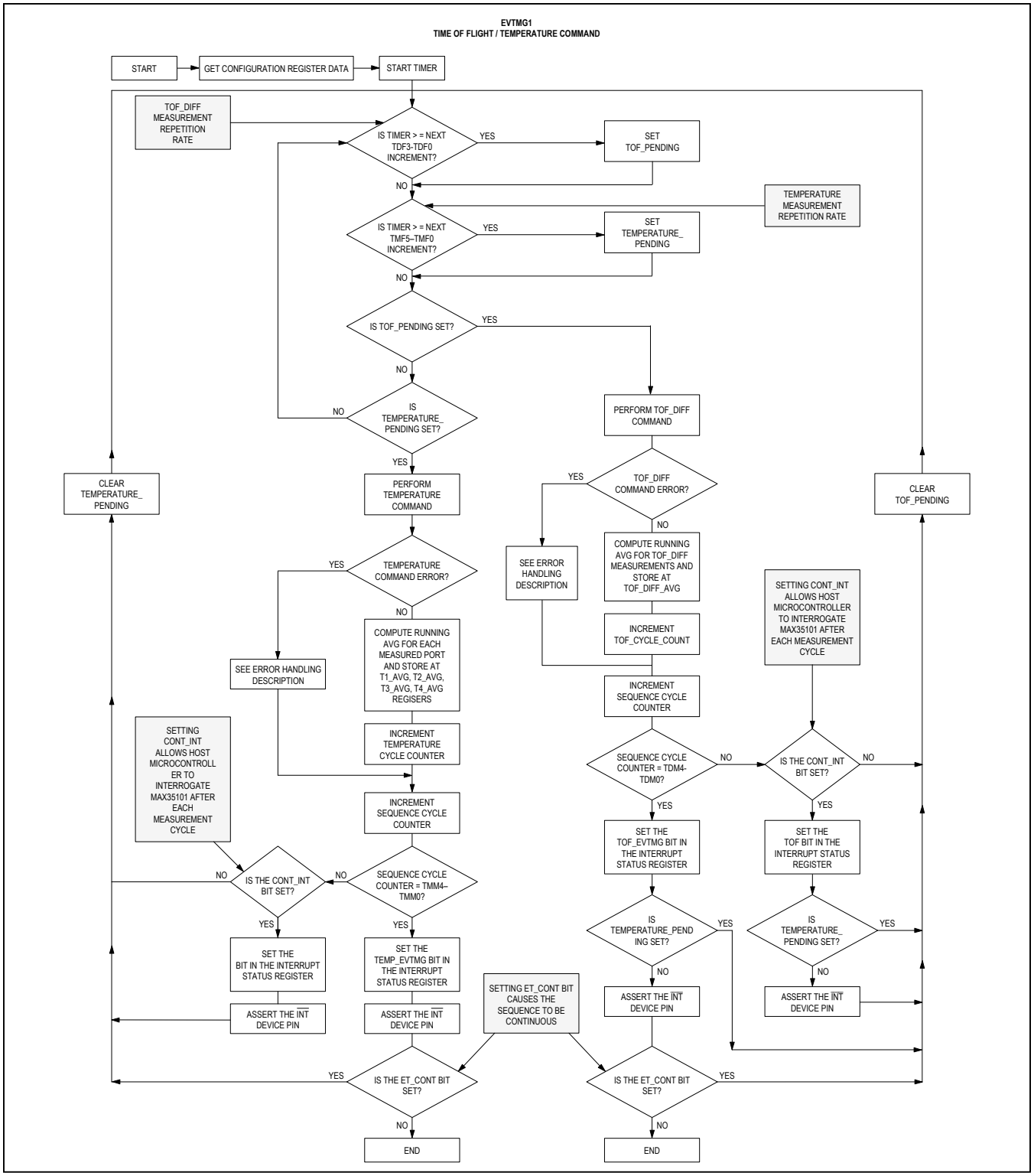


Figure 12. EVTMG1 Command

Calibration Operation

For more accurate results, calibration of the TDC can be performed. Calibration allows the MAX35101 to perform a calibration measurement that is based upon the 32.768kHz crystal, which is the most accurate clock in the system. This calibration is used when a ceramic oscillator is used in place of an AT-cut crystal for the 4MHz reference. The MAX35101 automatically generates START and STOP signals based upon edges of the 32.768kHz clock. The number of 32.768kHz clock periods that are used and then averaged are selected with the CAL_PERIOD[3:0] bits in the Calibration and Control register. The TDC measures the number of 4MHz clock pulses that occur during the 32.768kHz pulses. The measured time of a 32.768kHz clock pulse is reported in the CalibrationInt and CalibrationFrac Results registers. These results can then be used as a gain factor for calculating actual time-to-digital converter measurement if the CAL_USE bit in the Event Timing 2 Register is set.

Following is a description of an example calibration. Each TDC measurement is a 15-bit fixed-point integer value concatenated with a 16-bit fractional value binary representation of the number of t_{4MHz} periods that contribute to the time result, the actual period of t_{4MHz} needs to be known. If the CAL_PERIOD[3:0] bits in the Calibration and Control register are set to 6, then 6 measurements of 32.768kHz periods are measured by the TDC and then averaged. The expected measured value would be 30.5176µs/250ns = 122.0703125 t_{4MHz} periods. Assume that the 4MHz ceramic resonator is actually running at 4.02MHz. The TDC measurement unit would then measure 30.5176µs/248.7562ns = 122.6806641 t_{4MHz} periods and this result would be returned in the Calibration Results register. For all TDC measurements, a gain value of 122.0703125/122.6806641 = 0.995024876 would then be applied.

Calibration is performed at the following events:

- When the Calibration command is sent to the MAX35101. At the completion of this calibration, the CAL bit in the Interrupt Status register and the $\overline{INT}$ pin asserts (if enabled).
- During event timing operation, automatic calibrations can be performed before executing TOF or temperature measurements. This is selectable with the CAL_CFG[2:0] bits in the Event Timing 2 register. Upon completion of an automatic calibration during event timing, the result is updated in the Calibration Results register, but the CAL bit in the Interrupt Status register is not set and the $\overline{INT}$ pin does not assert.

Error Handling During Calibration

Since calibration can be set to be automatic by configuring the CAL_CFG[2:0] bits in the Event Timing 2 register, any errors that occur during the Calibrate command stop the CalibrationInt and the CalibrationFrac Results registers from being updated with new calibration coefficients. The results for the previous Calibration data remain in these two registers and are used for scaling measured results. If the calibration error is caused by the internal calibration time measurement exceeding the time set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

RTC, Alarm, Watchdog, and Tamper Operation

RTC Operation

The MAX35101 contains a real-time clock that is driven by a 32kHz oscillator. The time and calendar information is obtained by reading the appropriate register words. The time and calendar are set or initialized by writing the appropriate register words. The contents of the time and calendar registers are in the Binary-Coded Decimal (BCD) format. The clock/calendar provides hundredths of seconds, tenths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year valid up to 2100. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The MAX35101 real-time clock can be programmed for either 12-hour or 24-hour formats. If using the 24-hour format, Bit6 (12 HR MODE) of the Mins_Hrs register should be cleared to 0 and then Bit5 represents the 20-hour indicator. If using the 12-hour format, Bit6 should be set to 1 and Bit5 represents AM (if 0) or PM (if 1). The day-of-week register increments at midnight. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Alarm Operation

The MAX35101 real-time clock provides one programmable alarm. The alarm is activated when either the AM1 or AM2 bits in the Real-Time Clock register are set. Based upon these bits, an alarm can occur when either the minutes and/or hours programmed in the Alarm register match the current value in the Mins_Hrs register. When an alarm occurs, the AF bit in the Interrupt Status register is set and the $\overline{INT}$ device pin asserts (if enabled).

For proper alarm function, programming of the ALARM register HOURS bits must match the format (12- or 24-hour modes) used in the Mins_Hrs register.

Watchdog Operation

The MAX35101 also contains a watchdog alarm. The Watchdog Alarm Counter register is a 16-bit BCD counter that is programmable in 10ms intervals from 0.01s to 99.99s. A seed value may be written to this register representing the start value for the countdown. The watchdog counter begins decrementing when the WD_EN bit in the RTC register is set.

An immediate read of Watchdog Alarm Counter register returns the value just written. A read after a wait duration causes a value seed minus wait to be returned. For example if the seed value was 28.01s, an immediate read returns 28.01. A read after a 4s returns 24.01s. The value read out for any read operation is a snapshot obtained at the instant of a serial read operation.

A write operation to the Watchdog Alarm Counter register causes a reload with the newly written seed.

When the watchdog is enabled and a nonzero value is written into the Watchdog Alarm Counter register, the Watchdog Alarm Counter register decrements every 1/100s, until it reaches zero. At this point, the WF bit in the Real-Time Clock register is set and the $\overline{WDO}$ pin asserts low for typically 250ms. At the end of the pulse, the $\overline{WDO}$ pin becomes high impedance.

The WF flag remains set until cleared by writing WF to a logic 0 in the Real-Time Clock register. If the WF bit is cleared while the $\overline{WDO}$ device pin is being held low, the $\overline{WDO}$ device pin is immediately released to its high-impedance state. Writing a seed value of 0 does not cause the WF bit to assert.

Tamper Detect Operation

The MAX35101 provides a single input that can be connected to a device case switch and used for tamper detection. Upon detection of a case switch event the CSWA in the Control register and the CSWI bit in the Interrupt Status register is set and the $\overline{INT}$ device pin is asserted (if enabled).

Device Interrupt Operations

The MAX35101 is designed to optimize the power efficiency of a flow metering application by allowing the host microprocessor to remain in a low-power sleep mode, instead of requiring the microprocessor to keep track of complex real-time events being performed by the MAX35101. Upon completion of any command, the MAX35101 alerts the host microprocessor using the $\overline{INT}$ pin. The assertion of the $\overline{INT}$ pin can be used to awaken the host microprocessor from its low power mode. Upon receiving an interrupt on the $\overline{INT}$ pin, the host microprocessor should read the Interrupt Status Register to determine which tasks were completed.

Interrupt Status Register

The interrupt status register contains flags for all for all commands and events that occur within the MAX35101. These flags are set when the event occurs or at the completion of the executing command. When the Interrupt Status Register is read, all asserted bits are cleared. If another interrupt source has generated an interrupt during the read, these new flags assert following the read.

$\overline{INT}$ Pin

The $\overline{INT}$ pin asserts when any of the bits in the Interrupt Status register are set. The $\overline{INT}$ pin remains asserted until the Interrupt Status register is read by the user and all bits in this register are clear. In order for the $\overline{INT}$ pin to operate, it must first be enabled by setting the INT_EN bit in the Calibration and Control register.

Serial Peripheral Interface Operation

Four pins are used for SPI-compatible communications: DOUT (serial-data out), DIN (serial-data in), $\overline{CE}$ (chip enable), and SCK (serial clock). DIN and DOUT are the serial data input and output pins for the devices, respectively. The $\overline{CE}$ input initiates and terminates a data transfer. SCK synchronizes data movement between the master (microcontroller) and the slave (MAX35101). The SCK, which is generated by the microcontroller, is active only when $\overline{CE}$ is low and during opcode and data transfer to any device on the SPI bus. The inactive clock polarity is logic-low. DIN is latched on the falling edge of SCK. There is one clock for each bit transferred. Opcode bits are transferred in groups of eight, MSB first. Data bits are transferred in groups of sixteen, MSB first.

The serial peripheral interface is used to access the features and memory of the MAX35101 using an opcode/command structure.

Opcode Commands

Table 2 shows the opcode/commands that are supported by the device.

Table 2. Opcode Commands

GROUP	COMMAND	OPCODE FIELD (HEX)	ADDRESS FIELD
Execution Opcode Commands	TOF_Up	00h	N/A
	TOF_Down	01h	N/A
	TOF_Diff	02h	N/A
	Temperature	03h	N/A
	Reset	04h	N/A
	Initialize	05h	N/A
	Transfer configuration to flash	06h	N/A
	EVTMG1	07h	N/A
	EVTMG2	08h	N/A
	EVTMG3	09h	N/A
	HALT	0Ah	N/A
	LDO_Timed	0Bh	N/A
	LDO_ON	0Ch	N/A
	LDO_OFF	0Dh	N/A
	Calibrate	0Eh	N/A
Register Opcode Commands	Read register	B0h through FFh. Each hex value represents the location of a single 16-bit register.	N/A
	Write register	30h through 43h. Each hex value represents the location of a single 16-bit register.	N/A
Flash Opcode Commands	Read flash	90h	0000h - 1FFFh 8 Kbytes Even Only
	Write flash	10h	0000h - 1FFFh 8 Kbytes Even Only
	Block erase flash	13h	0000h - 1FFFh

Execution Opcode Commands

The device supports several single byte opcode commands that cause the MAX35101 to execute various routines. All commands have the same SPI protocol sequence as shown in Figure 13. Once all 8 bits of the opcode are received by the MAX35101 and the $\overline{CE}$ device pin is deasserted, the MAX35101 begins execution of the specified command as described in that Command's description.

TOF_UP Command (00h)

The TOF_UP command generates a single TOF measurement in the upstream direction. Pulses launch from the LAUNCH_UP pin and are received by the STOP_UP pin. The measured hit results are reported in the HITxUPInt and HITxUPFrac registers, with the calculated average of all the measured hits being reported in the AVGUPInt and AVGUPFrac register. The t_1/t_2 and t_2/tideal wave ratios are reported in the WVRUP register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Note: The TOF_UP command yields a result that is only of use when used in conjunction with the TOF_DN command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

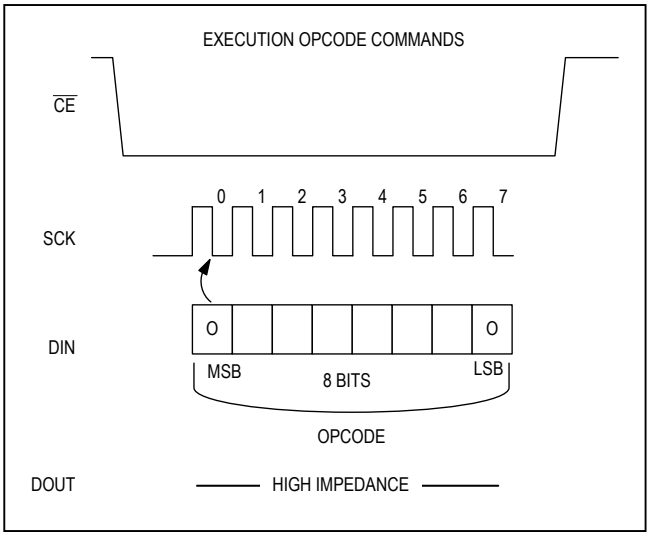


Figure 13. Execution Opcode Command Protocol

TOF_Down Command (01h)

The TOF_DOWN command generates a single TOF measurement in the downstream direction. Pulses launch from the LAUNCH_DN pin and are received by the STOP_DN pin. The measured hit results are reported in the HITxDnInt and HITxDnFrac registers, with the calculated average of all the measured hits being reported in the AVGDNInt and AVGDNFrac register. The t_1/t_2 and t_2/t_{ideal} wave ratios are reported in the WVRDN register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Note: The TOF_Down command yields a result that is only of use when used in conjunction with the TOF_UP command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

TOF_DIFF Command (02h)

The TOF_DIFF command performs back-to-back TOF_UP and TOF_DN measurements as required for a metering application. The TOF_UP sequence is followed by the TOF_DN sequence. The time between the start of the TOF_UP measurement and the start of the TOF_DN measurement is set by the TOF_CYC[2:0] bits in the TOF2 register. Upon completion of the TOF_DN measurement, the results of AVGUP minus AVGDN is computed and stored at the TOF_DIFFInt and TOF_DIFFFrac Results register locations. Once these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Temperature Command (03h)

The temperature command initiates a temperature measurement sequence as described in the *Temperature Measurement Operations* section. The characteristics the temperature measurement sequence depends upon the settings in the Event Timing 1 register, and Event Timing 2 register. Once all the measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register also is set and the $\overline{INT}$ pin asserts (if enabled).

Reset Command (04h)

The reset command essentially performs the same function as a power-on reset (POR), and causes all of the Configuration registers to be set to their prior programmed values stored in flash and all of the Results registers and the Interrupt Status register to be cleared and set to zero.

Initialize Command (05h)

The initialize command must be executed after all configuration of the device is complete. This initializes the time-to-digital converter so that TOF and temperature commands can be executed. The MAX35101 sets the INIT bit in the Interrupt Status register and asserts the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the initialize command has completed and the next desired command can be sent to the MAX35101.

Transfer Configuration to Flash Command (06h)

This command causes the Configuration register map to be transferred to flash for nonvolatile (NV) storage. The MAX35101 automatically turns on the LDO for the duration of this transfer. Upon device reset, the content of this flash restores the Configuration registers. This flash is not part of the 8KB array, and is reserved solely for the transfer configuration to the flash command. The MAX35101 sets the flash bit in the Interrupt Status register and asserts the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the transfer configuration to the flash command has completed and the next command can be sent to the device.

EVTMG1 Command (07h)

The EVTMG1 command initiates the event timing mode 1 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF and Temperature measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, Event Timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG2 Command (08h)

The EVTMG2 command initiates the event timing mode 2 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG3 Command (09h)

The EVTMG3 command initiates the event timing mode 3 advanced automatic measurement feature. This timing mode performs automatic temperature measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, Event timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

HALT Command (0Ah)

The HALT command is sent to the MAX35101 to stop any of the three EVTMG1/2/3 commands. All register data content is frozen and the SPI is then made available for access by the host microcontroller for commands, memory access, and register access. The HALT command takes time to execute. Since the EVTMGx commands are comprised of multiple TOF_DIFF and Temperature commands, the HALT command causes the MAX35101 to evaluate its own state and complete the currently executing TOF_DIFF or temperature command. Once the HALT command has completed, all registers update and the MAX35101 sets the halt bit in the Interrupt Status register and then asserts the $\overline{INT}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source.

LDO_Timed Command (0Bh)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_Timed command to the MAX35101 prior to the desired flash access command (read, write, block erase), the internal regulator is enabled and powers the flash circuitry. The LDO bit is set in the Interrupt Status register and the $\overline{INT}$ device pin asserts (if enabled) when the internal regulator has been turned on and is stable which takes approximately t_{STABLE}. The host microprocessor, upon detection of the asserted $\overline{INT}$ device pin, should read the Interrupt Status register LDO bit to determine that the internal regulator is stable and the flash is now ready to be accessed. The internal regulator remains enabled for a continuous period until the $\overline{CE}$ device pin is deasserted after any flash command (read, write, block erase). The LDO_Timed command is used in place of the LDO_ON command when a data access to the flash is required in a short burst. This minimizes SPI access since the LDO_OFF command is not required to be sent to the MAX35101 to turn off the internal regulator.

LDO_ON Command (0Ch)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_ON command to the MAX35101 prior to the desired flash access command (read, write, block erase), the internal regulator is enabled and powers the flash circuitry. The LDO bit is set in the Interrupt Status register and the $\overline{INT}$ device pin asserts (if enabled) when the internal regulator has been turned on and is stable which takes approximately t_{STABLE}. The host microprocessor, upon detection of the asserted $\overline{INT}$ device pin, should read the Interrupt Status register LDO bit to determine that the internal regulator is stable and the flash is now ready to be accessed. The internal regulator remains enabled for a continuous period until the LDO_OFF command is received by the MAX35101. The LDO_ON command is generally used when the host microprocessor needs to perform multiple-word writes to the MAX35101 since multiple-word writes require that the $\overline{CE}$ device pin be toggled after every word of data written. The LDO_ON command prevents the LDO from automatically disabling itself after each transition of the $\overline{CE}$ device pin.

LDO_OFF Command (0Dh)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_OFF command to the MAX35101, the internal regulator is disabled and the Interrupt Status register LDO bit is cleared. The $\overline{INT}$ device pin is not asserted. The LDO_OFF command is used in conjunction with the LDO_ON command.

Calibrate Command (0Eh)

The calibrate command performs the calibration routine as described in the calibration operation section. When the calibrate command has completed the measurement, the Calibration Results register contains the measured 32kHz period measuremnt value, the MAX35101 sets the calibration bit in the Interrupt Status register and then asserts the $\overline{INT}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source and then read the Calibration Results register to be able to calculate the 4MHz ceramic oscillator gain factor.

Register Opcode Commands

To manipulate the register memory, there are two commands supported by the device: Read Register and Write register. Each register accessed with these commands is 16 bits in length. These commands are used to access all sections of the memory map including the RTC and Watchdog registers, Configuration registers, Conversion Results registers, and Status registers. The Conversion Results registers and the Interrupt Status register of the Status registers are all read only.

Read Register Command

The opcode must be clocked into the DIN device pin before the DOUT device pin produces the register data. The SPI protocol sequence is shown in Figure 14.

The read register command can also be used to read consecutive addresses. In this case, the data bits are continuously delivered in sequence starting with the MSB of the data register that is addressed in the opcode, and continues with each SCK rising edge until the $\overline{CE}$ device pin is deasserted as shown in Figure 15. The address counter automatically increments.

Write Register Command

This command applies to all writable registers. See the *Register Memory Map* for more detail. The SPI protocol sequence is shown in Figure 16.

The write register command can also be used to write consecutive addresses. In this case, the data bits are continuously received on the DIN device pin and bound for the initial starting address register that is addressed in the opcode. The address counter automatically increments after each 16 bits of data if the SCK device pin is continually clocked and the $\overline{CE}$ device pin remain asserted as shown in Figure 17.

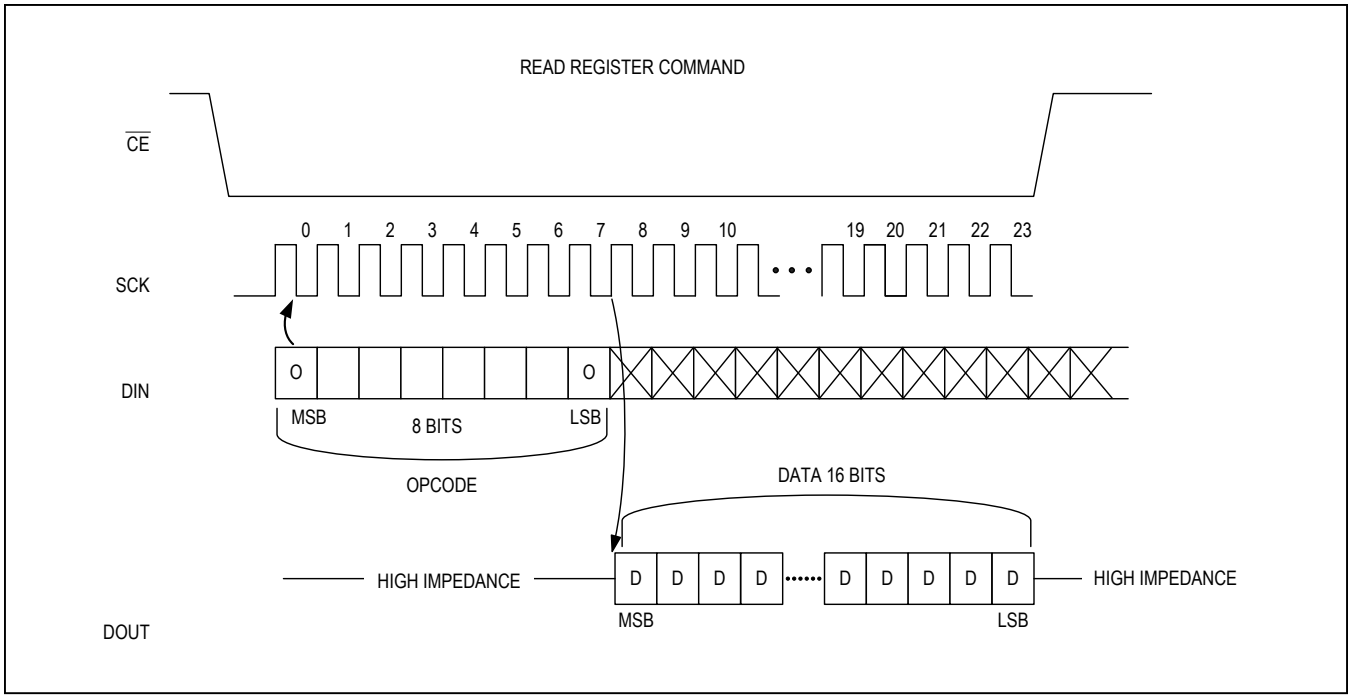


Figure 14. Read Register Opcode Command Protocol