Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX35104

Gas Flow Meter SoC

General Description

The MAX35104 is a gas flow meter system-on-chip (SoC) targeted as an analog front-end solution for the ultrasonic gas meter and medical ventilator markets. With a time measurement accuracy of 700ps and automatic differential time of flight (TOF), the device makes for simplified computation of gaseous flow.

Power consumption is the lowest available with ultra-low 62µA time-of-flight measurement and 125nA duty-cycled temperature measurement. Multi-hit (up to six per wave) capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, a configurable three-stage integrated operational amplifier chain amplifier, and an ultra-low input offset comparator provide the analog interface and control for a minimal electrical bill of material solution. A programmable high-voltage (up to 30V) pulse launcher provides up to 19dB of transducer launch amplitude adjustment to compensate for transducer aging and temperature, pressure, humidity affects. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements and programmable receiver hit accumulators to minimize the host microprocessor access. For temperature measurement, the device supports a single 2-wire PT1000 platinum resistive temperature detector (RTD) or NTC thermistor. A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

Applications

- Ultrasonic Gas Meters
- Medical Ventilators

Benefits and Features

- High Accuracy Flow Measurement for Billing and Leak Detection
  - Time-to-Digital Accuracy Down to 700ps Measurement Range Up to 400µs
  - 2 Channels: Single-Stop Channel
- High Accuracy Temperature Measurement for Precise Flow Calculations
  - One 2-Wire Sensor: PT1000, PT500 RTD, and Thermistor Support
- Maximizes Battery Life with Low Device and Overall System Power
  - Ultra-Low 62µA TOF Measurement and 125nA Duty-Cycled Temperature Measurement
  - Event Timing Mode with Randomizer Reduces Host µC Overhead to Minimize System Power Consumption
  - 2.3V to 3.6V Single-Supply Operation
- High Integration Solution Minimizes Parts Count and Reduces BOM Cost
  - Built-In Real-Time Clock
  - Small, 5mm x 5mm, 40-Pin TQFN Package
  - -40°C to +85°C Operation

***Ordering Information* appears at end of data sheet.**

19-8501; Rev 0; 3/16

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES (continued)

Absolute Maximum Ratings

(Voltage relative to ground.)
Voltage Range on V_{CC} Pins.....-0.5V to +4.0V
Voltage Range on All Other
Pins (not to exceed 4.0V).....-0.5V to (V_{CC} + 0.3V)
Voltage Range on High Voltage Pins.....32V
Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 35.70mW/ºC above +70ºC).....2857.10mW

Operating Temperature Range.....-40ºC to +85ºC
Junction Temperature.....+150ºC
Storage Temperature Range.....-55ºC to +125ºC
Soldering Temperature (reflow).....+260ºC
Lead Temperature (soldering, 10s).....+300ºC
ESD Protection (All Pins, Human Body Model).....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.3	3.6	V
Input Logic 1 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.3	V
Input Logic 0 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IL}		-0.3		V_{CC} x 0.3	V
Input Logic 1 (32KX1)	$V_{IH32KX1}$		V_{CC} x 0.85		V_{CC} + 0.3	V
Input Logic 0 (32KX1)	$V_{IL32KX1}$		-0.3		V_{CC} x 0.15	V

Electrical Characteristics

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (CSW, $\overline{RST}$, SCK, DIN, $\overline{CE}$, $\overline{CIP}$, $\overline{CIN}$)	I_L		-0.1		+0.1	µA
Output Leakage ($\overline{INT}$, $\overline{WDO}$, T1,T2)	O_L		-0.1		+0.1	µA
Output Voltage Low (32KOUT)	V_{OL32K}	2mA			0.2 x V_{CC}	V
Output Voltage High (32KOUT)	V_{OH32K}	-1mA	0.8 x V_{CC}			V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	V_{OH}	-4mA	0.8 x V_{CC}			V
Output Voltage High (TC)	V_{OHTC}	V_{CC} = 3.6V, I_{OUT} = -4mA	3.4			V
Output Voltage Low ($\overline{WDO}$, $\overline{INT}$, DOUT, MP_OUT/UP_DN)	V_{OL}	4mA			0.2 x V_{CC}	V
Pulldown Resistance (TC)	R_{TC}	ITC	650	1000	1750	Ω

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Low (TC)	V_{ILTC}			0.36 x V_{CC}		V
Pulldown (RXP, RXN)		AFE_BP = 0, pins disabled		80		µA
Resistance (T1, T2)	R_{ON}			1.5		Ω
Input Capacitance ($\overline{CE}$, SCK, DIN, $\overline{RST}$, CSW)	C_{IN}	Not tested		7		pF
$\overline{RST}$ Low Time	t_{RST}				100	ns
CURRENT						
Standby Current	I_{DDQ}	No oscillators running			10	µA
32kHz OSC Current	I_{32KHZ}	32kHz oscillator only, V_{CC} = 3.6V		0.42	1	µA
4MHz OSC Current	I_{4MHZ}	4MHz oscillator only, V_{CC} = 3.6V		82	135	µA
Time Measurement Unit Current	I_{CCTMU}	V_{CC} = 3.3V		4.3	8	mA
Calculator Current	I_{CCCPU}			1.2	3	mA
Device Current Drain	I_{CC}	V_{CC} = 3.3V, TOF_DIFF = 2 per second, temperature = 1 per 30 seconds		62		µA
TRANSMITTER: BOOST SWITCH$_{ER}$						
Output Voltage Range				9 30		V
Programmable Output Voltage Step Size				1.7		V
Output Switching Frequency			100		200	kHz
Current-Limit Trip Level	V_{CS-SW}		100	150	200	mV
TRANSMITTER: FET GATE DRIVER						
External FET Gate Charge	Q_G				2	nC
Rise Time	t_R	C_L = 1nF (Figure 2, Note 3)		100		ns
Fall Time	t_F	C_L = 1nF (Figure 2, Note 3)		100		ns
TRANSMITTER: HIGH-VOLTAGE REGULATOR						
Output Voltage Range		Low		5.4		V
Output Voltage Range		High		26.4		V
Programmable Output Voltage Step Size				1.7		V
Output Voltage Accuracy				5		%
Load Regulation		I_{LOAD} = 15mA		150		mV

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER: PIEZO DRIVER						
Driver Output Resistance Pulling Down (n-Channel)	$R_{ON-N-PD}$	V_{IN} = 10V, I_{LD} =10mA		50		Ω
Driver Output Resistance Pulling Up (p-Channel)	$R_{ON-P-PU}$	V_{IN} = 10V, I_{LD} =10mA		50		Ω
Output Leakage Current	I_{LK-PD}			0.05		µA
Rise Time	t_{R-PD}	C_L = 1nF		100		ns
Fall Time	t_{F-PD}	C_L = 1nF		100		ns
FILTER SPECIFICATION						
Input Amplitude			1		10	mV
Differential Input Impedance				4		kΩ
Programmable Gain Resolution	Per bit			1.5		dB
COMPARATOR SPECIFICATION						
Input Offset Voltage	V_{OFFSET}	C_OFFSETUP or C_OFFSETDN register programmed to 00h		2		mV
Input Offset Step Size	V_{STEP}			1		mV
Receiver Sensitivity	V_{SENS}	Stop hit detect level	10			mV_{P-P}
ANALOG RECEIVER: BANDPASS FILTER						
Center Frequency Accuracy	f_{0A}	f = 200kHz		6		%
Q Range				4		Hz/Hz
				12		
Q Accuracy				20		%
200kHz PERFORMANCE						
A1 Differential Gain		200kHz, V_{IN} = $6mV_{P-P}$		10		V/V
UP/DN Gain Match				±1		%

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGA Gain	PGA[3:0] = 0000b		V_{OUT} = 600mV$_{P-P}$	V_{IN} = 19.0mV$_{P-P}$		3.16		V/V
	PGA[3:0]= 0001b			V_{IN} = 16.3mV$_{P-P}$		3.69		
	PGA[3:0]= 0010b			V_{IN} = 14.0mV$_{P-P}$		4.30		
	PGA[3:0]= 0011b			V_{IN} = 12.0mV$_{P-P}$		5.01		
	PGA[3:0]= 0100b			V_{IN} = 10.3mV$_{P-P}$		5.84		
	PGA[3:0]= 0101b			V_{IN} = 8.80mV$_{P-P}$		6.81		
	PGA[3:0]= 0110b			V_{IN} = 7.55mV$_{P-P}$		7.94		
	PGA[3:0]= 0111b			V_{IN} = 6.48mV$_{P-P}$		9.26		
	PGA[3:0]= 1000b			V_{IN} = 5.56mV$_{P-P}$		10.8		
	PGA[3:0]= 1001b			V_{IN} = 4.76mV$_{P-P}$		12.6		
	PGA[3:0]= 1010b			V_{IN} = 4.09mV$_{P-P}$		14.7		
	PGA[3:0]= 1011b			V_{IN} = 3.51mV$_{P-P}$		17.1		
	PGA[3:0]= 1100b			V_{IN} = 3.02mV$_{P-P}$		20.0		
	PGA[3:0]= 1101b			V_{IN} = 2.58mV$_{P-P}$		23.3		
	PGA[3:0]= 1110b			V_{IN} = 2.21mV$_{P-P}$		27.1		
	PGA[3:0]= 1111b			V_{IN} = 1.90mV$_{P-P}$		31.6		
Filter Gain at 200kHz Trim			V_{IN} = 19mV$_{P-P}$			1.0		V/V
Filter Gain with Bypass			V_{IN} = 19mV$_{P-P}$			0.01		V/V

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIME MEASUREMENT UNIT						
Measurement Range	t_{MEAS}	Time of flight	4		8000	µs
Time Measurement Accuracy	t_{ACC}	Differential time measurement		700		ps
Time Measurement Resolution	t_{RES}			3.8		ps
EXECUTION TIMES						
Power-On-Reset Time		V_{CC} MIN to POR bit set		275		µs
Case Switch Time		CSW pin logic-high until CSWI bit set		20		ns
CAL Command Time		Command received until CAL bit set		1.25		ms
SERIAL PERIPHERAL INTERFACE (Figure 1 and Figure 2)						
DIN to SCK Setup	t_{DC}				20	ns
SCK to DIN Hold	t_{CDH}			2	20	ns
SCK to DOUT Delay	t_{CDD}			5	20	ns
SCK Low Time	t_{CL}	$V_{CC} \geq 3.0V$	25	4		ns
		V_{CC} = 2.3V	50	30		
SCK High Time	t_{CH}		25	4		ns
SCK Frequency	t_{SCK}				20	MHz
SCK Rise and Fall	t_R, t_F				10	ns
$\overline{CE}$ to SCK Setup	t_{CC}			5	40	ns
SCK to $\overline{CE}$ Hold	t_{CCH}				20	ns
$\overline{CE}$ Inactive Time	t_{CWH}			2	40	ns
$\overline{CE}$ to DOUT High Impedance	t_{CCZ}			5	40	ns

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Recommended External Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f_{32K}			32.768		kHz
32kHz Frequency Tolerance	$\Delta f_{32K}/f_{32K}$	25°C	-20		+20	ppm
32kHz Load Capacitance	C_{L32K}			12.5		pF
32kHz Series Resistance	R_{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	f_{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	$\Delta f_{4M}/f_{4M}$	25°C	-30		+30	ppm
4MHz Crystal Loadapacitance	C_{L4M}			12.0		pF
4MHz Crystal Series Resistance	R_{S4M}				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF

Timing Diagrams

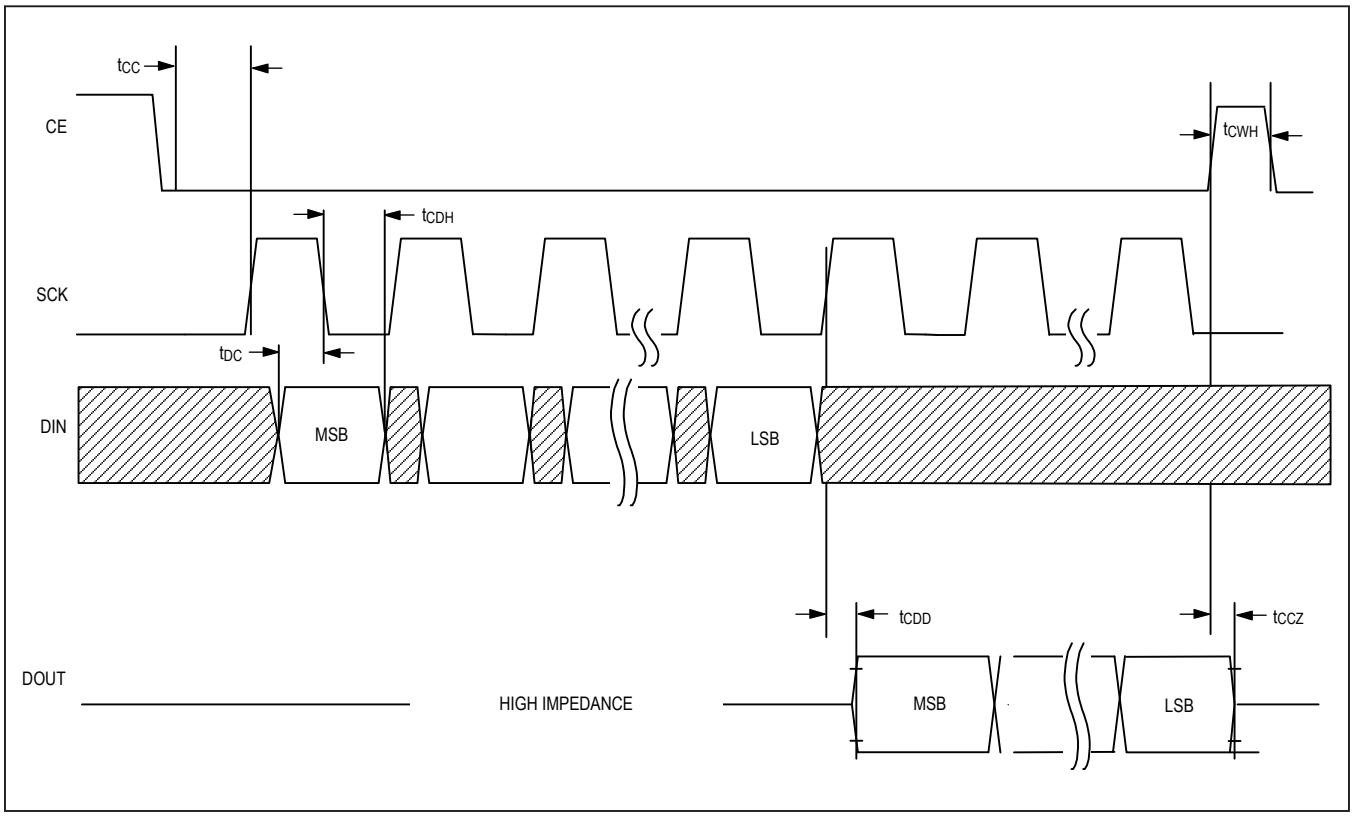


Figure 1. SPI Timing Diagram Read

Timing Diagrams (continued)

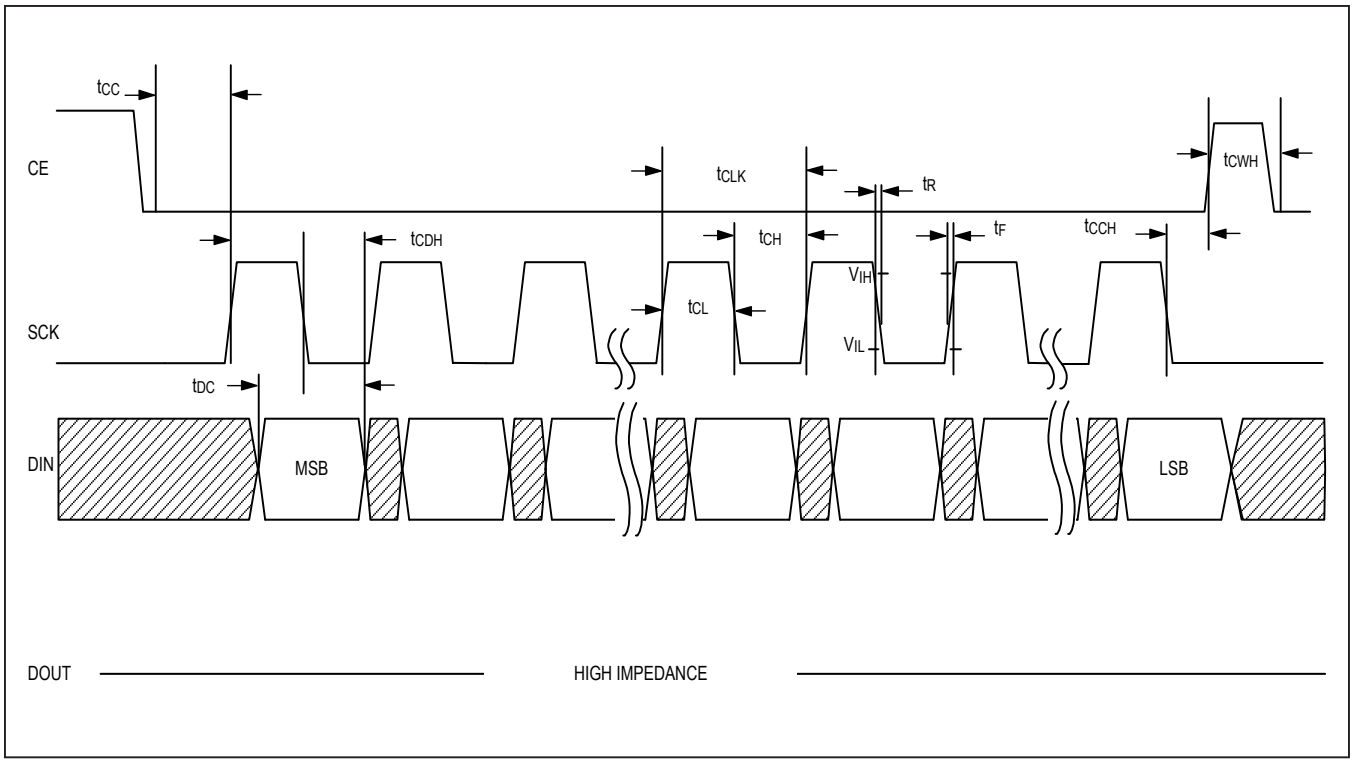
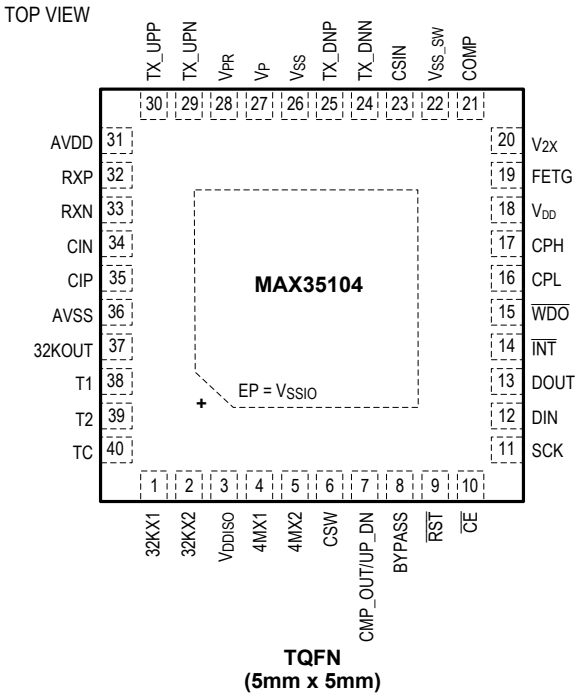


Figure 2. SPI Timing Diagram Write

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	32KX1	Connections for 32.768kHz Quartz Crystal, Connect a 12pF ceramic capacitor from each pin to ground. An external CMOS 32.768kHz signal can also drive the device. In this configuration, the 32KX1 pin is connected to the external signal and the 32KX2 pin is left unconnected.
2	32KX2	
3	V_{DDISO}	LDO Supply Voltage. This pin should be decoupled to V_{SSISO} with a 100nF ceramic capacitor (Note 1).
4	4MX1	Connections for 4MHz Quartz Crystal, connect a 12pF ceramic capacitor from each pin to ground. A ceramic resonator can also be used. An external CMOS 4MHz signal can also drive the device. In this configuration, the 4MX1 pin is connected to the external signal and the 4MX2 pin is left unconnected.
5	4MX2	
6	CSW	CMOS Digital Input Case Switch. Active high tamper detect input.
7	CMP_OUT/UP_DN	CMOS output that indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output (Note 2).
8	BYPASS	Connect this pin to ground with a 100nF ceramic capacitor to provide stability for the on-board low-dropout regulator. The effective series resistance of this capacitor needs to be in the range of 1Ω to 2Ω (Note 3).

Pin Description (continued)

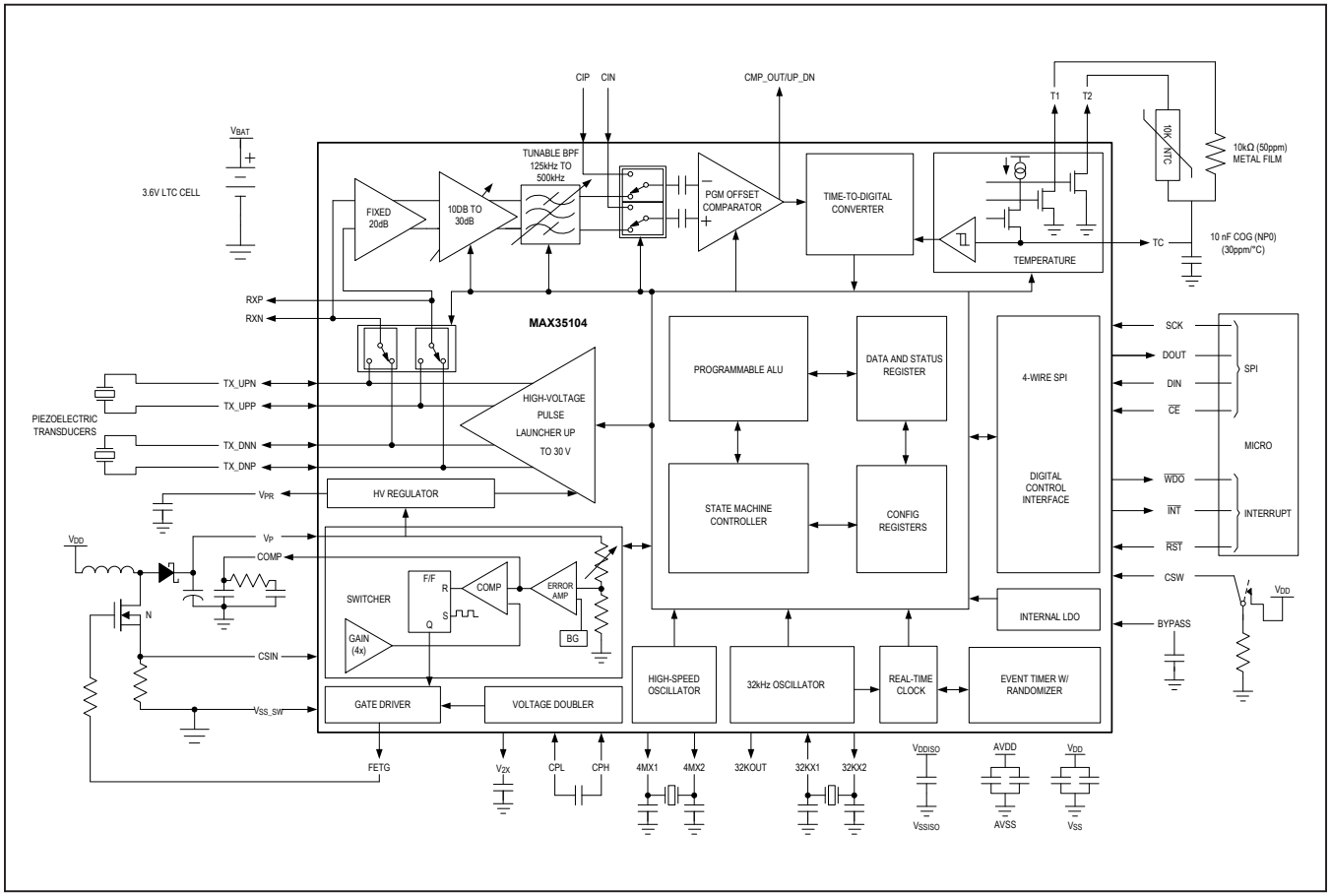
PIN	NAME	FUNCTION
9	$\overline{RST}$	Active-Low Reset (CMOS Digital Input). Performs the same function as a power-on reset (POR).
10	$\overline{CE}$	Active-Low Serial Peripheral Interface Chip Enable Input (CMOS Digital Input)
11	SCK	Serial Peripheral Interface Clock Input (CMOS Digital Input)
12	DIN	Serial Peripheral Interface Data Input (CMOS Digital Input)
13	DOUT	Serial Peripheral Interface Data Output (CMOS Output)
14	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
15	$\overline{WDO}$	Active-Low, Open-Drain Watchdog Output. The pin is driven low when the watchdog counter reaches zero (if enabled).
16	CPL	Negative terminal of the flying capacitor for the voltage doubler. Connect this pin to CPH with a 100nF ceramic capacitor. (Note 4)
17	CPH	Positive terminal of the flying capacitor for the voltage doubler. Connect this pin to CPL with a 100nF ceramic capacitor. (Note 4,5)
18	V_{DD}	Supply Voltage. This pin should be decoupled to V_{SS} with a 100nF and a 22µF ceramic capacitor (Note 1).
19	FETG	PWM Modulated CMOS Gate Driver Output for External n-Channel Power Transistor used in the Boost Switcher. Place a 25Ω series resistor between this pin and the transistor gate.
20	V_{2X}	Connect this pin to ground with a 100nF ceramic capacitor to provide stability for the on-board voltage doubler (Notes 3, 4).
21	COMP	Error-Amplifier Output of Boost Converter. Connect the frequency-compensation network between COMP and AVSS. See Figure 6 (Notes 3, 4).
22	V_{SS_SW}	High-Current Ground Return for the Boost Switcher. Connect the current-sense resistor between this pin and CSIN+ (Note 4).
23	CSIN	Positive Analog Input to the Current-Sense Amplifier for the Boost Switcher. Connect the current-sense resistor between this pin and CSIN (Note 4).
24	TX_DNN	Connect to the negative terminal of the piezo transducer located downstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the negative output of the bridged differential output driver pair. In the receive case, it is the negative input of the analog differential return signal from the piezo transducer (Notes 2, 4).
25	TX_DNP	Connect to the positive terminal of the piezo transducer located downstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the positive output of the bridged differential output driver pair. In the receive case, it is the positive input of the analog differential return signal from the piezo transducer (Notes 2, 4).
26	V_{SS}	Ground Connection
27	V_P	Resulting High-Voltage Bias Generated by the Boost Switcher Circuit. Used as the supply for the high-voltage regulator and to generate the feedback voltage fed into the error-amplifier for closed loop control. (Notes 3, 4).

Pin Description (continued)

PIN	NAME	FUNCTION
28	V_{PR}	Connect this pin to ground with a 1µF ceramic capacitor to provide stability for the on-board high-voltage regulator. When the high-voltage regulator is not used and constantly disabled, short this pin to VP (Notes 3, 4).
29	TX_UPN	Connected to the negative terminal of the piezo transducer located upstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the negative output of the bridged differential output driver pair. In the receive case, it is the negative input of the analog differential return signal from the piezo transducer (Notes 2, 4).
30	TX_UPP	Connected to the positive terminal of the piezo transducer located upstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the positive output of the bridged differential output driver pair. In the receive case, it is the positive input of the analog differential return signal from the piezo transducer (Notes 2, 4).
31	AVDD	Analog Supply Voltage. This pin should be decoupled to AVSS with a 100nF ceramic capacitor (Note 1).
32	RXP	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Positive analog output from the selected transducer's differential return signal. When used with the CIP pin provides a way to construct an external analog front-end (Note 5).
33	RXN	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Negative analog output from the selected transducer's differential return signal. When used with the CIN pin provides a way to construct an external analog front-end (Note 5).
34	CIN	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Negative analog input to the differential receive comparator. When used with the RXN pin provides a way to construct an external analog front-end (Note 5). OR negative analog output of selectable AFE stages (Note 2).
35	CIP	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Positive analog input to the differential receive comparator. When used with the RXP pin provides a way to construct an external analog front-end (Note 5). OR positive analog output of selectable AFE stages (Note 2).
36	AVSS	Ground Connection
37	32KOUT	CMOS Output That Repeats the 32kHz Crystal Oscillator Frequency
38	T1	Open-Drain Probe 1 Temperature Measurement (Note 5)
39	T2	Open-Drain Probe 2 Temperature Measurement (Note 5)
40	TC	Input/Output Temperature Measurement Capacitor Connection (Note 5)
EP	V_{SSISO}	Exposed Pad, Ground Connection

Note 1: A +2.7V to +3.6V supply. Typically sourced from a single lithium cell.
Note 2: Dual functionality pin.
Note 3: Do not connect to additional non-recommended external circuitry.
Note 4: High-voltage tolerant.
Note 5: This pin can be left open circuit if not needed.

Block Diagram



Detailed Description

The MAX35104 is a gas flow meter SoC targeted as an analog front-end solution for the ultrasonic gas meter and medical ventilator markets. With a time measurement accuracy of 700ps and automatic differential Time-of-Flight measurement, the device makes for simplified computation of gaseous flow. Power consumption is the lowest available with ultra-low 62µA TOF measurement and 125nA duty-cycled temperature measurement.

Multihit (up to 6 per wave) capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, a configurable 3-stage integrated operational amplifier chain amplifier, and an ultra-low input offset comparator provide the analog interface and control for a minimal electrical bill of material solution. A programmable high-voltage (up to 30V) pulse launcher provides up to 19dB of transducer launch amplitude adjustment to compensate for transducer aging and temperature, pressure, humidity affects.

Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. A built-in arithmetic logic unit provides TOF difference measurements and programmable receiver hit accumulators to minimize the host microprocessor access. For temperature measurement, the device supports a single 2-wire PT1000 platinum resistive temperature detector (RTD) or NTC thermistor. A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

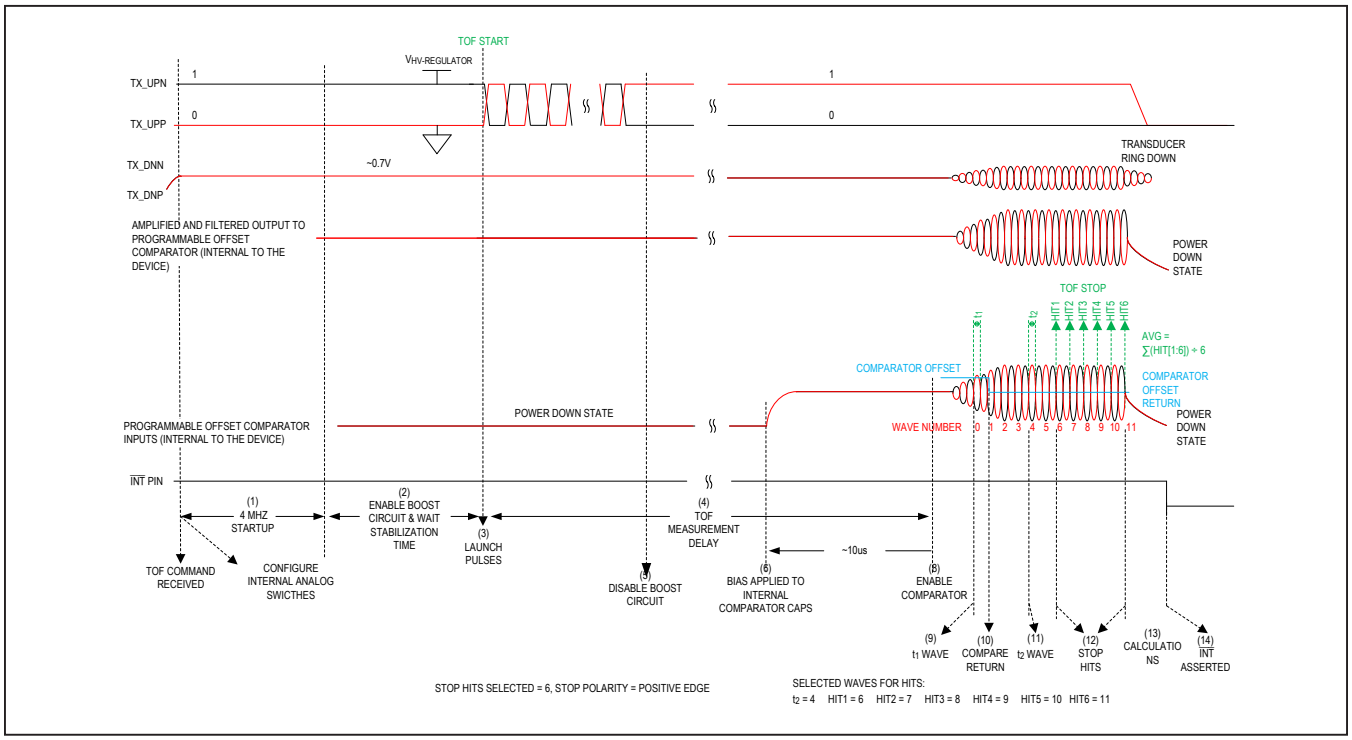


Figure 3. Time-of-Flight Up Measurement Sequence

Time-of-Flight (TOF) Measurement Operations

TOF is measured by launching pulses from one piezoelectric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The device contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The device can measure two separate TOFs, which are defined as TOF Up and TOF Down.

A TOF Up measurement has pulses launched from the TX_UPN and TX_UPP pins, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the TX_DNN and TX_DNP pins. A TOF Down measurement has pulses launched from the TX_DNN and TX_DNP pins, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the TX_UPN and TX_UPP pins.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands. TOF_DIFF measurements can also be automatically executed using Event Timing Mode commands EVTMG1 or EVTMG2.

The steps involved in a single TOF measurement are described below and labeled in Figure 3.

1) The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
2) The boost circuit is enabled and attempts to reach the targeted set output voltage. Once at the target voltage, the stabilization time to wait before moving to the next step is set by the ST[3:0] bits in the Switcher 2 register.
3) The pulse launcher drives the appropriate TX pins with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% duty-cycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses generates a start signal for the Time-to-Digital Converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted in Figure 4.
4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate pins are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
5) Once the pulse launcher has completed transmitting the sequence of pulses, the boost circuit is disabled.

6) A common mode bias is enabled on the internal capacitor connecting the output of the bandpass filter to the input of the programmable offset comparator. This bias charge time is fixed at approximately 10µs.
7) The comparator is enabled.
8) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the appropriate pins according to the setting of the STOP_POL bit in the TOF1 register. When a wave received at the receiving pins exceeds the Comparator Offset Voltage, which is set in the TOF6 and TOF7 registers, this wave is detected and identified as wave number 0. The width of the wave's pulse that exceeds the Comparator Offset Voltage is measured and stored as the t_1 time.
9) The offset of the comparator then automatically and immediately switches to the Comparator Return Offset, which is set in the TOF6 and TOF7 registers.
10) The t_2 wave is detected and the width of the t_2 pulse is measured and stored as the t_2 time. The wave number for the measurement of the t_2 wave width is set by the T2WV[5:0] bits in the TOF2 register.
11) The preferred number of stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[2:0] bits in the TOF2 register. The wave number to measure for each stop hit is set by the Hitx Wave Select bits in the TOF3, TOF4, and TOF5 registers.
12) After receiving all the programmed hits, the device calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t_1/t_2 and t_2/t_{IDEAL} are calculated and stored in the WVRUP or WVRDN register.
13) Once all the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a Read register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTER VALUE		CONVERTER VALUE
TOF_DIFFInt (hex)	**TOF_DIFFFrac (hex)**	**TOF DIFF Value (ns)**
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

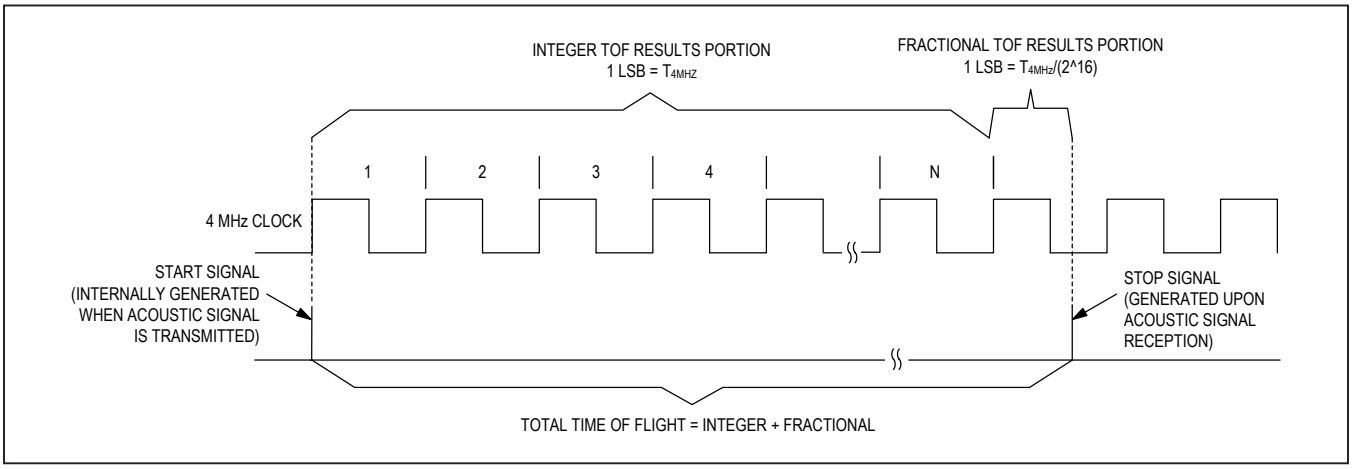


Figure 4. Start/Stop for Time-to-Digital Timing

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHz} or ~ 8.19ms. The maximum size of the fraction is FFFFh or (2^{16} - 1)/2^{16} x t_{4MHz}. or ~ 249.9961 ns.

Pulse Echo TOF Mode

The device also has a pulse echo mode of operation. This mode allows time-of-flight measurements to be taken when only one transducer is used. The sole transducer transmits the high-voltage pulses and then receives the return signal. The time-of-flight measurement operation acts exactly as described in steps 1–13 except that the common mode of the AFE is applied to the same pins that transmitted the high-voltage pulses (Figure 5A).

The resulting data from the measurement is reported in the same manner as described in the TOF_UP, TOF_DOWN, or TOF_DIFF sections depending upon which command was executed.

The pulse echo mode is enabled by setting the PECHO bit in the Switcher 2 Register.

Early Edge Detect

The Early Edge Detect method of measuring the TOF of acoustic waves is used for all the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the device to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +127 LSBs if triggering on a positive edge and -127 LSBs if triggering on a negative edge, with 1 LSB = V_{CC}/3072. Separate input offset settings are available for the Upstream received signal and the Downstream received signal. The input offset for the Upstream received signal is programmed using the C_OFFSETUP[6:0] bits in the TOF6 register,. The input offset for the Downstream received signal is programmed using the C_OFFSETDN[6:0] bits in the TOF7 register. Once the first hit is detected, the time t_1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to a preprogrammed comparator offset value. This return offset value has a range of +127 LSB's to -128 LSB's in 1 LSB steps and is programmed into the C_OFFSETUPR[7:0] bits in the TOF6 register for the Upstream received signal and programmed into the C_OFFSETDNR[7:0] bits in the TOF7 register. This preprogrammed comparator offset return value is provided to allow for common-mode shifts that can be present in the received acoustic wave.

The device is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5B, this is the 7th wave after the Early Edge Detect wave. The selection of the t_2 wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5B, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{IDEAL} is calculated and registered for the user. For this calculation, t_{IDEAL} is one-half the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

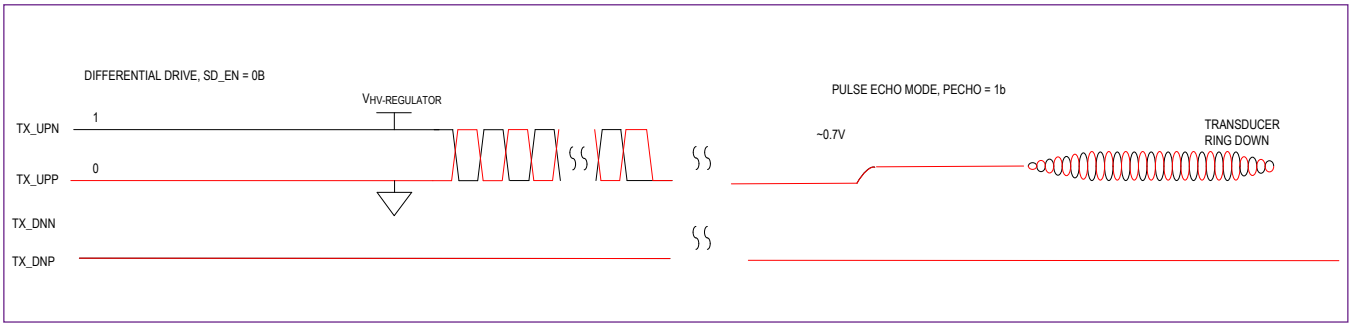


Figure 5A. Pulse Echo Measurement Mode

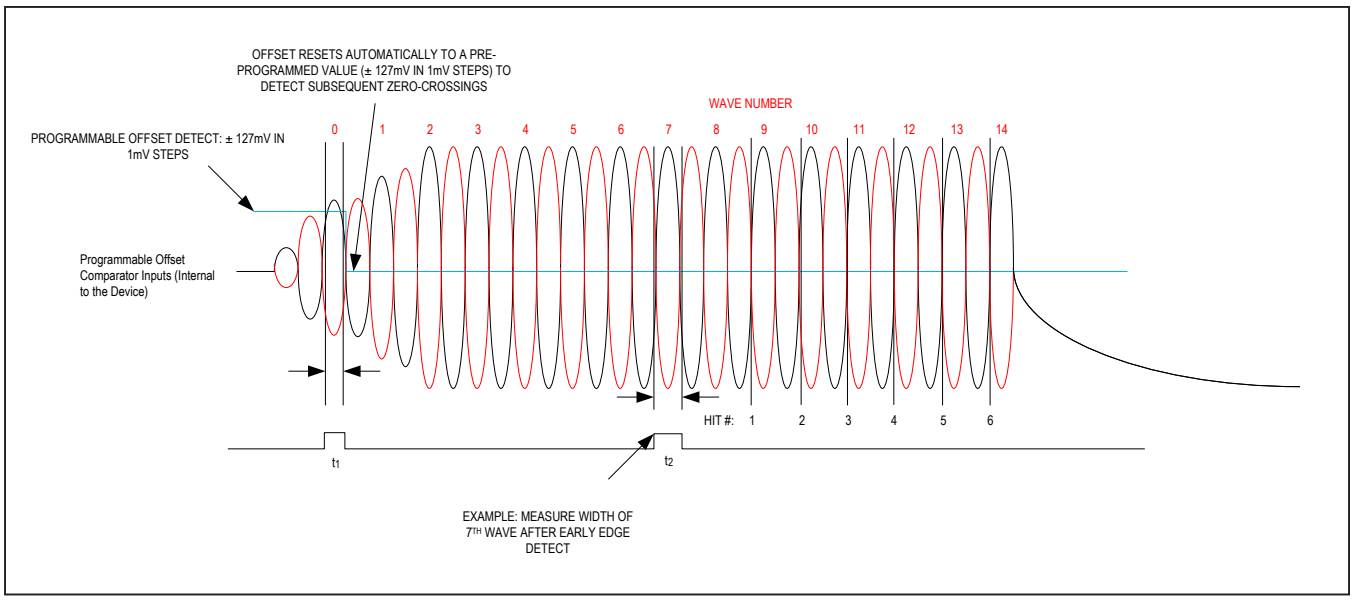


Figure 5B. Early Edge Detect Received Wave Example

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. The TOF_DIFF_AVG Results registers do not include the error measurement. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ device pin is asserted (if enabled).

Step-Up DC-DC Controller

In order to increase the power transferred to the transducers during a launch sequence which is required to counteract the high attenuation factors for ultrasonic waves in gaseous mediums the device contains an integrated DC-DC Step-Up controller designed to operate in discontinuous-conduction mode (DCM boost). The controller provides adjustable-output voltage operation including programmable stabilization times with built in under voltage monitoring. The MAX35104's integrated gate driver utilizes the onboard voltage double in order to drive an external N-channel MOSFET's gate from ground to 2 x V_{DD}. The controller uses an external sense resistor to control the peak inductor current and operates at adjustable switching frequencies.

The integrated boost controller in enabled and disabled automatically by the device. The logic enables the boost before executing a time of flight command and disables the boost once the transmit pulse train is complete, see example timing in the Figure 3. The boost is disabled upon completion of the transmit pulses in order to reduce overall system power consumption as well as to eliminate any controller switching noise that would be introduced during the return signal's timing measurements.

Control and Operation

The switching frequency of the controller is programmable from 100kHz to 200kHz in 4 steps set by the SFREQ[1:0] bits in the Switcher 1 register. In order to set the output voltage the controller uses an outer loop feedback topology along with a peak current mode inner loop control.

The controller's outer loop targets an output voltage from 9V to 30V based on the programmed value set by the VS[3:0] bits in the Switcher 1 register. An internal error amplifier creates a control voltage, which generates a duty-modulated signal to control the operation of the internal gate driver used to switch the external MOSFET.

Additionally, the MOSFET's source needs an external current sense resistor, which feeds back the inductor's current per cycle as a voltage and compares with the error amplifier's output to further adjust the duty-modulated signal, thus forming an inner loop.

The controller has an undervoltage comparator that determines if the target output voltage is at target voltage, considered power good, or undervoltage. If the output voltage is below target, the switcher operates in startup limit mode that is determined by user selectable peak current limit set by the LT_S[3:0] bits in the Switcher 2 register. This is essentially a slew rate control on how fast the boost powers up and can be used to control the current signatures seen by the supply battery. After the output voltage crosses the undervoltage threshold, the switcher runs in normal duty mode. There is an additional optional peak current limit setting for the normal duty mode that is set by the LT_N[3:0] bits in the Switcher 2 register. Once in normal duty mode the device waits a programmable switcher stabilization time before a launch sequence begins. The stabilization time ensure that the controller has reaches a stable and repeatable output voltage each time it is powered. This time is set by the ST[3:0] bits in the Switcher 2 register. See Figure 6.

Compensation Component Values

In order to achieve standard operations the boost controller requires that proper loop compensation be applied to the error-amplifier output (COMP pin). The goal of the compensator design is to achieve the desired closed-loop bandwidth and sufficient phase margin at the crossover frequency of the open-loop gain-transfer function of the converter. The error amplifier included in the devices is a transconductance amplifier. Figure 6 shows the compensation network used to apply the necessary loop compensation for the example inductor and output capacitor values provided, where:

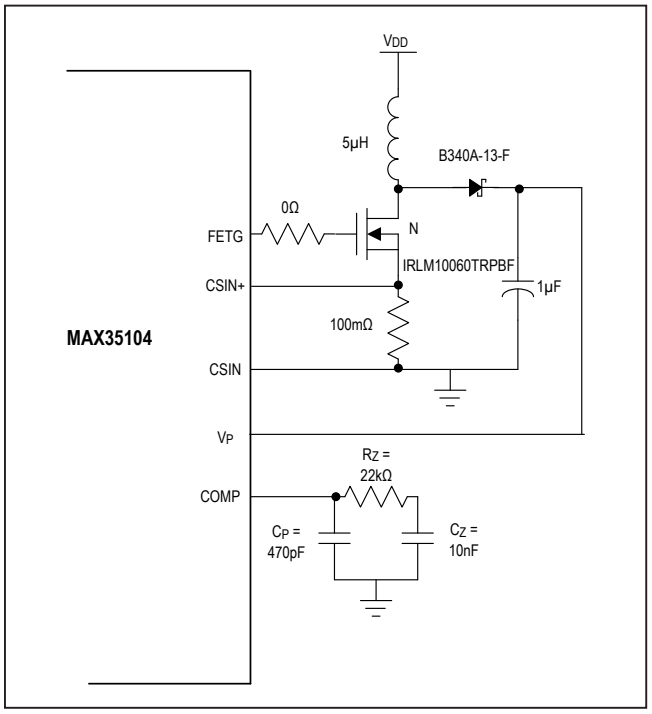


Figure 6. Boost Circuits Components

$$RZ = 22k\Omega$$

$$CP = 470pF$$

$$CZ = 10nF$$

RSENSE

The external sense resistor value determines the peak allowable inductor current. For a given limit trim setting, LT_N[3:0] and LT_S[3:0] in the Switcher 2 register. Adjust the RSENSE value to adjust the peak allowable current. Select RSENSE based on the following criteria:

Resistor Value: Select an RSENSE resistor value in which the largest desired current would result in a 200mV full-scale current sense voltage. Assuming an LT_x setting of 0h, select RSENSE in accordance to the following equation and see Table 2 for examples:

$$RSENSE = 200mV/(Max\ Current)$$

Power Dissipation: Select a sense resistor that is rated for the max expected current and power dissipation (wattage). The sense resistor's value might drift if it is allowed to heat up excessively.

Kelvin Sense

For best performance, a Kelvin Sense arrangement is recommended for sense resistor as shown in Figure 7. In a Kelvin Sense arrangement, the voltage-sensing nodes across the sense element are placed such that they measure the true voltage drop across the sense element and not any additional excess voltage drop that can occur in the copper PCB traces or the solder mounting of the sense element. Routing the differential sense lines along the same path to the device and keeping the path short also improves the system performance. The analog differential current-sense traces should be routed close together to maximize common-mode rejection.

Power Transistor

Use an n-channel MOSFET power transistor with the MAX35104. To ensure the external n-channel MOSFET (nFET) is turned on hard, use logic-level or low-threshold nFETs such that the MAX35104's internal gate driver's 2 x V_{DD} supply voltage is sufficient for proper switching operation. nFETs provide the highest efficiency because they do not draw any DC gate-drive current. When selecting

an nFET, three important parameters are the total gate charge (Qg), on-resistance ($R_{DS(ON)}$), and reverse transfer capacitance (CRSS).

Qg takes into account all capacitances associated with charging the gate. Use the typical Qg value for best results; the maximum value is usually grossly over specified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the FETG pins may not be able to adequately drive the gate.

The two most significant losses contributing to the nFET's power dissipation are I^2R losses and switching losses. Select a transistor with low $r_{DS(ON)}$ and low CRSS to minimize these losses.

Determine the maximum required gate-drive current from the Qg specification in the nFET data sheet. The MAX35104's maximum allowed switching frequency is 200kHz, so the maximum current required to charge the nFET's gate is f(max) x Qg(typ). Use the typical Qg number from the transistor data sheet. For example, the Si9410DY has a Qg(typ) of 17nC (at V_{GS} = 5V), therefore, the current required to charge the gate is:

$$IGATE\ (max) = (300kHz)\ (17nC) = 5.1mA$$

The bypass capacitor (C1) on the voltage double pin V2X must instantaneously furnish the gate charge without excessive droop (e.g., less than 200mV):

$$\Delta V2X = Qg/C1$$

Continuing with the example, $\Delta V+ = 17nC/0.1\mu F = 170mV$.

Figure 6 uses an IRLM10060TRPBF logic-level nFET with a guaranteed threshold voltage (V_{TH}) of 2.5V.

Table 2. RSENSE Example Values

RLIM (Ω)	LIMIT TRIM SETTING (STARTUP AND NORMAL)	CSIN TRIP VOLTAGE (V)	MAX CURRENT (A)
0.1	0	0.2	2
	1	0.4	4
	2	0.8	8
	4	1.6	16
0.25	0	0.2	0.8
	1	0.4	1.6
	2	0.8	3.2
	4	1.6	6.4
0.5	0	0.2	0.4
	1	0.4	0.8
	2	0.8	1.6
	4	1.6	3.2
1	0	0.2	0.2
	1	0.4	0.4
	2	0.8	0.8
	4	1.6	1.6
2	0	0.2	0.1
	1	0.4	0.2
	2	0.8	0.4
	4	1.6	0.8

Note: *The current must be large enough such that the switcher can reach its target output voltage (< 1s).*

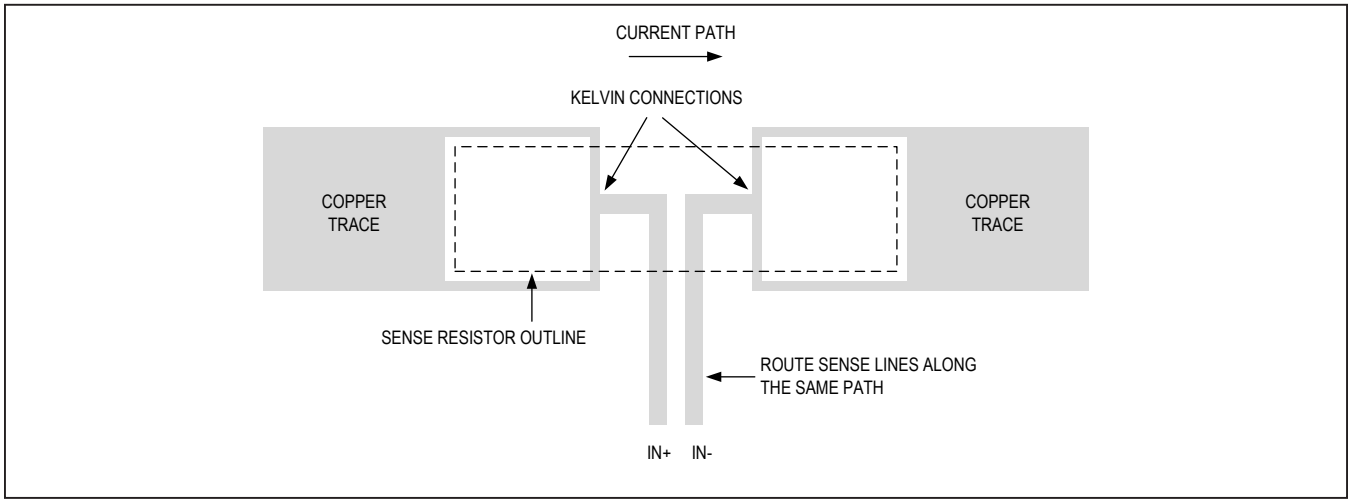


Figure 7. Kelvin Sense Connection Layout Example

Inductor (L)

Practical inductor values range from 5µH to 150µH. 56µH is a good choice for most applications. Larger inductance values tend to increase the startup time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the over current switch halts switching, increasing the ripple at light loads. Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by R_{SENSE}. For highest efficiency, use a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Diode

The device high switching frequency demands a high-speed rectifier. Schottky diodes such as the B340A-13-F are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. Smaller-value and/or higher- ESR capacitors are acceptable for light loads or in applications that can tolerate higher output ripple. Since the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance.

Piezo Driver Regulator

The MAX35104 provides an internal high voltage low dropout linear regulator. The input to this regulator is the boost switcher's output and the output of the regulator supplies the high side bias used for the CMOS push pull high voltage transducer drivers. The regulator is used to provide a more stable higher bandwidth source from which the transducers can be driven. This helps mitigate any loading mismatches between the two transducers and provides a more repeatable launch signature between upstream and downstream measurements, ultimately reducing overall system error.

The high-voltage linear regulator operates from 5.4V to 27V in programmable 1.7V steps set by the VS[3:0] bits in the Switcher 1 register. There is an option to not use the high voltage regulator in the case where it is not desired and the switcher voltage is deem sufficient to drive the transducers. Disable the regulator with the HREG_EN bit in the Switcher 1 register. When disabled the VPR and VP pins must be externally shorted together.

When the regulator is enabled, its output is cycled off and on automatically by the device at the same time as the boost switcher, see example timing Figure 3.

Output Capacitor Selection

For stable operation over the full temperature range, use a low-ESR 1µF (min) 0805 ceramic output capacitor on the VPR pin. Ceramic capacitors exhibit capacitance and ESR variations over temperature. Ensure that the minimum capacitance under worst-case conditions does not drop below 1µF to ensure output stability. With a 1µF X7R dielectric, is sufficient at all operation temperatures.

Transducer Driver

The device has two integrated high voltage full-bridge transducer drivers, one for the upstream and one for the downstream transducer as shown in Figure 8. The drivers direct connect to the transducers without any external components required. The drivers can also be configured to drive the transducer in a single-ended manner. Set the single-ended drive enable bit, SD_EN, in the AFE 1 register. In this configuration, the negative terminal of the drivers are held at ground and the positive terminal is modulated between the high-voltage node and ground.

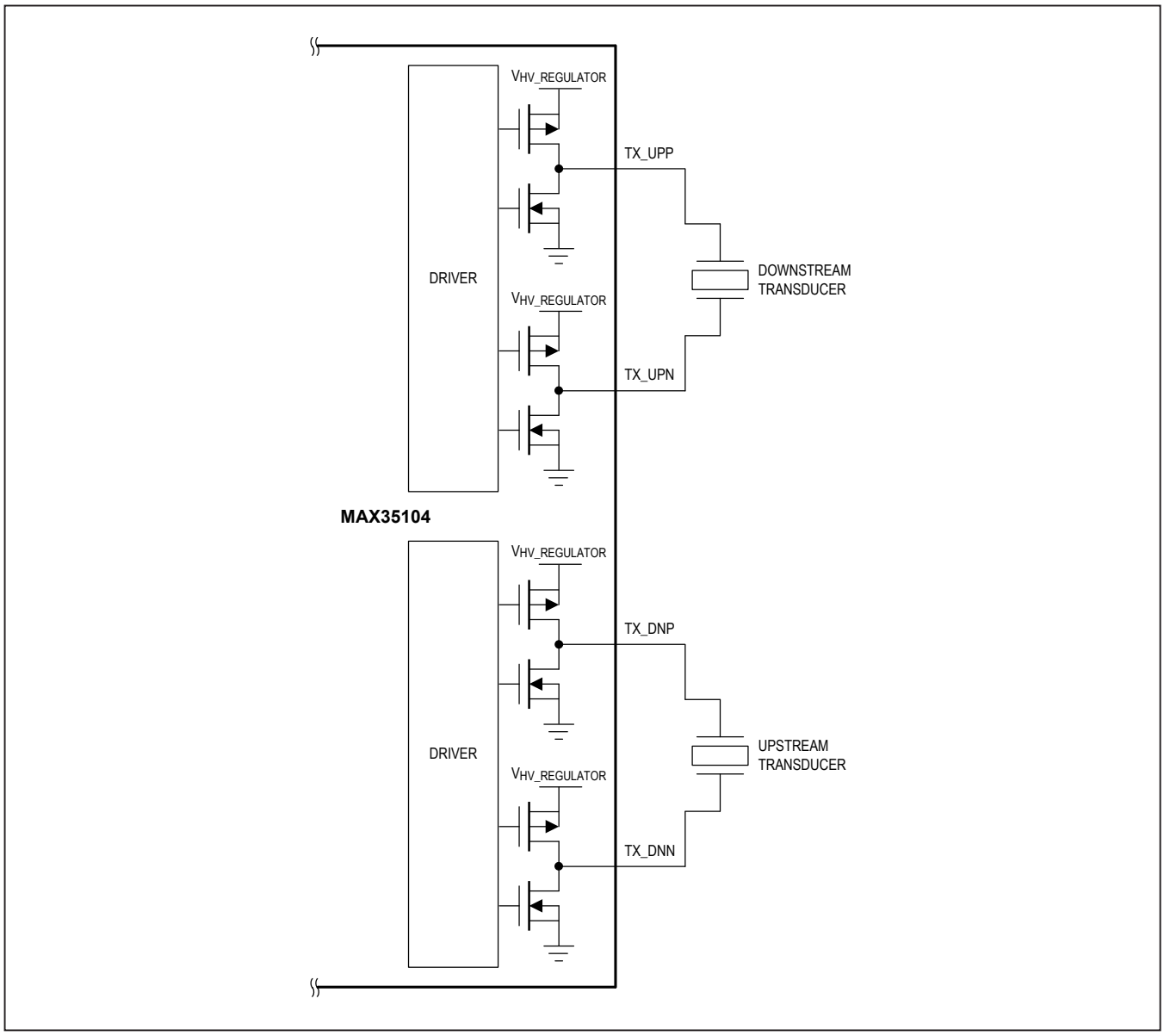


Figure 8. Piezo Driver Connection

Analog Front-End

The device has a programmable analog front-end used to condition the return signal before the signal is used to determine when the stop-hit timing should occur. This analog front-end consists of two amplifications stages, followed by a band pass filter, which feeds into the final comparator. The return signal is sampled differentially from the transducer. The entire AFE operates differentially all the way to the final comparator. By operating differently, the receive chain is less susceptible to noise injections applied to the common mode, providing an additional level of system accuracy and robustness.

The first stage is a fixed 20dB gain amplifier. An internal analog switch automatically connects the input of this amplifier to the appropriate receiving transducer. When enabled, the input is pulled to VBIAS ~0.7V through 2kΩ input resistance. The valid input range for the first amplification stage, and, therefore, the targeted return amplitude from the receiving transducer is 1mV to 10mV.

The second amplification stage is a programmable gain amplifier (PGA). The PGA is has a programmable range from 10 dB to 30dB in 1.33dB steps set by the PGA[3:0] bits in the AFE 1 register. Figure 9 shows the possible gain settings and input voltage amplitude combinations. The ideal input amplitude for the differential stop comparator is 350mV and therefore this should be the target for the output of the AFE. Table 3 shows ideals settings highlighted in green for all return signal amplitudes.

The bandpass filter is a 2-pole bandpass filter with programmable Q and center frequency. The Q of the filter can be adjusted with four programmable options in the range for 4.2 to 12 (Hz/Hz) set by the LOWQ[1:0] bits in the AFE 1 register. The center frequency is programmable from 125kHz to 500kHz in 3kHz steps set by the F0[6:0] bits in the AFE 2 register. The MAX35104 provides an integrated and automated center-frequency calibration routine that can be used to select and set the appropriate center frequency. To use this feature send the BYPASS_CALIBRATE command and wait until the complete bit is set. This routine performs the required calibration and automatically sets the F0 Adjust settings, bits F0[6:0] in the AFE 2 register to the correct value.

The bandpass filter can be bypassed as shown in Figure 9 by enabling the BP_BP bit in the AFE1 register. If the internal analog front-end is not required it can be completely bypassed by externally shorting the RNX/RXP pins to the CIN/CIP pins as shown in Figure 9 and setting the AFE_BYPASS bit in the AFE1 register. This allows for an external AFE to be constructed with external components. The CIN/CIP pins can also be used to output each stage of the AFE by setting the AFEOUT[1:0] bits in the AFE 2 register.

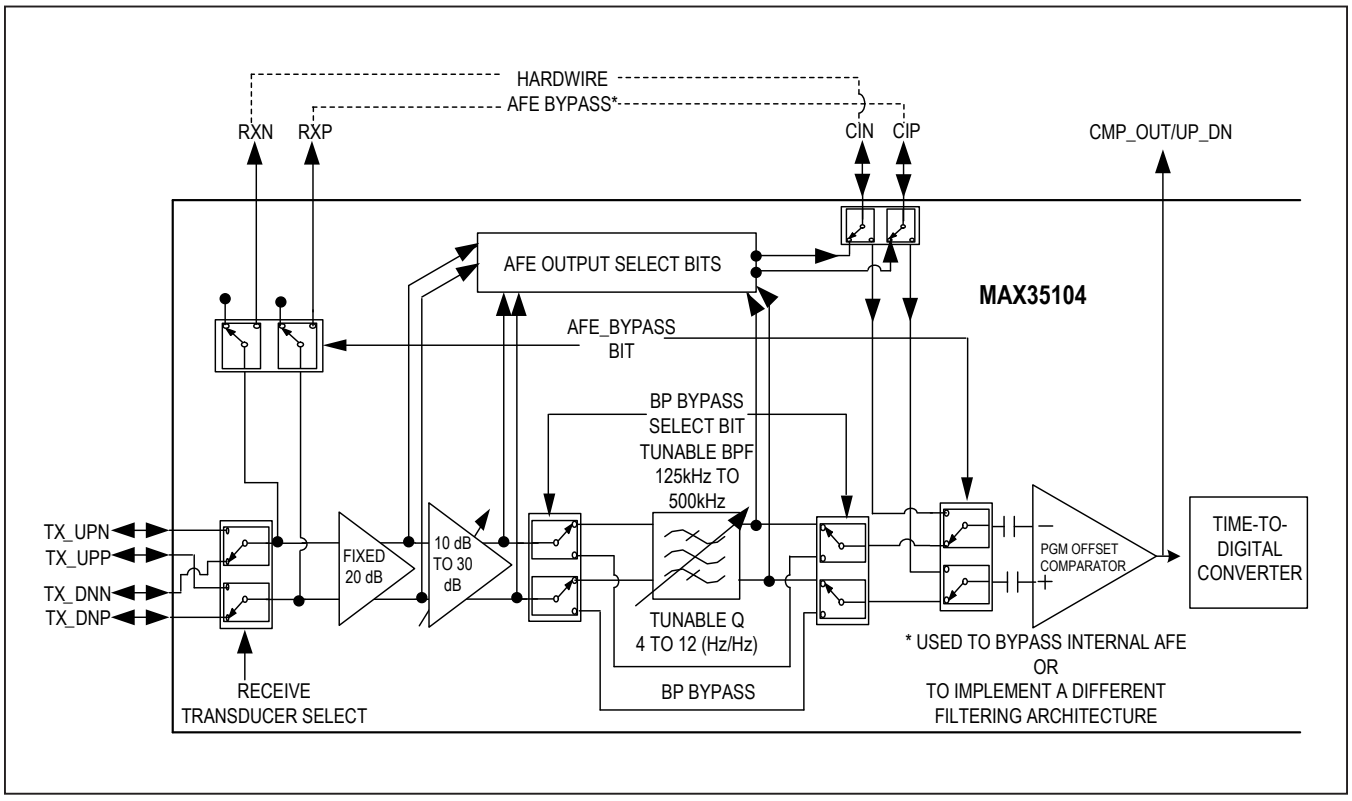


Figure 9. Analog Front-End