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19-4720; Rev 2; 8/10

Laser Driver for Projectors

MAX3600

General Description

The MAX3600 laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes a 10-bit video digital-to-analog converter (DAC) with programmable gain and offset. For operation with synthetic green lasers, the driver includes a periodic off function and a fourth output with a random-noise generator.

The MAX3600B/R/G are monochrome drivers for blue, red, and green lasers. The MAX3600A guarantees higher full-scale output currents than the MAX3600, and is recommended for new designs.

Applications

RGB Pico Laser Projector

Up to WXGA and 1080p Resolution Projectors

Monochrome Blue, Green, or Red Pico Laser Projector

Typical Operating Circuits and Pin Configuration appear at end of data sheet.

Features

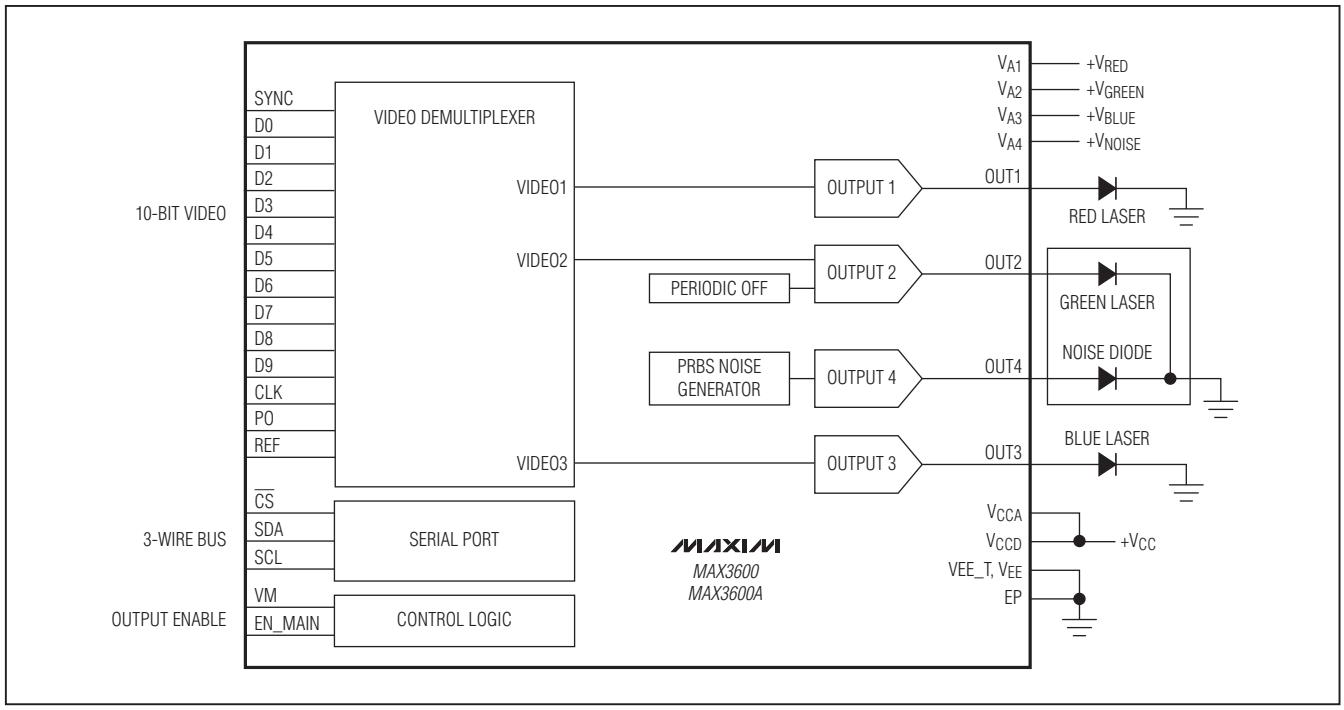
- **Integrates Four Current-Output Laser Drivers**
- **Compatible with Red, Blue, and Green Lasers**
- **10-Bit Video DACs, f_{CLK} = 1MHz to 160MHz**
- **8-Bit Gain and Offset DACs**
- **2ns Output Switching Time**
- **Serial Port Control**
- **Laser Enable**
- **Random-Noise Generator and Periodic Off**
- **5mm x 5mm, 40-Pin TQFN Package (0.4mm Pitch)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3600CTL+†	0°C to +70°C	40 TQFN-EP*
MAX3600ACTL+	0°C to +70°C	40 TQFN-EP*
MAX3600RCTL+††	0°C to +70°C	40 TQFN-EP*
MAX3600GCTL+††	0°C to +70°C	40 TQFN-EP*
MAX3600BCTL+††	0°C to +70°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
†Not recommended for new designs.
††Future product—contact factory for availability.

Simplified Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CCA}, V_{CCD} ..... -0.3V to +4.0V
Voltage Range at V_{A1}, V_{A2}, V_{A4} ..... -0.3V to +6.0V
Voltage Range at V_{A3} ..... -0.3V to +8.5V
Voltage Range at OUT1 ..... -0.3V to (V_{A1} + 0.3V)
Voltage Range at OUT2 ..... -0.3V to (V_{A2} + 0.3V)
Voltage Range at OUT3 ..... -0.3V to (V_{A3} + 0.3V)
Voltage Range at OUT4 ..... -0.3V to (V_{A4} + 0.3V)
Voltage Range (V_{A1} - V_{OUT1}), (V_{A2} - V_{OUT2}), (V_{A4} - V_{OUT4}) ..... 0 to +6.0V
Voltage Range (V_{A3} - V_{OUT3}) ..... 0 to +7.5V
Voltage Range at D0 to D9, SYNC, CLK, PO, SCL, SDA, $\overline{CS}$, EN_MAIN, VM, REF, VEE_T, RES .. -0.3V to (V_{CC} + 0.3V)
Current at OUT1, OUT2, OUT3, OUT4 ..... See Table 3
Current at D0 to D9, SYNC, CLK, PO, SCL, SDA, $\overline{CS}$, EN_MAIN, VM, REF, VEE_T, RES ..... ±50mA
Current at REF ..... ±0.5mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range ..... -40°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±5%, T_A = 0°C to +70°C, $T_J \le$ +125°C, EN_MAIN high, $V_{C_} \ge$ 0.9V, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIDEO DAC (10 BITS)							
Maximum Conversion Rate				100	160		Msps
Settling Time		(Note 2)			4		ns
Rise/Fall Time (20% to 80%)		(Note 2)			1	(4)	ns
Analog Supply Voltage	V_{A1}, V_{A2}, V_{A4}				> 3.1	6.0	V
	V_{A3}	OUT3 enabled			> 4.0	8.5	V
		OUT3 disabled			> 3.1	8.5	V
Compliance Voltage	$V_{C_}$	$V_{C_} = V_{A_} - V_{OUT_}$			0.5	(6.0)	V
Analog Supply Current (I_{VA} - I_{OUT}) (Note 3, Figure 8)	I_{DAC_G0}	CLK static	OUT1		18	31	mA
			OUT2		18	34	mA
			OUT3		19	26	mA
			OUT4		15	23	mA
	I_{DAC_G1}				3		mA
	I_{DAC_G2}			(30)	80		mA
GAIN DAC (8 BITS): VIDEO_ = 3FFh							
Minimum Full-Scale Current (gs_ = 00h)	G_{LOW}	OUT1		(6)	12	(18)	mA
		OUT2		(15)	40	(60)	mA
		OUT3		(3.5)	10	(15)	mA
		OUT4		(3)	10	(25)	mA
Maximum Full-Scale Current: MAX3600 (gs_ = FFh)	G_{HIGH} + G_{LOW}	OUT1		175	227	(270)	mA
		OUT2		550	690	(850)	mA
		OUT3		140	170	(200)	mA
		OUT4		140	185	(230)	mA
Maximum Full-Scale Current: MAX3600A/R/G/B (gs_ = FFh)	G_{HIGH} + G_{LOW}	OUT1		210	280	(330)	mA
		OUT2		630	760	(955)	mA
		OUT3		140	170	(210)	mA
		OUT4		140	185	(300)	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±5%, T_A = 0°C to +70°C, $T_J \leq$ +125°C, EN_MAIN high, $V_{C_} \geq$ 0.9V, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time	t_{SG}	To 5% of final value		10	(50)	µs
OFFSET DAC (8 BITS): VIDEO_ = 00h, gs_ = 00h						
Maximum Offset: MAX3600/A/R/G/B	OS_{HIGH}	OUT1	60	83	(110)	mA
		OUT2, OUT3	65	83	(110)	
		OUT4	120	155	(200)	
Offset Error	OS_{LOW}	V_{OUT1}, V_{OUT2}, V_{OUT4} = 1.6V; V_{OUT3} = 2.5V	-25	+0.2	+25	µA
Offset Settling Time	t_{SO}	To 5% of final value		10	(50)	µs
LOGIC I/O: SDA, SCL, $\overline{CS}$, VM, EN_MAIN						
Input High Voltage	V_{IH1}	Operating condition	V_{CC} - 0.3		V_{CC} + 0.3	V
Input Low Voltage	V_{IL1}	Operating condition	-0.3		+0.3	V
Input Current		SDA (write), SCL, $\overline{CS}$	-10	±0.2	+10	µA
Input Resistance		VM to V_{CCD}	25	60	100	kΩ
		EN_MAIN to V_{EE}	25	60	100	
Input Capacitance		SCL, $\overline{CS}$, SDA, VM, EN_MAIN			(1)	pF
Input Hysteresis				100		mV
Enable/Disable Time		From serial port load		< 10		µs
		VM↑ to final value		< 0.25		
		EN_MAIN↑ to final value		< 0.25		
Disable Time	t_{DIS}	EN_MAIN↓ to I_{OUT}↓		0.01	(1)	µs
Sink Current at SDA		Read mode, V_{SDA} = 0.6V	10	16		mA
VIDEO DATA INPUTS: D0 TO D9, CLK, SYNC, PO						
Minimum Frequency	f_{CLK_MIN}			0.01	(1)	MHz
Maximum Frequency	f_{CLK_MAX}		(140)	> 160		MHz
Clock Duty Cycle		DDR clock, operating condition	(45)		(55)	%
		Standard clock, operating condition	(42)		(58)	
Setup Time	t_{SU}	Operating condition	(0.8)			ns
Hold Time	t_H	Operating condition	(0.8)			ns
Input Switching Time		Operating condition (10% to 90%)		1.5		ns
Input Voltage Range	V_{IN}		-0.3		V_{CC} + 0.3	V
Input High Threshold	V_{IH2}	Relative to V_{REF}			+170	mV
Input Low Threshold	V_{IL2}	Relative to V_{REF}	-170			mV
Reference Voltage	V_{REF}	Operating condition	0.83		V_{CC}/2	V
Data Input Capacitance	C_D			0.4		pF
Termination Resistors	R_{TT}	Figure 6	450	900	1500	Ω
REF Input Current	I_{REF}	V_{REF} = V_{CC}/2	-5	-1.2	+5	µA
Propagation Delay		D0:D9 to OUT_, pixel clocks		3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±5%, T_A = 0°C to +70°C, $T_J \le$ +125°C, EN_MAIN high, $V_{C_} \ge$ 0.9V, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PO GENERATOR						
Pixel Clock Range for PO		Operating condition	24		(102)	MHz
Minimum PO Pulse Width		Four subpixels		3.5		ns
PLL Bandwidth			(560)	800	(1040)	kHz
PRBS OSCILLATOR						
PRBS Oscillator Frequency	f_{PRBS1}	f_{PIXEL} = 24MHz to 102MHz	(100)		(150)	MHz
SERIAL PORT: SDA, SCL, $\overline{CS}$ (Figure 14)						
Maximum Clock Frequency	f_{SCL}	Write mode	(25)			MHz
Input Edge Time		20% to 80%		5		ns
$\overline{CS}$ Leading Time	t_L		(4)			ns
SCL Pulse-Width High	t_{CH}			20		ns
SCL Pulse-Width Low	t_{CL}			20		ns
SCL to SDA Propagation Delay	t_D		(10)			ns
Data In Setup Time	t_{DS}		(10)			ns
Data In Hold Time	t_{DH}		(10)			ns
$\overline{CS}$ Trailing Time	t_T		(10)			ns
POWER SUPPLY: V_{CCA}, V_{CCD}						
Supply Current (I_{VCCA} + I_{VCCD}, gs_ = 80h, os_ = 80h, f_{CLK} = 75MHz)	I_{VCC1}	VIDEO_ = 1F0h, CLK_SEL = 0, output disabled		62	80	mA
	I_{VCC2}	CLK_SEL = 1, VIDEO_: 0 ↔ 3FFh repeating		65	90	
	I_{VCC2_ENLO}	Output disabled		60	(70)	
POWER-ON RESET (Figure 15)						
V_{CC} for Chip Enabled	V_{POR1+}			2.9		V
Power-On Reset Parameters	V_{POR2+}	Voltage for output on		V_{CC} - 0.8		V
	V_{POR2-}	Voltage for output off		V_{CC} - 0.9		
	V_{POR3+}	Voltage for output on		3.3		
	V_{POR3-}	Voltage for output off		3.2		
IC Power-Up Time				200		µs

Note 1: Parameters in parentheses ( ) are provided for guidance, but are not tested or guaranteed.

Note 2: Figure 1 shows the AC test circuit. Settling time is defined from the 50% point of a transition to the greater of ±5% of I_{FINAL} or ±1% of I_{SWITCH}. Control register *gs_* ≥ 34. See Figure 18.

Note 3: $I_{DAC} \approx G0 + I_{DAC_G1} \times VD + I_{OUT}/I_{DAC_G2}$, where VD is the average video bit density (Δbits/ns) as shown in Table 1.

Table 1. Example Calculation of Video Bit Density

PIXEL	TIME (ns)	VIDEO CODE	ΔBITS	VD
0	0	1111111111	—	—
1	10	0000000000	10	1.0
2	20	0111111111	9	0.9
3	30	1000000000	10	1.0
4	40	1000000001	1	0.1

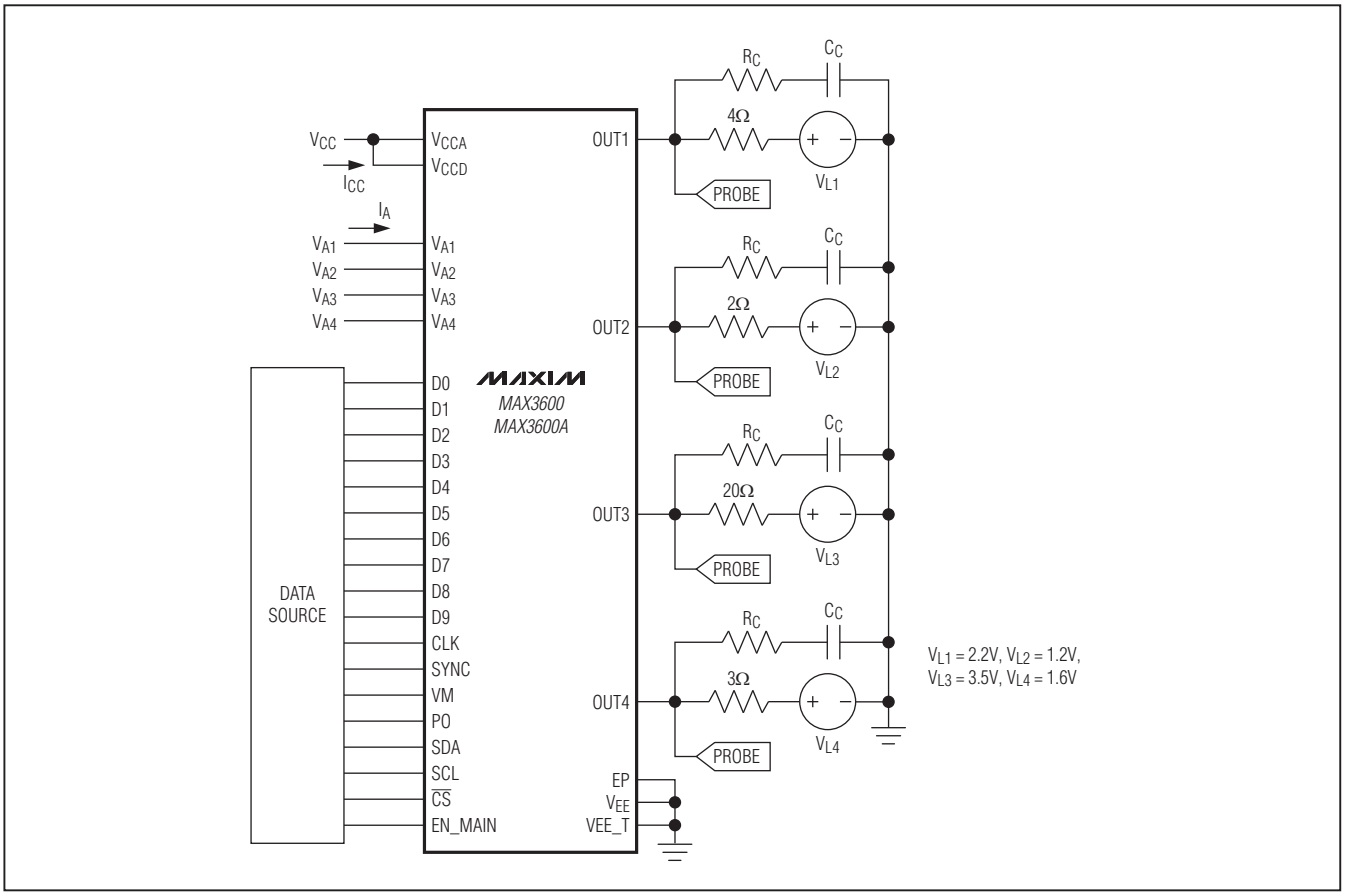


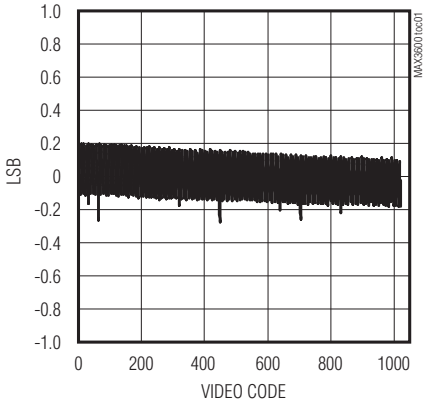
Figure 1. Test Circuit

Laser Driver for Projectors

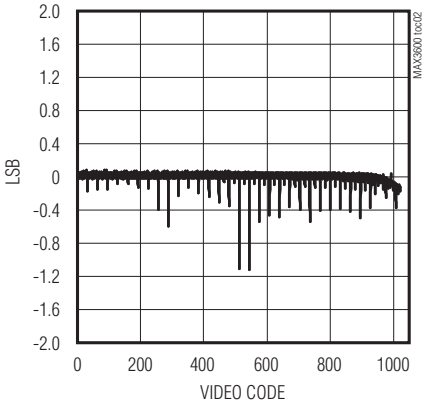
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, EN_MAIN high, unless otherwise noted. $V_{C_}$ = $V_{A_}$ - $V_{OUT_}$.)

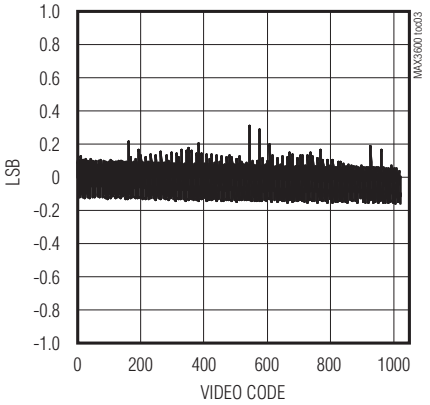
VIDEO DNL OUT1
(gs1 = FFh, T_J = +125°C, $V_{C_}$ = 0.9V)



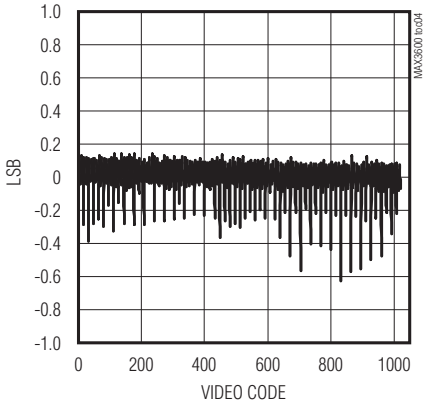
VIDEO DNL OUT2
(gs2 = FFh, T_J = +125°C, $V_{C_}$ = 0.9V)



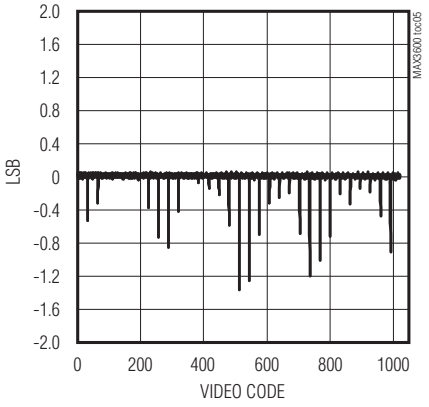
VIDEO DNL OUT3
(gs3 = FFh, T_J = +125°C, $V_{C_}$ = 0.9V)



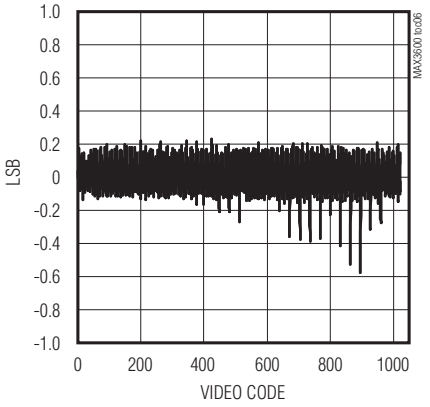
VIDEO DNL OUT1
(gs1 = 20h, T_A = -40°C)



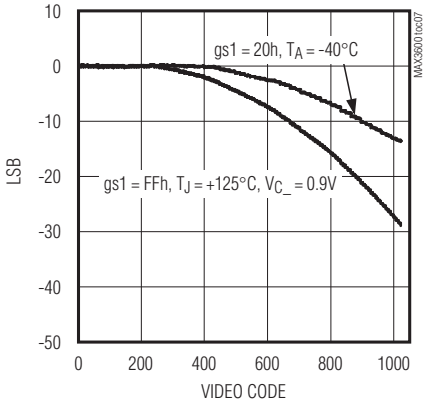
VIDEO DNL OUT2
(gs2 = 20h, T_A = -40°C)



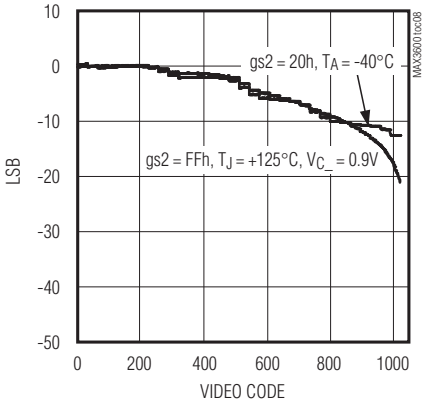
VIDEO DNL OUT3
(gs3 = 20h, T_A = -40°C)



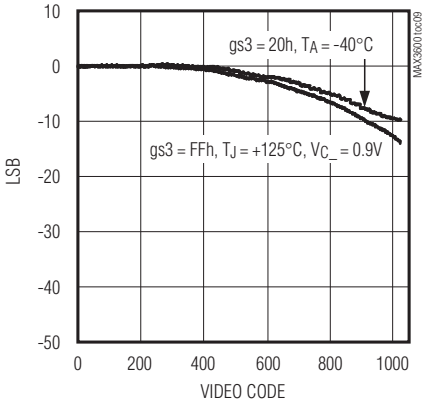
VIDEO INL OUT1



VIDEO INL OUT2



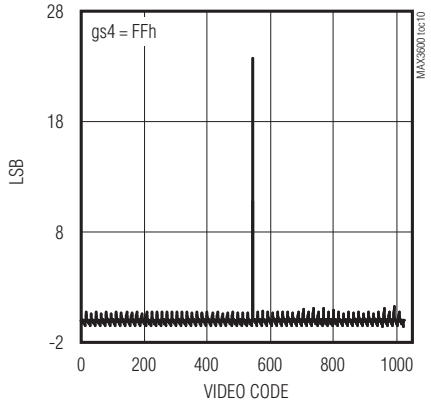
VIDEO INL OUT3



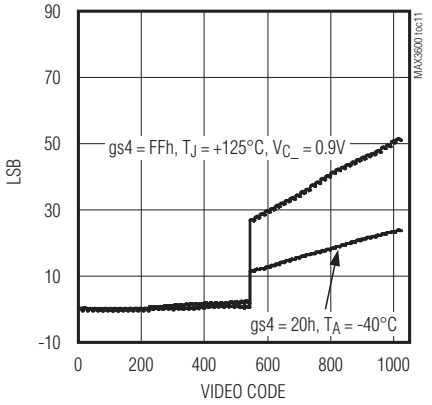
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, EN_MAIN high, unless otherwise noted. $V_{C_}$ = $V_{A_}$ - $V_{OUT_}$.)

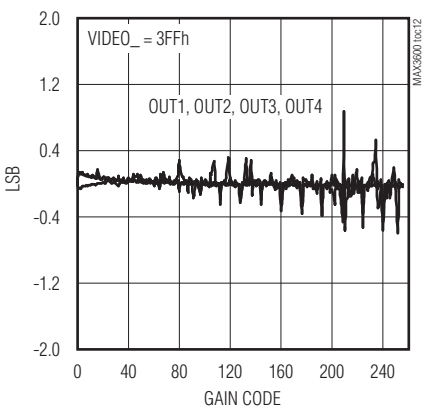
VIDEO DNL OUT4



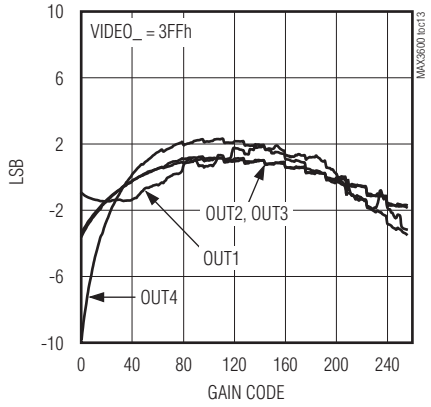
VIDEO INL OUT4



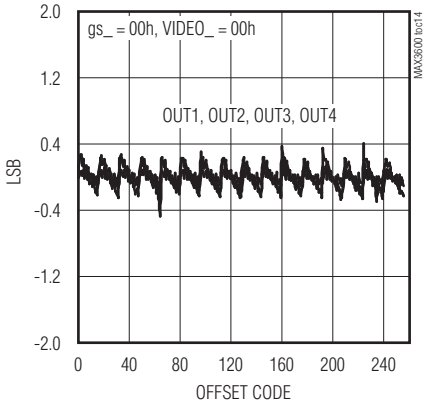
GAIN DNL



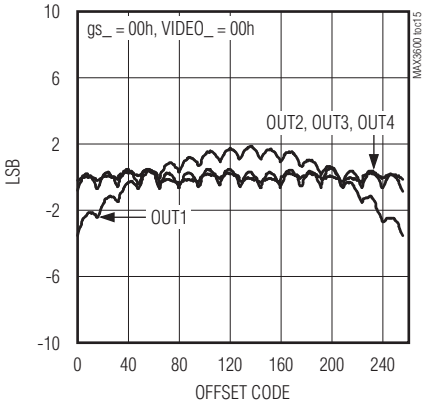
GAIN INL



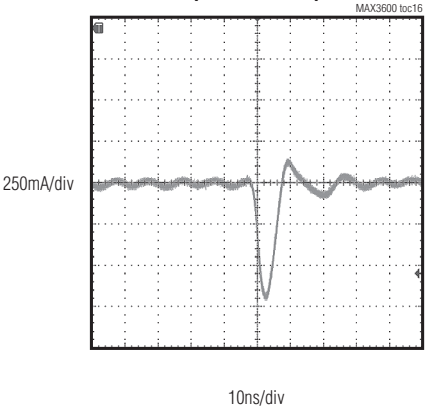
OFFSET DNL



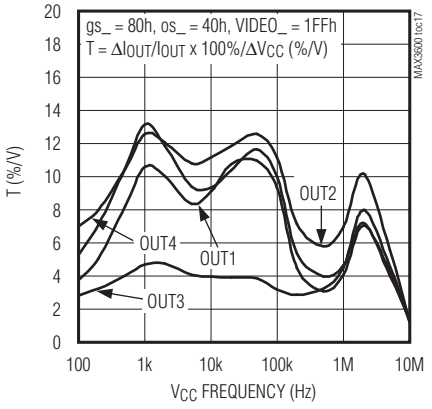
OFFSET INL



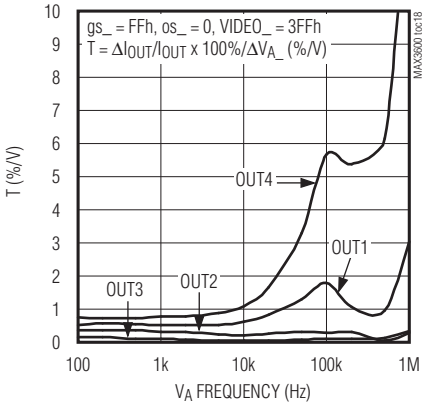
OUT2 PO PULSE (f_{CLK} = 50MHz)



TRANSFER FROM V_{CC} TO I_{OUT}



TRANSFER FROM V_A TO I_{OUT}

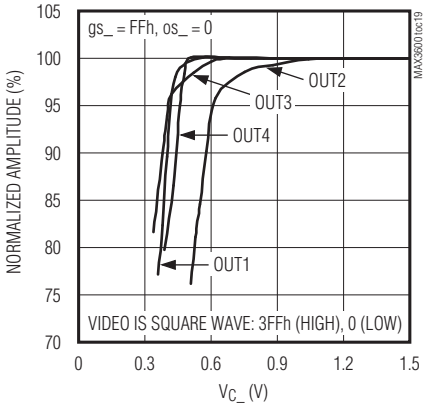


Laser Driver for Projectors

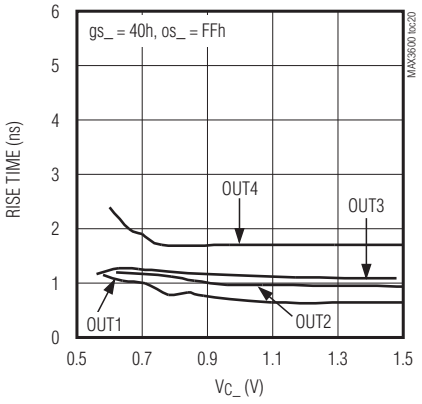
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, EN_MAIN high, unless otherwise noted. $V_{C_}$ = $V_{A_}$ - $V_{OUT_}$.)

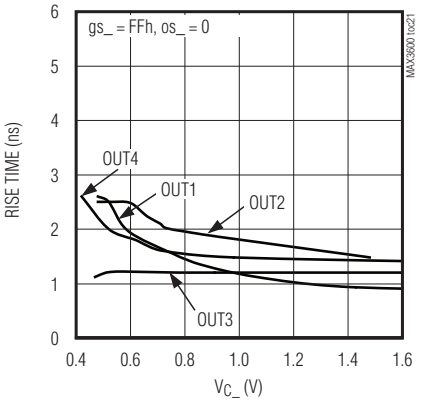
NORMALIZED OUTPUT CURRENT vs. COMPLIANCE VOLTAGE ($V_{A_}$ - $V_{OUT_}$)



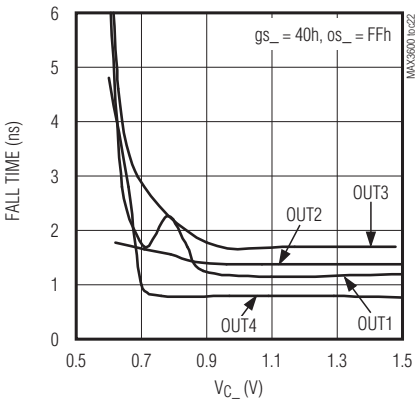
OUTPUT RISE TIME vs. COMPLIANCE VOLTAGE ($V_{A_}$ - $V_{OUT_}$)



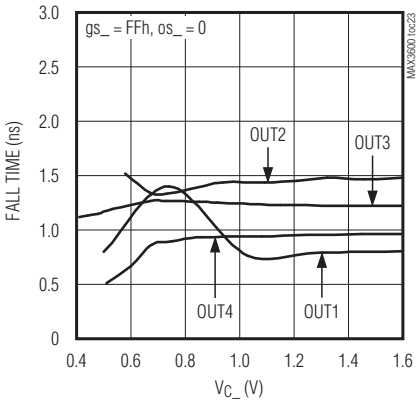
OUTPUT RISE TIME vs. COMPLIANCE VOLTAGE ($V_{A_}$ - $V_{OUT_}$)



OUTPUT FALL TIME vs. COMPLIANCE VOLTAGE ($V_{A_}$ - $V_{OUT_}$)



OUTPUT FALL TIME vs. COMPLIANCE VOLTAGE ($V_{A_}$ - $V_{OUT_}$)



Pin Description

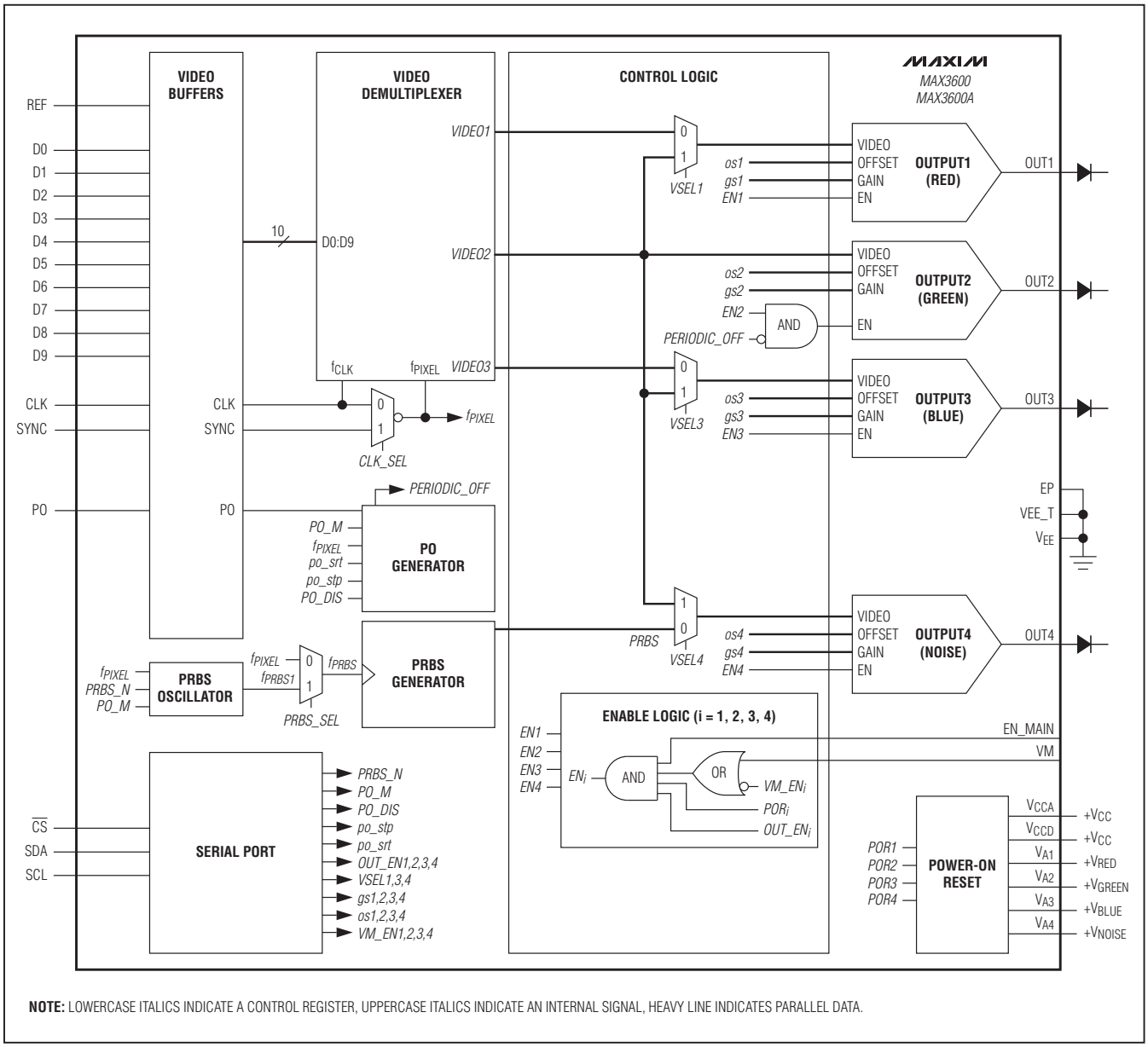
PIN	NAME	FUNCTION
1	D0	Synchronous Video Data Inputs. D0 is the LSB; D9 is the MSB.
2	D1	
3	D2	
4	D3	
5	D4	
6	D5	
7	D6	
8	D7	
9	D8	
10	D9	
11	SYNC	Pixel Clock Input in Configuration 1. See the *Typical Operating Circuits*.
12	CLK	Video Clock Input
13	RES	Reserved for Future Use. Leave open.
14	OUT3	Connect to Blue Laser Anode. If unused leave open. Available on the MAX3600/A/B only.
15	V_{A3}	Blue Laser Supply Voltage
16, 24, 32	V_{EE}	Ground Connections. Connect to 0V.
17	SDA	Data I/O for Serial Port
18	$\overline{CS}$	Active-Low Chip Select
19	SCL	Clock Input for Serial Port
20	EN_MAIN	Laser Enable Input. When low, laser current is reduced (3.3V CMOS input with 60kΩ resistor to V_{EE}).
21	VEE_T	Test. Connect to V_{EE} for normal operation.
22	V_{A4}	Noise Diode Supply Voltage
23	OUT4	Connect to Noise Diode Anode. If unused, leave open. Available on the MAX3600/A/G only.
25, 27, 29	V_{A2}	Green Laser Supply Voltage
26, 28, 30	OUT2	Connect to Green Laser Anode. If unused, leave open. Available on the MAX3600/A/G only.
31	N.C.	No Connection. There is no connection from the package to the IC.
33	VM	Video Marker Input. 3.3V CMOS input with 60kΩ pullup to V_{CCD}.
34	V_{CCA}	3.3V Analog Supply. Connect directly to V_{CCD}.
35, 37	V_{A1}	Red Laser Supply Voltage
36	OUT1	Connect to Red Laser Anode. If unused, leave open. Available on the MAX3600/A/R only.
38	V_{CCD}	3.3V Digital Supply. Connect directly to V_{CCA}.
39	REF	Reference Threshold Voltage for Synchronous Inputs
40	PO	Periodic Off Video Data Input. If the periodic off feature is not used, connect the PO pin to ground through a resistor. For periodic off on every pixel, connect PO to V_{CC} through a resistor. ($R_{PO} \approx$ 2.2kΩ is suitable for all configurations. The resistor is optional, but reduces power.)
—	EP	Exposed Pad. The exposed pad must be connected to V_{EE}.

Laser Driver for Projectors

Detailed Description

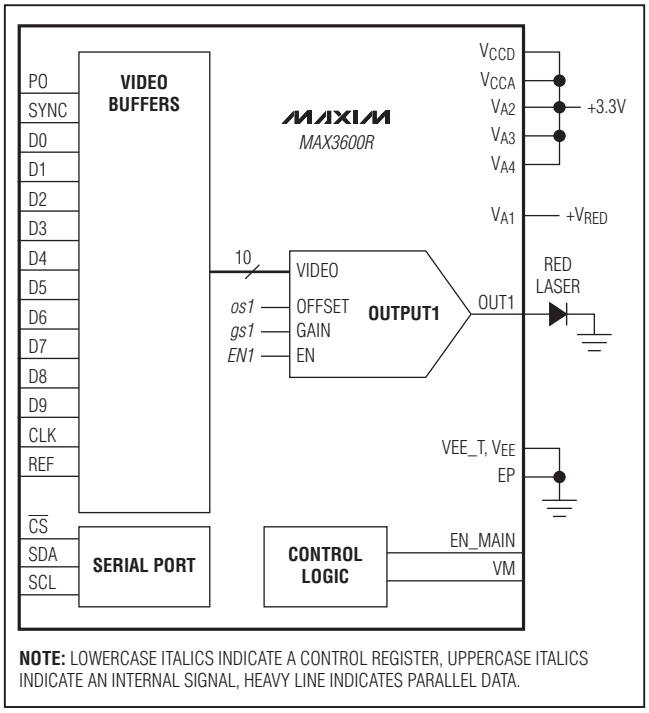
The laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes a 10-bit video DAC with programmable gain and offset.

OUTPUT1, OUTPUT2, and OUTPUT3 support operation with red, green, and blue lasers. OUTPUT4 and the PRBS generator provide noise as required for certain synthetic green lasers. The MAX3600R (Figure 3), MAX3600G (Figure 4), and MAX3600B (Figure 5) are monochrome laser drivers.



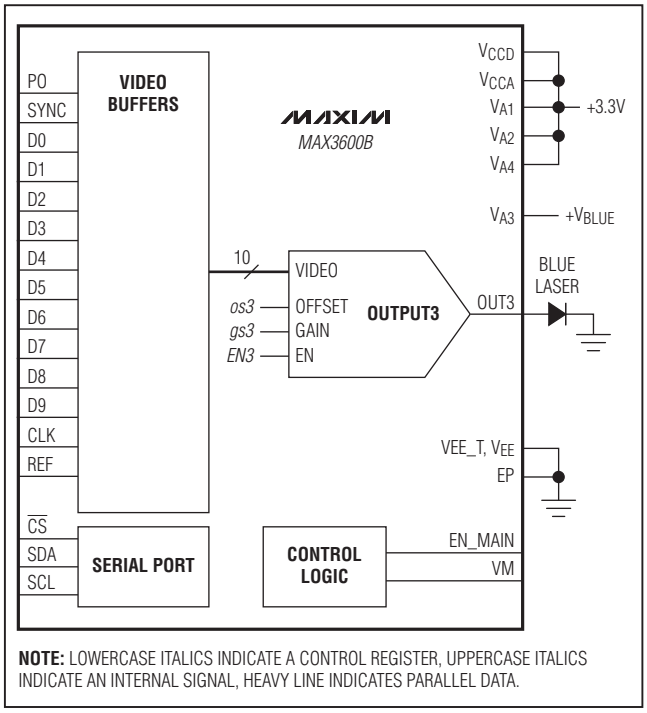
NOTE: LOWERCASE ITALICS INDICATE A CONTROL REGISTER, UPPERCASE ITALICS INDICATE AN INTERNAL SIGNAL, HEAVY LINE INDICATES PARALLEL DATA.

Figure 2. MAX3600/MAX3600A Functional Diagram



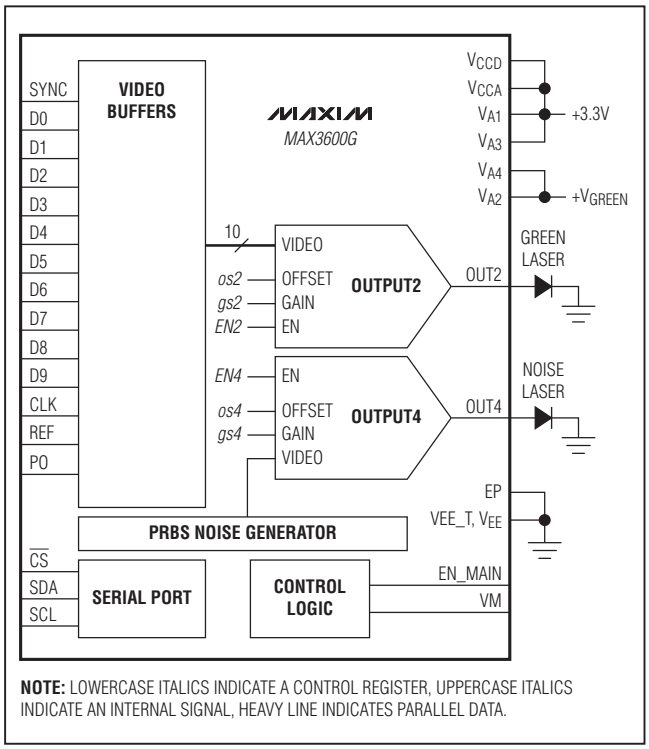
NOTE: LOWERCASE ITALICS INDICATE A CONTROL REGISTER, UPPERCASE ITALICS INDICATE AN INTERNAL SIGNAL, HEAVY LINE INDICATES PARALLEL DATA.

Figure 3. MAX3600R Functional Diagram



NOTE: LOWERCASE ITALICS INDICATE A CONTROL REGISTER, UPPERCASE ITALICS INDICATE AN INTERNAL SIGNAL, HEAVY LINE INDICATES PARALLEL DATA.

Figure 5. MAX3600B Functional Diagram



NOTE: LOWERCASE ITALICS INDICATE A CONTROL REGISTER, UPPERCASE ITALICS INDICATE AN INTERNAL SIGNAL, HEAVY LINE INDICATES PARALLEL DATA.

Figure 4. MAX3600G Functional Diagram

Laser Driver for Projectors

Video Input Buffers

The synchronous video data inputs (D0 to D9, SYNC, CLK, and PO) are pseudo-differential. Each input is compared to V_{REF}, as shown in Figure 6.

D0 to D9, PO, and SYNC can be left open. SYNC can be connected to REF if not used (for reduced power consumption).

Video Demultiplexer

The video demultiplexer (Figure 7) can accommodate configurations as shown in the *Typical Operating Circuits*. In Configuration 1 (Figure 19), 10-bit red, green, and blue video data is time multiplexed. The SYNC signal is used to demultiplex the video data.

In Configuration 2 (Figure 21), each output driver uses VIDEO2 as a data source.

Driver Outputs

The driver outputs provide currents to the lasers as shown in Figure 8.

The transfer characteristic of the driver outputs is shown in Figure 10 and Equation 1.

Equation 1:

$$-I_{OUT} = \frac{VIDEO}{3FFh}\left[\frac{G_{HIGH} \times gs}{FFh} + G_{LOW}\right] + \left[\frac{OS_{HIGH} \times os}{FFh}\right] + OS_{LOW}$$

where:

- Current into the laser driver is positive (out is negative)
- VIDEO is the 10-bit video input
- *gs* is the 8-bit gain setting register
- *os* is the 8-bit offset setting register
- G_{LOW} is the minimum gain (mA)
- (G_{LOW} + G_{HIGH}) is the maximum gain (mA)
- OS_{HIGH} is the maximum offset (mA)
- OS_{LOW} is the minimum offset (mA)

The output compliance voltage ($V_{C_}$ = $V_{A_}$ - $V_{OUT_}$, Figure 9) defines the output voltage required to obtain low overshoot and fast settling time.

Table 2 summarizes the typical output current capability for each driver output. Table 3 summarizes the maximum ratings for each driver output.

Table 2. Driver Output Typical Parameter Summary

PARAMETER	OUT1 (mA)	OUT2 (mA)	OUT3 (mA)	OUT4 (mA)
Minimum Gain (G_{LOW})	12	40	10	10
Maximum Gain (G_{LOW} + G_{HIGH})	227	690	170	185
Maximum Offset (OS_{HIGH})	83	83	83	155

Table 3. Driver Output Absolute Maximum Ratings (Current Out of Part)

PARAMETER	OUT1 (mA)	OUT2 (mA)	OUT3 (mA)	OUT4 (mA)
DC Current (T_J = +125°C)	320	735	245	310
DC Current (T_J = +110°C)	480	1100	382	465
Peak Current (t < 1µs, T_J = +125°C)	640	1470	490	620

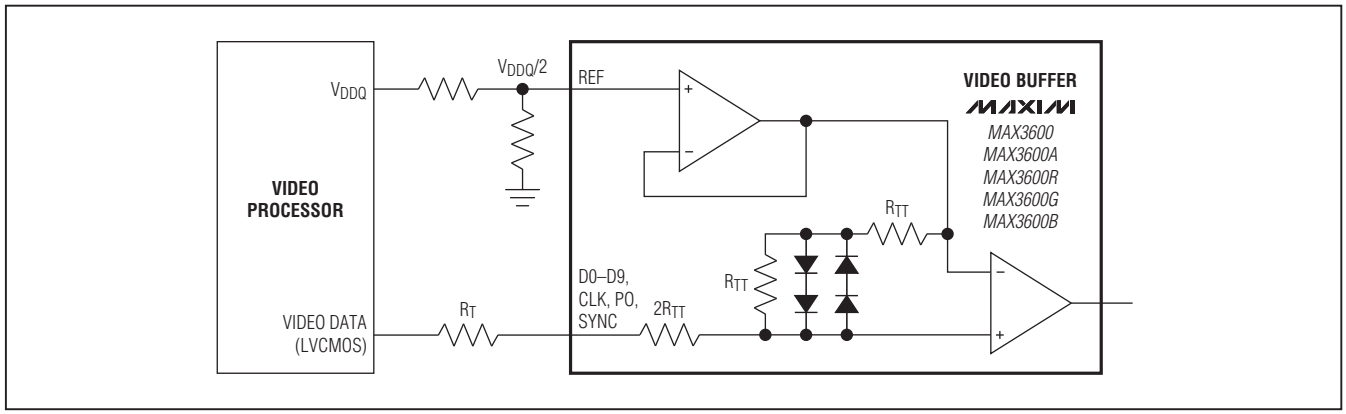


Figure 6. Video Inputs

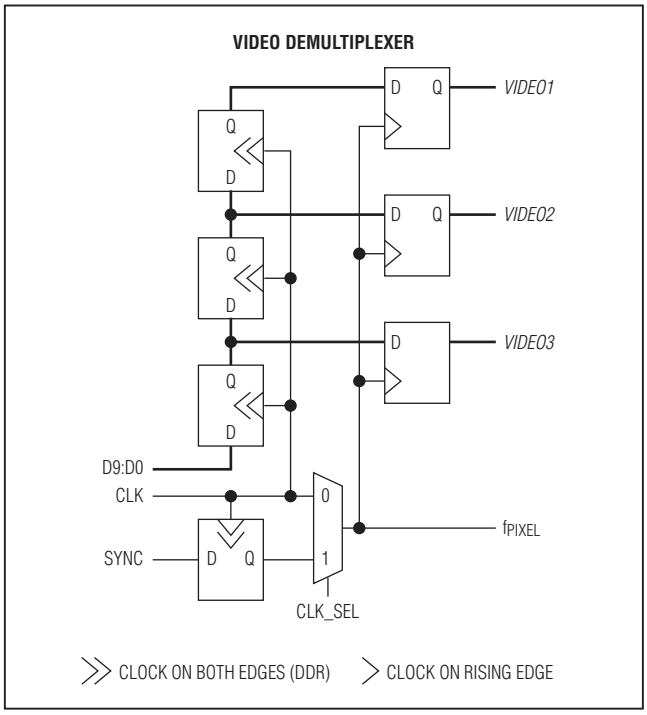


Figure 7. Video Demultiplexer

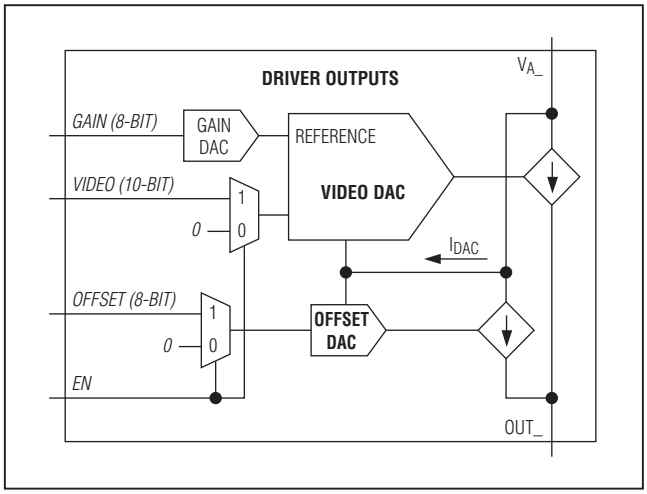


Figure 8. Driver Output

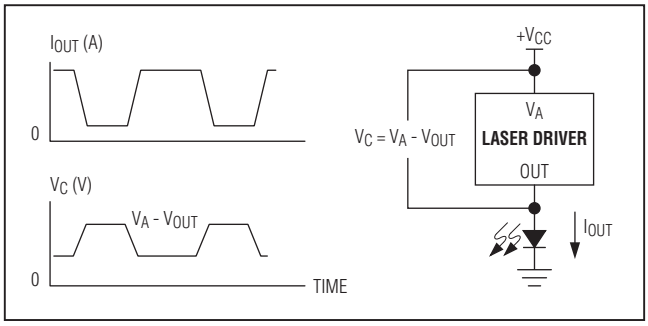


Figure 9. Output Compliance Voltage

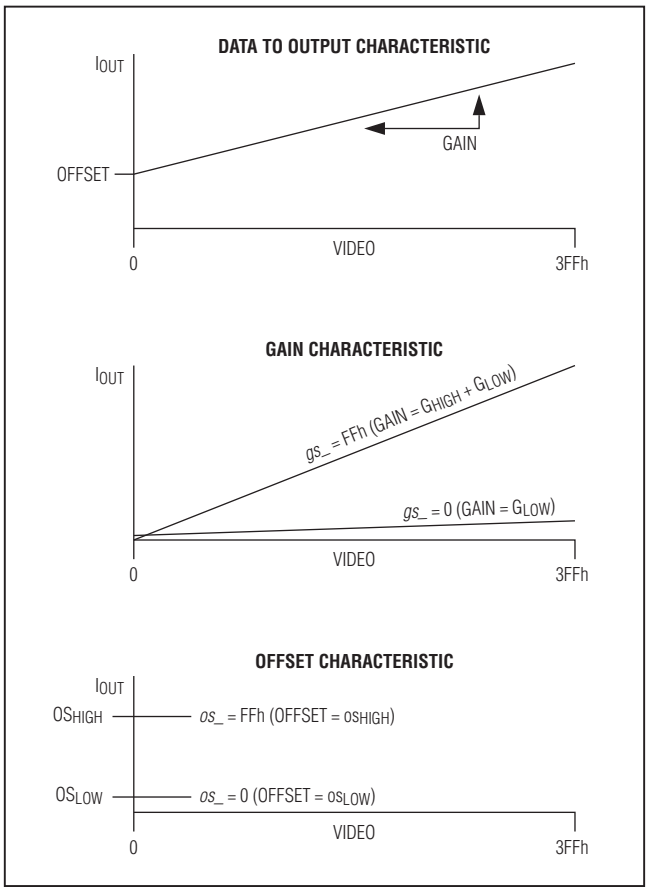


Figure 10. Data to Output Characteristics

Laser Driver for Projectors

Control Logic

The control logic provides video selection, laser enable, and power savings.

Video Selection

The video demultiplexer creates signals *VIDEO1*, *VIDEO2*, and *VIDEO3*. The VSEL[1/3/4] bits can be used to select the input video for OUTPUT1, OUTPUT3, and OUTPUT4.

Laser Control

When EN_MAIN is low, all driver outputs are off. This signal works asynchronously (no clock is required to disable outputs).

The video marker (VM) input can be used to disable selected outputs when a video signal is not present (Figure 11). The VM_EN[1:4] bit settings determine which outputs respond to the VM signal.

Propagation delay from VM↑ or EN_MAIN↑ to output active is typically 35ns + 2/f_{PIXEL}.

Periodic Off Generator

The periodic off (PO) generator quickly switches off OUTPUT2. The PO event is placed within a pixel if PO is set high during a pixel as shown in Figure 12.

The PO event location within the pixel is programmed from the serial port. Each pixel is divided into "m" equal time subpixels as shown in Figure 13. The PO_M setting determines the number of subpixels, where:

$$m = (PO_M + 1) \times 8$$

The PO start and PO stop locations (in subpixels) are defined by the P1, P1S, P2, and P2S bits.

Start Subpixel =

$$[(P1 + 1) \text{ MOD } (PO_M + 1)] \times 8 + P1S + 1$$

Stop Subpixel =

$$[(P2 + 1) \text{ MOD } (PO_M + 1)] \times 8 + P2S + 1$$

The start and stop locations should be selected to ensure that the PO event occurs > one rise/fall time from the pixel update. The minimum off-time is four subpixels. Select P1, P2 ≤ PO_M.

The PO oscillator frequency (f_{PO}) = f_{PIXEL} x (PO_M + 1). The intended operating range for f_{PO} is 133MHz to 200MHz.

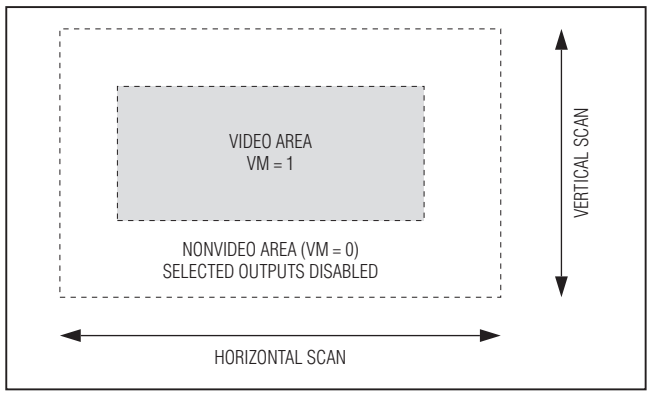


Figure 11. Video Marker

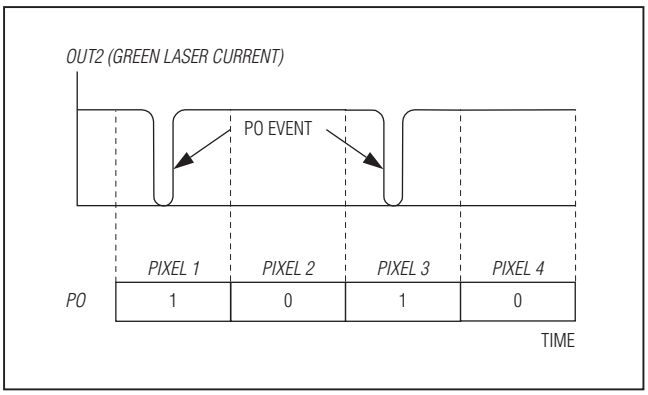


Figure 12. Periodic Off (PO) Example

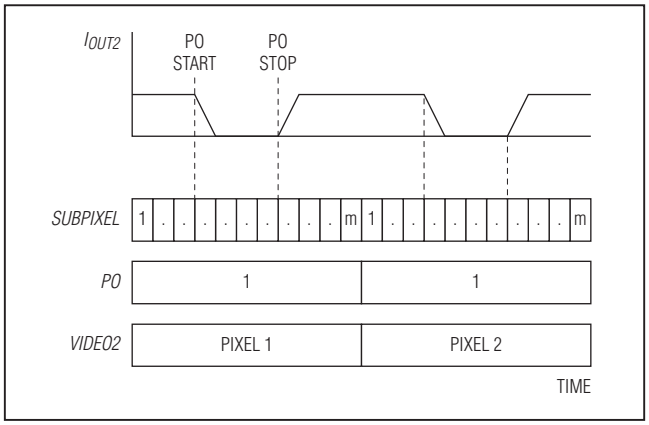


Figure 13. PO Subpixels

Table 4. PO Subpixel Programming

t_{PIXEL} (ns)	PO_M	PRBS_N	SUBPIXELS (m)	f_{PRBS1} (MHz)
10	1	3	16	136
12	1	2	16	125
14	1	0	16	129
16	2	3	24	128
18	2	2	24	125
20	2	1	24	120
22	2	0	24	123
24	3	2	32	125
26	4	3	40	131
28	4	3	40	121
30	4	2	40	125
32	4	1	40	125
34	5	3	48	120
36	5	2	48	125
38	6	3	56	125
40	6	3	56	119

Table 5. PRBS Oscillator

PRBS_N	f_{PRBS1}/f_{PO}
0	0.9
1	0.8
2	0.75
3	0.68

PRBS Oscillator

The PRBS oscillator creates clock f_{PRBS1}, which can be input to the PRBS generator. The oscillator frequency is determined by the PRBS_N bit setting as shown in Table 5. The recommended range for f_{PRBS1} is 100MHz to 150MHz. Note that the PRBS oscillator is not phase-locked to the pixel clock. Therefore, OUT4 updates are not synchronous to the pixel clock when the PRBS oscillator is used.

PRBS Generator

Output 4 can be used to generate random noise. A 32-bit shift register with feedback generates pseudo-random codes. The PRBS_SEL bit selects the PRBS clock source.

Serial Port and Registers

The serial port provides a 3-wire interface with bidirectional data (SDA), clock input (SCL), and a chip-select input ($\overline{CS}$) as shown in Figure 14. Table 6 shows the register addresses. The external master initiates a data transfer by asserting the $\overline{CS}$ pin.

Write Mode (R/$\overline{W}$ = 0): The master generates 16 clock cycles. It outputs 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master ends the transmission by setting $\overline{CS}$ high. The laser driver updates control registers on the rising clock edge of the last data bit.

Read Mode (R/$\overline{W}$ = 1): The master generates 16 clock cycles. It outputs 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the R/$\overline{W}$ bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master ends the transmission by setting the $\overline{CS}$ pin high. Read clock speed is determined by the external pullup resistor and parasitic capacitance at the SDA pin.

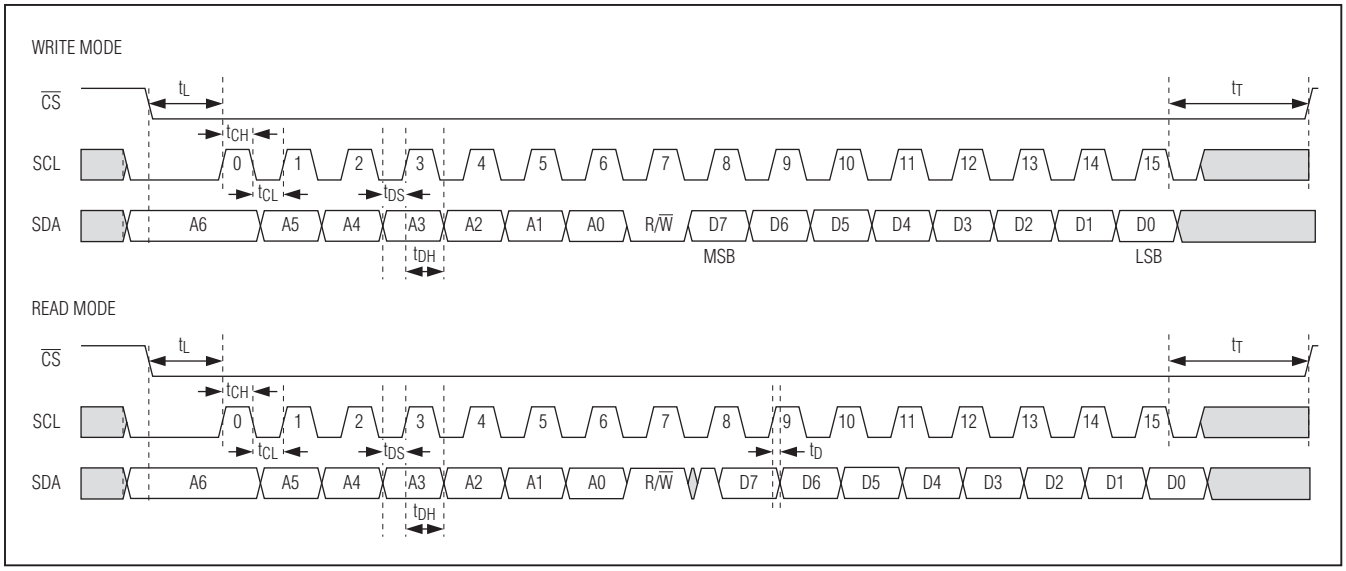


Figure 14. Serial Port Timing Diagram

Table 6. Register Map

ADDRESS	NAME	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	os1	OUTPUT1 Offset	MSB							LSB
01h	gs1	OUTPUT1 Gain	MSB							LSB
02h	os2	OUTPUT2 Offset	MSB							LSB
03h	gs2	OUTPUT2 Gain	MSB							LSB
04h	os3	OUTPUT3 Offset	MSB							LSB
05h	gs3	OUTPUT3 Gain	MSB							LSB
06h	os4	OUTPUT4 Offset	MSB							LSB
07h	gs4	OUTPUT4 Gain	MSB							LSB
08h	enable	Enable	OUT_ EN1	OUT_ EN2	OUT_ EN3	OUT_ EN4	VM_EN1	VM_EN2	VM_EN3	VM_EN4
09h	cnfig	Video Data Control	X	X	X	VSEL1	VSEL3	VSEL4	PRBS_ SEL	CLK_ SEL
0Ah	osc	Oscillator	X	X	PRBS_N MSB	PRBS_N LSB	PO_DIS	PO_M MSB	PO_M	PO_M LSB
0Bh	po_srt	PO Start Subpixels	X	X	P1 MSB	P1	P1 LSB	P1S MSB	P1S	P1S LSB
0Ch	po_stp	PO Stop Subpixels	X	X	P2 MSB	P2	P2 LSB	P2S MSB	P2S	P2S LSB

Note: *Registers default to (0) at power-on (unless a different default value is noted).*

Table 7. cnfig Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:5	X	0	Unused.
4	VSEL1	0	Video select for OUTPUT1. 0 = VIDEO1, 1 = VIDEO2.
3	VSEL3	0	Video select for OUTPUT3. 0 = VIDEO3, 1 = VIDEO2.
2	VSEL4	0	Video select for OUTPUT4. 0 = PRBS, 1 = VIDEO2.
1	PRBS_SEL	0	PRBS clock source select. 1 = f_{PRBS1}, 0 = f_{PIXEL}.
0	CLK_SEL	1	Pixel clock source select. 0 = CLK pin, 1 = SYNC pin.

Table 8. osc Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:4	PRBS_N	0	PRBS oscillator configuration. See Table 5. Bit 5 is the MSB, and bit 4 is the LSB.
3	PO_DIS	0	Disables the output of the PO pulse generator. When the value is 1, no PO pulses are created.
2:0	PO_M	1	PO oscillator control. See Table 4. Bit 2 is the MSB, and bit 0 is the LSB.

Table 9. po_srt Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:3	P1	1	These bits contain the P1 parameter used to program the PO start subpixel.
2:0	P1S	4	These bits contain the P1S parameter used to program the PO start subpixel.

Table 10. po_stp Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:3	P2	0	These bits contain the P2 parameter used to program the PO stop subpixel.
2:0	P2S	1	These bits contain the P2S parameter used to program the PO stop subpixel.

Laser Driver for Projectors

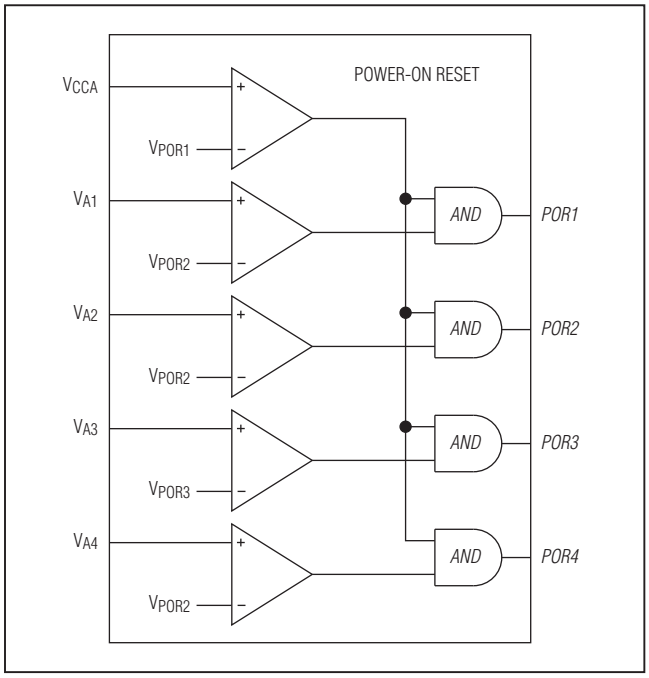


Figure 15. Power-On Reset

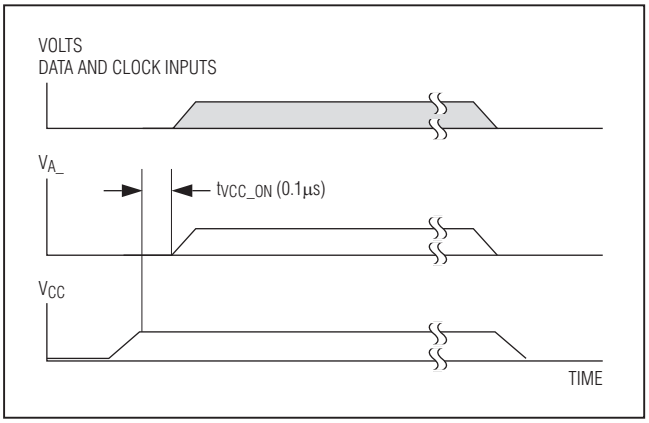


Figure 16. Power-Supply Sequencing

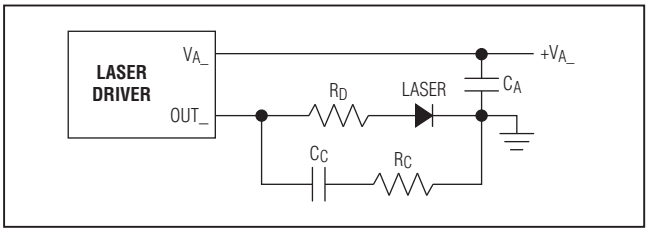


Figure 17. Optional Compensation Components

Power-On-Reset

The power-on reset monitors the supply voltages of the circuit (Figure 15). It is recommended that V_{CC} be applied to the IC before V_{A1} to V_{A4} are applied as shown in Figure 16. On power-down, it is recommended that V_{A1} to V_{A4} are powered down before V_{CC}. *Failure to follow the sequencing recommendation can result in device stress, but has not been observed to cause immediate damage.*

Design Procedure

Supply Filter

Element C_A (see the *Typical Operating Circuits*) is present to reduce supply noise and provide a ground return path for switched current. Select $C_A \geq 10\mu F$. C_A can be composed of two or three capacitors in parallel.

Use care to ensure V_{A3} does not exceed +9V at any time, including power-on, as this can damage the ESD protection circuitry.

Compensation Network

Optional compensation elements R_C and C_C can be used to compensate the inductive load of the laser (Figure 17). The resulting filter reduces ringing and increases the switching time of the laser driver. The best values for R_C and C_C should be found by experimentation. Note that C_C must be charged before light output appears from the laser. If a compensation network is used, minimize inductance in the ground return.

Typical starting values:

$$R_C \approx R_L \text{ to } 2 \times R_L \ (R_L = \text{Laser Resistance})$$

$$C_C \approx 1/(2\pi f_{VIDEO} \times R_L)$$

Ringing of the green laser can be reduced with resistor R_D.

PCB Layout

Place the green laser as close to the laser driver as possible. The green laser typically has a small resistive component and is more sensitive to inductance than other laser connections. The green laser connection should appear as a low-impedance transmission line. Use wide traces located close to the ground plane for maximum capacitance.

The connection from OUT2 to the laser should be as short as possible, ideally < 1cm. The connection distance from the laser cathode, across the ground plane, through the filter capacitor, to V_{A2}, is ideally < 1cm.

Consider the power supply on the $V_{A_}$ pins. Droop on these pins reduces the compliance voltage. Use two or three capacitors to bypass $V_{A_}$ to ground. Place a small capacitor close to the V_{A2} pin to keep the ground return loop small. A larger capacitor can be located farther from $V_{A_}$.

It is best to solder the laser to the PCB. If a connector is required, minimize inductance. Inductance > 10nH at OUT2 could cause large ringing. When routing OUTPUT1 and OUTPUT2, route connections to the $V_{A_}$ pins on the top layer, and connect the OUT_ pins to the laser through vias.

Laser Driver Thermal Considerations

The circuit is designed to meet specifications with an operating junction temperature (T_J) up to +125°C. The junction temperature is estimated by:

$$T_J \approx [(I_{CC})(V_{CC}) + \Sigma (I_{VA_})(V_{C_})]\ \theta_{JA} + T_A$$

The recommended thermal path is through the package backside exposed pad (EP). A heatsink on the package top does not significantly reduce junction temperature. Recommendations for PCB design are found in Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Table 11. Thermal Design Properties

PARAMETER	SYMBOL	VALUE
Ambient Temperature	T_A	—
Operating Junction Temperature	T_J	≤ +125°C
Thermal Resistance, Junction-to-Case	θ_{JC}	+2°C/W
Thermal Resistance, Junction-to-Ambient, Multilayer Board	θ_{JA-2}	+28°C/W

Note: *Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to* ***www.maxim-ic.com/thermal-tutorial****.*

Applications Information

Connecting OUT2 and OUT4

It is possible to connect OUT4 and OUT2 to achieve a higher output current. There is a small delay on OUT4 relative to OUT2. Note that OUT4 linearity performance is lower than OUT2 linearity.

Eye Safety

Specification IEC 825 defines the maximum safe output of optical devices. This laser driver provides enable features that aid compliance with IEC 825. Using this laser driver alone does not ensure that a product is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Maxim products are not designed for use as components in systems where the failure of a Maxim product could create a situation where injury could occur.

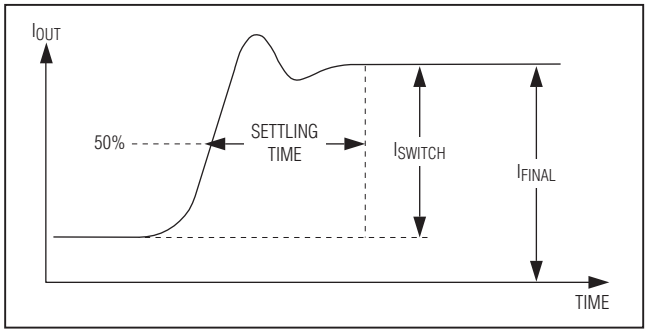


Figure 18. Settling Time and Measurement

Laser Driver for Projectors

Typical Operating Circuits

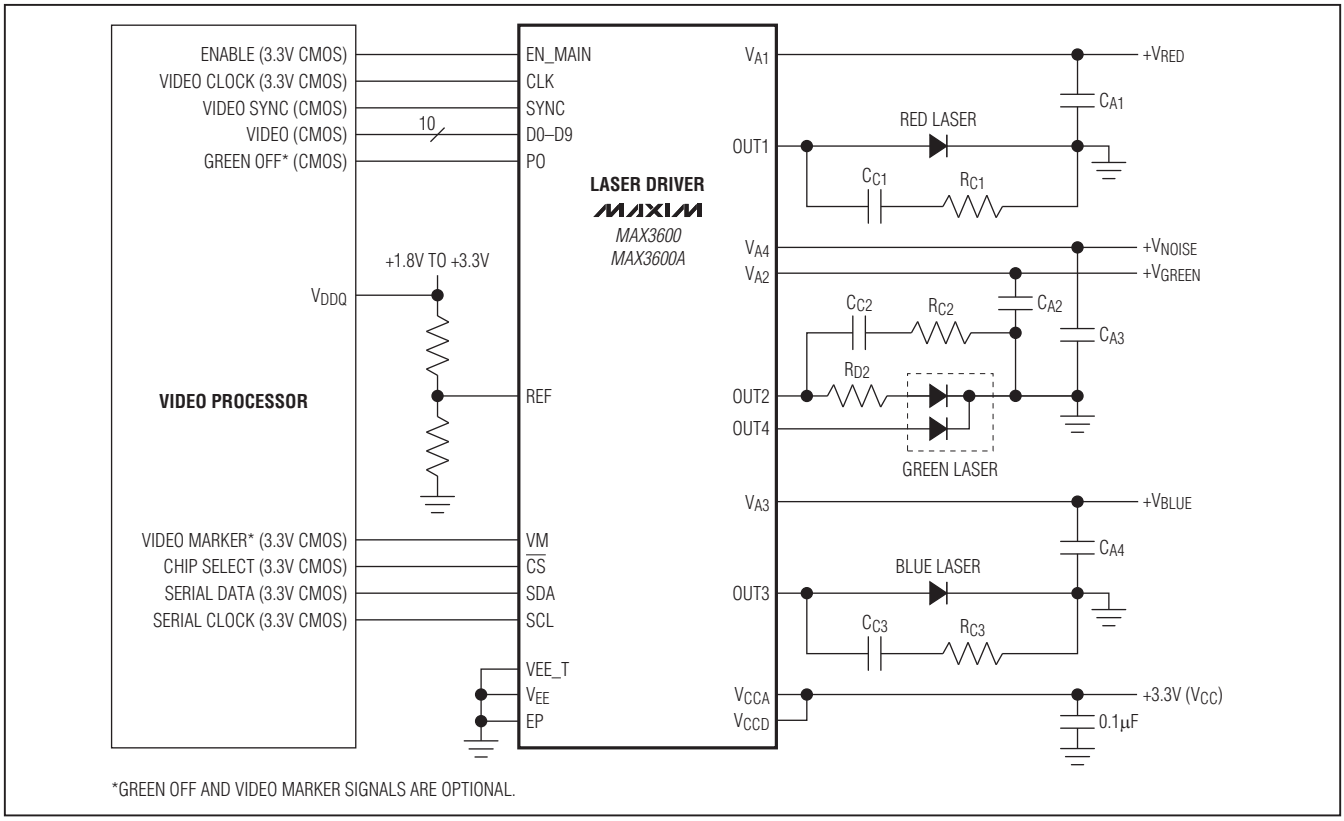


Figure 19. Typical Operating Circuit: Configuration 1

Configuration 1: RGB Laser Driver with DDR Clock

Configuration 1 is described in Figures 19 and 20 and Table 12.

- 10-bit video (D0 = LSB, D9 = MSB), DDR clock
- Data is multiplexed R-G-B (Figure 20)
- SYNC = 1 when blue data is on D0 to D9
- PO event occurs when PO = 1

Table 12. Configuration 1 Register Settings

BIT	SETTING	NOTES
VSEL1	0	*VIDEO1* → red laser
VSEL3	0	*VIDEO3* → blue laser
VSEL4	0	PRBS → noise diode
CLK_SEL	1	DDR clock with SYNC
OUT_EN[1:4]	1	Enable outputs

Note: *See the* Detailed Description *section for more information about register programming.*

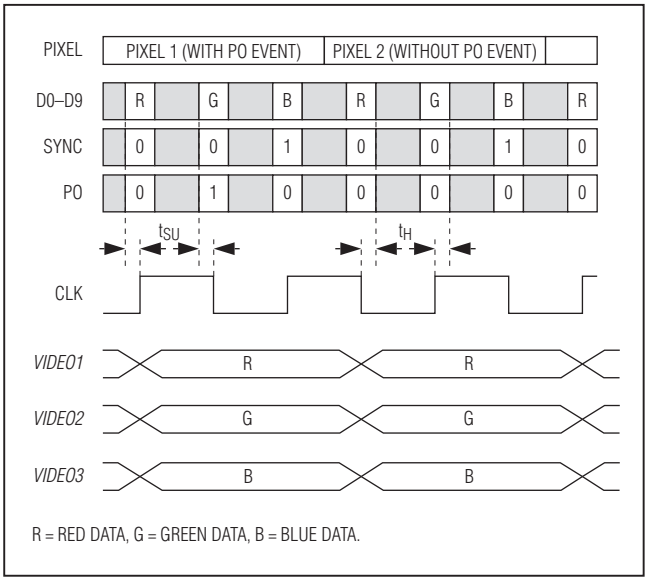


Figure 20. Configuration 1: Video Data Format

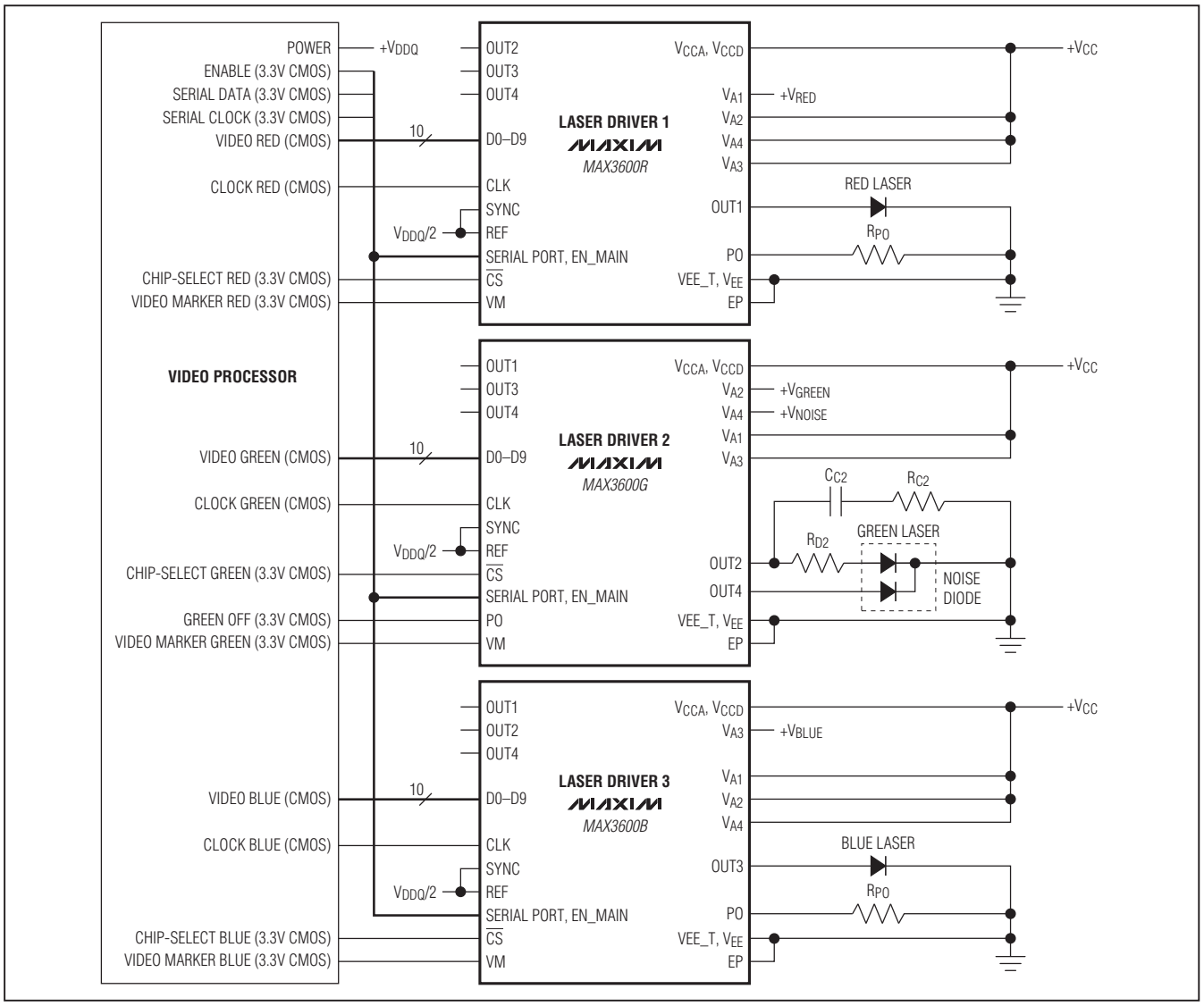


Figure 21. Typical Operating Circuit: Configuration 2

Configuration 2: Video Data with RZ Clock

Configuration 2 is described in Figures 21 and 22 and Table 13.

- 10-bit video (D0 = LSB, D9 = MSB)
- Return-to-zero clock
- Video data is always routed to VIDEO2, for constant delay from clock to output
- Achieves highest possible resolution

Table 13. Configuration 2 Register Settings

LDD	BIT	VALUE	NOTES
1	VSEL1	1	*VIDEO2* → red laser
1	OUT_EN1	1	Enable OUT1
1, 2, 3	CLK_SEL	0	Select RZ clock
2	OUT_EN2, OUT_EN4	1	Enable OUT2, OUT4
3	VSEL3	1	*VIDEO2* → blue laser
3	OUT_EN3	1	Enable OUT3

Note: *See the* Detailed Description *section for more information about register settings.*

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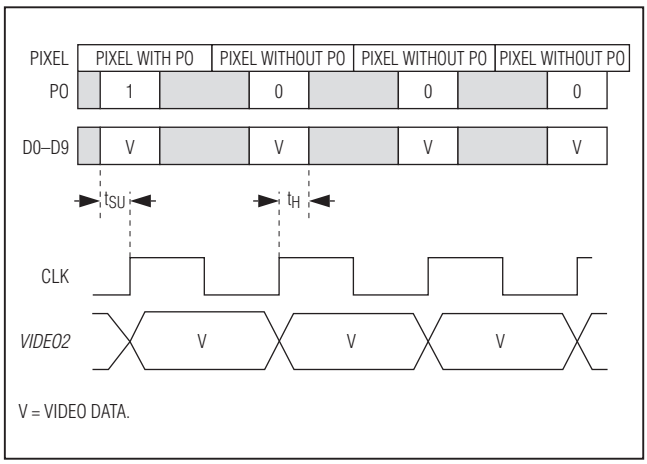
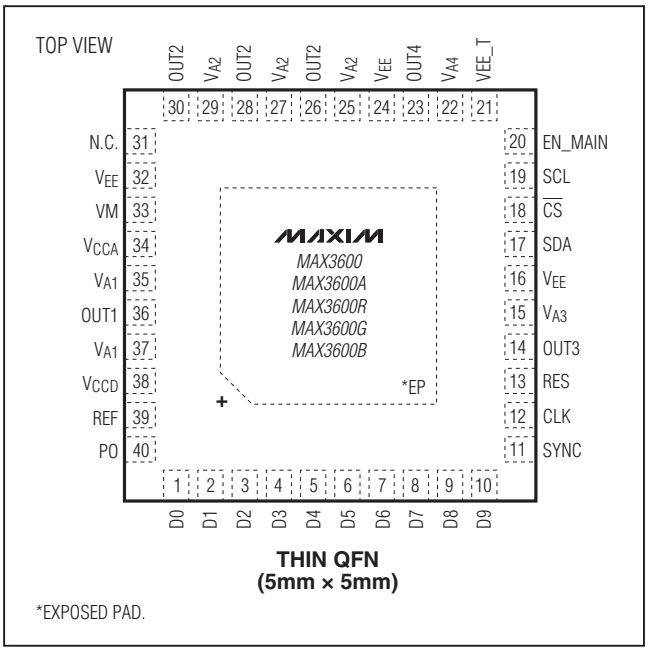


Figure 22. Configuration 2: Video Data Format

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	10/09	Corrected errors for SCL in Figure 14	16
2	8/10	Removed future status from the MAX3600A in the *Ordering Information* table; added the soldering temperature to the *Absolute Maximum Ratings* section; in the *Electrical Characteristics* table updated the analog supply voltage and analog supply current values, added compliance voltage, updated maximum offset values, and added propagation delay; corrected the equation in Note 3; corrected the units for VD in Table 1; replaced Figure 7; added the land pattern no. to the *Package Information* table	1–5, 13, 22

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