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MAX3601

Laser Driver for Projectors

General Description

The MAX3601 laser driver for pico projectors supports video imaging with red, blue, and green lasers. Each output includes two 8-bit digital-to-analog converters (DACs) with programmable gain and up to 400mA driving capability per channel. DAC A has a full-scale current up to 320mA, while DAC B has full-scale current up to 80mA. All three channels can be combined into a single channel with up to 1.2A drive capability.

Maxim's patented technology allows pulsed current to operate lasers efficiently while reducing speckle. This feature operates from the video data clock. The driver is available in a 3.0mm x 3.5mm, 42-bump wafer-level package for commercial applications and a 5mm x 5mm, 40-pin TQFN package for industrial and automotive applications.

Applications

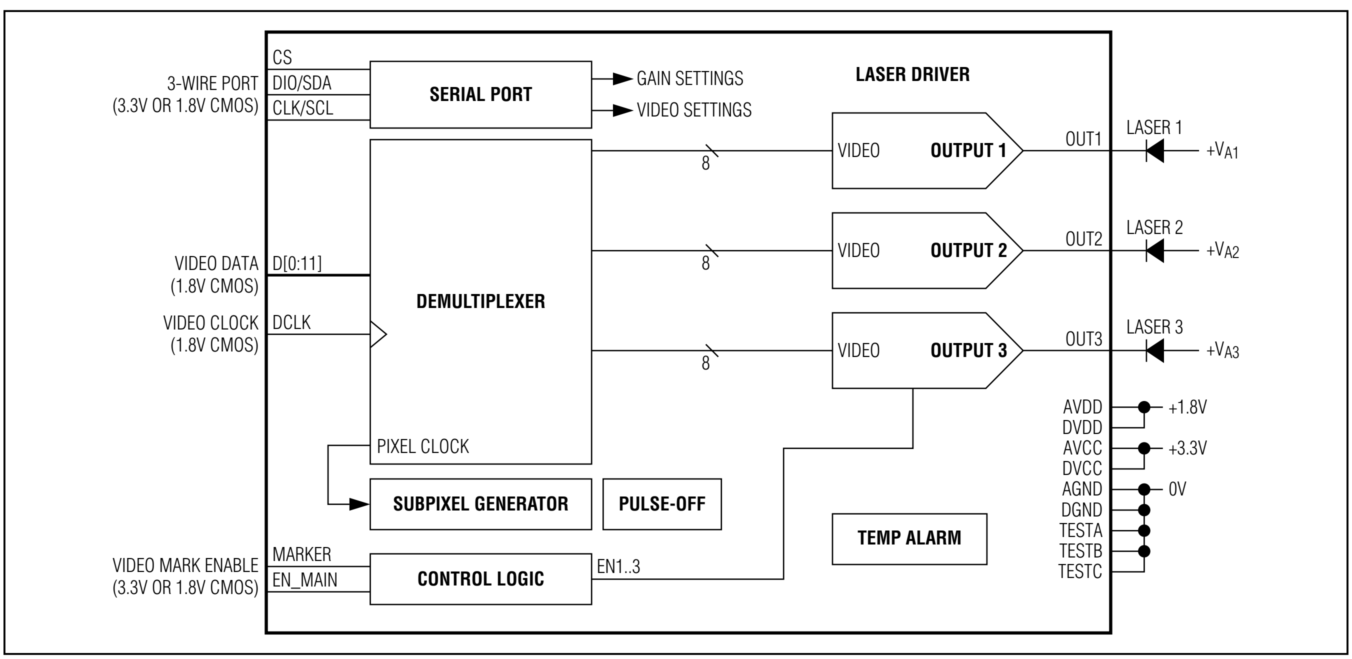
- RGB Pico Laser Projector
- Laser Light Source for LCOS Projectors
- High-Current LED or Laser Pulse Generator

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Integrates Three Current-Output Laser Drivers**
  - **Compatible with Most Red, Blue, and Green Lasers**
  - **8-Bit Video DACs, DC to 167MHz operation**
  - **Patented Pulsing Feature Reduces Laser Speckling**
  - **1ns Output Switching Time**
  - **Pulse Switching Speed Enhancer**
- **Minimizes PCB Area with Functional Integration**
  - **SPI or I²C Serial Port Control**
  - **1.8V to 3.3V Operation**
  - **8-Bit Gain Adjustment**
  - **Programmable Pulse Current**
  - **42-Bump WLP (3.0mm x 3.5mm) and 40-Pin TQFN (5mm x 5mm) Packages**
  - **Integrated Temperature Sensor**
- **Low Power Requirements**
  - **< 80mW for Black Video Images**
  - **Output Disable Using Video Marker**
  - **Output Voltage Sensor**
- **Laser Enable Function Supports Safety Compliance**

Simplified Functional Diagram



For related parts and recommended products to use with this part, refer to: ***www.maximintegrated.com/MAX3601.related***

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ABSOLUTE MAXIMUM RATINGS

AVDD to AGND ....-0.3V to +2.2V
DVDD to DGND....................................-0.3V to +2.2V
AVCC to AGND ....-0.3V to +4.0V
DVCC to DGND....................................-0.3V to +4.0V
AVDD to DVDD....................................-0.3V to +0.3V
AVCC to DVCC....................................-0.3V to +0.3V
AGND to DGND ....-0.3V to +0.3V
OUT_ to DGND....................................-0.3V to +8.4V
OUT_ Current
  Continuous....................................400mA
  Peak ($t < 1\mu s$)....................................800mA
D0–D11, DCLK, TESTC to DGND...... -0.3V to lower of +2.2V or (V_{DVDD} + 0.3V)
CLK/SCL, DIO/SDA, CS, EN_MAIN, MARKER,
  TESTA, TESTB to DGND ....-0.3V to lower of +4.0V or (V_{DVCC} + 0.3V)
D0–D11, DCLK, SCL, SDA,
  CS, EN_MAIN, MARKER Current .... -50mA to +50mA
Continuous Power Dissipation
  TQFN (T_A = +85°C, derate 35.7mW/°C above +85°C)..2320mW
  WLP (T_A = +70°C, derate 28.5mW/°C above +70°C)..2200mW
Junction Temperature ....+150°C
Operating Temperature Range
  TQFN .... -40°C to +105°C
  WLP .... 0°C to +70°C
Storage Temperature Range........................... -55°C to +150°C
Lead Temperature (soldering, 10s; TQFN only)............+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
  Junction-to-Case Thermal Resistance (θ_{JC})..................2°C/W
  Junction-to-Ambient Thermal Resistance (θ_{JA})..........28°C/W
WLP
  Junction-to-Ambient Thermal Resistance (θ_{JA})..........36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, $V_{OUT} \geq$ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
Output Voltage	V_{OUT}	Output enabled	0.5	0.6	7.5	V
POWER SUPPLY (Note 3, Figure 4)						
+1.8V Supply Current	I_{AVDD_DIS}	EN_MAIN low or SP_EN = 1		0.01	(1)	µA
	I_{AVDD}	SP_EN High		5	7	mA
	I_{DVDD1}	SP_EN = 0		0.02	(0.03)	mA/MHz
		SP_EN = 1, f_{PO} = 75MHz		0.1	(0.2)	
	I_{DVDD_G1A}	Video dependency DAC A		1.1	(1.5)	µA/ (MHz x ΔCODE
	I_{DVDD_G1B}	Video dependency DAC B		0.5	(0.6)	
	I_{DVDD}	Maximum digital supply current f_{PIXEL} = 150MHz, f_{PO} = 75MHz			(45)	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+3.3V Supply Current	I_{AVCC}	Core analog		1.5	1.8	mA
	I_{DVCC_DIS}	ENA_ = ENB_ = 0		0.01	0.1	
	I_{DVCC_G1A}	GA_ = 0x00 (per channel)		3.4	4.8	
	I_{DVCC_G2A}	GA_ = 0xFF (per channel)		8.2	9.1	
	I_{DVCC_G1B}	GB_ = 0x00 (per channel)		1.2	1.6	
	I_{DVCC_G2B}	GB_ = 0xFF (per channel), MAX3601C		2.5	2.8	
		GB_ = 0xFF (per channel), MAX3601G		2.5	3.3	
	I_{AVCC}	Maximum analog supply current GA_= GB_ = 0xFF, ENA_ = ENB_ = 1, MAX3601C			(37.6)	
		Maximum analog supply current GA_= GB_ = 0xFF, ENA_ = ENB_ = 1, MAX3601G			(39.1)	
Pulse-Off Assist Current (Note 4)	I_{CCD_G1}	PHS_= 0		5	(10)	µA/MHz
	I_{CCD_G2}	f_{PO} = f_{POH} = 75MHz, f_{PIXEL}= 150MHz, C_L = 0pF, V_{OUT_MIN} = 0.8V to 1.8V		2.3	(4.6)	
Power In MAX3601 Driver (Note 5)		Outputs off, clock stopped		0.2		mW
		0% video		< 83	(100)	
		27% video		130		
		100% video		270		
		27% video with pulse-off		150		
		27% video with pulse-off assist		160		
Typical Output Sensitivity to Supply Voltage (Note 6)		I_{OUT}/V_{AVDD}		1		%/V
		I_{OUT}/V_{DVDD}		1	(3)	
		I_{OUT}/V_{AVCC}		2	(17)	
		I_{OUT}/V_{DVCC}		2.2	(6)	
VIDEO DAC (8-Bit, Note 7)						
Maximum Conversion Rate			150	160	(250)	Msps
Settling Time	t_S	Within 12 LSBs (GAIN = 0x0F to 0xFF)		6.7	(12)	ns
		Within 3 LSBs (GAIN = 0xFF)		12	(25)	
		Within 1 LSB (GAIN = 0xFF)		23	(34)	
Rise/Fall Time		20% to 80%		1.5	(2.5)	ns
Offset Error (GSA_ = GSB+ = 0xFF, ENA_ = ENB_ = 1)	OS_ER	0V ≤ V_{OUT} ≤ V_{AVCC} + 0.5V		1.0	24	µA
		V_{OUT} = 7.5V	(1.0)	10.5	37	
Resistor ROUT1	R_{OUT1}	V_{OUT} = 7.5V, see Figure 12	(290)	400	(490)	kΩ
Video INL (Notes 8 and 9)		Code > 0x1F	(-15)		(15)	LSB
INL Drift (Notes 8 and 9)		0x1F < GAIN < 0xFF, 0°C < T_J < +125°C V_{OUT_MIN} = 0.6V to 1.6V		1.5	(3)	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, $V_{OUT} \geq$ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Video DNL (GAIN = 0x0F to 0xFF) (Note 8)		Guaranteed monotonic		(-1)		(+1)	LSB
Propagation Delay (Delay = PD1 + PD2)		PD1			2		Pixel clocks
		PD2			11		ns
Propagation Delay Variation				(-1)		(+1)	ns
Transfer of V_{OUT} to I_{OUT} (Note 5)		f < 50kHz, V_{OUT} > 0.9V			0.2	(1)	%/V
		f < 1MHz, V_{OUT} > 0.6V			6	(10)	
		f < 1MHz, V_{OUT} > 0.5V			12	(15)	
Output Capacitance (CODE_A = CODE_B = 0x00)	C_{DVR}	V_{OUT} = 0.6V			260		pF
		V_{OUT} = 1.1V			125		
		V_{OUT} = 2.0V			100		
PULSE OFF ASSIST							
Rise Time		20% to 80%, $V_{A\_}$ = 1.0V, C_L = 0pF, PHS_ = 3, VIDEO = 0x00			1.6	(3)	ns
Incremental Resistance PH_= 0xFFFF		PHS_= 3,			8		Ω
		PHS_= 2			16		
		PHS_= 1			32		
		PHS_= 0			64		
Compliance Voltage	V_{O_POH}	Relative to V_{AVCC}, I_{OUT} = 1mA (T_A = 0 to +125°C)				(-0.8)	V
		T_A = -40°C to +125°C				(-0.9)	
OUTPUT GAIN (VIDEO_ = 0xFF)							
Resolution					8		Bits
Current at OUT		GA_= 0x00, GB_= 0x00			0.01	(1)	mA
		GA_= 0xFF, GB_= 0x00	MAX3601C	280	320	400	
			MAX3601G, T_A = +25°C to +105°C	275	320	400	
			MAX3601G, T_A < +25°C	260	320	400	
		GA_= 0x00, GB_= 0xFF	MAX3601C	69	80	100	
			MAX3601G, T_A = +25°C to +105°C	68	80	100	
			MAX3601G, T_A < +25°C	60	80	100	
		GA_= 0xFF, GB_= 0xFF	MAX3601C	(349)	400	(500)	
			MAX3601G	(320)	400	(500)	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPLIANCE ALARM						
VSET DAC Resolution		4 bit	(70)	80	(90)	mV
VSET DAC Range		VSET_ = 0x0	0.32	0.4	0.48	V
		VSET_ = 0xF	1.4	1.6	1.8	
Filter 1 Time Constant				1		ns
Filter 2 Time Constant				2.7		ns
TEMPERATURE ALARM						
Temperature Range			(5)		(150)	°C
Temperature Accuracy		T_J = +20°C to +125°C	(-10)		(10)	°C
Temperature Resolution		T_J = +20°C to +125°C	(2.25)	2.5	(2.75)	°C/LSB
LOGIC I/O (DIO/SDA, CLK/SCL, CS, MARKER, EN_MAIN)						
Input Low Voltage	V_{IL2}	Test condition			0.4	V
Input High Voltage	V_{IH2}	Test condition	1.45			V
Input High Threshold		Relative to V_{DVDD}	(50)	60	(70)	%
Input Low Threshold		Relative to V_{DVDD}	(40	50	(60)	%
Input Hysteresis		Relative to V_{DVDD}	(5)			%
Input Current		DIO/SDA, CLK/SCL	-10	±0.2	+10	µA
Input Resistance	R_{EN_MAIN}	EN_MAIN to DGND	50	100	200	kΩ
	R_{MARKER}	MARKER to DVDD	50	100	200	
	R_{CS}	CS to DGND	50	100	200	
Input Capacitance				1		pF
Disable Time	t_{DIS}	EN_MAIN or MARKER to I_{OUT} falling		0.1	1	µs
Enable Settling Time Constant	t_{EN}	EN_MAIN rising or MARKER rising		0.5	1.5	µs
DIO/SDA Low Voltage		$I_{DIO/SDA}$ = 16mA		0.1	0.4	V
VIDEO DATA INPUTS						
Maximum Frequency	f_{DCLK_MAX}		150	> 160		MHz
DCLK Duty Cycle		f_{DCLK} > 100MHz	(45)		(55)	%
DCLK High Time		Relative to $2/f_{DCLK}$	(-0.5)		(+0.5)	ns
Video Input Setup Time	t_{SU}	Operating condition	1			ns
Video Input Hold Time	t_H	Operating condition, MAX3601C	0.25			ns
		Operating condition, MAX3601G	0.35			
Input Switching Time		10% to 90%, operating condition		1.2		ns
Input Low Voltage	V_{IN-L}				0.5 x V_{DVDD} - 0.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IN-H}		0.5 x V_{DVDD} + 0.1			V
Input Threshold		Relative to V_{DVDD}		50		%
Input Hysteresis				0.1		V
Input Current			-10	<±1	+10	µA
Data Input Capacitance	C_D			1		pF
SUBPIXEL GENERATOR						
Pixel Clock Frequency Range		Subpixel generator active	24	150	(250)	MHz
Minimum Pulse Width		1 subpixel			(2)	ns
Subpixel Timing Accuracy		T_{PODM} - T_{POD}	(-1)		(+1)	ns
PLL Bandwidth			(1200)	2000	(3100)	kHz
I²C TIMING						
Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between START and STOP	t_{BUF}		1.3			µs
HOLD Time for a START Condition	t_{HD_STA}		0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
SCL High Time	t_{HIGH}		0.6			µs
SDA Hold Time	t_{HD_DAT}		0.1		0.6	µs
SDA Setup Time	t_{SU_DAT}		0.1			µs
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Pulse Width of Suppressed Spikes	t_{SP}			0.05		µs
SPI TIMING						
SPI Clock Cycle	t_{CLK}		83			ns
SCL High Pulse Width	t_{WH}		41.5			ns
SCL Low Pulse Width	t_{WL}		41.5			ns
SCL Rise/Fall Time	t_{RF}	At f_{CLK} = 12MHz		16		ns
SCL Setup Time	t_{CLKS}		8			ns
CS Setup/Hold Time	$t_{CS,}$		32			ns
CS Recovery Time	t_{CR}		50			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, $V_{OUT} \geq$ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write Data Setup Time	t_{DS}		16			ns
Write Data Hold Time	t_{DH}		16			ns
Read Data Delay Time	t_{RD}				34	ns
DIO Output Switching Time	t_{ZR}	R_{DIO} = 390Ω, C_{DIO} = 20pF		11	(16)	ns
DIO Output Disable Time	t_{RZ}	MAX3601C			34	ns
		MAX3601G			36	
DIO Conflict Avoid Time	t_{ZZ}		0			ns
POWER-ON RESET (Figure 27)						
V_{AVDD},V_{DVDD} On Threshold	$2V_{POR+}$			1.32	(1.6)	V
V_{AVDD},V_{DVDD} Off Threshold	$2V_{POR-}$		(1)	1.28		V
V_{DVCC},V_{DVCC} On Threshold	$3V_{POR+}$			2.5	(2.8)	V
V_{AVCC},V_{DVCC} Off Threshold	$3V_{POR-}$		(2.2)	2.4		V

Note 2: Parameters measured using circuit of Figure 1. R_S, C_S, C_L = open, unless otherwise noted. Parameters in parentheses ( ) are provided for guidance, but are not tested or guaranteed.

Note 3: Power Consumption Calculations:

$$I_{DVDD}(mA) = I_{DVDD}(mA/MHz) \times f_{PIXEL}(MHz) + \sum_{N=1}^{3}\left[ENA_N \times I_{DVDD_{G1A}}(mA/MHz) \times \Delta CODE_{A_N} + ENB_N \times I_{DVDD_{G1B}}(mA/MHz) \times \Delta CODE_{B_N}\right] + f_{PIXEL}(MHz)$$

$$I_{DVCC}(mA) = \sum_{N=1}^{3}\left[ENA_N \times I_{DVCCD_{G1A}} + \left(I_{DVCC_{G2A}} - I_{DVCC_{G1A}}\right) \times \frac{GA_N}{255} + ENB_N \times I_{DVCC_{G1B}} + \left(I_{DVCC_{G2B}} - I_{DVCC_{G1B}}\right) \times \frac{GB_N}{255}\right]$$

where:

N = OUTPUT 1,2,3, f_{PIXEL} is the pixel clock frequency (MHz), ENA_ and ENB_ are the DAC enable signals with value 0 or 1, ΔCODE is the average number of video code changes per pixel (0 to 255). If the Pulse-Off feature is used 1 time per pixel, ΔCODE = 2x Average Video Code Value. If Pulse-Off is used 2 times per pixel, ΔCODE = 4x Average Video Code Value (Figure 3).

Note 4: Pulse-Off Assist Current Calculation:

$$I_{DVCCD} \approx \sum_{N=1}^{3}\left[\left(I_{DVCC_{G1}} + C_{OUTN} \times \Delta V_{OUTN}\right) \times f_{PON}\right]$$

where:

N = Output 1,2,3, C_{OUTN} is the total capacitance at OUTN (MAX3601 output capacitance + external capacitance), ΔV_{OUTN} is the resulting voltage change at OUTN, f_{PON} is the frequency of pulse-events in MHz. f_{PON} is generally equal to the pixel clock, but could be lower or higher, depending on the pulse-off duty cycle and number of pulse-off events per pixel.

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, $V_{OUT} \geq$ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

Note 5: Power Estimation Conditions:
For each output, DAC A is enabled, DAC B is off, VIDEO = 27% data as shown in Figure 2, f_{PIXEL} = 150MHz. Vertical Image Duty cycle is 70%, and the MARKER signal is used to reduce power during vertical flyback.
The load emulates:
Red Laser on OUT1: 4I + 2.3V
Green Laser on OUT2: 8I + 3.8V
Blue Laser on OUT3: 16I + 3.5V

	PARAMETER	VIDEO	GAIN1 (mA)	GAIN2 (mA)	GAIN3 (mA)	V_{OUT} @I_{PEAK}	VA1 (V)	VA2 (V)	VA3 (V)	PO_EN	POC	POM_	PHM_
1	0% Video	00h	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
2	27% Video	27%	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
3	100% Video	FFh	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
4	Pulse-Off	27%	300	270	105	0.8V	4.3	6.8	6.0	1	4h	FF00h	0
5	With Pulse-off Assist	27%	300	270	105	0.8V	4.3	6.8	6.0	1	4h	FF00h	FF00h

Note 6: Transfer from supply to I_{OUT} measured with 100mV_{P-P} sine wave applied at the supply.

$$T = \frac{f'I_{OUT}}{I_{OUT}} \times \frac{100\%}{f'V}$$

with units %/V. I_{OUT} = 325mA, $T_J \leq$ +110°C, f_{OUT} = 60Hz to 1MHz. Typical values are at 10kHz, maximum value at 1MHz typical corner.

Note 7: AC Parameters characterized with a video pattern of 0x00 to 0xFF, GAIN = 0xFF, 0x3F, 0x1F, 0x0F. All combinations of output VIDEO DACs: DAC A only, DAC B only, DAC A and DAC B. An external filter network (R_S, C_S) or digital filter may be used to reduce ringing.

Note 8: $$1\text{lsb} = \frac{I_{OUT(CODE=0xFF)} - I_{OUT(CODE=0x00)}}{255}$$

Note 9: Integral nonlinearity (INL) is measured as: [I_{OUT} - Least Squares approximation of current].

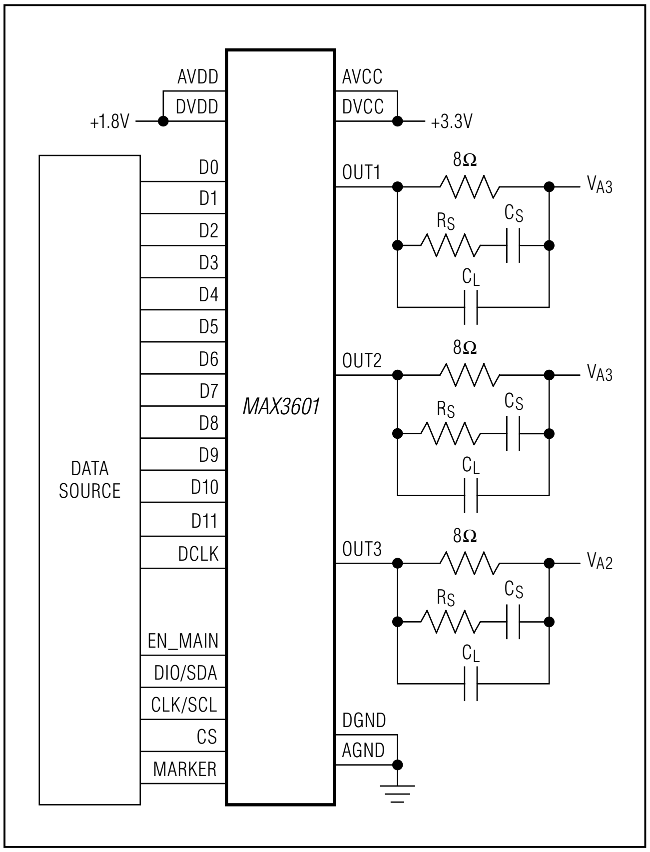


Figure 1. Test Circuit

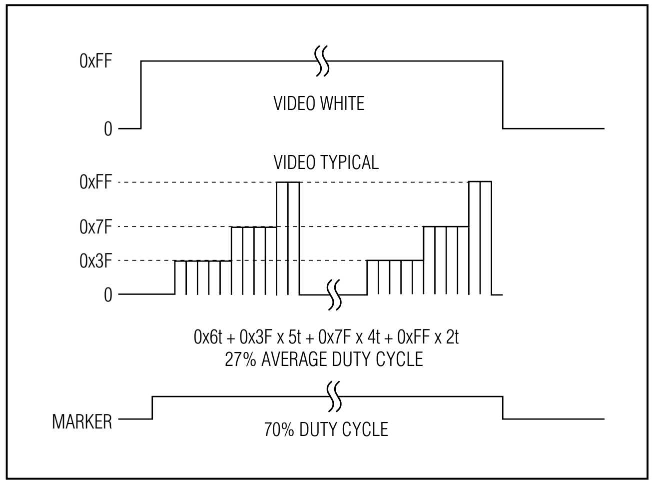


Figure 2. Video Test Pattern

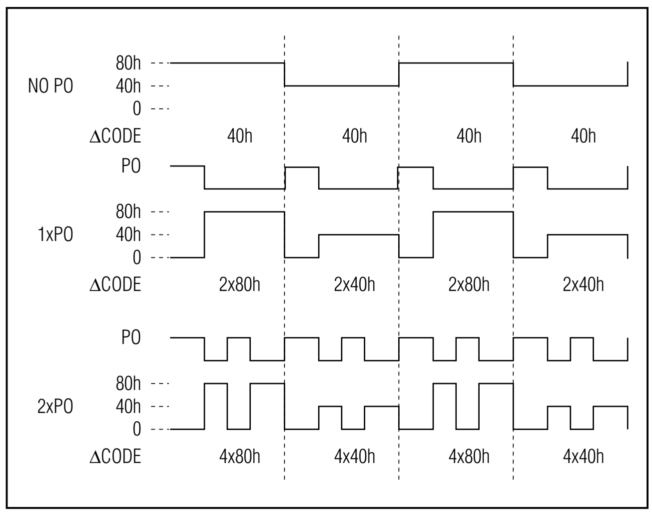


Figure 3. ΔCode Example

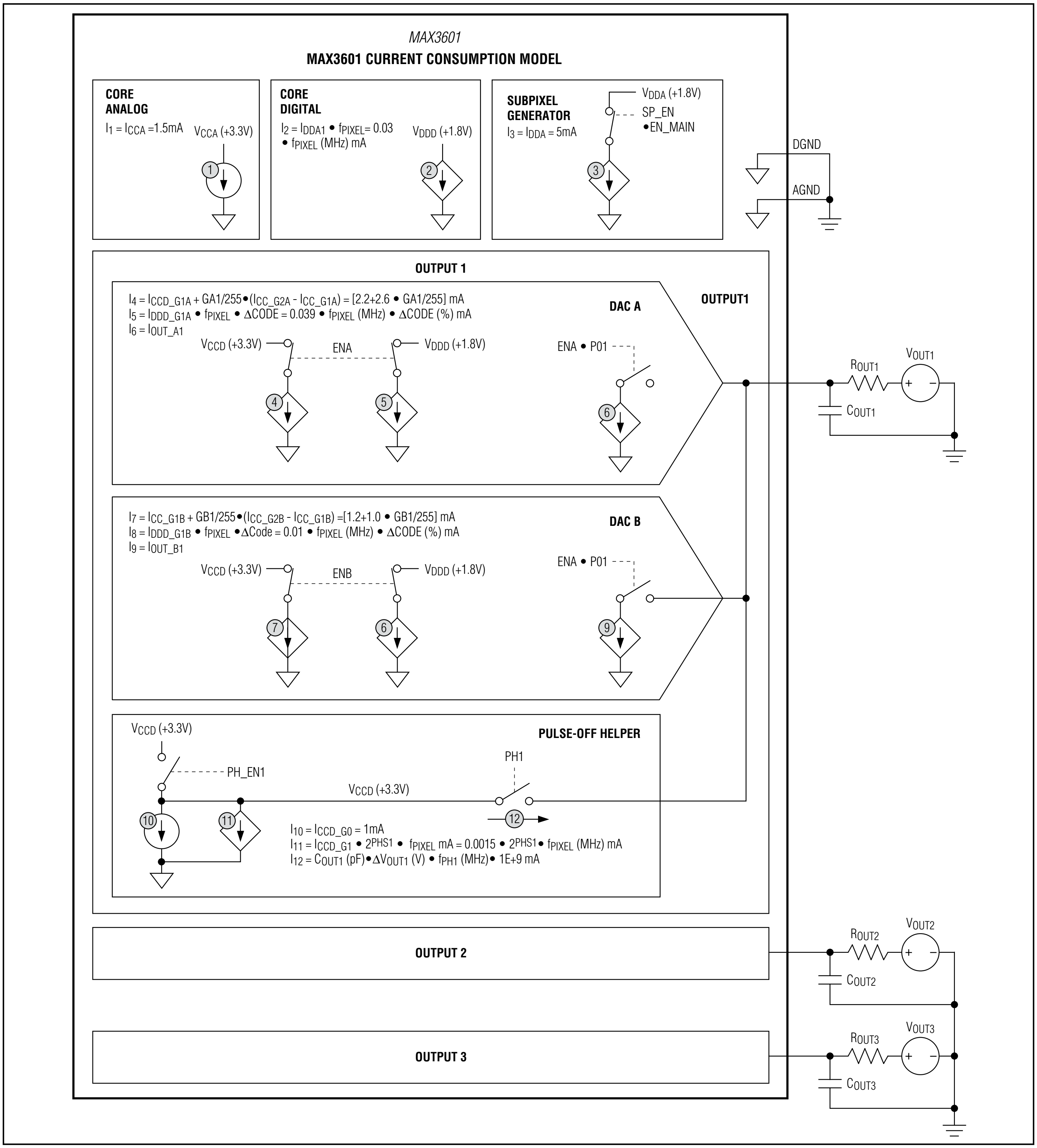
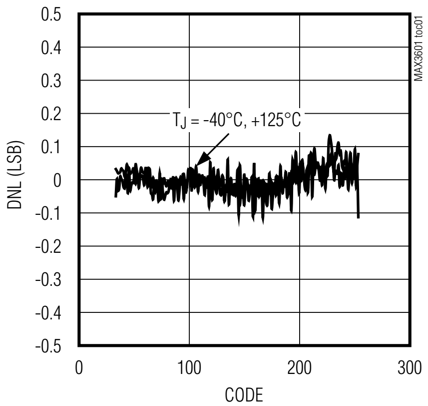


Figure 4. Power-Supply Calculations

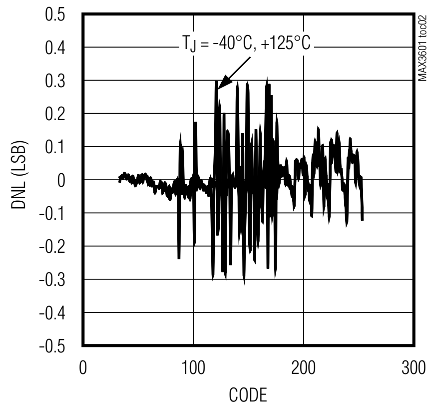
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

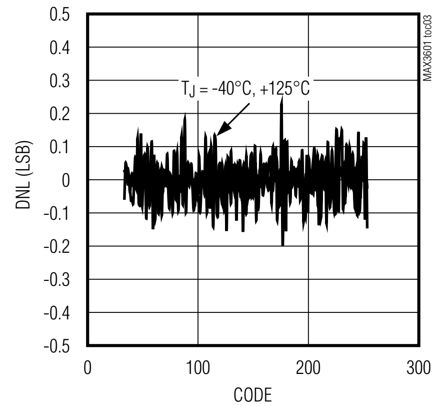
VIDEO DNL DAC A (GAIN = 0x20)



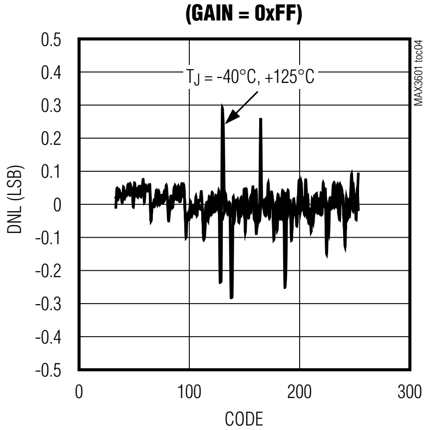
VIDEO DNL DAC A (GAIN = 0xFF)



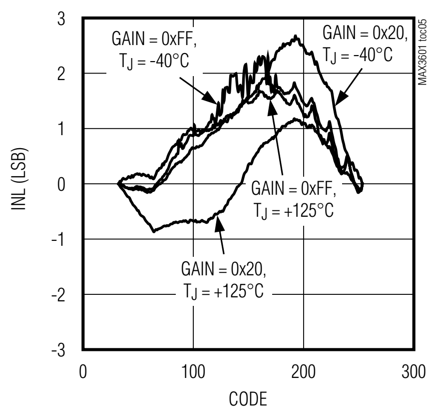
VIDEO DNL DAC B (GAIN = 0x20)



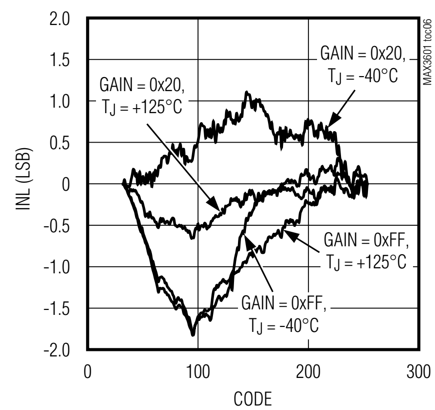
VIDEO DNL DAC B (GAIN = 0xFF)



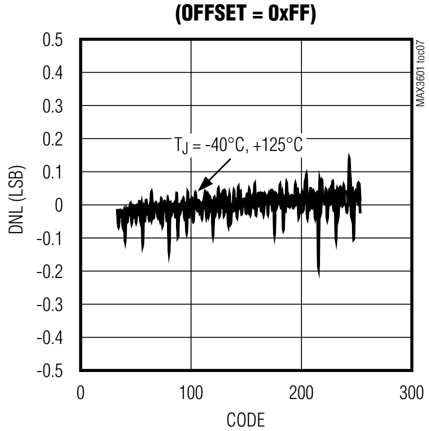
VIDEO INL DAC A



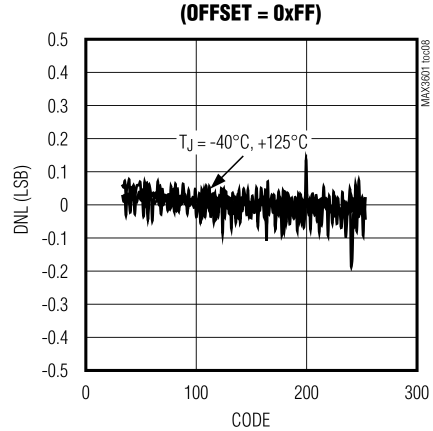
VIDEO INL DAC B



GAIN DNL DAC A (OFFSET = 0xFF)



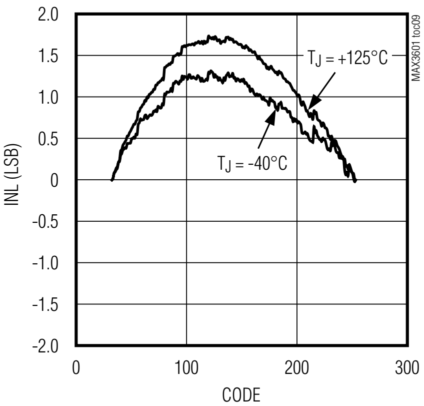
GAIN DNL DAC B (OFFSET = 0xFF)



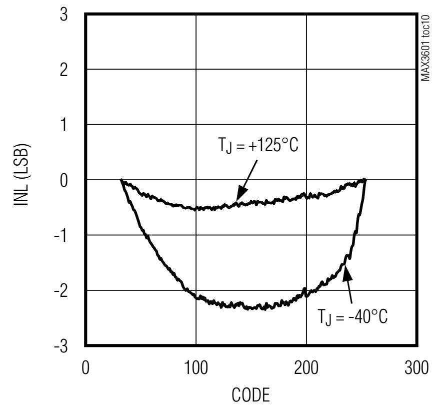
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

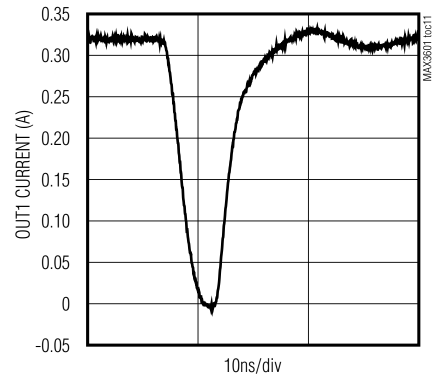
GAIN INL DAC A (OFFSET = 0xFF)



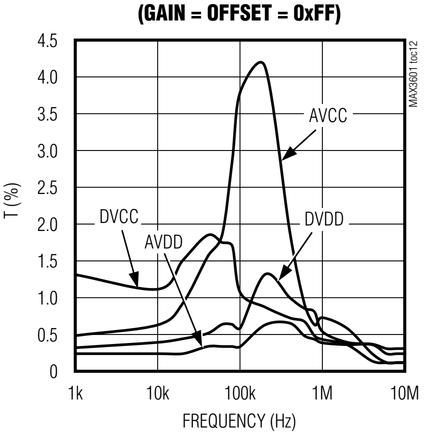
GAIN INL DAC B (OFFSET = 0xFF)



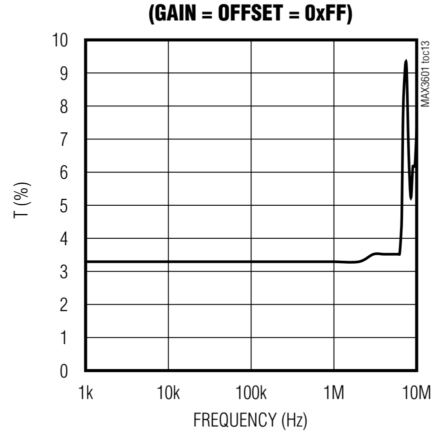
OUT1 PULSE OFF



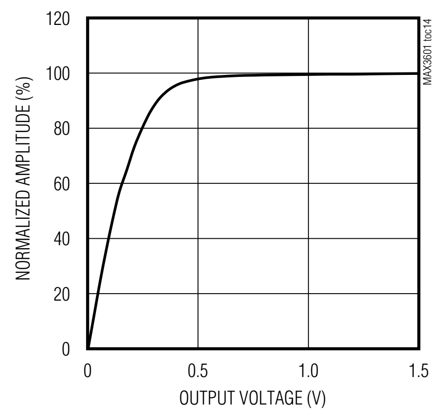
POWER-SUPPLY TRANSFER TO I_{OUT} (GAIN = OFFSET = 0xFF)



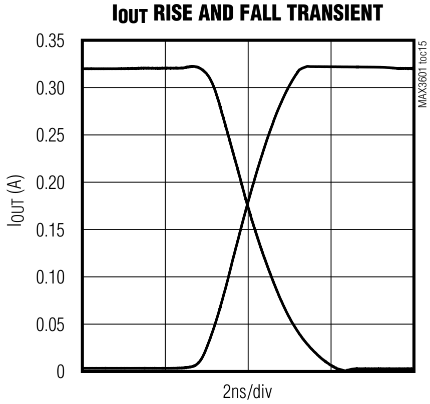
V_A TRANSFER TO I_{OUT} (GAIN = OFFSET = 0xFF)



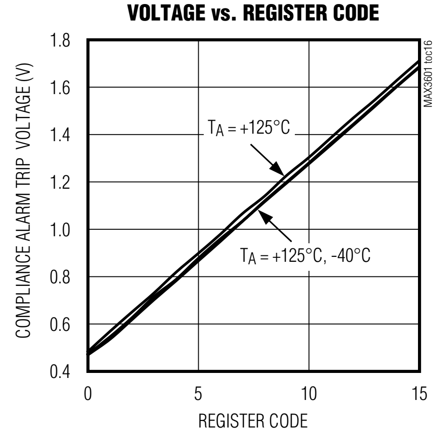
NORMALIZED OUTPUT CURRENT vs. OUTPUT VOLTAGE



I_{OUT} RISE AND FALL TRANSIENT

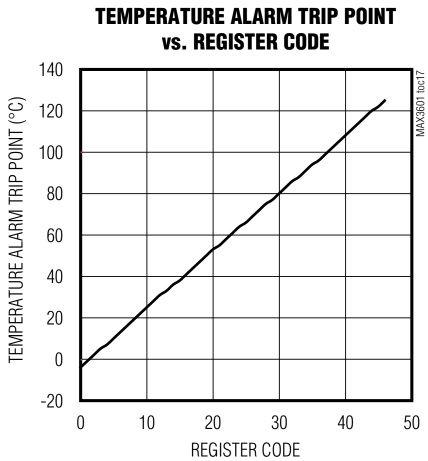


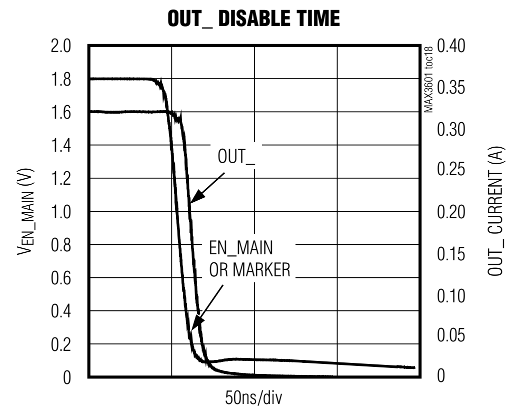
OUT_ COMPLIANCE ALARM TRIP VOLTAGE vs. REGISTER CODE

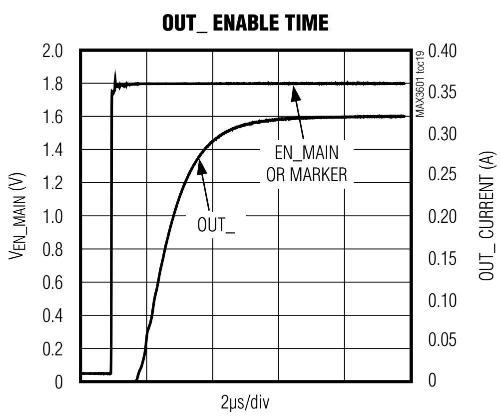


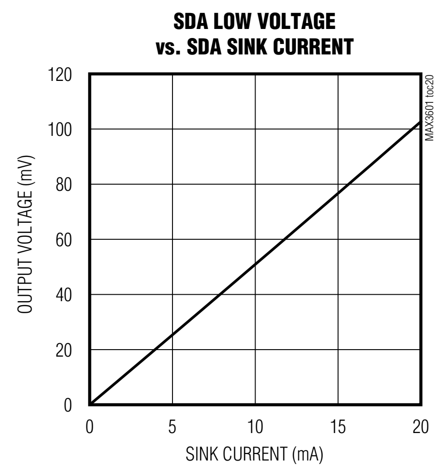
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

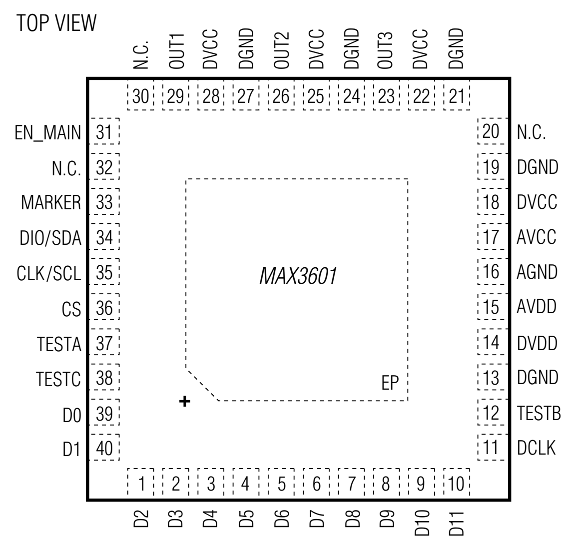




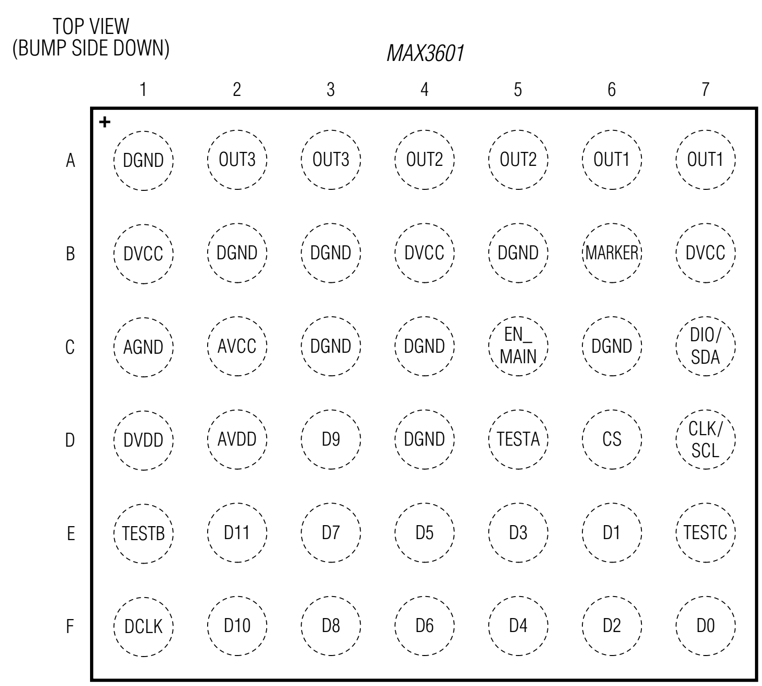




Pin/Bump Configurations

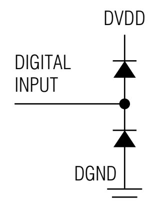


THIN QFN
(5mm x 5mm)

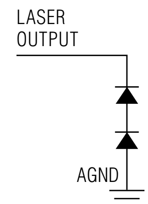
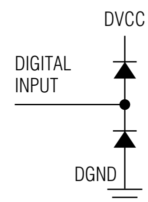
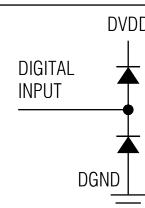


WLP
(3.5mm x 3.0mm)

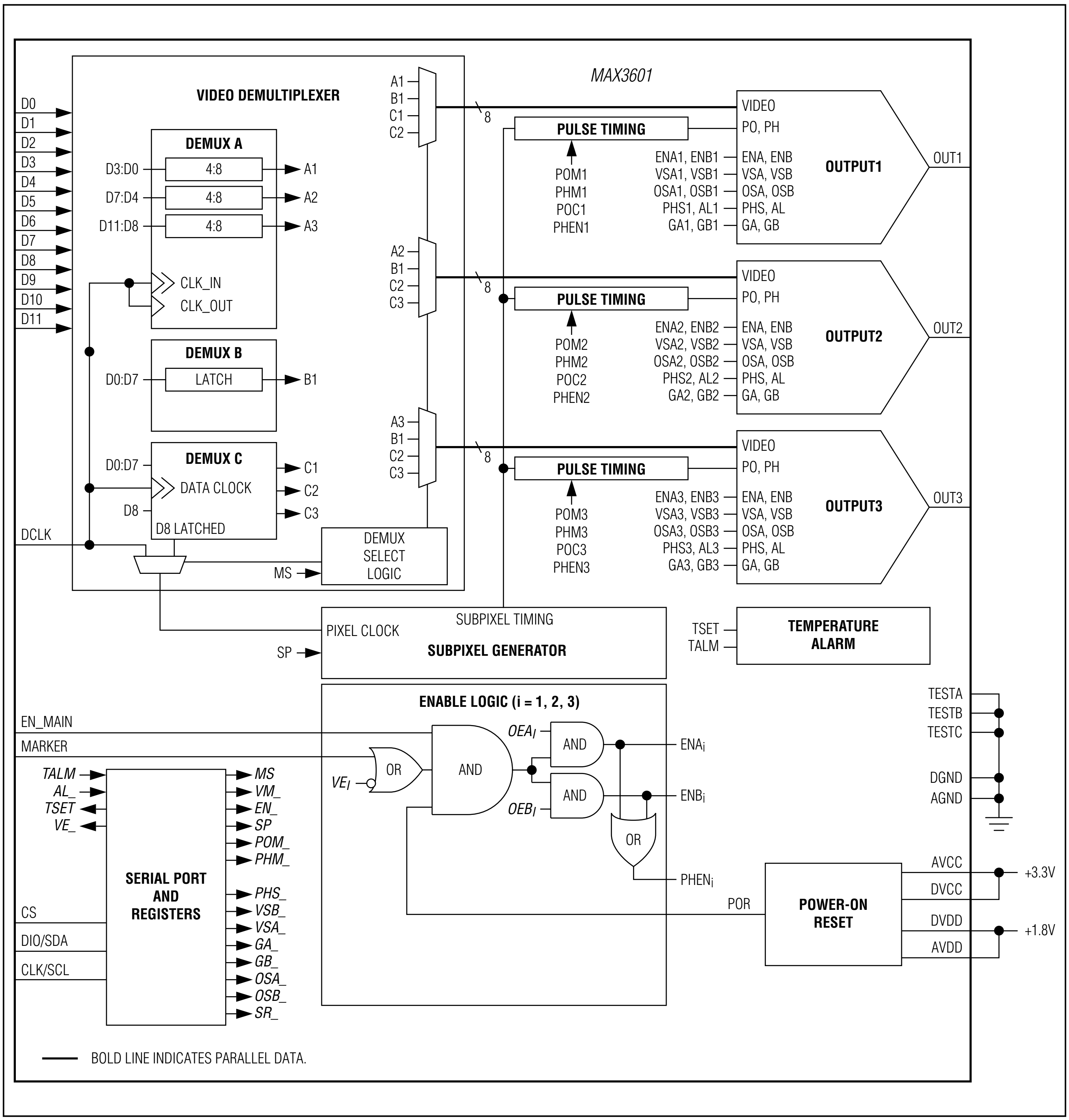
Pin/Bump Description

PIN		NAME	FUNCTION	EQUIVALENT INPUT SCHEMATIC
TQFN-EP	WLP			
1	F6	D2	Synchronous Video Data Inputs	
2	E5	D3		
3	F5	D4		
4	E4	D5		
5	F4	D6		
6	E3	D7		
7	F3	D8	Synchronous Video Data Input. In DEMUX C mode, D8 functions as the pixel clock.	
8	D3	D9	Synchronous Video Data Inputs	
9	F2	D10		
10	E2	D11	Synchronous Video Data Input, MSB	
11	F1	DCLK	Video Clock Input	
12, 37, 38	D5, E1, E7	TESTA, TESTB, TESTC	Test Pins. Connect to DGND.	—
13, 19, 21, 24, 27	A1, B2, B3, B5, C3, C4, C6, D4	DGND	Digital Ground. Connect to 0V.	—
14	D1	DVDD	1.8V Digital Power Supply. Bypass DVDD to DGND with 0.1μF and 0.01μF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.	—
15	D2	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1μF and 0.01μF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.	—
16	C1	AGND	Analog Ground. Connect to 0V.	—
17	C2	AVCC	3.3V Analog Power Supply. Bypass AVCC to AGND with 0.1μF and 0.01μF capacitors as close as possible to the device with the smaller capacitor closest to AVCC.	—
18, 22, 25, 28	B1, B4, B7	DVCC	3.3V Digital Power Supply. Bypass DVCC to DGND with 0.1μF and 0.01μF capacitors (1 pair per pin) as close as possible to the device with the smaller value capacitor closest to DVCC.	—
20, 30, 32	—	N.C.	No Connection. There is no connection from the package to the IC.	—

Pin/Bump Description (continued)

PIN		NAME	FUNCTION	EQUIVALENT INPUT SCHEMATIC
TQFN-EP	WLP			
23	A2, A3	OUT3	Connection for Laser 3. Leave OUT3 unconnected if unused.	
26	A4, A5	OUT2	Connection for Laser 2. Leave OUT2 unconnected if unused.	
29	A6, A7	OUT1	Connection for Laser 1. Leave OUT1 unconnected if unused.	
31	C5	EN_MAIN	Laser Enable Input with 100kΩ Pulldown to DGND. Set EN_MAIN = high to enable OUT1–OUT3.	
33	B6	MARKER	Video Marker Input with 100kΩ Pullup to DVDD	
34	C7	DIO/SDA	SPI and I2C Serial Data Input/Output	
35	D7	CLK/SCL	SPI and I2C Serial Clock Input	
36	D6	CS	SPI Chip Select with 100kΩ Pulldown to DGND. Connect CS to DVDD for I2C mode. Set CS = low on power-up for SPI mode.	
39	F7	D0	Synchronous Video Data Input, LSB	
40	E6	D1	Synchronous Video Data Input	
—	—	EP	Exposed Pad (TQFN Only). EP is internally connected to DGND. The EP **must** be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.	—

Functional Diagram



Detailed Description

The laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes two 8-bit video/offset DACs with programmable gain and offset.

Video Demultiplexer

The Video Demultiplexer supports three video formats and pixel clock configurations. The video format and demultiplexer are selected by the MUX select register (MS) as shown in Table 7.

Demux A

Demux A converts 4-bit input with DDR clock to 8-bit data with pixel clock. Input data must be formatted as shown in Figure 5. Four MSBs are latched on the rising edge of DCLK, and four LSBs are latched on the falling edge of DCLK.

Demux B

Demux B latches an 8-bit video input on the rising edge of clock. The same video is sent to all outputs.

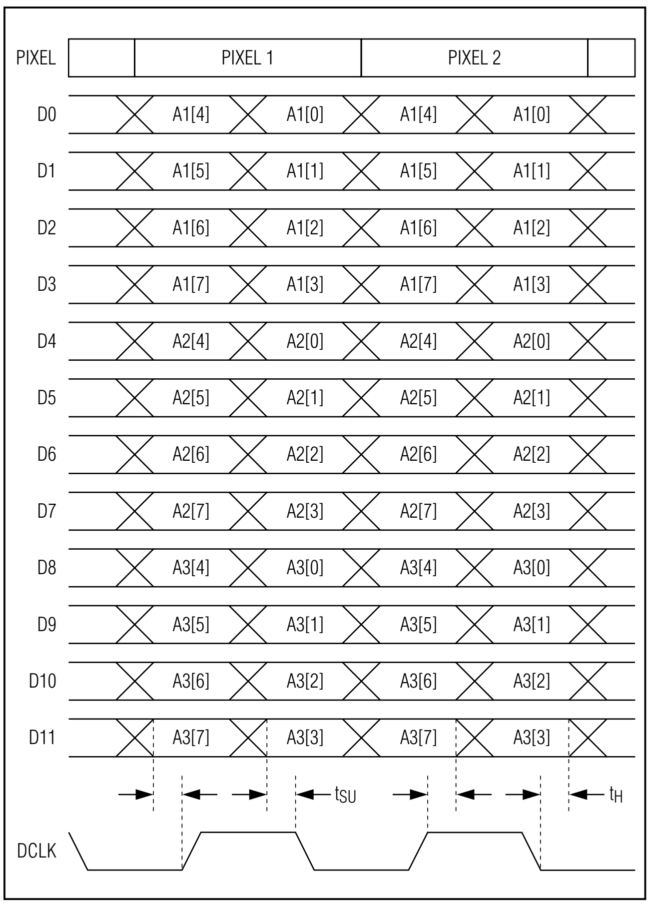


Figure 5. Video Demultiplexer A Input Waveform

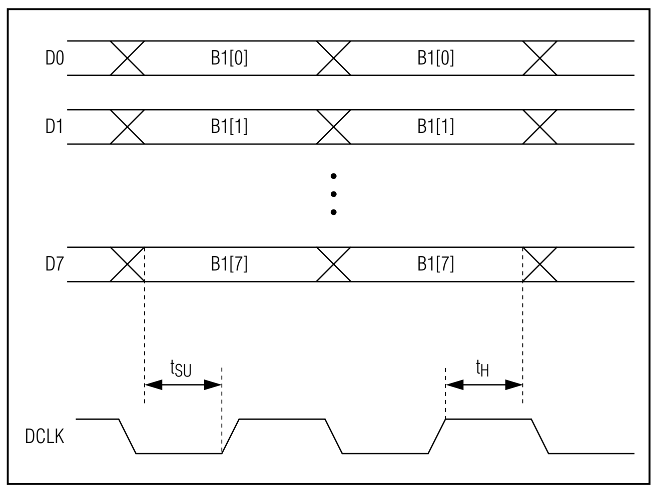


Figure 6. Video Demultiplexer B Input Waveform

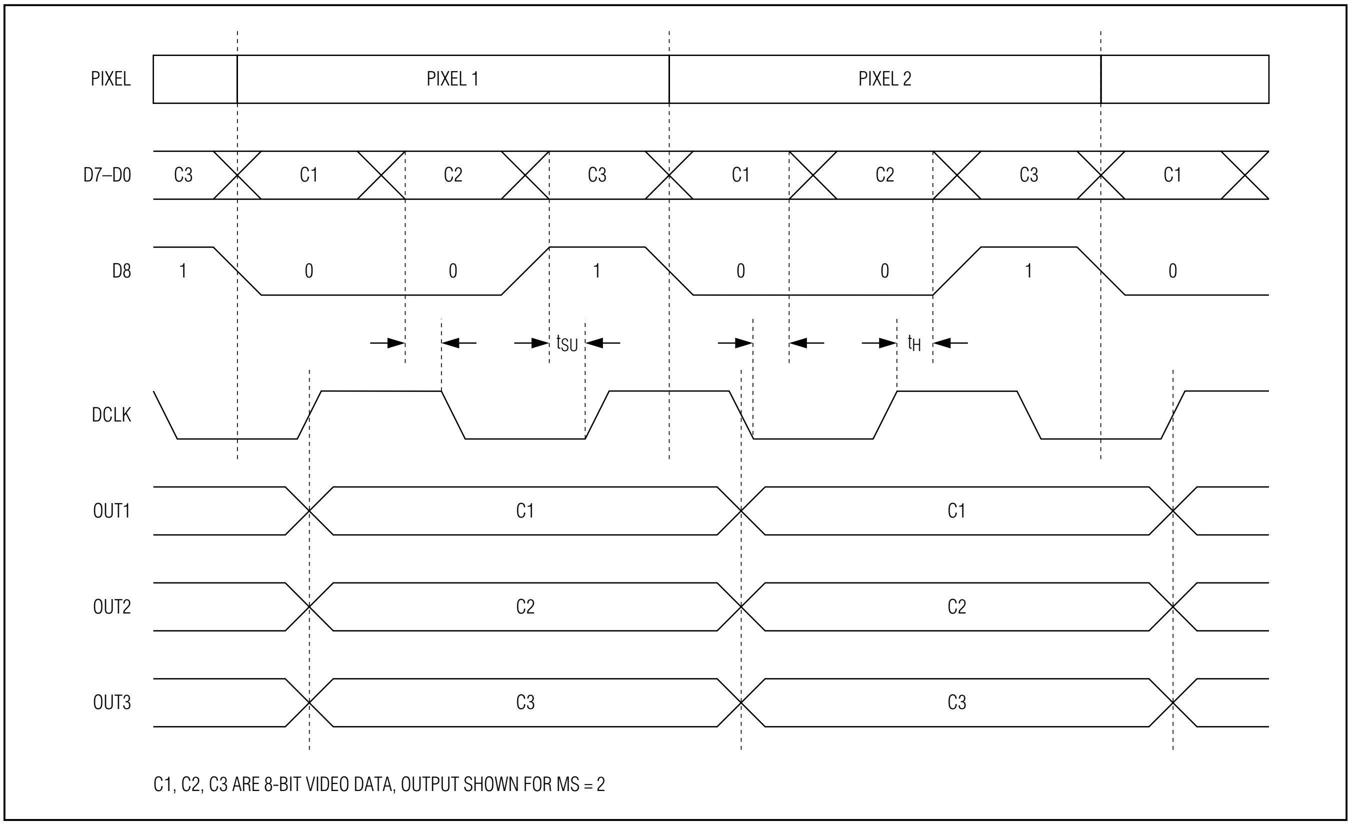


Figure 7. Video C Demultiplexer Input Waveform

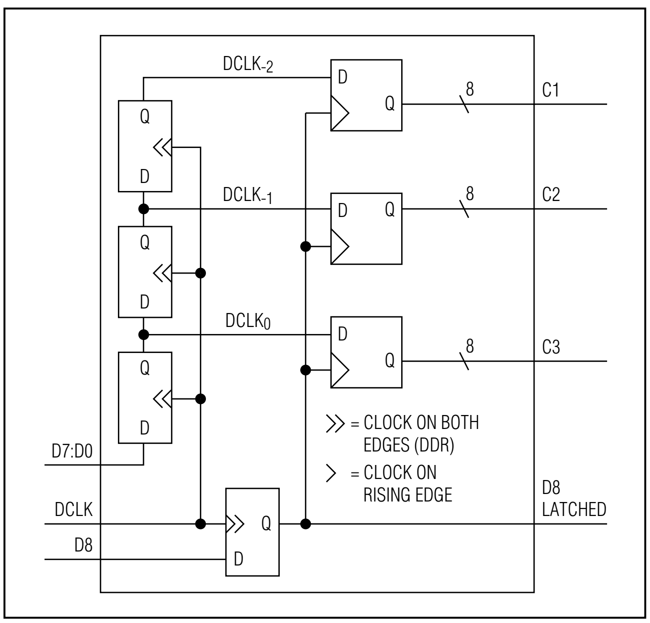


Figure 8. Video C Demultiplexer

Demux C

Demux C is compatible with the data format of the MAX3600. Data for the three outputs is multiplexed in time and uses a DDR clock.

Pulse Timing Generator

The Pulse Timing generator creates phases of the pixel clock called subpixels (Figure 9). The subpixel timing signals enable laser current output pulsing for use with despeckling the laser light. Each output of the laser driver can have different pulse widths or multiple pulses. If unused, disable the subpixel generator (D0 of register 0x0B) for additional power savings.

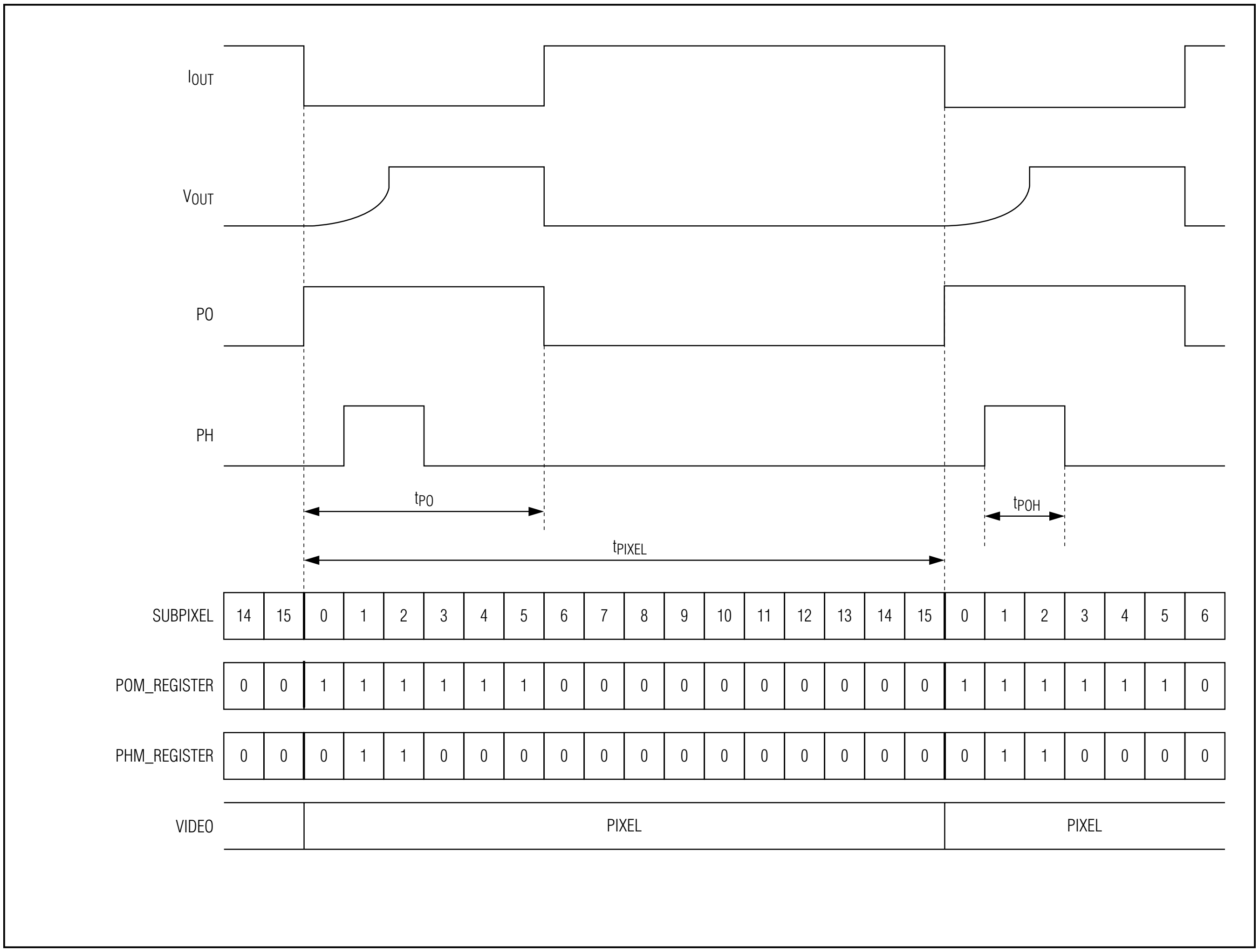


Figure 9. Pulse Timing Generator

Subpixel Programming

The subpixel programming bits (D[2:0] of register 0x0C) determine the number of subpixels and duration of the pulse time (Table 1). The pulse width is applied to every pixel when the programmed pulse-off length > 0. This can be dynamically implemented to adjust for various lighting conditions.

Pulse-Off

The pulse-timing generator can be configured to skip pulse events to save power. The Pulse-Off Configuration (POC) register selects options shown in Table 2. Random pulse-off events are triggered from a 31-bit pseudo-random bit-stream. By default, the PRBS is common to all outputs. Bit D4 of the POC_ registers determine which PRBS bits control each output (Table 3).

Pulse-off synchronization between outputs occurs when POC_ registers match and POC_[4] = 0. For example, if POC1 = POC2 = POC3 and POC_[4] = 0, the occurrence of randomized pulse-off events at all outputs will be synchronized.

Table 1. Subpixel Programming (SP Register)

SP	f_{PIXEL} (MHz)		ACTIVE SUBPIXELS	INACTIVE SUBPIXELS
	MIN	MAX		
000	150	200	0:7	8:15
001*	**75**	**150**	**0:15**	**—**
010	50	100	0:11	12;15
011	37.5	75	0:15	—
100	30	60	0:9	10:15
101	25	50	0:15	—
110	21.4	42.8	0:13	14:15
111	18.75	37.5	0:15	—

**Power-on default*

Table 2. Pulse-Off Duty Cycle (POC_ Register)

POC_[3:0]	PULSE-OFF DUTY CYCLE
0000*	**Every pixel, 100%**
0001	Random, 87.5%
0010	Random, 75.0%
0011	Random, 62.5%
0100	Random, 50.0%
0101	Random, 37.5%
0110	Random, 25.0%
0111	Random, 12.0%
1XXX	Every other pixel, 50%

**Power-on default*

Table 3. Random Pulse-Off Programming

POC_[4]	PRBS31 BITS USED		
	OUTPUT 1	OUTPUT 2	OUTPUT 3
0*	**PRBS31[4], [3], [0]**	**PRBS31[8], [7], [0]**	**PRBS31[16], [15], [0]**
1	PRBS31[2:0]	PRBS31[2:0]	PRBS31[2:0]

**Power-on default*