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19-5171; Rev 0; 2/10

Microsemi

MAX3624A Evaluation Kit

Evaluates: MAX3624A

General Description

The MAX3624A evaluation kit (EV kit) is an assembled demonstration board that provides convenient evaluation of the MAX3624A low-jitter, precision clock generator. The EV kit includes an on-board 25MHz crystal to allow immediate testing.

The EV kit includes switches to allow easy selection of different modes of operation. The reference input and clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

Features

- **AC-Coupled I/Os for Ease of Testing**
- **Fully Assembled and Tested**
- **+3.3V Power-Supply Operation**
- **On-Board 25MHz Crystal**

Ordering Information

PART	TYPE
MAX3624AEVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C3, C4, C5, C7–C10, C19, C25–C30, C54	16	0.1µF ±10% ceramic capacitors (0402)
C2	1	10µF ±10% ceramic capacitor (0603)
C6, C57–C60	5	0.01µF ±10% ceramic capacitors (0402)
C22	1	27pF ±10% ceramic capacitor (0402)
C23	1	33pF ±10% ceramic capacitor (0402)
C65	1	4.7pF ±10% ceramic capacitor (0402)
J1, J3, J5	0	Not installed
J2, J48	2	Test points
J4	1	2-pin header, 0.1in centers
J13–J16, J18, J19, J36, J43	8	SMA connectors
L1	1	2.7µH inductor
R1–R5, R7	6	150Ω ±5% resistors (0402)
R6, R8, R9	0	Not installed
R42	1	499Ω ±1% resistor (0402)
R57	1	49.9Ω ±1% resistor (0402)
R59	1	10.5Ω ±1% resistor (0402)
R61	1	36Ω ±5% resistor (0402)
SW1, SW2, SW3, SW11	4	SP3T switches
SW4, SW6–SW9, SW12, SW13, SW15	8	SPDT switches
TP6, TP7	2	Test points
U1	1	Low-jitter, precision clock generator (32 TQFN-EP*) Microsemi MAX3624AETJ+
Y1	1	25MHz crystal NDK EXS00A-AT00429
—	1	Shunt
—	1	PCB: MAX3624A EVALUATION BOARD+, REV A

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Component Supplier

SUPPLIER	PHONE	WEBSITE
NDK America	815-544-7900	www.ndk.com/en

Note: *Indicate that you are using the MAX3624A when contacting this component supplier.*

MAX3624A Evaluation Kit

Quick Start

For evaluation of the MAX3624A, configure the EV kit as follows:

1) Determine which output is going to be evaluated and connect to the test equipment through SMA cables. Be sure not to leave any outputs unterminated (i.e., place 50Ω terminators on all unused outputs).
2) Connect a +3.3V power supply to J48 (VCC) and J2 (GND). Set the current limit to 200mA.
3) If the on-board crystal is used (IN_SEL set HIGH), the PLL divider should be set to divide by 25 (FB_SEL1 and FB_SEL0 set LOW) to achieve the standard output rates shown in Table 3.
4) Use Table 3 to set the output divider switches to achieve the output frequency desired.
5) Enable the output under test by setting the related output-enable switch (Qx_OE) HIGH.

Table 1. Adjustment and Control Descriptions (see *Quick Start* first)

COMPONENT	NAME	FUNCTION
J4	INDUCTOR SHUNT	J4 shunts the power-supply inductor. Normal operation is J4 shunted.
SW1	SELB1	SW1 and SW2 set the output divider for the QB outputs. See Table 3 for more information.
SW2	SELB0	SW1 and SW2 set the output divider for the QB outputs. See Table 3 for more information.
SW3	SELA1	SW3 and SW11 set the output divider for the QA outputs. See Table 3 for more information.
SW4	QAC_OE	Set HIGH to enable the LVCMOS output, QA_C. Set LOW to disable QA_C.
SW6	$\overline{\text{BYPASS}}$	Set LOW to bypass the PLL. Set HIGH to engage the PLL. Note that when the PLL is bypassed the output dividers are automatically set to divide by 1.
SW7	FB_SEL1	SW7 and SW8 set the PLL divider. See Table 2 for more information.
SW8	FB_SEL0	SW7 and SW8 set the PLL divider. See Table 2 for more information.
SW9	QA_OE	Set HIGH to enable LVPECL output QA. Set LOW to force a logic zero at QA.
SW11	SELA0	SW3 and SW11 set the output divider for the QA outputs. See Table 3 for more information.
SW12	QB1_OE	Set HIGH to enable LVPECL output QB1. Set LOW to force a logic zero at QB1.
SW13	IN_SEL	Set HIGH to select the crystal as the frequency source. Set LOW to select the REF_IN as the frequency source.
SW15	QB0_OE	Set HIGH to enable LVPECL output QB0. Set LOW to force a logic zero at QB0.

Table 2. PLL Divider Settings

INPUT		M DIVIDER
FB_SEL1	FB_SEL0	
LOW	LOW	÷25
LOW	HIGH	÷24
HIGH	LOW	÷32
HIGH	HIGH	÷16

Table 3. Output Divider Settings

INPUT		NA/NB DIVIDER	OUTPUT FREQUENCY (MHz)
SELA1/ SELB1	SELA0/ SELB0		M = 25 AND XTAL = 25MHz
LOW	LOW	÷2	312.5
LOW	HIGH	÷3	208.33
HIGH	LOW	÷4	156.25
HIGH	HIGH	÷5	125
HIGH	OPEN	÷6	104.16
OPEN	HIGH	÷8	78.125
LOW	OPEN	÷10	62.5
OPEN	LOW	÷12	52.08
OPEN	OPEN	÷1	625

Note: *625MHz is beyond maximum specified operating frequency.*

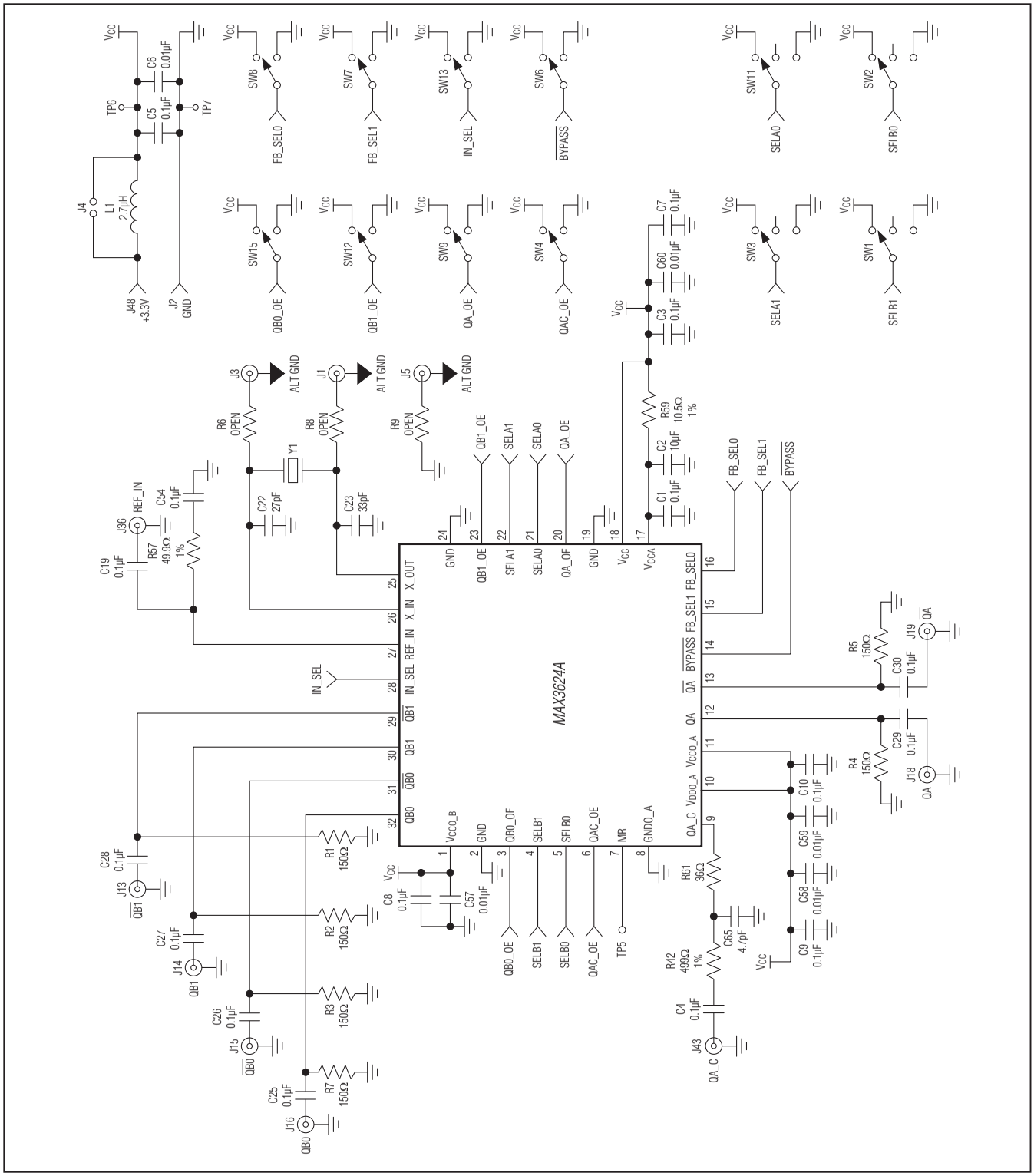

Figure 1. MAX3624A EV Kit Schematic

MAX3624A Evaluation Kit

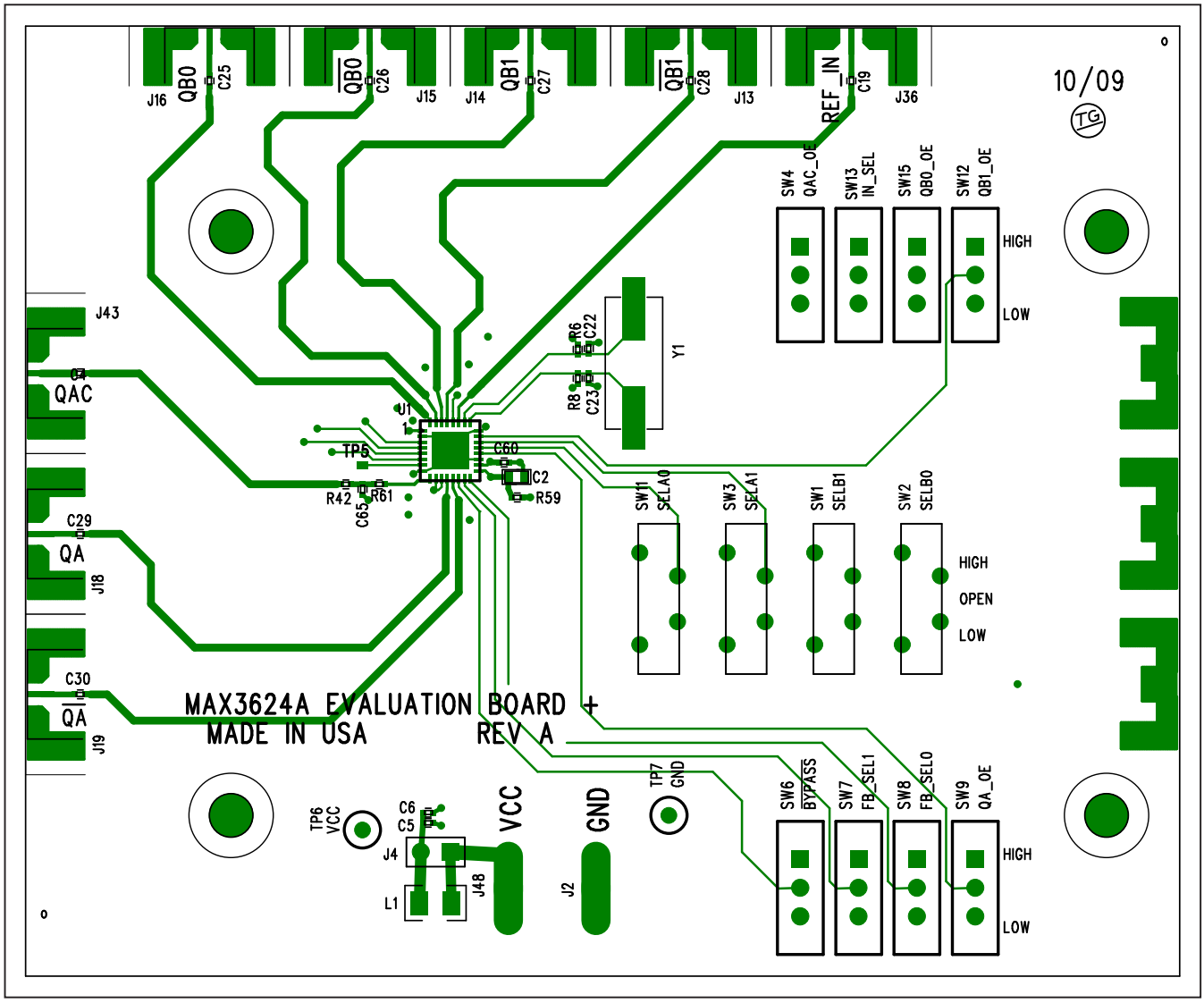

Figure 2. MAX3624A EV Kit Assembly Drawing—Top Side

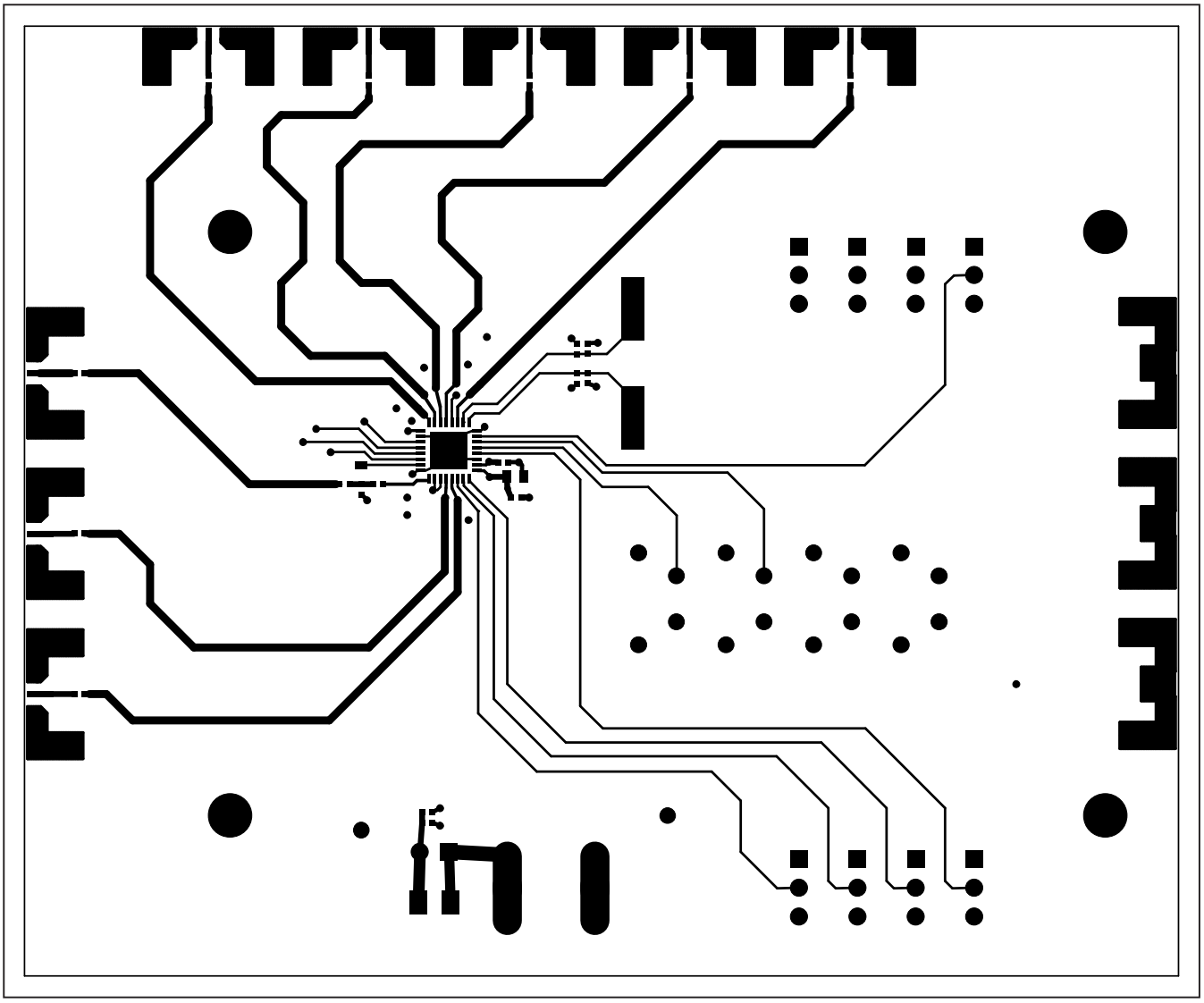

Figure 3. MAX3624A EV Kit Layout—Component Side

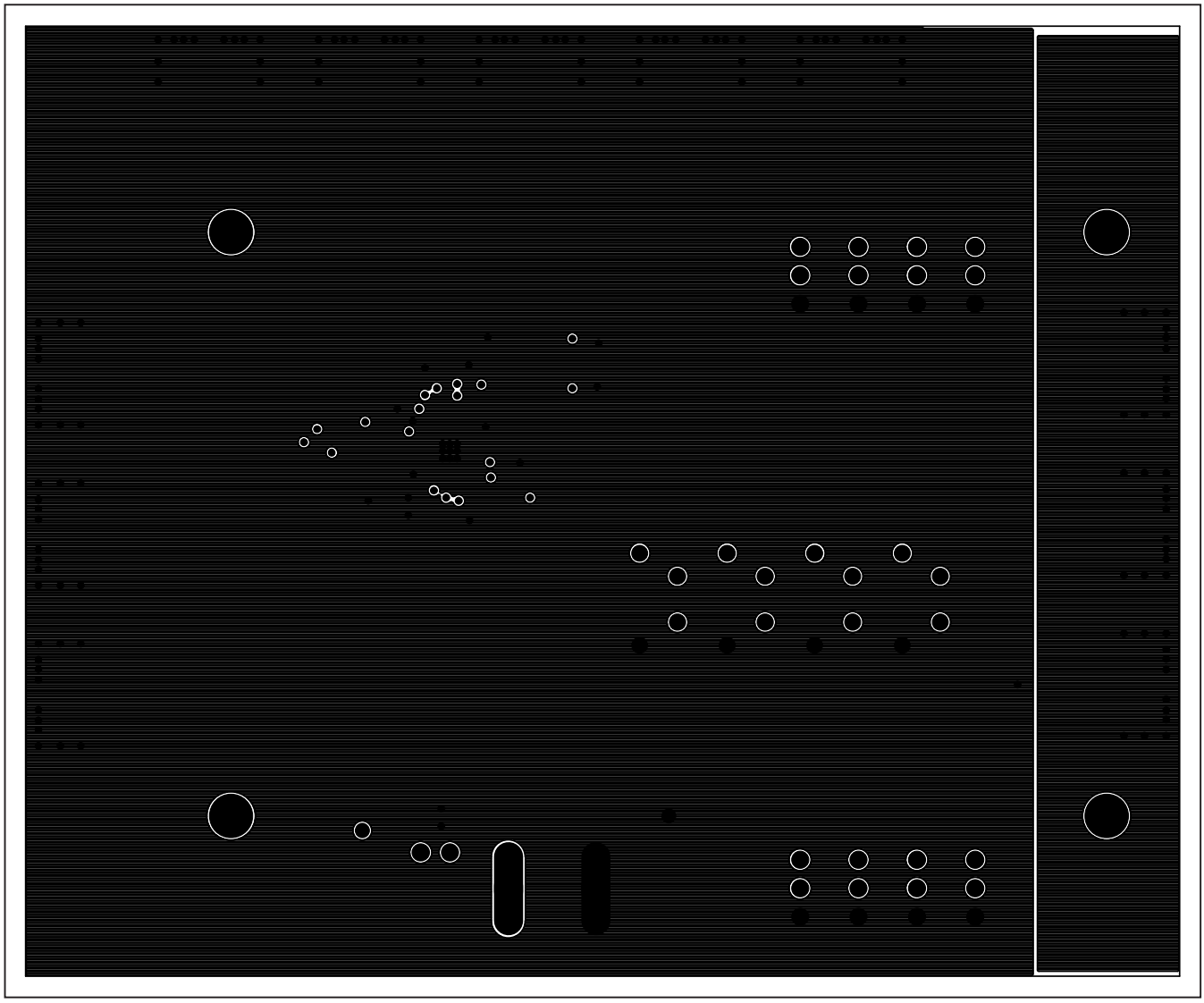

Figure 4. MAX3624A EV Kit Layout—Ground Plane

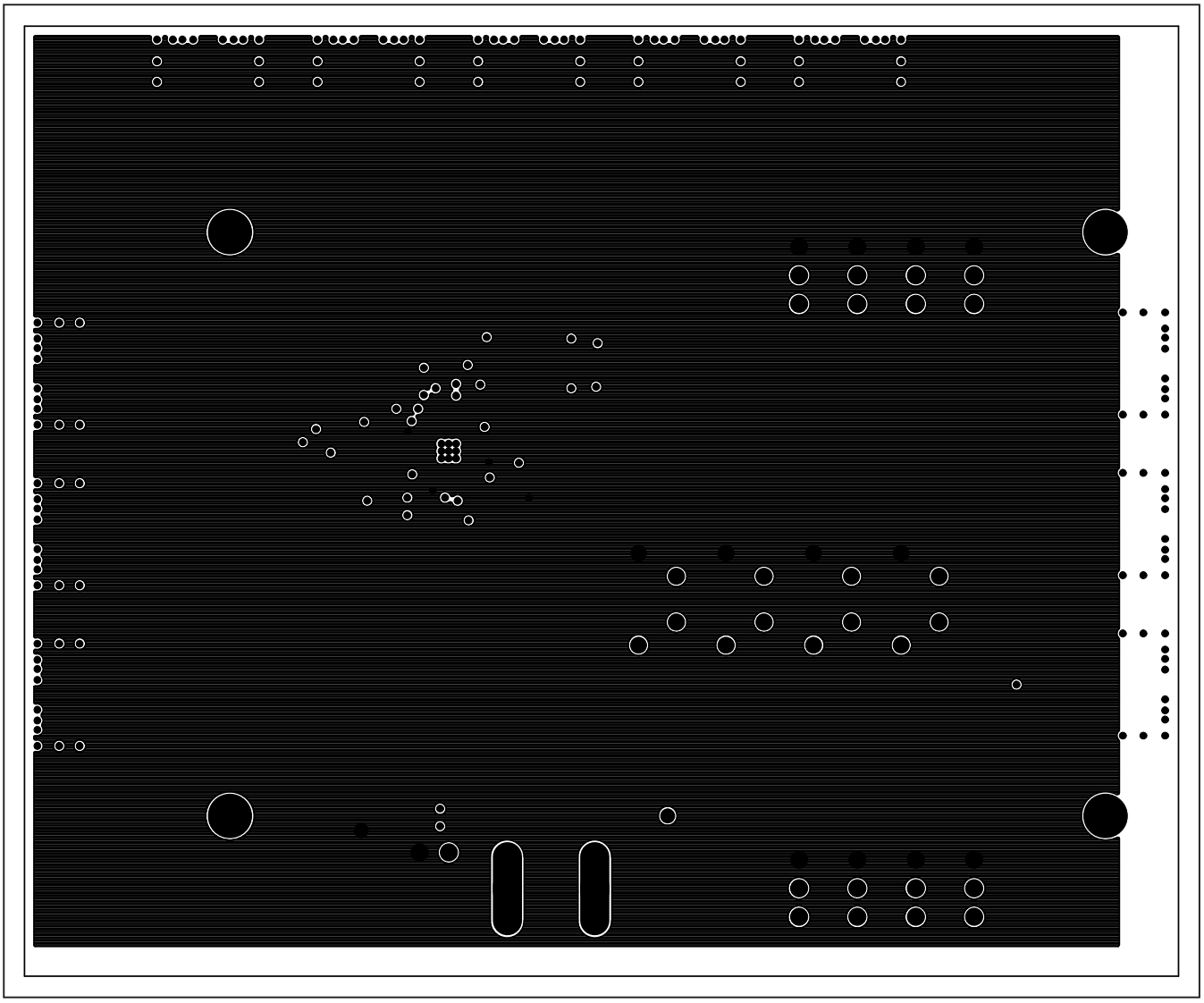

Figure 5. MAX3624A EV Kit Layout—Power Plane

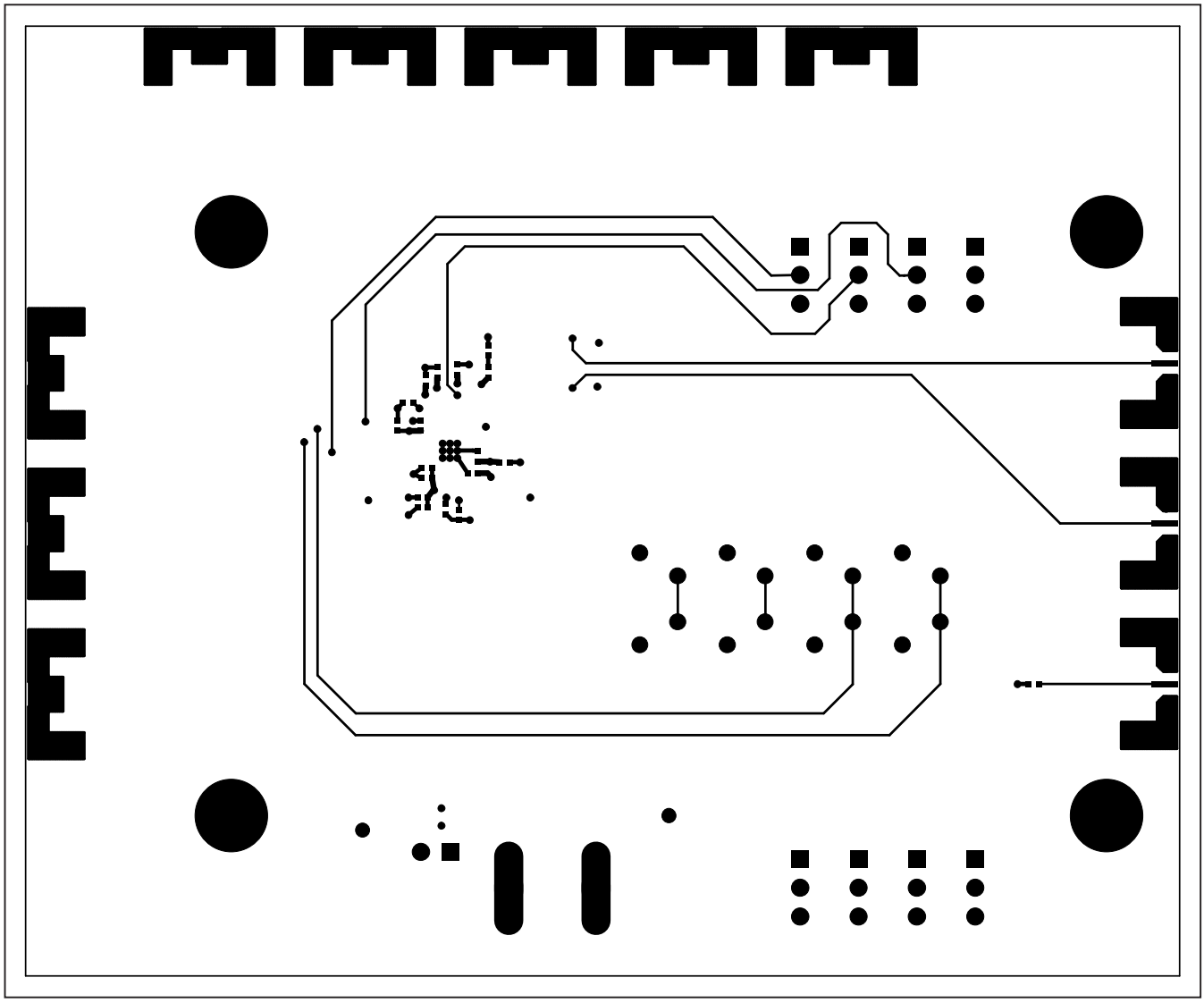

Figure 6. MAX3624A EV Kit Layout—Solder Side

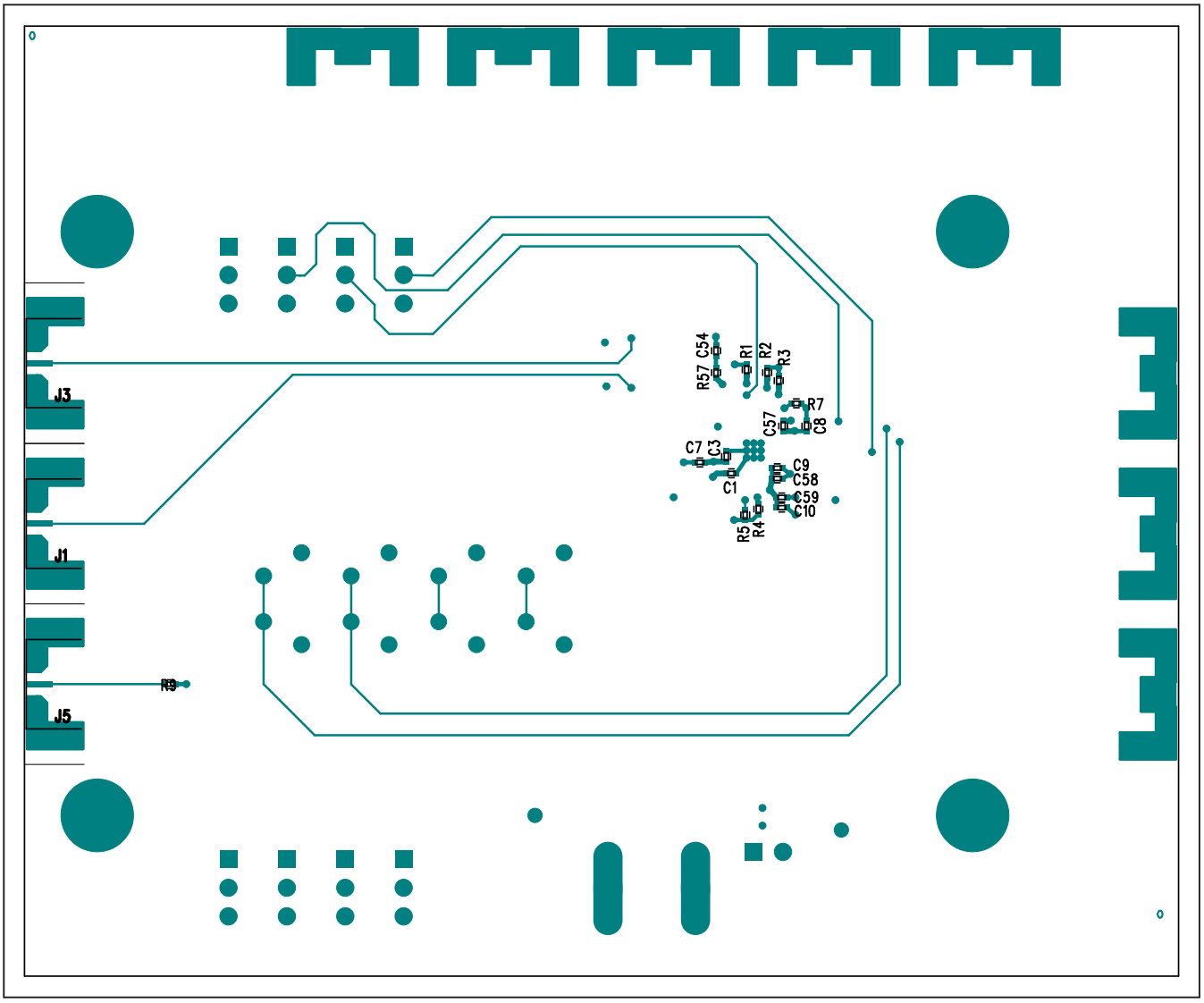

Figure 7. MAX3624A EV Kit Assembly Drawing—Bottom Side

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