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19-3229; Rev 0; 3/04

622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

General Description

The MAX3632 burst-mode limiting amplifier is designed specifically for 622Mbps or 1244Mbps GPON (G.984) optical line terminal (OLT) receiver applications. Together with the MAX3630/MAX3631 burst-mode transimpedance amplifiers (TIAs), a wide-dynamic-range burst-mode signal current (from a PIN or avalanche photodiode) can be translated to a differential LVPECL output. The MAX3632 has an electrical input sensitivity of 4mV$_{P-P}$ that supports GPON class-B optical sensitivity at 622Mbps with a PIN photodiode. An LVPECL-compatible burst reset input ($\overline{RST}$) connected to the limiting amplifier is used to control the offset correction loop of the MAX3632 as required for burst-mode operation, as well as to arm the threshold-setting circuitry of MAX3630/MAX3631 TIAs.

The MAX3632 is available in a low-profile, 4mm x 4mm, 24-lead thin QFN package. It operates from a single +3.3V power supply over a -40°C to +85°C temperature range.

Applications

622Mbps GPON OLT Receivers

1244Mbps GPON OLT Receivers

Features

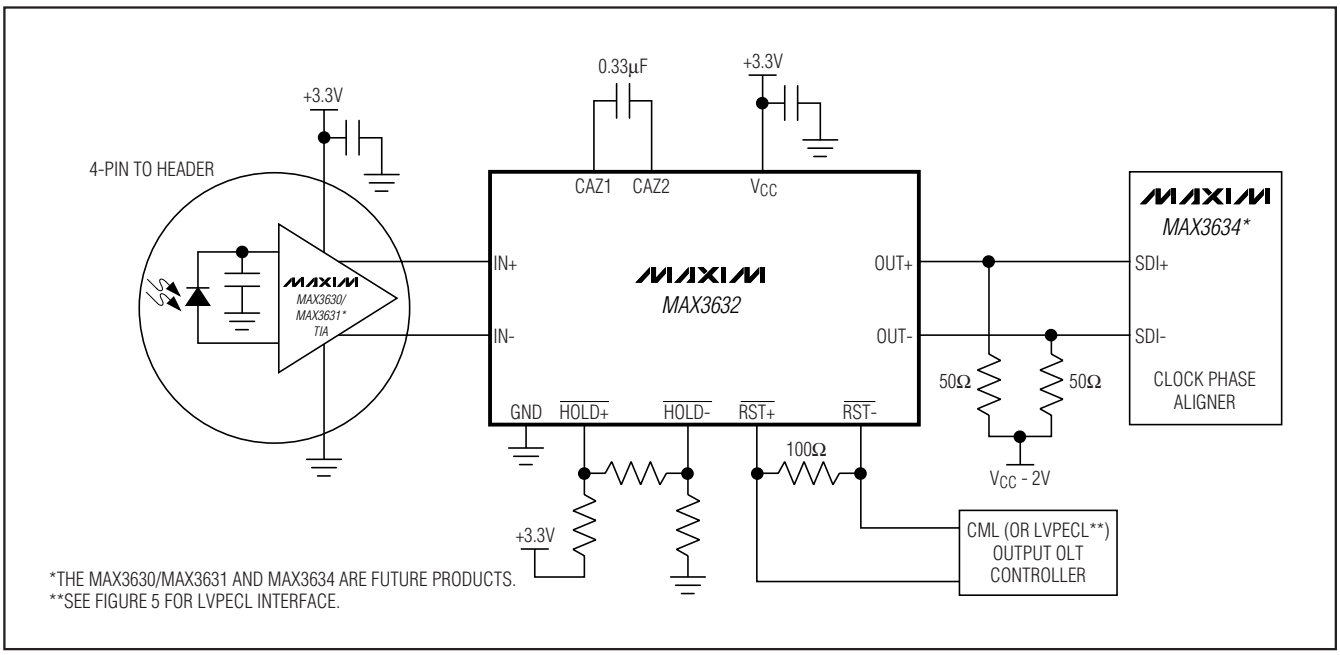
- **DC-Coupled Limiting Amplifier for Burst-Mode GPON Applications**
- **Operates with Maxim's Burst-Mode Transimpedance Amplifier (MAX3630/MAX3631)**
- **LVPECL Data Output**
- **4mV$_{P-P}$ Input Sensitivity**
- **LVPECL Reset Input ($\overline{RST}$)**
- **LVPECL $\overline{HOLD}$ Input for Optional Control Modes**
- **4mm x 4mm TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3632ETG	-40°C to +85°C	24 Thin QFN	T2444-4

Pin Configuration appears at end of data sheet.

Typical Application Circuit



622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) ..... -0.5V to +4.5V
Voltage at IN+, IN-, $\overline{RST}$-, $\overline{RST}$+, $\overline{HOLD}$+, $\overline{HOLD}$-, CAZ1, CAZ2 ..... -0.5V to (V_{CC} + 0.5V)
LVPECL Output Current (OUT+, OUT-) 50mA
Continuous Power Dissipation (T_A = +85°C)
Derate 20.8mW/°C above +85°C 1354mW
Operating Junction Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, V_{IN} = 4mV_{P-P}, and T_A= +25°C, unless otherwise noted. Input (IN+, IN-) terminated with 100Ω resistors to V_{CC}.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS							
Data Rate					622, 1244		Mbps
Power-Supply Current	I_{CC}	(Note 2)			80	100	mA
Low-Frequency Cutoff						30	kHz
CAZ Leakage Current						25	nA
Power-Supply Noise Rejection	PSNR	f ≤ 10MHz (Note 3)			24		dB
INPUT SPECIFICATIONS (IN+, IN-)							
Minimum Input Offset Tolerance		(Note 1)				5	mV
Input Resistance	R_{IN}	Differential		168		232	Ω
Input Sensitivity		BER = 10^{-10}, 2^{23}-1 PRBS			2		mV_{P-P}
OUTPUT SPECIFICATIONS (OUT+, OUT-)							
Random Jitter (Notes 1, 4, 5)	RJ	622Mbps			28	40	ps_{RMS}
		1244Mbps			18	22	
Deterministic Jitter (Notes 1, 4, 6)	DJ	622Mbps			14	30	ps_{P-P}
		1244Mbps			14	30	
LVPECL Output Low Voltage	V_{OL}	Terminated 50Ω to V_{CC} - 2V	T_A = 0°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
			T_A = -40°C to 0°C	V_{CC} - 1.788		V_{CC} - 1.588	
LVPECL Output High Voltage	V_{OH}	Terminated 50Ω to V_{CC} - 2V		V_{CC} - 1.025		V_{CC} - 0.88	V
Data Output Edge Speed		20% to 80% (Notes 1, 4, 5, 7)			150	265	ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, V_{IN} = 4mV_{P-P}, and T_A= +25°C, unless otherwise noted. Input (IN+, IN-) terminated with 100Ω resistors to V_{CC}.)

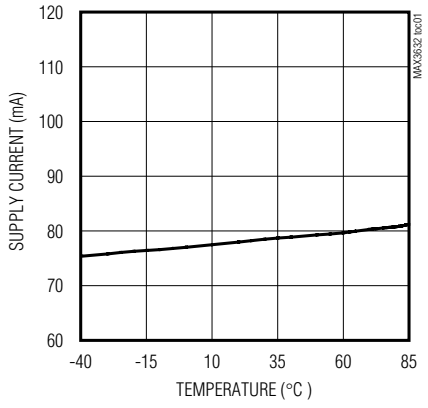
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVPECL INPUT SPECIFICATIONS ($\overline{RST}$+, $\overline{RST}$-, $\overline{HOLD}$+, $\overline{HOLD}$-) (Note 8)						
LVPECL-Differential Input Voltage	V_{IN}		200		1600	mV_{P-P}
LVPECL Input Common-Mode Range	V_{CM}		V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - V_{IN}/4	V
LVPECL Input Current			-150		190	µA

Note 1: AC parameters are guaranteed by design and characterization.
Note 2: Supply current is measured with LVPECL data outputs open.
Note 3: PSNR is measured on the differential output signal while applying a 100mV_{P-P} sinusoidal signal at the power supply with the input open, and the DC cancellation loop activated.
Note 4: Input-data transition time controlled by 4th order bessel filter with f_{-3dB} = 0.75 x data rate. The deterministic jitter caused by this filter is not included in the DJ specifications.
Note 5: Measured with a repeating 0000011111 data pattern at 1244Mbps.
Note 6: Deterministic jitter is measured at the differential-output eye crossing. Peak-to-peak input deterministic jitter is subtracted from peak-to-peak output deterministic jitter.
Note 7: Each output (OUT+, OUT-) terminated with R_{LOAD} = 50Ω and C_{LOAD} = 4pF.
Note 8: The $\overline{HOLD}$ input transition time, 20% to 80%, must be less than 0.3ns for timing method 3. See Figure 10.

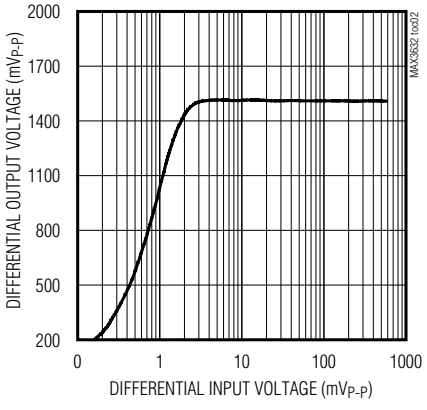
Typical Operating Characteristics

(Input signal is unfiltered, V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.)

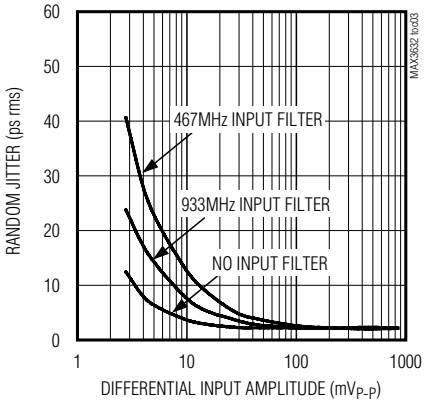
SUPPLY CURRENT vs. TEMPERATURE



TRANSFER FUNCTION (OUTPUT VOLTAGE vs. INPUT VOLTAGE)



RANDOM JITTER vs. INPUT AMPLITUDE

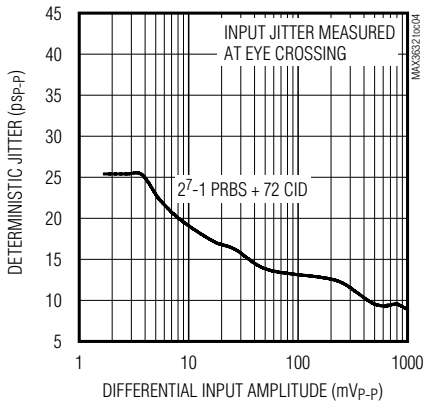


622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

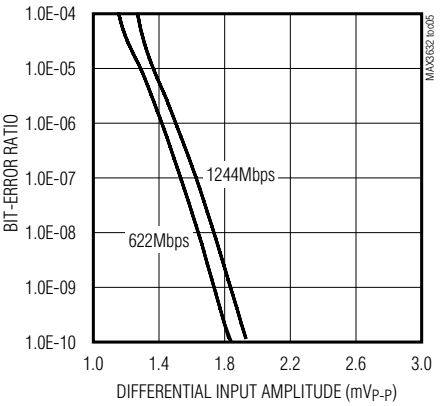
Typical Operating Characteristics (continued)

(Input signal is unfiltered, V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.)

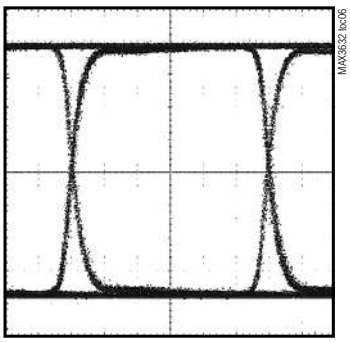
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



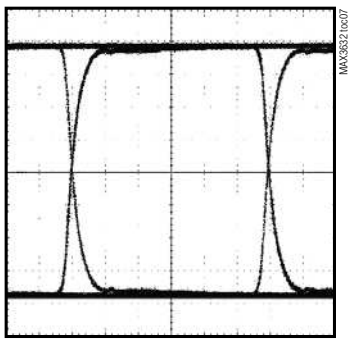
BIT-ERROR RATIO vs. INPUT AMPLITUDE



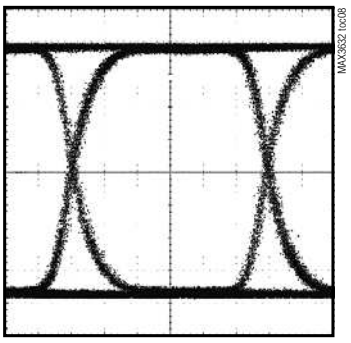
ELECTRICAL EYE DIAGRAM (4mVP-P INPUT, 622Mbps)



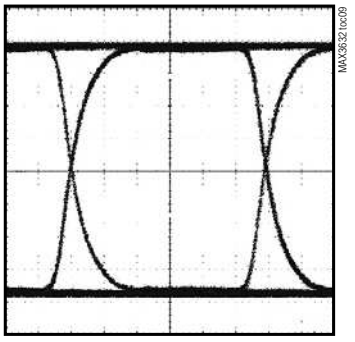
ELECTRICAL EYE DIAGRAM (800mVP-P INPUT, 622Mbps)



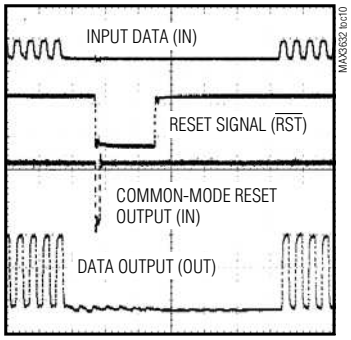
ELECTRICAL EYE DIAGRAM (4mVP-P INPUT, 1244Mbps)



ELECTRICAL EYE DIAGRAM (800mVP-P INPUT, 1244Mbps)



RESET TIMING DIAGRAM



Pin Description

PIN	NAME	FUNCTION
1, 6, 7, 13, 19, 24	GND	Ground
2, 5, 10, 14, 17, 20, 21	V_{CC}	+3.3V Supply Voltage
3	IN+	Positive Data Input, Common-Mode Reset Output
4	IN-	Negative Data Input, Common-Mode Reset Output
8	$\overline{RST}$+	Positive Burst-Mode Reset Input, LVPECL Compatible
9	$\overline{RST}$-	Negative Burst-Mode Reset Input, LVPECL Compatible
11	$\overline{HOLD}$+	Positive Offset Correction Loop Hold Input, LVPECL Compatible
12	$\overline{HOLD}$-	Negative Offset Correction Loop Hold Input, LVPECL Compatible
15	OUT-	Negative Data Output, LVPECL
16	OUT+	Positive Data Output, LVPECL
18	N.C.	No External Connection. Leave open.
22	CAZ2	Offset Correction Loop Capacitor Connection. Place a 330nF capacitor between CAZ1 and CAZ2.
23	CAZ1	Offset Correction Loop Capacitor Connection. Place a 330nF capacitor between CAZ1 and CAZ2.
EP	Exposed Paddle	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance (see *Exposed Pad (EP) Package* section).

Detailed Description

The MAX3632 burst-mode limiting amplifier is designed for 622Mbps or 1244Mbps GPON OLT receiver applications. It operates, together with the MAX3630/MAX3631 burst-mode transimpedance amplifiers, to convert current from a photodiode into an LVPECL output signal. The MAX3632 contains a data input stage, a gain stage, an offset correction loop, a reset and hold section, and an LVPECL output buffer.

Input Stage

The MAX3632 input stage provides a 200Ω differential termination and buffers the data input signal. Using a proprietary common-mode signaling technique, the input stage of the MAX3632 also sends the burst-mode reset signal from the $\overline{RST}$ inputs ($\overline{RST}$+, $\overline{RST}$-) to the MAX3630/MAX3631 TIAs. By using the common mode of the differential pair for the TIAs burst-mode reset signal, the MAX3630/MAX3631 TIAs can be assembled into 4-pin TO headers that reduce assembly costs and complexity. For proper operation of the reset signal, the MAX3630/MAX3631 data outputs (OUT+, OUT-) must be DC-coupled to the MAX3632 data inputs (IN+, IN-).

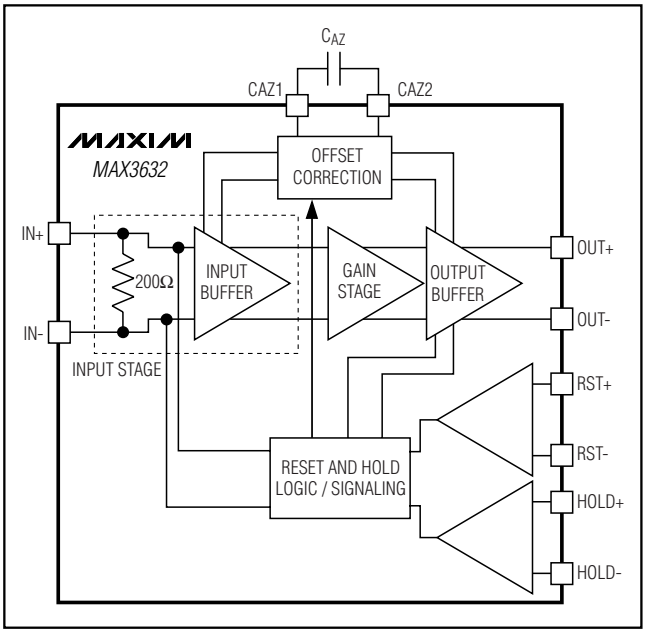


Figure 1. Functional Diagram

622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

Gain Stage/Offset Correction Loop

The high-bandwidth gain stage of the MAX3632 provides approximately 64dB of gain. The large gain of a limiting amplifier makes it susceptible to DC offsets in the signal path that are caused by pulse-width distortion of the input signal, as well as internal offsets. The offset correction loop of the MAX3632 cancels the internal and external offsets in the signal path, which reduces the deterministic jitter at the output.

Reset and Hold Section

The offset correction loop is a necessary component for proper operation of a high-gain limiting amplifier; however, it introduces a low-frequency cutoff in the signal path. If the offset correction loop is not controlled, the low-frequency cutoff prohibits burst-mode operation. Using the $\overline{RST}$ and optional $\overline{HOLD}$ input(s), the offset correction loop can be enabled or disabled, allowing proper operation of the limiting amplifier in burst-mode applications.

The LVPECL-compatible reset input ($\overline{RST}$) is used to transmit a reset signal to the MAX3630/MAX3631 TIAs. When the $\overline{RST}$ input transitions low, a reset signal is generated by the internal logic and transmitted to the MAX3630/MAX3631 TIAs as described above in the *Input Stage* section. The data input (IN) must be a logic zero when $\overline{RST}$ is asserted during the guard time (Figure 7). The $\overline{RST}$ signal is also used to disable (hold) the offset correction loop until the first transition is detected by the reset and hold logic, thus indicating the beginning of the next burst signal. The hold input ($\overline{HOLD}$) may be used to provide alternative offset cancellation control modes. Timing and operation of the $\overline{RST}$ and $\overline{HOLD}$ inputs are described in more detail in the *Applications Information* section.

LVPECL Output Buffer

The output buffer provides a high-speed LVPECL signal. For burst-mode applications, each output (OUT+, OUT-) must be DC-coupled to an equivalent LVPECL termination.

Design Procedure

IN and OUT Terminations Requirements

The IN+ and IN- inputs (Figure 2) of the MAX3632 must be DC-coupled to the MAX3630/MAX3631 data outputs for burst-mode operation. No external termination components are necessary between the MAX3632 and MAX3630/MAX3631 (see the *Typical Applications Circuit* section). The proper termination for each output of the MAX3632 OUT+, OUT- (Figure 3), is 50Ω to V_{CC} - 2V. An equivalent LVPECL termination technique (e.g., Thevenin termination) may be used as long as OUT+ and OUT- are DC-coupled to the load. For more information on PECL terminations and how to interface with other logic families, refer to Maxim Application Note HFAN-01.0: *Introduction to LVDS, PECL, and CML.*

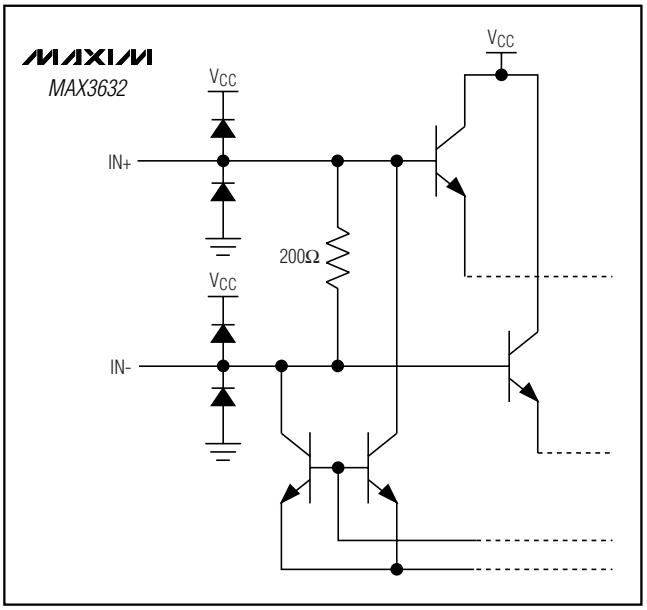


Figure 2. Simplified Data Input Structure

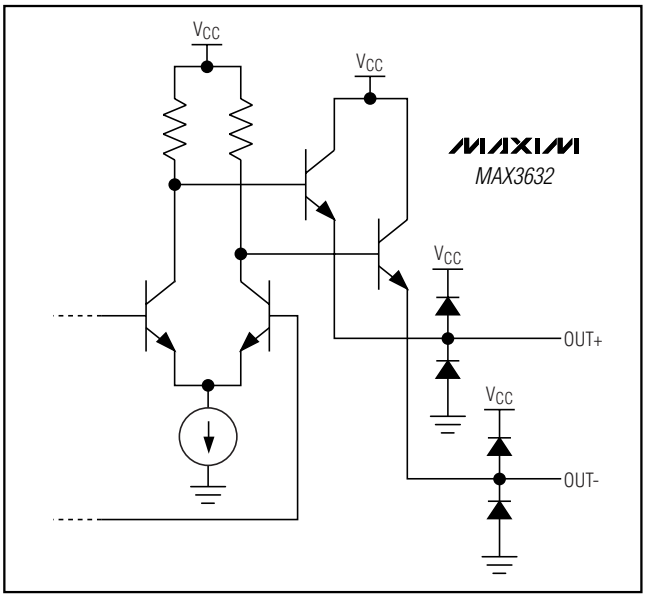


Figure 3. Simplified Data Output Structure

RST and HOLD Input Termination Requirements

The MAX3632 $\overline{RST}$ and $\overline{HOLD}$ inputs are LVPECL compatible and internally biased (high impedance; see Figure 4). Although the inputs are compatible with LVPECL signals, it is not necessary to drive the MAX3632 $\overline{RST}$ and $\overline{HOLD}$ inputs with a standard LVPECL signal. The $\overline{RST}$ and $\overline{HOLD}$ inputs of the MAX3632 operate properly as long as the specified common-mode voltage and differential voltage swings are met.

Figures 5 and 6 show how to connect an LVPECL or CML signals to the MAX3632 $\overline{RST}$ and $\overline{HOLD}$ inputs. For more information on interfacing a single-ended LVPECL or LVTTL signal to the $\overline{RST}$ or $\overline{HOLD}$ input, see *Single-Ended Operation of RST and HOLD* in the *Applications Information* section.

Selecting the Offset-Correction Capacitor (C_{AZ})

The capacitor between CAZ1 and CAZ2 determines the time constant and low-frequency cutoff (f_{OC}) of the offset correction loop. To maintain stability, there must be a one decade separation between the data input frequency (f_{IN}) and the low-frequency cutoff (f_{OC}) of the offset correction loop. For GPON systems operating at 622Mbps or 1244Mbps, a 330nF capacitor (C_{AZ}) connected between pins 22 (CAZ2) and 23 (CAZ1) is recommended. With this capacitor, the low-frequency cutoff of the offset correction loop is low enough (f_{OC} < 30kHz) to tolerate 72 CIDs within a burst signal.

Applications Information

RST and HOLD Timing / Operation

The $\overline{RST}$ and $\overline{HOLD}$ LVPECL-compatible inputs of the MAX3632 provide three different modes for disabling (holding) the offset correction loop during routine operations. The first mode of operation requires the single reset input, $\overline{RST}$, which is the same signal used to create the reset signal for the MAX3630/MAX3631 TIAs to arm its threshold setting circuitry. Refer to the MAX3630/MAX3631 data sheet and the *Input Stage* section for additional information. For this method, illustrated in Figure 7, the $\overline{RST}$ signal disables (holds) the offset correction loop until the transition detector in the MAX3632 identifies the beginning of the next burst. The burst-mode reset signal, $\overline{RST}$, must occur entirely within the guard time interval to prevent corrupted data. The data input (IN) must be a logic zero when $\overline{RST}$ is asserted (Figure 7). When operating in this mode, the $\overline{HOLD}$ input should be set to a valid LVPECL high (1600mV ≥ $V_{\overline{HOLD}+}$ - $V_{\overline{HOLD}-}$ ≥ 200mV). If the functionality of the $\overline{HOLD}$ input is not used in the application, it can be con-

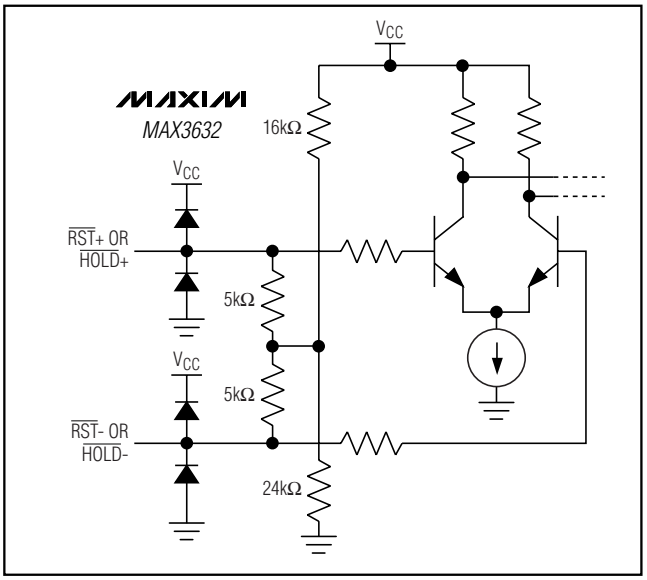


Figure 4. Simplified $\overline{RST}$ and $\overline{HOLD}$ Input Structures

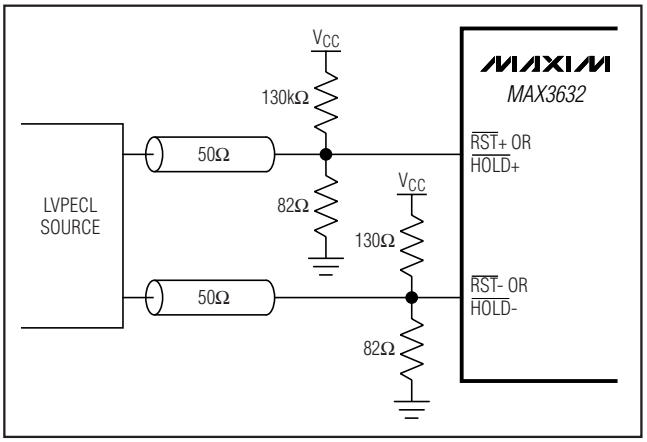


Figure 5. Interfacing $\overline{RST}$ / $\overline{HOLD}$ to Differential LVPECL

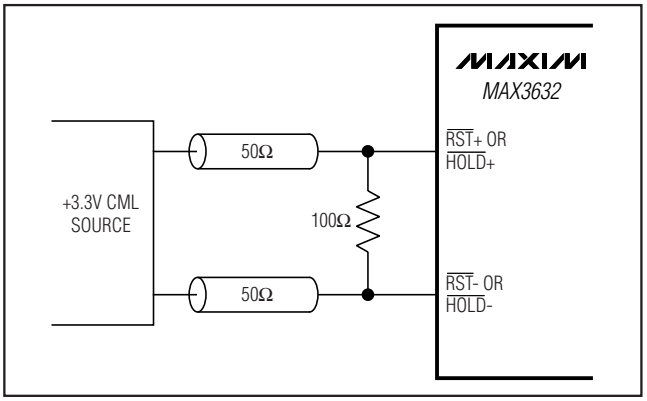


Figure 6. Interfacing $\overline{RST}$ / $\overline{HOLD}$ to Differential CML

622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

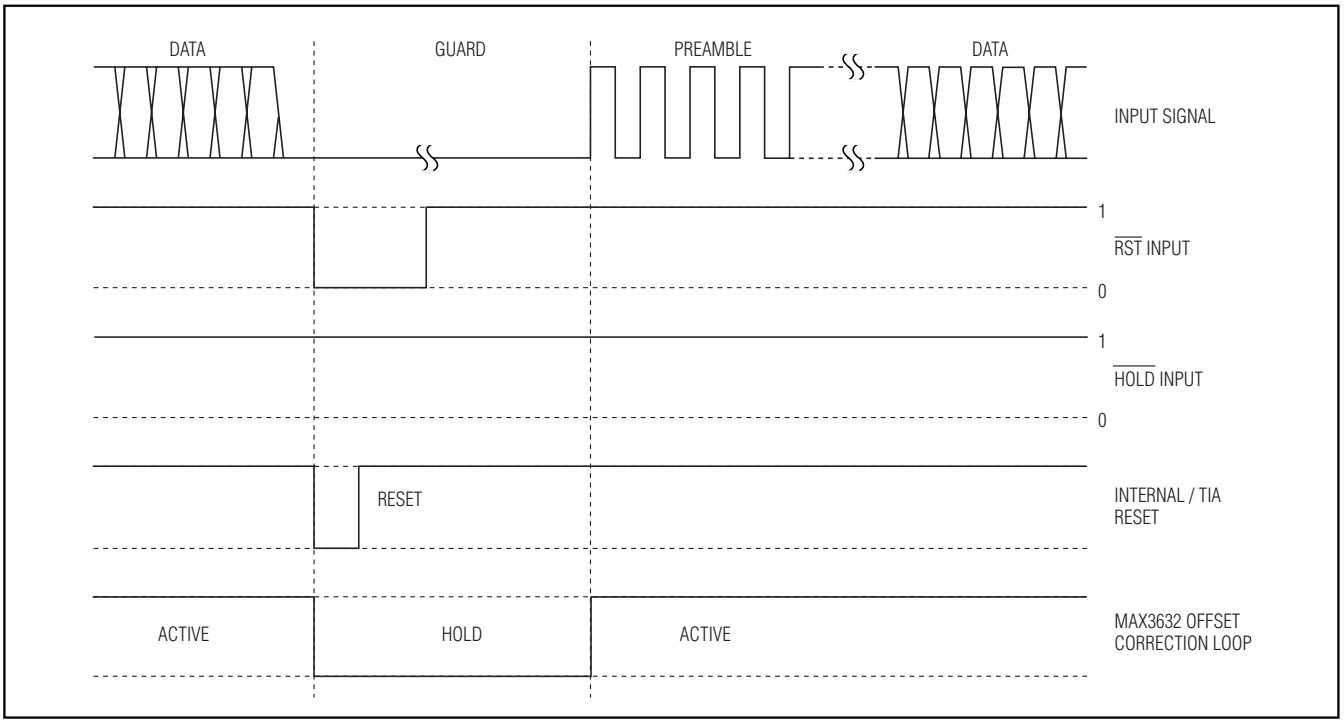


Figure 7. $\overline{RST}$ Timing Method 1

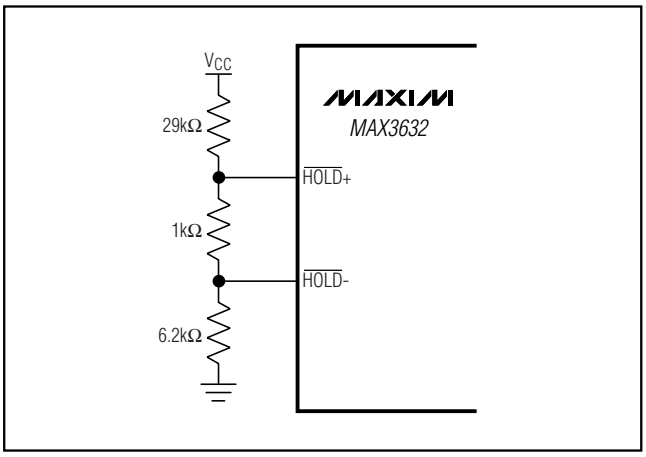


Figure 8. Asserting $\overline{HOLD}$ to a Valid LVPECL High Level

nected to a valid LVPECL-high level using three external resistors as shown in Figure 8.

The other two optional modes of burst operation use the $\overline{HOLD}$ input. For both methods, the $\overline{HOLD}$ input should be transitioned to a low prior to the end of a burst. Using the $\overline{HOLD}$ input, the offset correction loop is held to a known good state between the end of a data burst and the burst-mode reset signal. When the $\overline{HOLD}$ input is transitioned high again, prior to the end of the guard time, the transition detector restarts the offset cancellation loop at the beginning of the next burst (Figure 9). When the $\overline{HOLD}$ input is transitioned high again after the end of the guard time, the offset correction loop restarts (Figure 10). This mode can be used to hold a valid offset for long periods during the ranging operations.

The $\overline{RST}$ input is edge triggered and must be transitioned low during the guard time in all cases to ensure proper operation of the MAX3630/MAX3631 burst-mode TIAs. The transition time, 20% to 80%, of the signal at the MAX3632 $\overline{HOLD}$ input, must be < 0.3ns for proper operation for method 3.

Single-Ended Operation of RST and HOLD

The $\overline{RST}$ and $\overline{HOLD}$ inputs are designed to operate with a differential-LVPECL or -CML input signal and this is the recommended mode of operation. However, it is possible to drive the $\overline{RST}$ and $\overline{HOLD}$ inputs with a single-ended LVPECL, LVTTL, or LVCMOS signal.

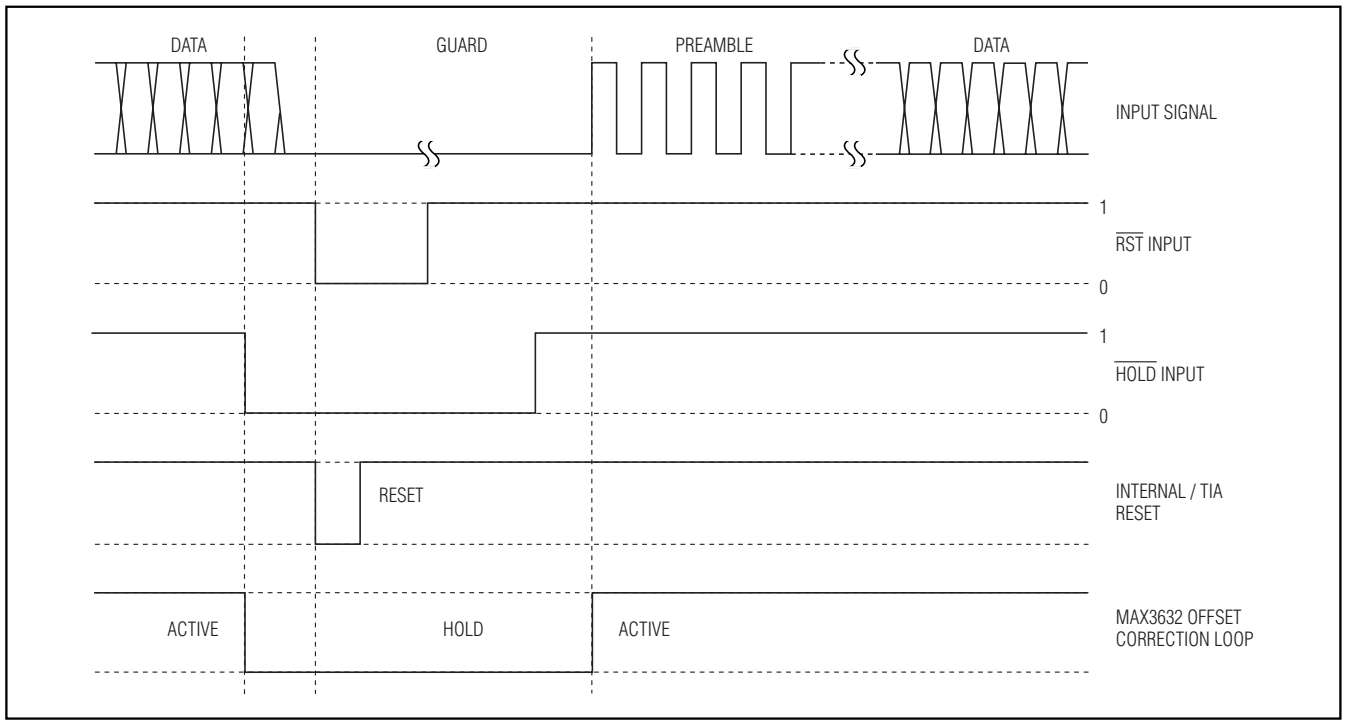


Figure 9. $\overline{RST}$ or $\overline{HOLD}$ Timing Method 2

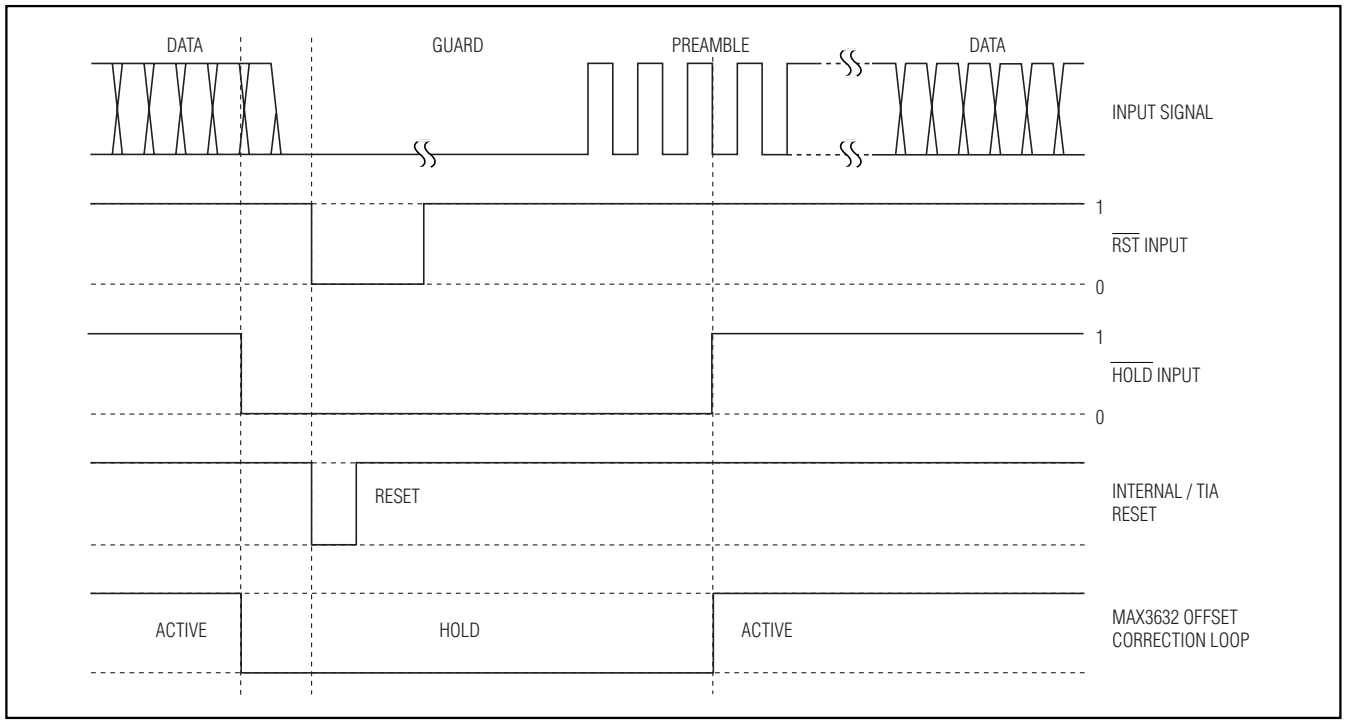


Figure 10. $\overline{RST}$/$\overline{HOLD}$ Timing Method 3

622Mbps/1244Mbps Burst-Mode Limiting Amplifier for GPON OLT Applications

To connect a single-ended LVPECL signal to $\overline{RST}$ (Figure 11), connect a 130Ω resistor (R1) from $\overline{RST}$+ or $\overline{HOLD}$+ to V_{CC}, and an 82Ω resistor (R2) from $\overline{RST}$+ or $\overline{HOLD}$+ to ground. The $\overline{RST}$+ or $\overline{HOLD}$+ pin must also be DC-coupled to the single-ended LVPECL source. Connect a resistor (R3) from V_{CC} to $\overline{RST}$- or $\overline{HOLD}$- and another resistor (R4) from $\overline{RST}$- or $\overline{HOLD}$- to ground. The parallel combination of R3 and R4 should be less than 1kΩ. Choose the values of R3 and R4 to set the common-mode voltage in the range defined in the *Electrical Characteristics* table. This configuration with typical values is shown in Figure 11.

An LVTTL or LVCMOS signal may also be used if the transition time is fast enough. For single-ended operation with an LVTTL or LVCMOS signal (Figure 12), connect a 4kΩ resistor (R6) from the $\overline{RST}$+ or $\overline{HOLD}$+ to the signal source, and a 1kΩ resistor (R5) from $\overline{RST}$+ or $\overline{HOLD}$+ to V_{CC}. A 1kΩ resistor (R7) to V_{CC}, and a 9kΩ resistor (R8) to ground, should then be connected to $\overline{RST}$- or $\overline{HOLD}$-. For typical LVTTL or LVCMOS specifications of V_{CC} to 2.8V for a high, and 0.4V to 0V for a low, the LVTTL or LVCMOS needs to source approximately zero current and sink a maximum of approximately 720µA using this configuration.

Layout Considerations

Use good high-frequency layout techniques and multiple-layer boards with uninterrupted ground planes to minimize EMI and crosstalk. If the electrical length between the MAX3630/MAX3631 output and the MAX3632 input path delay is long compared to the input transition time, a controlled 200Ω differential-impedance transmission line should be used to interface the two devices. A controlled-impedance transmission line of 50Ω single-ended (100Ω differential) should be used to interface the MAX3632 output (OUT+, OUT-) to other devices. The $\overline{RST}$ and $\overline{HOLD}$ inputs should also be connected to the LVPECL- or CML-signal source with a controlled impedance (50Ω single ended, 100Ω differential) transmission line. Place the CAZ capacitor as close as possible to pin 22 (CAZ2) and pin 23 (CAZ1).

Exposed Pad (EP) Package

The exposed-pad on the 24-pin QFN provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3632 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note HFAN-08.1: *Thermal Considerations for QFN and Other Exposed Pad Packages* (available at www.maxim-ic.com).

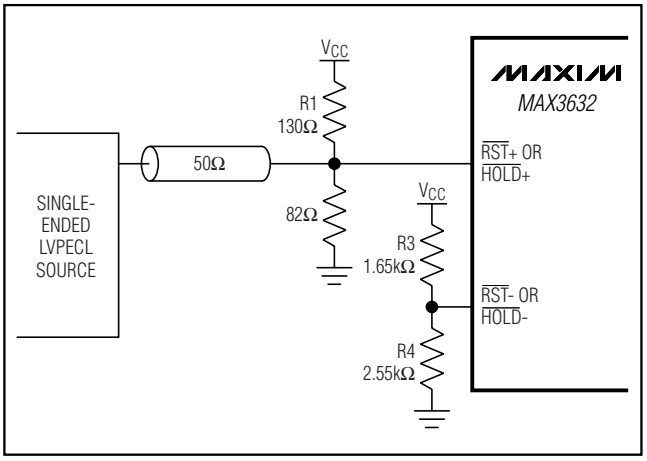


Figure 11. Interfacing $\overline{RST}$ or $\overline{HOLD}$ to Single-Ended LVPECL

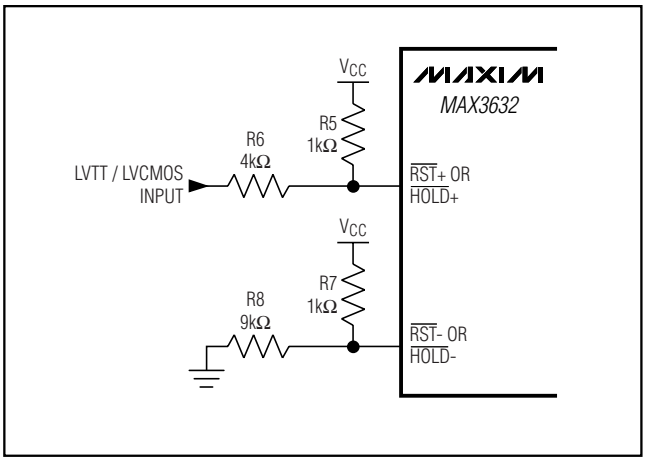


Figure 12. Interfacing $\overline{RST}$ or $\overline{HOLD}$ to Single-Ended LVTTL/LVCMOS

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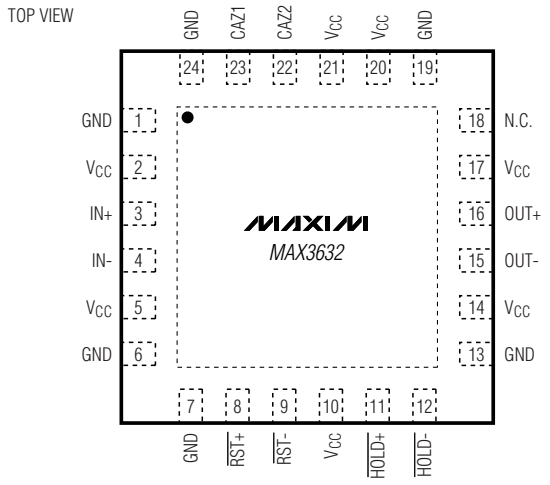
Pin Configuration



*THE EXPOSED PAD MUST BE CONNECTED TO CIRCUIT BOARD GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

Chip Information

TRANSISTOR COUNT: 1363 (1232 bipolar, 131 MOS)

PROCESS: SiGe BiCMOS

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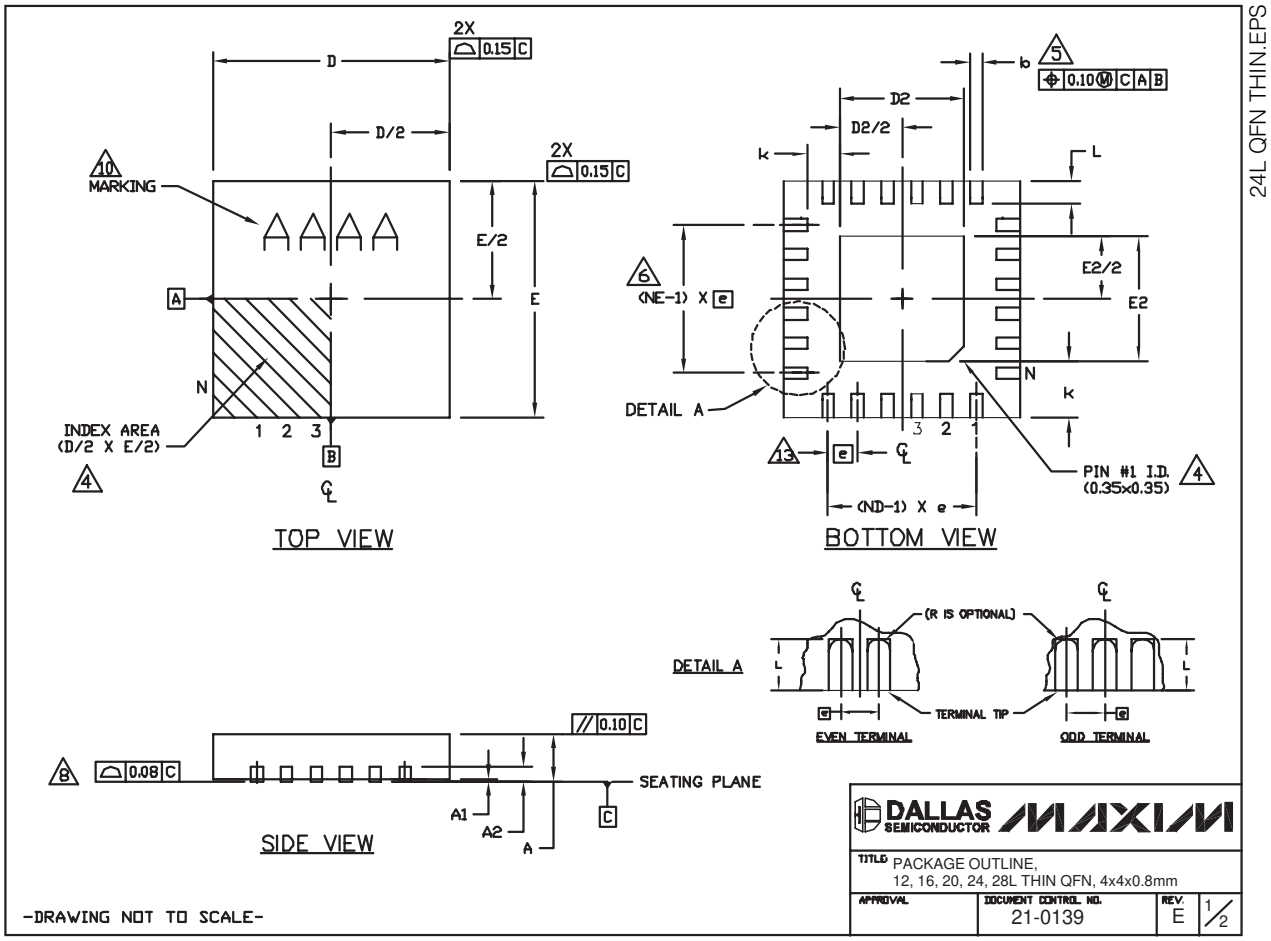
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2