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19-5910; Rev 0; 8/11

EVALUATION KIT AVAILABLE

MAX3710

125Mbps to 2.5Gbps Integrated Limiting Amplifier/ Burst Mode Laser Driver with Dual-Loop Power Control

General Description

The MAX3710 limiting amplifier and burst mode laser driver provides a highly integrated, low-cost, high-performance PMD solution for GPON/EPON ONU applications in modules or directly on the ONU board.

The low-jitter laser diode driver provides transmit burst mode average power control (APC) of laser bias current as well as an integrated modulation current control loop (extinction ratio control, or ERC). The ERC eliminates the need for temperature lookup tables (LUTs) controlling the modulation current.

The low-noise limiting amplifier maximizes optical sensitivity and has adjustable SD/LOS threshold plus programmable output levels. The differential CML output stage features a slew-rate adjustment for 1.25Gbps EPON operation. Integrated bias current monitor, burst mode Tx power monitor, and a digital laser power monitor enable a low-cost implementation of the next-generation GPON and EPON modules with digital diagnostics.

A novel auto-calibration mode enables low-cost fiber optic module production. An integrated 3-wire digital interface controls the laser driver and limiting amplifier functions, and enables communication with a low-cost controller.

The MAX3710 is offered in a small, 4mm x 4mm, 24-pin TQFN package with exposed pad, and operates over the -40°C to +95°C temperature range.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Simplifies Module Manufacturing**
  - **Enables Single-Temperature Module Testing**
  - **Production Laser Auto-Calibration Mode**
- **Improved ONU Performance**
  - **Integrated APC and ERC Loops**
  - **1.3mV$_{P-P}$ Receiver Sensitivity**
  - **Separate Laser Driver Supply (Rogue ONU Shutdown)**
- **Flexibility**
  - **LVDS, LVPECL, and CML Compatible High-Speed I/Os**
  - **Programmable I/O Polarity**
  - **3-Wire Digital Interface**
- **Safety and Reliability**
  - **Integrated Safety Features with FAULT Mask Register**
  - **Supports SFP MSA and SFF-8472 Digital Diagnostic**
  - **Selectable Analog Monitor of Laser Power or BIAS Current at BMON Pin**

Applications

BOSA On-Board

GPON/EPON ONU

ABSOLUTE MAXIMUM RATINGS

V_{CCX}, V_{CCTO}, V_{CCD} ..... -0.3V to 4.0V
Voltage Range at DISABLE, SDA, SCL, CSEL, FAULT, LOS, MDREF, LPD ..... -0.3V to (V_{CC} + 0.3V)
Voltage Range at RIN+, RIN- ..... (V_{CC} - 1.7V) to (V_{CC} + 0.3V)
Voltage Range at ROUT+, ROUT- ..... (V_{CC} - 2V) to (V_{CC} + 0.3V)
Voltage Range at TIN+, TIN-, BEN+, BEN- ..... -0.3V to (V_{CC} + 0.3V)
Voltage Range at TOUT ..... 0.3V to V_{CCTO}
Voltage Range at IOUT ..... (V_{CCTO} - 1.8V) to (V_{CCTO} + 1.2V)
Current Range into FAULT, LOS, MDIN, SDA ..... -1mA to +5mA
Current Range into LPD ..... -5mA to +5mA
Current out of ROUT+, ROUT- 40mA
Current into TOUT 180mA
Current into IOUT 120mA
Voltage Range at BMON ..... -0.3V to V_{CC}
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C) 2222mW
Storage Temperature Range ..... -55°C to +150°C
Die Attach Temperature ..... +400°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
Power Supply Voltage	V_{CC}		2.97	3.3	3.63	V
POWER SUPPLY						
Power-Supply Current	I_{CC}	Includes Rx CML output current, excludes Tx I_{BIAS} = 20mA, I_{MOD} = 40mA		75	110	mA
POWER-ON RESET						
V_{CC} for Enable High		V_{CCX} connected to V_{CCD}		2.55	2.75	V
V_{CC} for Enable Low		V_{CCX} connected to V_{CCD}	2.3	2.45		V
Rx INPUT SPECIFICATION						
Differential Input Resistance	R_{IN}		75	100	125	Ω
Input Sensitivity	V_{INMIN}	2^{23} - 1 PRBS, 2.5Gbps, TX_EN = 0 (Note 2)		1.3	2	mV_{P-P}
Input Overload	V_{INMAX}	(Note 2)	1.2			V_{P-P}
Differential Input Return Loss	S_{DD11}	Device powered on, f ≤ 2GHz		19		dB
		Device powered on, f ≤ 5GHz		12		
Common-Mode Input Return Loss	S_{CC11}	Device powered on, 1GHz ≤ f ≤ 2GHz		11		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		14		
Rx OUTPUT SPECIFICATION						
Differential Output Resistance	$R_{OUTDIFF}$		75	100	125	Ω
Differential Output Return Loss	S_{DD22}	Device powered on, f ≤ 2GHz		19		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		15		
Common-Mode Output Return Loss	S_{CC22}	Device powered on, f ≤ 2GHz		14		dB
		Device powered on, 2GHz ≤ f ≤ 5GHz		10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CML Differential Output Voltage		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d		600	800	1000	mV_{P-P}
		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 0			410		
CML Differential Output Voltage When Disabled		Output AC-coupled, V_{INMAX} at input, SET_CML[3:0] = 10d (Note 2)				5	mV_{P-P}
Data Output Transition Time (20% to 80%) (Note 2)		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SLEW_RATE = 1			85	115	ps
		$4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SLEW_RATE = 0			140	200	
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}		V_{CC} - 0.1			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}		0		0.4	V
Rx TRANSFER CHARACTERISTICS							
Deterministic Jitter (Notes 2, 3)	DJ	2.5Gbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d			7	15	ps_{P-P}
		1.25Gbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d			10	20	
		125Mbps, $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[3:0] = 10d, K28.5 pattern			21		
Random Jitter	RJ	Input = $4mV_{P-P}$ at 2.5Gbps, 1111 0000 pattern, SET_CML[3:0] = 10d (Notes 2, 4)			3.5	5	ps_{RMS}
Low-Frequency Cutoff (Simulated Value)		I/O coupling capacitors = 1µF			10		kHz
Small-Signal Bandwidth (Simulated Value)		SLEW_RATE = 1			2.0		GHz
LOS SPECIFICATIONS (Notes 2, 5)							
LOS Hysteresis		$10log(V_{DEASSERT}/V_{ASSERT})$		1.25	2.2		dB
LOS Assert/Deassert Time		(Note 6)		2.3		30	µs
LOS Assert Sensitivity Range		LOS_RANGE = 0		4.6		36	mV_{P-P}
		LOS_RANGE = 1		14		115	
LOS Assert/Deassert Level (Low Range, LOS_RANGE = 0)		LOS assert	SET_LOS = 5	3	3.8	4.6	mV_{P-P}
			SET_LOS = 31	18	23	28	
			SET_LOS = 63	36	47	56	
		LOS deassert	SET_LOS = 5	5	6.5	8	
			SET_LOS = 31	32	39	46	
			SET_LOS = 63	64	80	95	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOS Assert/Deassert Level (High Range, LOS_RANGE = 1)		LOS assert	SET_LOS = 5	9	11.5	14	mV_{P-P}
			SET_LOS = 31	55	68	80	
			SET_LOS = 63	115	138	160	
		LOS deassert	SET_LOS = 5	15	19	23	
			SET_LOS = 31	97	117	136	
			SET_LOS = 63	197	238	278	
Tx INPUT SPECIFICATIONS							
Differential Input Resistance (TIN and BEN)					13		kΩ
Internal Common-Mode Bias Voltage (TIN and BEN)		For AC-coupled operation			1.3		V
Differential Input Voltage (TIN and BEN)		DC-coupled, 100Ω, differential resistors, Figure 1 and Figure 3		0.2		1.6	V_{P-P}
Common-Mode Input Voltage Range (TIN and BEN)		DC-coupled, Figure 1 and Figure 3		1.125		V_{CC} - V_{IN}/2.5	V
DISABLE Input Current		DISABLE = V_{CC}				10	µA
		DISABLE = GND			33	60.5	
DISABLE Input High Voltage	V_{IH}			1.8		V_{CC}	V
DISABLE Input Low Voltage	V_{IL}			0		0.8	V
DISABLE Input Hysteresis	V_{HYST}				80		mV
DISABLE Input Impedance	R_{PULL}	Pullup resistor		60	100	138	kΩ
Tx OUTPUT SPECIFICATIONS							
FAULT Output High Voltage	V_{OH}	R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC}		V_{CC} - 0.1			V
FAULT Output Low Voltage	V_{OL}	R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC}		0		0.4	V
LPD Output High Voltage	V_{OH}	I_{LPD} = -1mA		V_{CC} - 0.5			V
LPD Output Low Voltage	V_{OL}	I_{LPD} = +1mA		0		0.4	V
LASER MODULATOR							
Maximum Modulation-On Current				85			mA
Minimum Modulation-On Current						5	mA
Modulation Current DAC Stability		10mA ≤ I_{MOD} ≤ 85mA (Notes 2, 7)			1	4	%
Modulation Current Rise/Fall Time (Note 2)		20% to 80%, 10mA ≤ I_{MOD} ≤ 85mA, R_{LOAD} = 12Ω, TRF[1:0] = 11b			65	120	ps
		20% to 80%, 10mA ≤ I_{MOD} ≤ 85mA, R_{LOAD} = 12Ω, TRF[1:0] = 00b			72		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Compliance Voltage at TOUT	V_{TOUT}	Instantaneous voltage, 10mA ≤ I_{MOD} ≤ 85mA	0.6		2.4	V
Deterministic Jitter (Notes 2, 3)	DJ	10mA ≤ I_{MOD} ≤ 85mA, 2.5Gbps		15	40	ps_{P-P}
		10mA ≤ I_{MOD} ≤ 85mA, 1.25Gbps		15		
		10mA ≤ I_{MOD} ≤ 85mA, 125Mbps, K28.5 pattern		20		
Random Jitter (Notes 2, 4)	RJ	10mA ≤ I_{MOD} ≤ 20mA, 1111 0000 pattern		1.2	1.65	ps_{RMS}
		20mA ≤ I_{MOD} ≤ 85mA, 1111 0000 pattern		1	1.45	
BIAS GENERATOR						
Maximum Bias Current		Current into TOUT	70			mA
Minimum Bias Current		Current into TOUT			1	mA
Bias Current DAC Stability		2mA ≤ I_{BIAS} ≤ 70mA, V_{TOUT} = 2V (Notes 2, 7)		1	4	%
Bias Current Monitor Current Gain	I_{BIAS}/ I_{BMON}	External resistor to GND defines voltage gain, 2mA ≤ I_{BIAS} ≤ 6mA	54	64	72	A/A
		External resistor to GND defines voltage gain, 6mA ≤ I_{BIAS} ≤ 70mA	64	72	80	
Compliance Voltage Range at BMON	V_{BMON}		0		1.8	V
BMON Current Gain Stability (as Bias Monitor)		2mA ≤ I_{BIAS} ≤ 70mA (Notes 2, 7)		2	5	%
LASER CONTROL SPECIFICATIONS						
APC Loop Stability (1.25Gbps, 2^{23} - 1 PRBS Pattern) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.1		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.1		
APC Loop Stability (2.5Gbps, 2^{23} - 1 PRBS Pattern) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.1		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.1		
ERC Loop Stability (1.25Gbps, 2^{23} - 1 PRBS Pattern, e_R = 11dB) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		0.5		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		0.5		
ERC Loop Stability (2.5Gbps, 2^{23} - 1 PRBS Pattern, e_R = 11dB) (Note 8)		$I_{MDINAVG}$ = 50µA, K_{MD} x SE = 0.005		1.3		10log(dB)
		$I_{MDINAVG}$ = 2mA, K_{MD} x SE = 0.05		1.1		
MDIN Bias Voltage	V_{MDIN}			1.2		V
MD Average Current Range	$I_{MDINAVG}$	Average current into MDIN	50		2000	µA
Programmable Extinction Ratio Range	e_R	P1/P0 (DPC closed-loop operation)	10	16	24	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MD Current Monitor/BMON Activation Time		From the rising edge of the final SCL clock of the 3-wire cycle to 90% of steady state at BMON		100		ns
SAFETY FEATURES						
Fault Threshold Voltage at TOUT	V_{TOUT}	Fault always occurs for V_{TOUT} < 0.35V, fault never occurs for V_{TOUT} ≥ 0.55V	0.35		0.55	V
Fault Threshold Voltage at MDIN	V_{MDIN}	Fault always occurs for V_{MDIN} < 0.3V, fault never occurs for V_{MDIN} ≥ 0.5V	0.3		0.5	V
Fault Threshold Voltage at IOUT		Fault always occurs for V_{IOUT} < V_{CCTO} - 1.7V, fault never occurs for V_{IOUT} ≥ V_{CCTO} - 1.45V, V_{CCTO} = 3.3V	V_{CCTO} - 1.7		V_{CCTO} - 1.45	V
Warning Threshold Voltage at BEN (Differential Voltage)		Warning occurs if I(BEN+) - (BEN-)I < 20mV and never occurs if I(BEN+) - (BEN-)I ≥ 100mV	20		100	mV
Warning Threshold Voltage at BEN (Common-Mode Voltage)		Warning occurs if both BEN+ and BEN- fall below 880mV		880		mV
Fault Threshold Voltage at V_{CCTO}		Fault always occurs for V_{CCTO} < 2V; fault never occurs for V_{CCTO} ≥ 2.95V	2		2.95	V
Maximum Laser Current in Disable State or Burst-Off State		Combined total current into TOUT during fault, DISABLE = 1, TX_EN = 0, or BEN = 0			100	µA
Tx TIMING SPECIFICATIONS						
DPC Loop Initialization Time	$t_{APCINIT}$	I_{BIAS} = 40mA and I_{MOD} = 60mA, I_{BIAS_INT} = 8mA, time from restart to I_{BIAS} and I_{MOD} at 90% of steady state		3		µs
Burst Enable Time	t_{BSTART}	Time from 50% of BEN± input signal to I_{BIAS} and I_{MOD} at 90% of steady state (Note 2)			2	ns
Burst Disable Time	t_{BSTOP}	Time from 50% of BEN± input signal to I_{BIAS} and I_{MOD} at 10% of steady state (Note 2)			2	ns
Minimum Burst-On Time to Update BIAS and MOD	t_{BRSTON}	MDON_DLY[1:0] = 00 (Note 2)		60	100	ns
Minimum Burst-Off Time to Update BIAS and MOD	$t_{BRSTOFF}$	(Note 2)		110	200	ns
DISABLE Assert Time	t_{OFF}	Time from rising edge of DISABLE input signal to I_{BIAS} and I_{MOD} at 10% of steady state (Note 2)		30	100	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DISABLE Negate Time	t_{ON}	Time from falling edge of DISABLE input signal to I_{BIAS} and I_{MOD} at 90% of steady state (Note 2)		200	300	ns
Fault Assert Time	t_{FAULT}	Time from fault condition to FAULT high, $C_{FAULT} \leq 20pF$, R_{FAULT} is 4.7kΩ - 10kΩ to V_{CC} (Note 2)		2.5	10	µs
LPD Assert Time	$t_{LPD-ASSERT}$	Time from positive BEN edge to 90% of steady state at LPD output, $C_{LPD} \leq 10pF$			100	ns
LPD Deassert Time	$t_{LPD-DEASSERT}$	Time from negative BEN edge to 90% of steady state at LPD output, $C_{LPD} \leq 10pF$			100	ns
DISABLE to Reset		Minimum required time DISABLE must be held high to reset a fault		100		ns
LASER POWER DETECTOR (LPD) SPECIFICATIONS						
LPD Threshold Values		KIMD[1:0] = 00: N = LPD_TH[2:0] + 1, KIMD[1:0] = 01: N = 2 x (LPD_TH[2:0] + 1), KIMD[1:0] = 1X: N = 4 x (LPD_TH[2:0] + 1)		N x 12.5		µA
Rx OUTPUT LEVEL DAC						
Full-Scale Voltage	V_{FS}	SET_CML[3:0] = 15d	820	1000		mV_{P-P}
Resolution		4 bits		40		mV_{P-P}
LOS THRESHOLD DAC						
Full-Scale Voltage		LOS_RANGE = 0		47		mV_{P-P}
		LOS_RANGE = 1		138		
Resolution		LOS_RANGE = 0		0.75		mV_{P-P}
		LOS_RANGE = 1		2.2		
Integral Nonlinearity		SET_LOS[5:0] = 5d to 63d		±0.7		LSB
BIAS CURRENT DAC						
Full-Scale Current	I_{FS_BIAS}	I_{BIAS} = (12 + BIASREG[9:0]) x LSB_BIAS	70	78		mA
Resolution	LSB_BIAS	10-bit DAC		75		µA
MODULATION CURRENT DAC						
Full-Scale Current	I_{FS_MOD}	I_{MOD} = (20 + MODREG[8:0]) x LSB_MOD	85	89		mA
Resolution	LSB_MOD	9-bit DAC		167		µA
3-WIRE DIGITAL INTERFACE						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			80		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to +3.63V, T_A = -40°C to +95°C; CML receiver output is AC-coupled to differential 100Ω load; registers are set to default values, unless implied by test conditions. Typical values are at V_{CC} = +3.3V, T_A = +25°C, data rate = 2.5Gbps, I_{BIAS} = 20mA, and I_{MOD} = 40mA, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}, I_{IH}	Voltage at pin 0V to V_{CC}, internal pullup or pulldown 75kΩ typical			85	µA
Output High Voltage	V_{OH}	External pullup of 4.7kΩ to V_{CC}	V_{CC} - 0.1			V
Output Low Voltage	V_{OL}	External pullup of 4.7kΩ to V_{CC}			0.4	V
3-WIRE DIGITAL INTERFACE TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}				1	MHz
SCL Pulse-Width High	t_{CH}		0.5			µs
SCL Pulse-Width Low	t_{CL}		0.5			µs
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL External Load	C_B	Total bus capacitance on one line			20	pF

Note 1: Specifications at T_A = -40°C and T_A = +95°C are guaranteed by design and characterization, .

Note 2: Guaranteed by design and characterization, T_A = -40°C to +95°C.

Note 3: The data input transition time is controlled by 4th-order Bessel filter with f_{-3dB} = 0.75 x 1.25GHz and f_{-3dB} = 0.75 x 2.5GHz, respectively. The deterministic jitter caused by this filter is not included in the DJ. A 2^{23} - 1 PRBS equivalent pattern was used.

Note 4: RJ was tested without input filter.

Note 5: For all Rx LOS specifications LOS_LOWBW = 1 for 1.25Gbps operation and LOS_LOWBW = 0 for 2.5Gbps operation.

Note 6: Measurement includes an input AC-coupling capacitor of 0.1µF. The signal at the RIN input is switched between two amplitudes: Signal_ON and Signal_OFF.

1) Receiver operates at sensitivity level plus 1dB power penalty
   a) Signal_OFF = 0
      Signal_ON = 10log(min_assert_level) + 8dB
   b) Signal_ON = 10log(max_deassert_level) + 1dB
      Signal_OFF = 0
2) Receiver operates at overload
      Signal_OFF = 0
      Signal_ON = $1.2V_{P-P}$
      max_deassert_level and min_assert_level are measured for one SET_LOS setting

Note 7: Stability is defined [($I_{MEASURED}$) - ($I_{REFERENCE}$)]/($I_{REFERENCE}$) over the listed current range temperature and supply variation. Reference current measured at V_{CC} = 3.3V and T_A = +25°C. Measured current is measured at V_{CC} = 3.3V ±5% and T_A = -40°C to +95°C.

Note 8: K_{MD} is the laser diode to monitor diode gain in A/W. SE is the laser's slope efficiency.

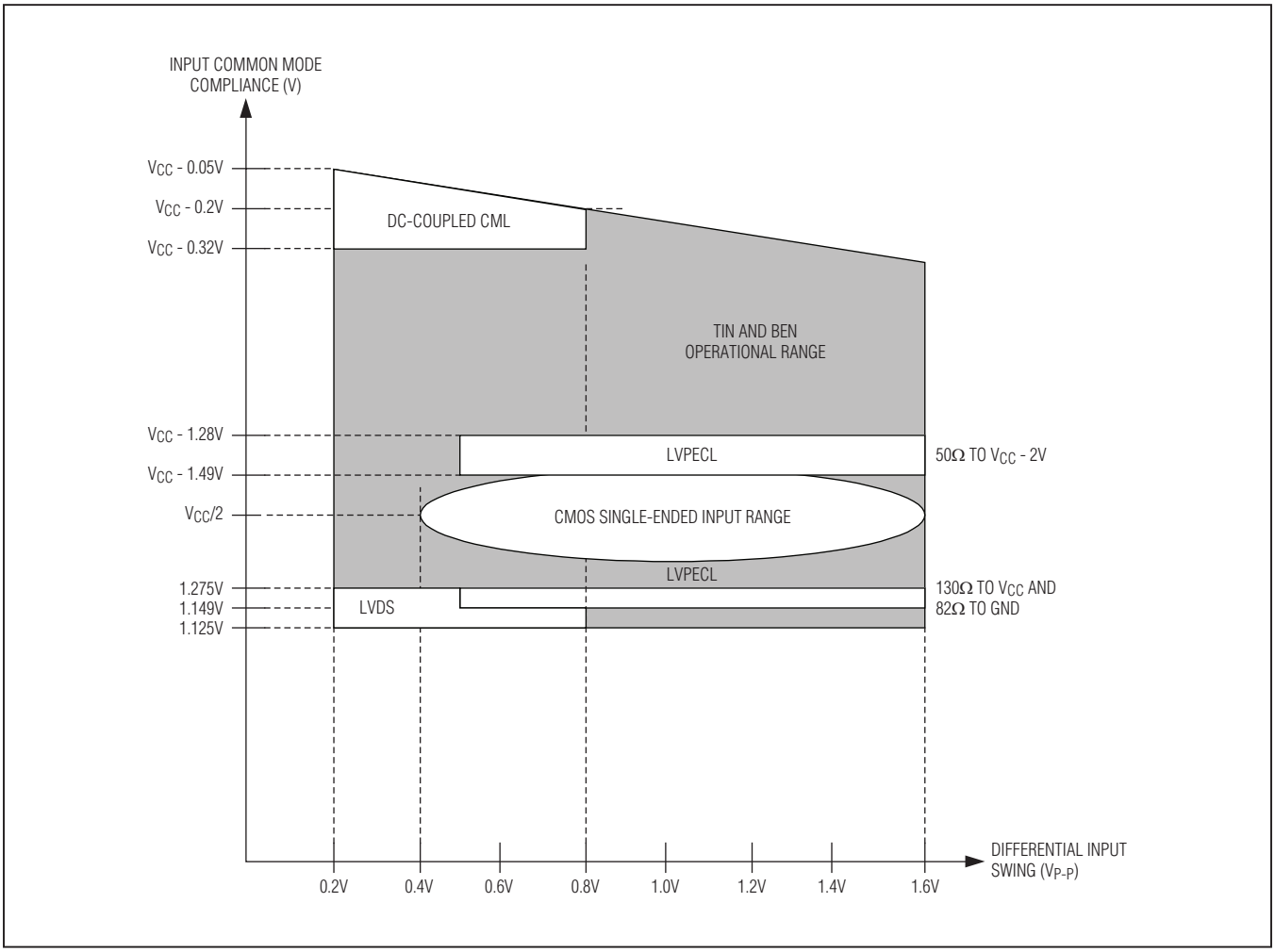


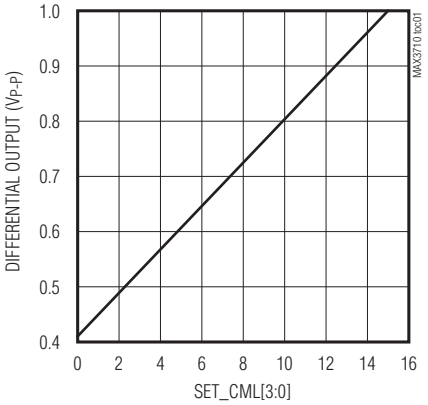
Figure 1. BEN/TIN Input Voltage Diagram

125Mbps to 2.5Gbps Integrated Limiting Amplifier/ Burst Mode Laser Driver with Dual-Loop Power Control

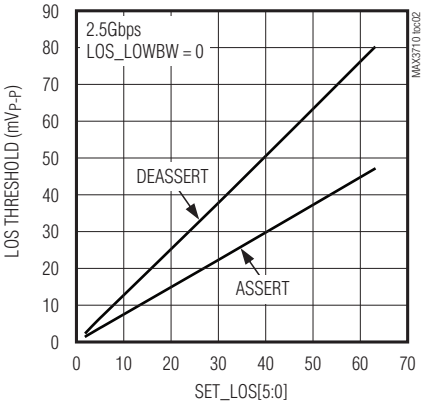
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^{23} - 1 PRBS, unless otherwise noted.)

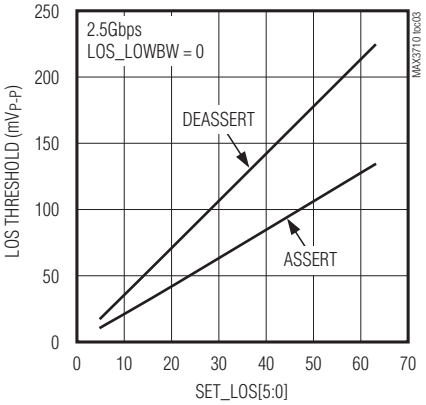
DIFFERENTIAL Rx OUTPUT SWING vs. SET_CML



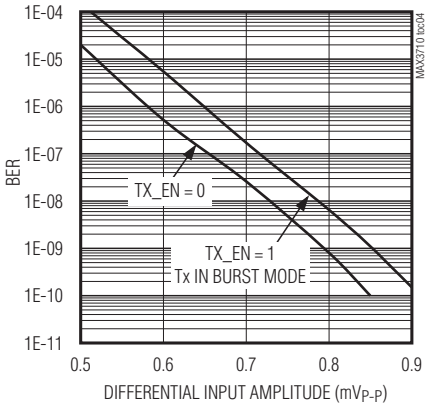
Rx INPUT-BASED LOS THRESHOLD vs. SET_LOS (LOS_EN = 1 AND LOS_RANGE = 0)



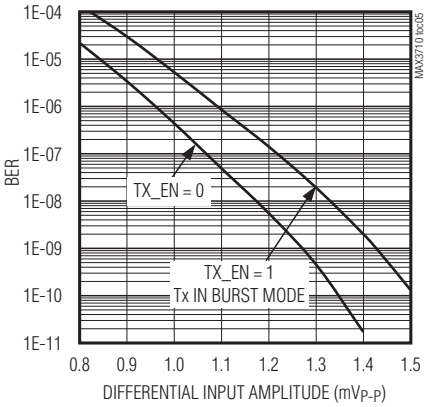
Rx INPUT-BASED LOS THRESHOLD vs. SET_LOS (LOS_EN = 1 AND LOS_RANGE = 1)



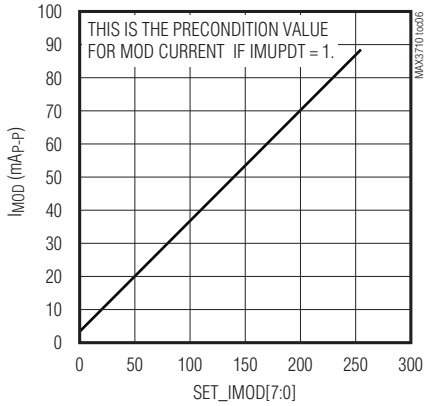
BIT-ERROR RATE vs. DIFFERENTIAL INPUT AMPLITUDE (1.25Gbps)



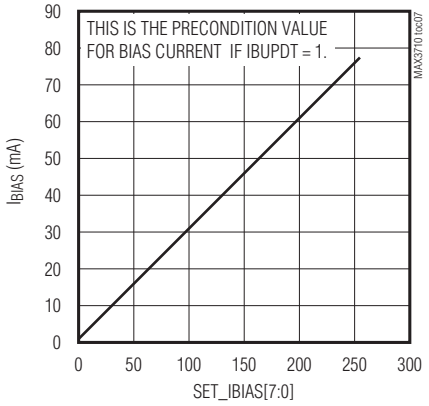
BIT-ERROR RATE vs. DIFFERENTIAL INPUT AMPLITUDE (2.5Gbps)



IMOD CURRENT vs. SET_IMOD[7:0] (OPEN LOOP OPERATION)



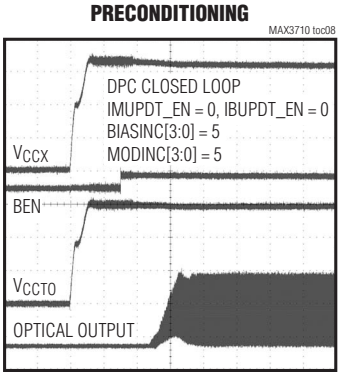
IBIAS CURRENT vs. SET_IBIAS[7:0] (OPEN LOOP OPERATION)



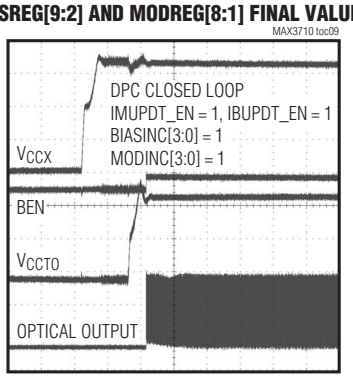
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^{23} - 1 PRBS, unless otherwise noted.)

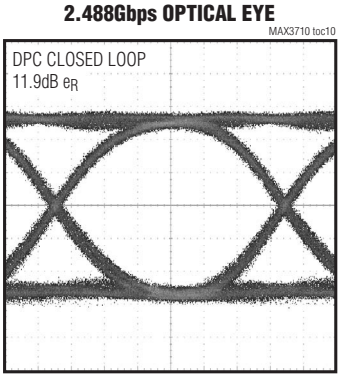
LASER STARTUP WITHOUT PRECONDITIONING



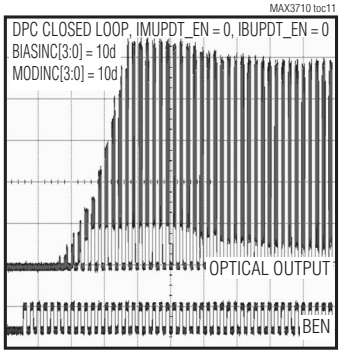
LASER STARTUP WITH PRECONDITIONING (SET_IBIAS[7:0] AND SET_IMOD[7:0] LOADED WITH VALUES CLOSE TO BIASREG[9:2] AND MODREG[8:1] FINAL VALUES)



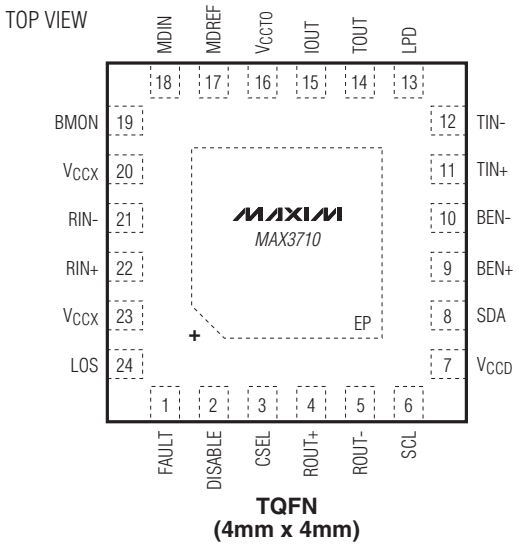
2.488Gbps OPTICAL EYE



LASER STARTUP WITHOUT PRECONDITIONING (200ns BURSTS), STARTING FROM MINIMUM I_{BIAS} AND I_{MOD}

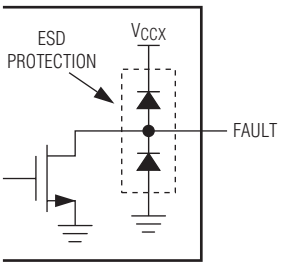
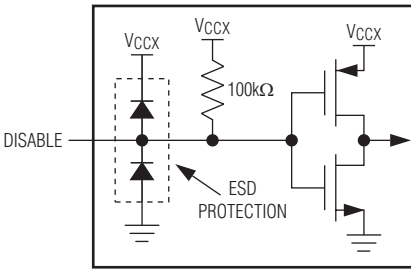


Pin Configuration

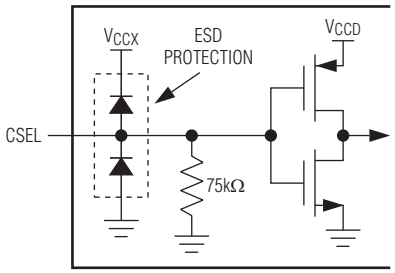
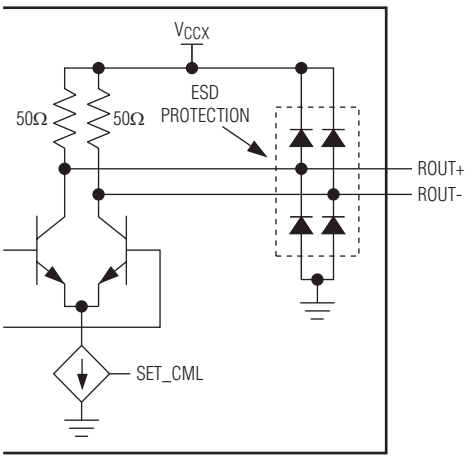
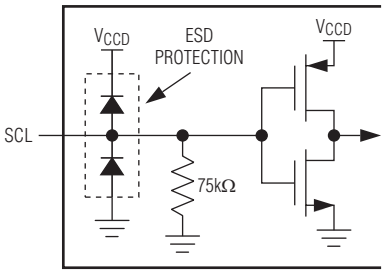
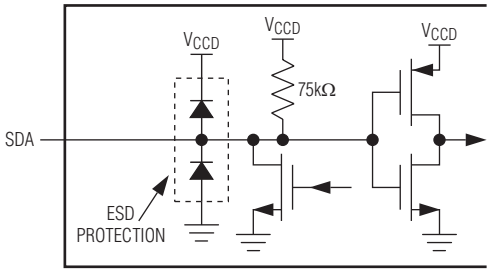


TQFN
(4mm x 4mm)

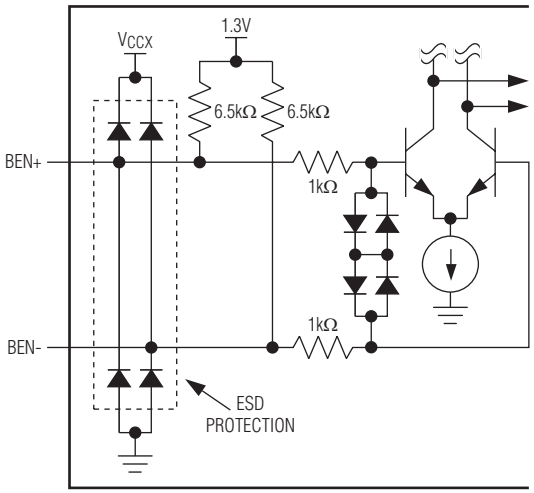
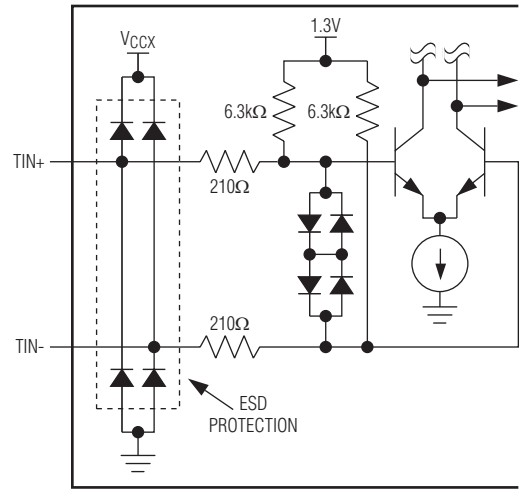
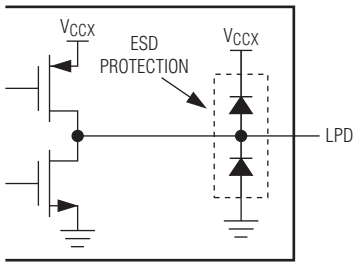
Pin Description

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
1	FAULT	Transmitter Fault, Open-Drain. Logic-high indicates a fault condition has been detected (FAULT_POL = 1). It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by toggling the DISABLE signal, or by setting MODECTRL = 68h. FAULT should be pulled up to 3.3V supply through a 4.7kΩ to 10kΩ resistor. Note that pulling up the pin to a supply voltage above V_{CCX} can turn on the ESD protection diode.	
2	DISABLE	Transmitter Disable Input, TTL/CMOS. Set to logic-low for normal operation (DIS_POL = 1). Logic-high or open disables both the modulation current and the bias current. Internally pulled up by a 100kΩ resistor to V_{CCX}.	

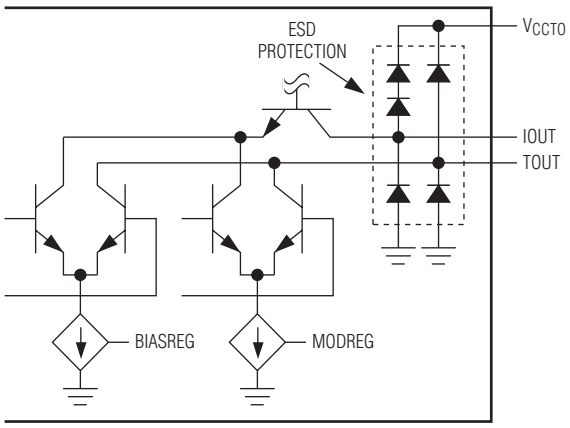
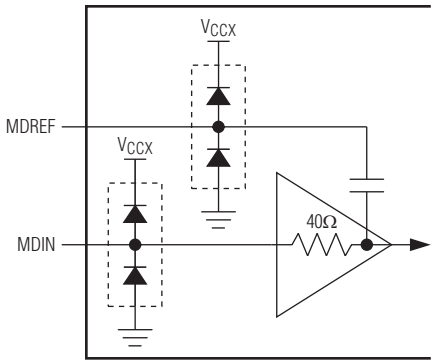
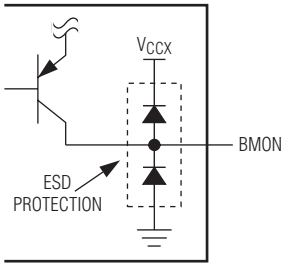
Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
3	CSEL	Chip-Select Input, CMOS. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down by a 75kΩ resistor to ground.	
4, 5	ROUT+, ROUT-	Differential Receiver Data Output, CML. This output has 50Ω terminations to V_{CC}. Polarity is set by the RX_POL bit.	
6	SCL	Serial-Clock Input, CMOS. Internally pulled down by a 75kΩ resistor to ground.	
7	V_{CCD}	Power Supply. Provides supply voltage to the digital block.	—
8	SDA	Serial-Data Bidirectional Input, CMOS. Open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ to 10kΩ pullup to meet 3-wire timing specifications.	

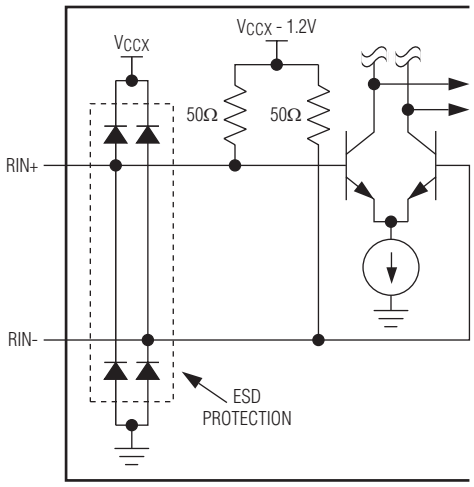
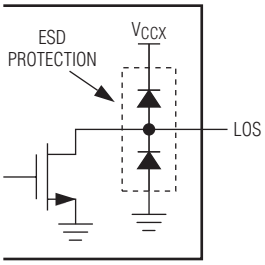
Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
9, 10	BEN+/ BEN-	Burst-Enable Input. This differential 13kΩ input is compatible with LVDS, PECL, and CML input levels. The polarity is set by the BEN_POL bit.	
11, 12	TIN+/TIN-	Differential Transmitter Data Input. This differential 13kΩ input is compatible with LVDS, PECL, and CML input levels. The polarity is set by the TX_POL bit.	
13	LPD	Laser Power Detector Output. The polarity of the LPD signal is controlled by the LPD_POL bit. The output impedance is approximately 150Ω.	

Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
14	TOUT	Noninverting Laser Diode Modulation and Bias Current Output. Connect to the cathode of the laser diode. A differential 1 at TIN± results in current flow at the laser.	
15	IOUT	Inverting Laser Diode Modulation and Bias Current Output. Connect to the anode of the laser diode.	
16	V_{CCTO}	Power-Supply Connection. Provides supply voltage to the transmitter output.	—
17	MDREF	Monitor Diode Reference. Connect this to a filtered V_{CCTO}.	
18	MDIN	Monitor Diode Input. Connect this pin to the anode of the monitor diode. MDIN can be left open for open-loop operation. Keep capacitance minimized at this pin.	
19	BMON	Bias Current/Laser Power Monitor Output. Current out of this pin develops a ground-referenced voltage across external resistor(s) that is proportional to the laser bias current or MDIN pin current. The current sourced by this pin is typically 1/72 the laser bias current.	
20, 23	V_{CCX}	Transceiver Power Supply. Provides supply voltage to the receiver and transmitter cores.	—

Pin Description (continued)

PIN	NAME	OUTPUT FUNCTION	EQUIVALENT CIRCUIT
21, 22	RIN-, RIN+	Differential Receiver Data Input. Contains 100Ω differential termination on-chip. Connect these inputs to the TIA outputs using 1µF coupling capacitors.	
24	LOS	Receiver Loss-of-Signal (LOS) Output, Open Drain. This output goes to a logic-high when the level of the input signal drops below the SET_LOS register threshold. Polarity is set by LOS_POL. All LOS circuitry can be disabled by setting LOS_EN = 0. The LOS output is pulled up to host V_{CC} with a 4.7kΩ to 10kΩ resistor.	
—	EP	Exposed Pad. Ground. This is the only electrical connection to ground on the MAX3710 and must be soldered to circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package and Thermal Considerations* section).	—

125Mbps to 2.5Gbps, Integrated Limiting Amplifier/ Burst Mode Laser Driver with Dual-Loop Power Control

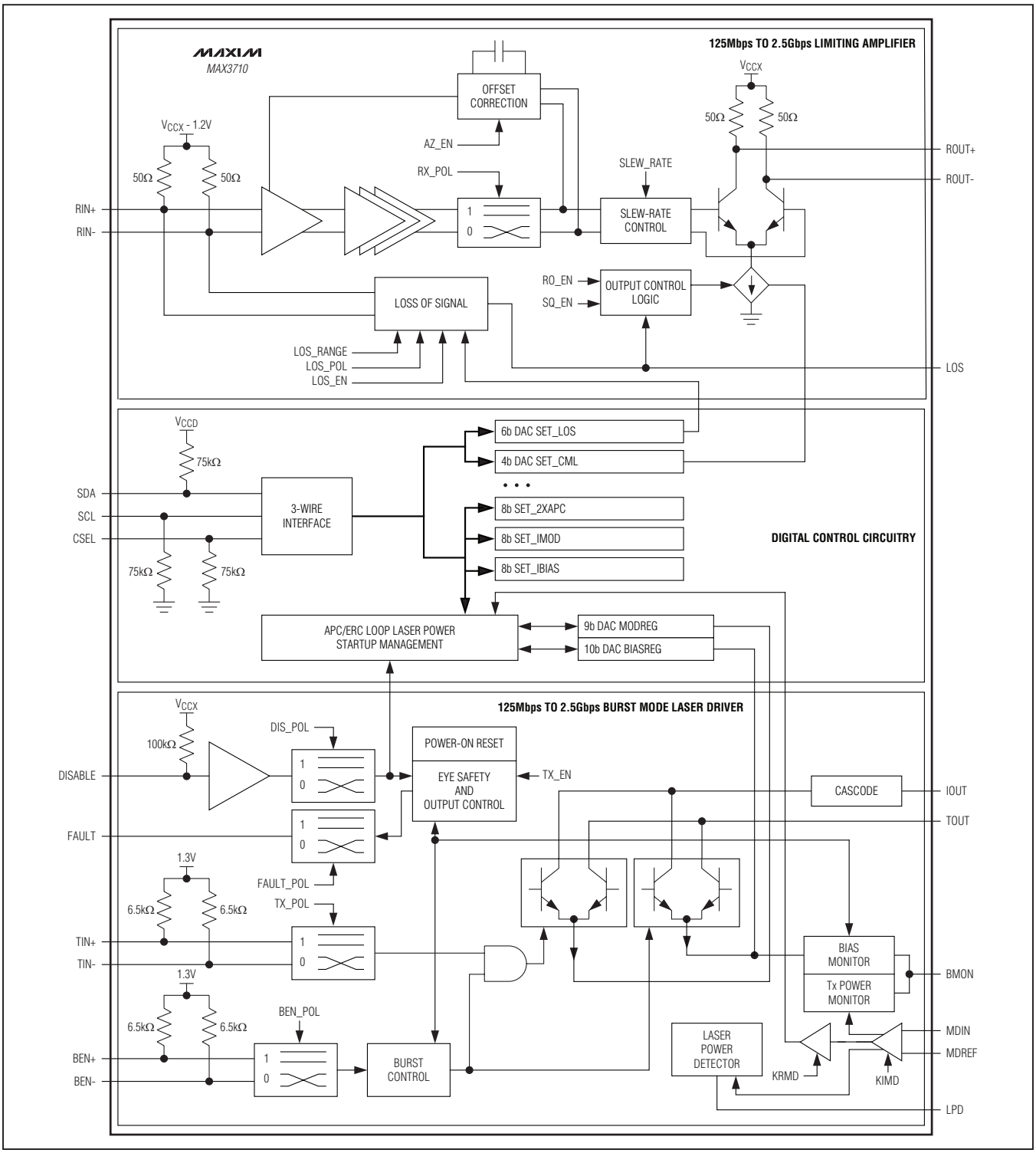


Figure 2. Functional Diagram

Detailed Description

The MAX3710 combines a high-gain limiting amplifier with a burst-mode laser driver. The limiting amplifier includes offset cancellation and programmable signal-detect threshold. The laser driver includes average power and extinction ratio control, average or peak laser power measurement capability, overcurrent limiting, laser power detector, bias current/MD current monitor, and fault detection. A 3-wire serial control interface enables an external controller to set all parameters necessary for operation of the limiting amplifier and laser diode driver. The interface enables real-time laser bias and/or modulation current control and provides operation and status readouts.

The features and performance are specifically designed to be compatible with low-cost microcontrollers and provide complete EPON and GPON PMD functionality, including laser fault detection, diagnostics, and average power control with extinction ratio control. The MAX3710 includes all the logic required for laser protection, control loop operation, and monitor diode current measurement.

1.25Mbps to 2.5Gbps Limiting Amplifier Block Description

Continuous Mode Limiter

The limiting amplifier consists of a multistage amplifier, offset-correction circuit, output buffer, and loss-of-signal/signal-detect circuitry. Its low noise (1.3mV$_{P-P}$ typical sensitivity) and high gain can provide 0.3dB to 0.5dB of additional sensitivity in typical 2.5Gbps GPON applications. Programmable configuration options (LOS threshold, LOS polarity, CML output with adjustable level, slew rate, and output polarity) enhance layout flexibility and triplexer/ROSA compatibility.

High-Speed Input Signal Path

The inputs, RIN±, have an internal 100Ω differential termination and should be AC-coupled to the transimpedance amplifier.

Offset Cancellation

The limiting amplifier has approximately 68dB of gain, which makes it very susceptible to both DC offsets and pulse-width distortion in the signal from the transimpedance amplifier. A low-frequency feedback loop provides offset cancellation to compensate for these effects; the nominal small-signal low-frequency cutoff of the offset cancellation loop is 10kHz when 1µF AC-coupling capacitors are used.

Loss-of-Signal Circuitry (LOS)

This block detects amplitude of the incoming signal and compares it against a preset threshold, which is controlled by SET_LOS[5:0]. The programming range of the LOS assert level is 3.8mV$_{P-P}$ to 138mV$_{P-P}$.

Changing the LOS threshold during operation (i.e., without executing a reset) does not cause a glitch or incorrect LOS output. The detector has 2dB of hysteresis to control chatter at the LOS output. The LOS output polarity is controlled by the LOS_POL bit. The entire LOS circuit block can be disabled by setting LOS_EN = 0.

Output Drivers

The CML data outputs, ROUT±, are terminated with 50Ω to V_{CCX}. The differential output level can be programmed through the SET_CML[3:0] register between 410mV$_{P-P}$ and 1000mV$_{P-P}$, and the output polarity can be inverted. Serial commands can also be used to manually disable the output (to its common-mode voltage, i.e., near zero differential voltage DC), or cause the limiting amp to automatically disable the output under an LOS condition (squelch through the SQ_EN bit). The output slew rate can be optimized for either 2.5Gbps or low data-rate operation by setting the SLEW_RATE bit.

1.25Mbps to 2.5Gbps Laser Driver Block Description

The burst mode laser driver consists of TIN±/BEN± differential high-speed input buffers, TIN±/BEN± polarity switch buffers, DISABLE TTL/CMOS input buffer, combined laser modulator and bias generator, monitor diode current input buffer with calibration features, digital laser power detector (LPD) with CMOS output buffer, analog bias current monitor, analog transmit power monitor, APC and ERC loop circuitry, eye-safety monitoring, and FAULT output buffer.

Differential High-Speed Input Buffers

The high-speed laser driver data inputs, BEN± and TIN±, are compatible with LVDS, LVPECL, and CML outputs. BEN can be driven single-ended (Figure 3). For burst mode operation TIN± should be DC-coupled with external differential termination of 100Ω placed close to the input pins. The BEN± and TIN± inputs can also be DC-coupled to LVDS outputs using a 100Ω differential termination. The polarity of TIN± and BEN± can be inverted by the TX_POL and BEN_POL bits, respectively.

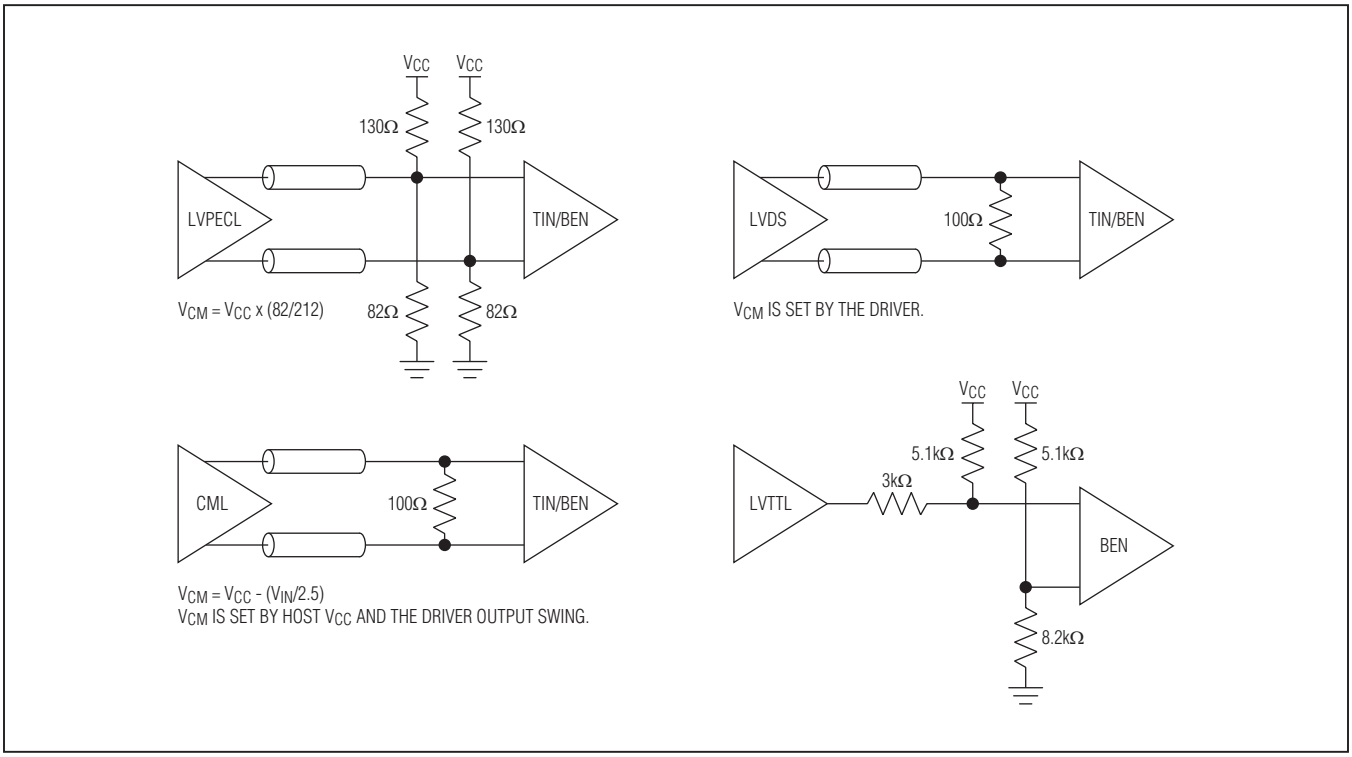


Figure 3. Interfacing to the MAX3710 TIN± and BEN± Inputs

Laser Modulator and Bias Generator

The laser modulator provides DC coupled current into the cathode of the laser diode at the TOUT pin. The modulation current amplitude is set by MODREG[8:0]. The modulation current DAC guarantees modulation amplitudes up to 85mA.

The laser bias current output stage is similar to the modulation current output stage because the burst mode operation requires fast switching on/off times. The amplitude of the laser bias current is controlled by BIASREG[9:0]. The laser bias current DAC guarantees values up to 70mA.

During burst-on the modulation and bias currents are summed at the TOUT pin. During burst-off the bias and modulation currents are switched to the IOUT pin. Note that TOUT and IOUT are not differential in the general sense; TOUT must be connected to the laser diode cathode and the cascoded IOUT pin must be connected to the laser diode anode.

Monitor Diode Current Input Buffer

The input stage covers a large input signal range by having adjustable gain settings. The KIMD[1:0] bits set the current gain. This is followed by an adjustable transimpedance amplifier (TIA). The TIA gain settings are programmed by the KRMD[2:0] bits. The input has high bandwidth, allowing the MAX3710 to monitor not only average laser power, but also extinction ratio. In addition, laser power detection (LPD) for rogue ONUs is made possible by the MDIN input.

MDIN current is mirrored at the BMON output and selected by setting MDMON_EN = 1 and MON_SEL = 1. In this mode, the current sourced by BMON is scaled by K_{IMD}, where the value K_{IMD} is set by the KIMD[1:0] bits. The high bandwidth of the MDIN–BMON path enables tuning of the laser-to-monitor diode external components to minimize crosstalk and to optimize filtering on the MDIN signal.

Digital Laser Power Detector

This detector compares the monitor diode current value with a preset threshold and generates a CMOS logic level output at the LPD pin. The threshold level scales with gain settings at MDIN through KIMD[1:0].

There are two basic modes for reporting the results of LPD, which performs light detection during the off_state: Off_state is defined as a disable of the device by DISABLE, TX_EN, MOD_EN, BIAS_EN, BEN, or a fault.

Mode 1, LPD_MODE = 1:

LPD reports any light burst (when BEN = 1, the LPD output is high).

Mode 2, LPD_MODE = 0:

LPD reports light bursts during a laser off state only (when BEN = 1, the LPD output is low).

Polarity of the LPD output is selectable by setting the LPD_POL bit. The mode of operation is controlled by the LPD_MODE bit.

Use the LPD_TH[2:0] bits to set the LPD threshold in steps of 12.5µA/K_{IMD}, where the value K_{IMD} is set by the KIMD[1:0] bits. If the monitor diode exhibits a "slow-tail" behavior where the monitor diode current slowly decays after light disappears, the LPD threshold may need to be adjusted high enough so the LPD output does not produce an unintentional pulse directly after BEN transitions low.

Average Power and Extinction Ratio Control Circuitry

The MAX3710 includes full closed-loop control of laser average power and extinction ratio. Figure 4 shows the dual power control, or DPC, loop. Operation is as follows:

The monitor diode (MD) is connected to the MDIN pin, and the MD current is amplified by a gain set by the KIMD[1:0] and KRMD[2:0] bits.

The output of the MDIN input buffer is sent through a programmable filter, controlled by the CPRG[4:0], MDLBW[1:0], and MDRNG bits.

The filter output is fed to a 10MS/s analog-to-digital converter (ADC), where the peak values of both the high current and the low current (proportional to the high power and low power of the laser) are determined and converted to 16-bit digital words, MD0REGH[7:0] and MD0REGL[7:0], and MD1REGH[7:0] and MD1REGL[7:0]. The values are MD0[15:8] = MD0REGH[7:0], MD0[7:0] = MD0REGL[7:0], MD1[15:8] = MD1REGH[7:0], MD1[7:0] = MD1REGL[7:0]. The number of averages used to generate MD1[15:0] and MD0[15:0] is determined by MDAVG_CNT.

To monitor average transmitter power, use the following equation:

$$P_{AVG} = 0.00292 \times \frac{\frac{MD0[15:0]}{8} + MD1[15:0]}{512 \times KIMD \times KRMD \times K_{MD}}$$

where K_{MD} is the laser diode to monitor diode gain in A/W.

For example, if K_{MD} = 0.1, KIMD[1:0] = 00 (gain = 1), KRMD[2:0] = 000 (gain = 2800Ω), MD0[15:0] = 35750d, and MD1[15:0] = 44680d, the calculated P_{AVG} = 1mW.

From the ADC to the TOUT/IOUT outputs, operation is dictated by the state of the BEN± pins. The ADC only samples during the burst-on time and is frozen during burst-off. Therefore, MD1 and MD0 values are held static during burst-off. The TX_EN bit must also be high for the ADC to sample.

The delay from the rising edge of BEN to the first sample is selected by the MDON_DLY[1:0] bits in 100ns steps. For MDON_DLY[1:0] = 00, the minimum burst-on time for DPC updating is approximately 60ns (typ), and it can be adjusted up to 360ns by setting MDON_DLY[1:0] = 11.

Returning to the main forward path of the DPC, MD1[15:0] and MD0[15:0] are used to compute the average power and extinction ratio at the MDIN input in the "COMPUTATION" block (Figure 4). These values are compared with the target values of average power (SET_2XAPC[7:0]) and extinction ratio (ERSET[3:0] bits). If the error magnitude is greater than the value set by THRSHLD, then the output registers BIASREG[9:0] and MODREG[8:0] are updated with the error value. The update value is limited by the BIASINC[3:0] and MODINC[3:0] registers.

The IBIASMAX[7:0] and IMODMAX[7:0] values are used to limit BIASREG[9:2] and MODREG[8:1]. Note only the upper 8 bits of the output current registers are compared.

The EOB_EN bit conditions updating of the output registers.

If EOB_EN = 1, the output registers are only updated once immediately following the falling edge of BEN. However, the DPC must acquire the entire set of averages, N, set by MDAVG_CNT, before changing BIASREG[9:0] and MODREG[8:0]. The averaging process can stretch over multiple bursts and freezes between bursts. Once the required number of averages has been satisfied, the ADC outputs freeze until BEN falls and BIASREG[9:0] and MODREG[8:0] can be updated.

If EOB_EN = 0, the output registers are updated continuously while BEN = 1.

The "CONTROL" block (Figure 4) controls the updating and startup behavior of the entire DPC.

The bits APC_EN and DPC_EN control the operating mode of the DPC:

Full DPC Mode. DPC_EN = 1, APC_EN = X: BIASREG[9:0] and MODREG[8:0] are controlled based on the SET_2XAPC[7:0] register and ERSET[3:0] targets.

APC Only Mode. DPC_EN = 0, APC_EN = 1: The BIASREG[9:0] register is controlled based on the SET_2XAPC[7:0] target and MODREG[8:0] is controlled directly through SET_IMOD[7:0]. MODINC[4:0] is used to adjust the lower bits of MODREG[8:0] using two's complement to increase or decrease its value.

Open Loop Mode. DPC_EN = 0, APC_EN = 0: The BIASREG[9:2] register is controlled directly by SET_IBIAS[7:0] and MODREG[8:1] is controlled directly by SET_IMOD[7:0]. Registers BIASINC[4:0] and MODINC[4:0] are used to adjust the lower bits of BIASREG[9:0] and MODREG[8:0] using two's complement.

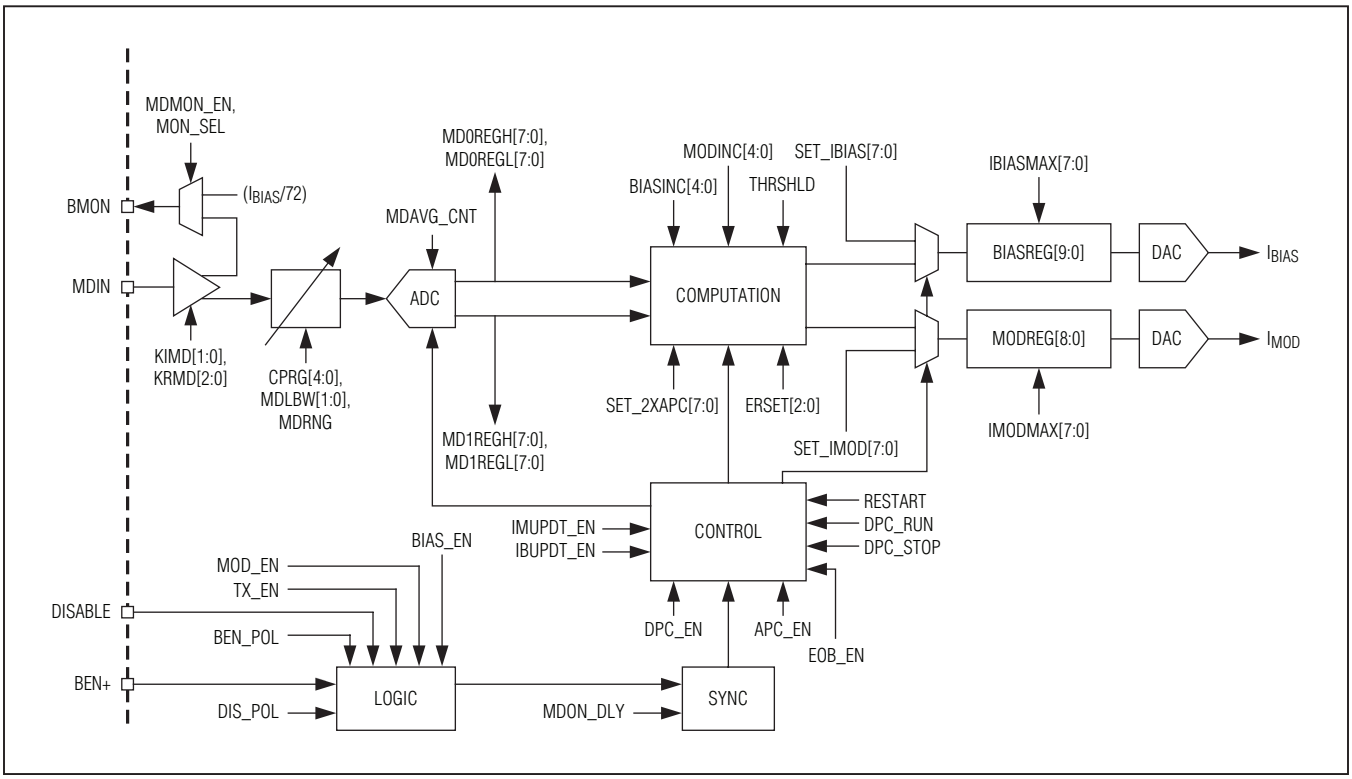


Figure 4. DPC Loop Diagram

The DPC acquisition mode is controlled by several bits: RESTART, IBUPDT_EN, IMUPDT_EN, DPC_RUN, and DPC_STOP.

Anytime the DPC FSM is reset (through an unmasked fault or if RESTART is issued), BIASREG[9:2] and MODREG[8:1] are optionally reinitialized to SET_IBIAS[7:0] and SET_IMOD[7:0], respectively. Reinitialization is accomplished by setting bit IBUPDT_EN (for BIASREG[9:0]) or IMUPDT_EN (for MODREG[8:0]) to 1. This allows accurate output current in the first burst.

The bit RESTART resets the state machine, sets DPC_RUN = 1, and reinitializes BIASREG[9:2] and MODREG[8:1], subject to IBUPDT_EN and IMUPDT_EN, respectively. The state machine then moves to a coarse acquisition mode, a binary-search mode, and finally a steady-state mode where averaging begins. In steady-state mode, the SSMODE status bit is set high and RESTART is reset.

In coarse acquisition mode, the BIASREG[9:0] step size is 2 x BIASINC[3:0] and the MODREG[8:0] step size is 2 x MODINC[3:0]. An update is made every 200ns.

The bit DPC_STOP prevents the DPC from updating the output registers, while DPC_RUN allows the DPC to operate. If a 1 is written to DPC_STOP, DPC_RUN is reset to 0. If a 1 is written to DPC_RUN, DPC_STOP is reset to 0. Writing a 0 to either bit has no affect. If the state machine is not in steady state, setting DPC_STOP = 1 forces it into steady state. Note that the loop no longer updates BIASREG[9:0] and MODREG[8:0] since DPC_STOP is high.

Power-On Reset (POR)

A power-on-reset circuit provides proper startup sequencing and ensures that the laser is off while the supply voltage is ramping or below a specified threshold (~2.55V). The serial interface can also be used to command a manual reset at any time by setting SOFTRESET = 1, which is identical to a power-on reset. When using SOFTRESET, the MAX3710 transmitter must be disabled, either by the DISABLE pin or by setting TX_EN = 0. Either power-on or soft reset requires approximately 50µs to complete. The recommended POR procedure is as follows:

- POR sets all registers to their defaults.
- Controller initiates 3-wire communication after POR with MAX3710 by repeatedly reading out the LVFLAG (V_{CCTO} flag) bit until the 1-to-0 transition occurs (V_{CCTO} is needed for the Tx output and DPC only).
- Controller writes/initializes all registers (see the DPC startup procedure).

BMON Functions

The BMON pin can be selected to either provide a monitor of the laser bias current or the MDIN pin current. It sources 1/72 of the laser bias current when the MON_SEL bit is 0 (default). A resistor to ground sets the full-scale voltage range and can be monitored by an external ADC. When BMON is set to replicate the MDIN current (MON_SEL = 1 and MDMON_EN = 1), the pin sources a KIMD[1:0]-scaled MD current.

Eye Safety Circuitry

The eye safety circuitry consists of fault detection, warning flags, faults, and fault masking. Certain pins of the device are monitored for conditions that indicate non-standard operation (Figure 5).

Less critical conditions are flagged by a warning flag. These conditions trigger a bit to go high and remain high until the condition is removed **and** the bit is read. These do not cause the device to disable itself. The Tx warning flags are located in the TXSTAT1[7:0] register and are LPDFLAG and BENLOS.

Critical conditions create a fault. A fault disables the transmitter's bias and modulation current DACs and the Tx circuitry remains in a fault state until cleared by toggling DISABLE, cycling power, or writing 68h to MODECTRL[7:0]. Faults are maskable, meaning that by setting the mask bits high, specific faults do not cause the device to become disabled. Faults are indicated by the TXINLOS, FMD, FIOUT, LVFLAG, and FTOUT bits. Note that a fault at MDIN (indicated by FMD) can be masked, but still causes the DPC to stop operation, regardless of the mask. In this condition, the DPC must be started to resume operation (set DPC_RUN = 1 or RESTART = 1).

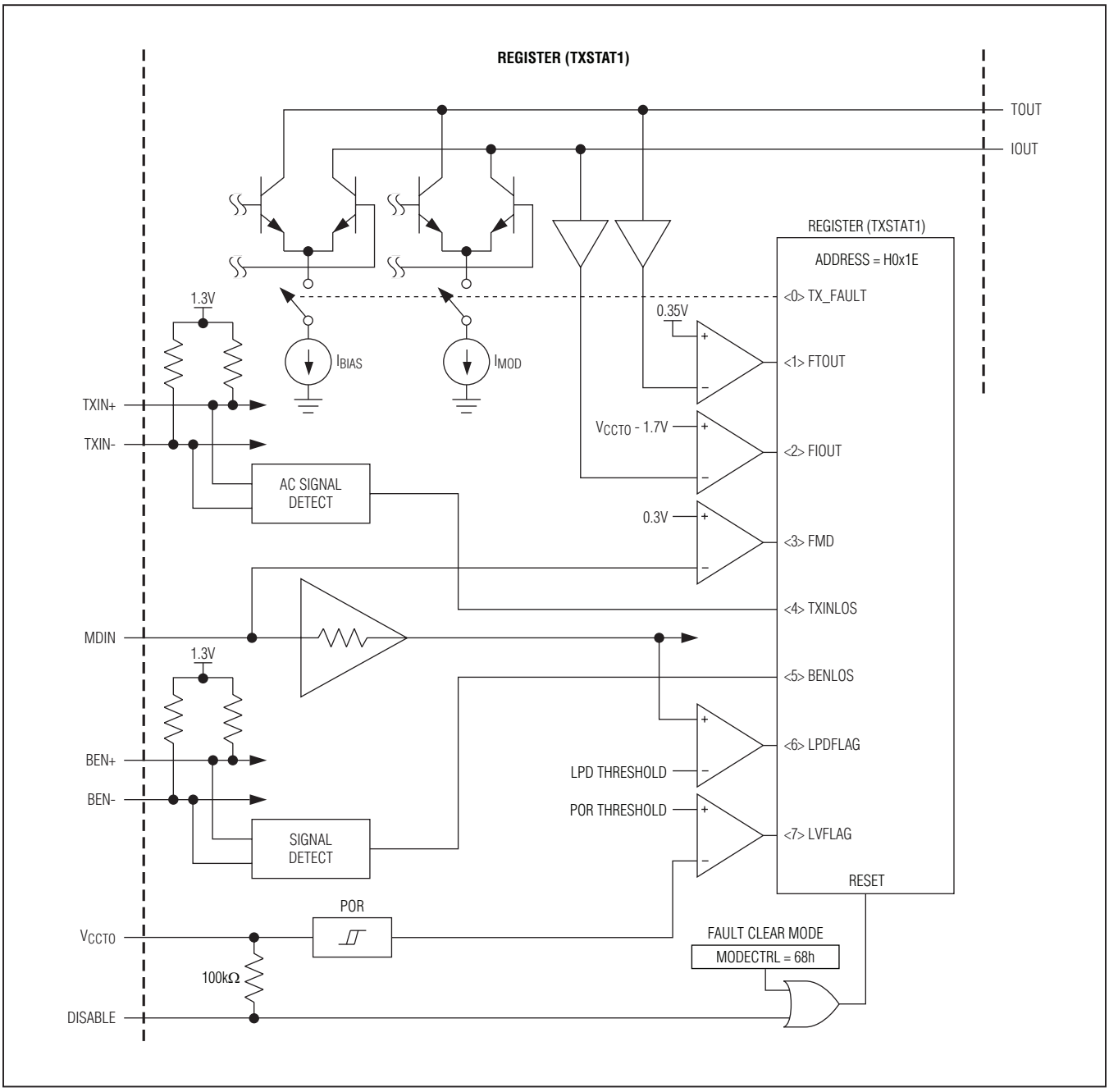


Figure 5. Eye Safety Circuitry

Table 1. Circuit Response to Single-Point Faults

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
1	FAULT	No effect, but open-drain nMOS output life can be stressed (Note 1)	No effect (Note 1)	No effect (Note 1)
2	DISABLE	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0	No effect if DIS_POL = 1 (default) Tx output is off if DIS_POL = 0 (Note 1)	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0
3	CSEL	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
4	ROUT+	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
5	ROUT-	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
6	SCL	No effect (Note 1)	No effect (Note 1)	No effect (Note 1)
7	V_{CCD}	No effect	POR on	POR on
8	SDA	No effect, but open-drain nMOS output life can be stressed (Note 1)	No effect (Note 1)	No effect (Note 1)
9	BEN+	No effect	No effect	No effect
10	BEN-	No effect	No effect	No effect
11	TIN+	TXINLOS flag asserted	TXINLOS flag is asserted	No effect depending on TIN- amplitude
12	TIN-	TXINLOS flag asserted	TXINLOS flag is asserted	No effect depending on TIN+ amplitude
13	LPD	No effect, but output device life can be stressed	No effect, but output device life can be stressed	No effect (Note 1)
14	TOUT	Laser diode is off	FAULT asserted, laser power exceeds programmed value	FAULT asserted
15	IOUT	No effect	FAULT asserted	FAULT asserted
16	V_{CCTO}	No effect	LVFLAG flag asserted, laser diode is off	LVFLAG asserted, laser diode is off
17	MDREF	No effect	No effect	No effect
18	MDIN	Output current limited by IBIASMAX[7:0] and IMODMAX[7:0]	FMD flag asserted	Output current limited by IBIASMAX[7:0] and IMODMAX[7:0]
19	BMON	No effect	No effect (Note 1)	No effect
20	V_{CCX}	No effect	Board supply collapsed, POR on (Note 2)	No effect (Note 3)—Redundant path
21	RIN-	No effect	No effect	No effect
22	RIN+	No effect	No effect	No effect
23	V_{CCX}	No effect	Board supply collapsed, POR on (Note 2)	No effect (Note 3)—Redundant path
24	LOS	No effect, but open-drain nMOS output life can be stressed	No effect	No effect
—	EP	POR on, I/O device life can be stressed (Note 2)	No effect	POR on

Note 1: Normal—Does not affect laser power.
Note 2: Supply-shorted current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.
Note 3: Normal in functionality, but performance could be affected.
Warning: Shorted to V_{CC} or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

3-Wire Interface

The MAX3710 implements a proprietary 3-wire digital interface, and an external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. Then it generates a clock signal after the CSEL pin has been set to a logic-high. All data transfers are most significant bit (MSB) first.

Protocol

Each nonblock operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3710; the RWN bit determines if the cycle is read or write. See Table 2.

Write Mode (RWN = 0)

The master generates 16 clock cycles at SCL in total. It outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 6 shows the 3-wire interface timing.

Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 6 shows the 3-wire interface timing.

Table 2. Digital Communication Word Structure

BIT	NAME	DESCRIPTION
15:9	Address	7-Bit Internal Register Address
8	RWN	0: Write; 1: Read
7:0	Data	8-Bit Read or Write Data

Block Write Mode (RWN = 0)

The master initiates the block write mode by writing H0x12 into the MODECTRL[7:0] register. The block write mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has written into any register other than MODECTRL[7:0] and CSEL has been set to 0. The two different modes of operation are described below:

BLOCK WRITE MODE 1 (STARTS AT ADDRESS H0x01)	
Master sets CSEL to 1	
ADDR H0x00 + RWN = 0	Data H0x12
Data 1 (ADDR H0x01)	Data 2 (ADDR H0x02)
Data 3 (ADDR H0x03)	Data 4 (ADDR H0x04)
. . .	
Data 19 (ADDR H0x13)	Master sets CSEL to 0
BLOCK WRITE MODE 2 (STARTS AT ANY ADDRESS)	
Master sets CSEL to 1	
ADDR H0x00 + RWN = 0	Data H0x12
Master sets CSEL to 0	Master sets CSEL to 1
ADDR H0xN + RWN = 0	Data 1 (ADDR H0xN)
. . .	
Data i (ADDR H0xN + i - 1)	Master sets CSEL to 0

Block Read Mode (RWN = 1)

The master initiates the block read mode by accessing any register address and setting the RWN bit to 1. The block read mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has set CSEL to 0.