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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EVALUATION KIT AVAILABLE

MAXIM

2.7Gbps Dual Mux/Buffer with Loopback

MAX3783

General Description

The MAX3783 is a dual serial multiplexer (mux) and buffer with selectable line-side loopback for system interconnect and serial backplane applications up to 2.7Gbps. Each independent channel consists of a transmitter with fanout of two and a receiver with a 2:1 input mux. Selectable loopback paths support system testing.

Operating from a single 3.3V supply, this device has current-mode logic (CML) inputs and outputs, which can be AC-coupled for PECL compatibility, if desired. The IC is packaged in a compact 48-pin TQFP-EP package with exposed pad. Typical power consumption is 1.12W.

Applications

2.7Gbps Serial Communications

System Interconnect

Serial Backplane

Fail-Over and Protection Switching

Features

♦ **Provides Redundant Serial I/O**

♦ **11ps Deterministic Jitter**

♦ **Selectable Loopback**

♦ **On-Chip 50Ω Termination Resistors**

♦ **3.3V Power Supply**

♦ **Two-Port Integration**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3783UCM	0°C to +85°C	48 TQFP-EP*
MAX3783UCM+	0°C to +85°C	48 TQFP-EP*

*EP = Exposed pad.
+ Denotes a lead-free package.
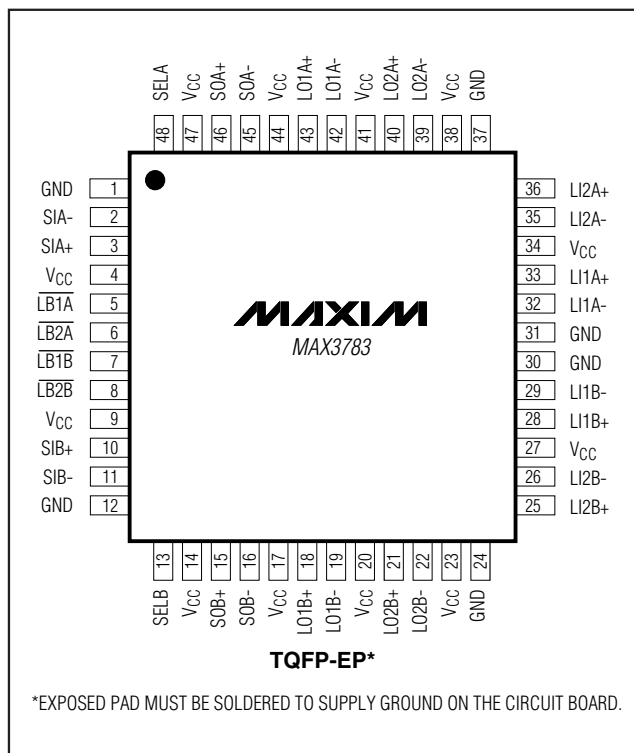
Typical Application Circuit appears at end of data sheet.

Pin Configuration

TQFP-EP*

*EXPOSED PAD MUST BE SOLDERED TO SUPPLY GROUND ON THE CIRCUIT BOARD.

MAXIM _____ *Maxim Integrated Products* 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2.7Gbps Dual Mux/Buffer with Loopback

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ....-0.5V to 4.0V
Continuous Current at Serial Outputs..............................±36mA
Voltage at SEL_, $\overline{LB}$_ Pins ....-0.5V to (V_{CC} + 0.5V)
Common-Mode Input Voltage (SI_, LI_).....-0.5V to (V_{CC} + 0.5V)
Differential Input Voltage (SI_, LI_) (Note 1) ....±2.8V

Continuous Power Dissipation (T_A = +85°C)
   48-Pin TQFP-EP (derate 27mW/°C above +85°C) 1.76W
Storage Ambient Temperature ....-55°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: The sum of the common-mode voltage and differential voltage on any input pin must be within -0.5V to (V_{CC} + 0.5V).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, serial data rate = 2.75Gbps, T_A = 0°C to +85°C. Typical values at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Data Rate			2.75	3.125		Gbps
Power Dissipation		AC-coupled inputs, outputs		1.12	1.68	W
Supply Current	I_{CC}			340	466	mA
CML Differential Output Voltage	V_{OD}	R_L = 50Ω to V_{CC}, or 100Ω differential (Note 2)	1200	1500	2200	mVp-p
CML Differential Input Voltage	V_{ID}		200	1600	2200	mVp-p
CML Output Impedance	R_{OUT}	Single ended	42.5	50	57.5	Ω
CML Input Impedance	R_{IN}	Differential	85	100	116	Ω
Random Jitter		(Note 3)		1	2	ps$_{RMS}$
Deterministic Jitter		(Notes 3, 4, 5)		11	25	ps$_{p-p}$
CML Output Edge Speed (20% to 80%)	t_R, t_F	2.5Gbps input (Note 6)		70	135	ps
		1.25Gbps input (Note 3)		80	200	
Propagation Delay		LI_ to SO_, SI_ to LO_, LI_ to LO_ (Note 3)		340	500	ps
Multiplexer Switch Time		SEL_ or $\overline{LB}$_ to valid output		9		ns
TTL Input Current High		V_{IH} = +2.0V to (V_{CC} +0.3V)			180	µA
TTL Input Current Low		V_{IL} = -0.3V to +0.8V			440	µA

Note 2: Tested using a repeating 1010 pattern at 500Mbps.
Note 3: AC specifications are guaranteed by design and characterization.
Note 4: Deterministic jitter is measured with a repeating K28.5 pattern.
Note 5: With the peak-to-peak input swing on the selected (transmitted) CML input equal to or greater than that on the nonselected inputs.
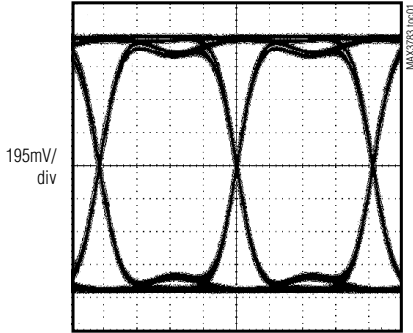**Note 6:** AC specifications are guaranteed by test.

MAXIM

2.7Gbps Dual Mux/Buffer with Loopback

_____*Typical Operating Characteristics*

(V$_{CC}$ = 3.3V, T$_A$ = +25°C, unless otherwise noted.)

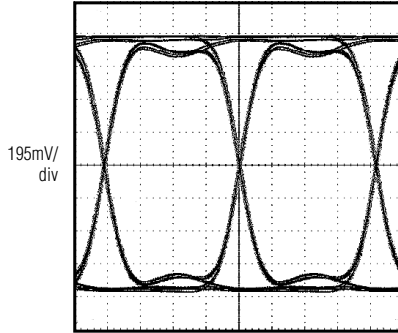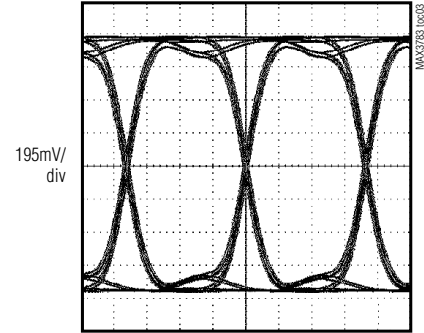**ELECTRICAL EYE DIAGRAM**
2.75 Gbps, 2^{23} - 1 PRBS PATTERN

195mV/div

88ps/div

ELECTRICAL EYE DIAGRAM
2.75 Gbps, K28.5 PATTERN

195mV/div

88ps/div

ELECTRICAL EYE DIAGRAM
3.125 Gbps, K28.5 PATTERN

195mV/div

88ps/div

SUPPLY CURRENT vs. TEMPERATURE
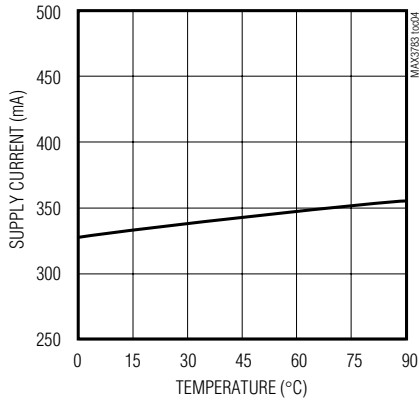
CML DIFFERENTIAL OUTPUT VOLTAGE
vs. CML DIFFERENTIAL INPUT VOLTAGE

MEASURED USING 1010 PATTERN, 500Mbps
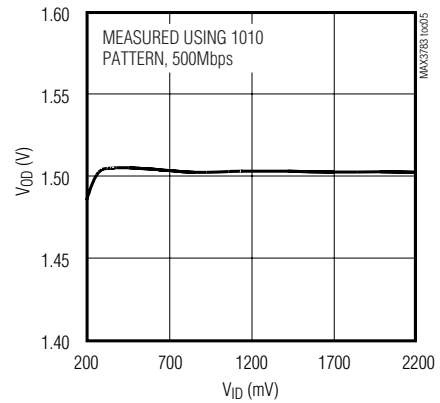
DETERMINISTIC JITTER vs. CML
DIFFERENTIAL INPUT VOLTAGE

3.125Gbps

2.75Gbps

MULITPLEXER SWITCH TIME

LO2A+

$\overline{LB2A}$
LO2A-

9ns

10ns

10ns/div

MAXIM _____ 3
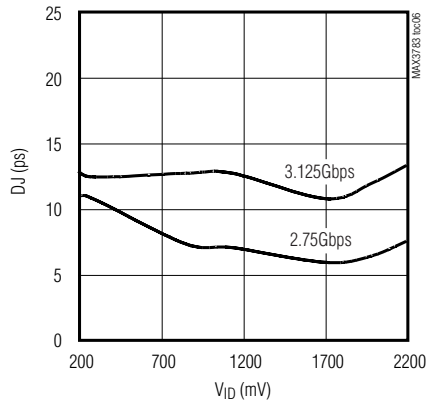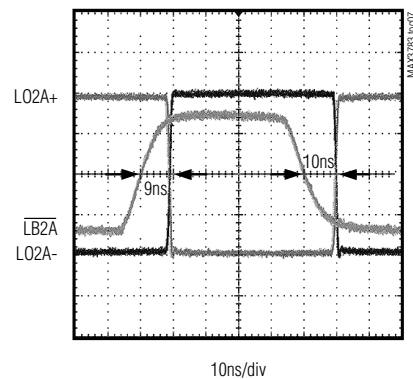
2.7Gbps Dual Mux/Buffer with Loopback

PIN	NAME	FUNCTION
1, 12, 24, 30, 31, 37	GND	Supply Ground
2	SIA-	Serial Input A Negative, CML
3	SIA+	Serial Input A Positive, CML
4, 9, 14, 17, 20, 23, 27, 34, 38, 41, 44, 47	V_{CC}	+3.3V Supply
5	$\overline{\text{LB1A}}$	Line Out 1A Loopback Mode Select. TTL low selects loopback.
6	$\overline{\text{LB2A}}$	Line Out 2A Loopback Mode Select. TTL low selects loopback.
7	$\overline{\text{LB1B}}$	Line Out 1B Loopback Mode Select. TTL low selects loopback.
8	$\overline{\text{LB2B}}$	Line Out 2B Loopback Mode Select. TTL low selects loopback.
10	SIB+	Serial Input B Positive, CML
11	SIB-	Serial Input B Negative, CML
13	SELB	Serial Output B Input Select, TTL
15	SOB+	Serial Output B Positive, CML
16	SOB-	Serial Output B Negative, CML
18	LO1B+	Line Out 1B Positive, CML
19	LO1B-	Line Out 1B Negative, CML
21	LO2B+	Line Out 2B Positive, CML
22	LO2B-	Line Out 2B Negative, CML
25	LI2B+	Line In 2B Positive, CML
26	LI2B-	Line In 2B Negative, CML
28	LI1B+	Line In 1B Positive, CML
29	LI1B-	Line In 1B Negative, CML
32	LI1A-	Line In 1A Negative, CML
33	LI1A+	Line In 1A Positive, CML
35	LI2A-	Line In 2A Negative, CML
36	LI2A+	Line In 2A Positive, CML
39	LO2A-	Line Out 2A Negative, CML
40	LO2A+	Line Out 2A Positive, CML
42	LO1A-	Line Out 1A Negative, CML
43	LO1A+	Line Out 1A Positive, CML
45	SOA-	Serial Output A Negative, CML
46	SOA+	Serial Output A Positive, CML
48	SELA	Serial Out A Input Select, TTL
EP	Exposed Pad	Ground. Must be soldered to the circuit board for proper thermal and electrical performance (see the *Exposed-Pad (EP) Package* section).

MAX3783

2.7Gbps Dual Mux/Buffer with Loopback

Functional Diagram
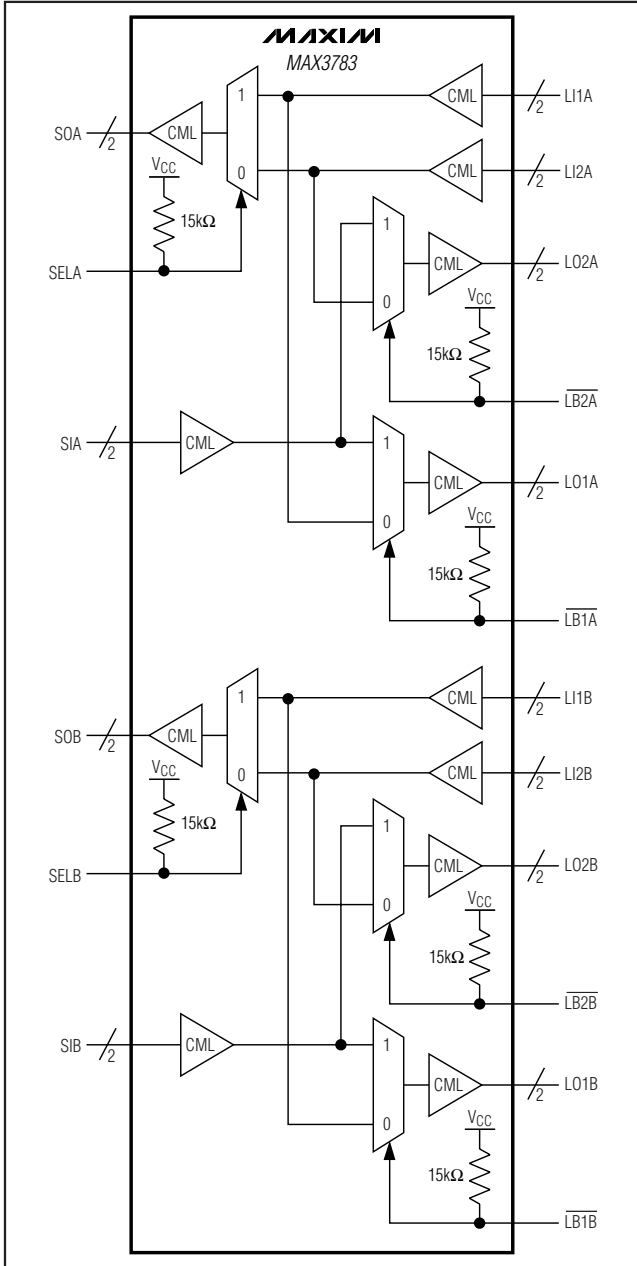
Detailed Description

The MAX3783 is a 2.7Gbps dual serial mux/buffer with selectable line-side loopback for system test. Each half of the MAX3783 provides a transmitter with a fanout of two and a receiver with a 2:1 mux, as shown in the functional diagram.

Input Stages

The input amplifiers accept CML or AC-coupled PECL signals and each input has an on-chip 100Ω differential impedance for optimal termination, as shown in Figure 1.
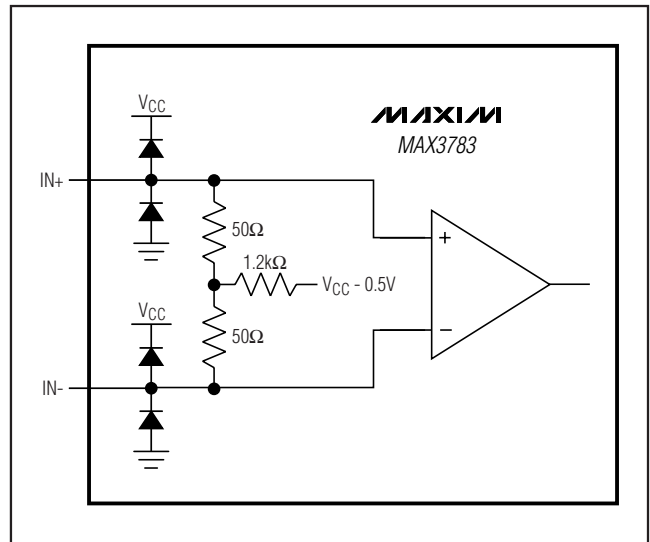

Figure 1. Input Structure

Control Lines

TTL-compatible control lines are provided to select the MAX3783's operating mode (Table 1). SELA and SELB set the mux for channels A and B, respectively, to select LI1_ or LI2_ to connect to the SO_ output. $\overline{LB1A}$, $\overline{LB1B}$, $\overline{LB2A}$, and $\overline{LB2B}$ enable loopback mode for each of the four LO_ outputs. All control lines are internally pulled high through 15kΩ resistors.

Table 1. Operating Modes

SEL_	SO_
0	LI2_
1	LI1_

$\overline{LB}$_	LO_
0	LI_
1	SI_

Output Buffers

The outputs are high-speed CML interfaces with 50Ω back termination, as shown in Figure 2.

Exposed-Pad (EP) Package

The exposed pad on the 48-pin TQFP-EP provides a very low thermal-resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3783 and must be soldered to the circuit board for proper thermal and electrical performance.
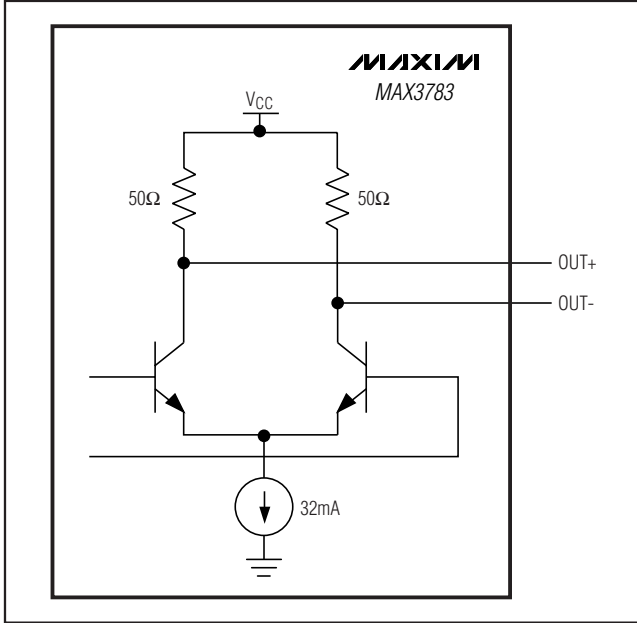
MAX3783

Figure 2. CML Output Structure

Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	DOCUMENT NO.
48 TQFP-EP	**21-0065**

Typical Application Circuit

NOTE: COUPLING CAPACITORS AND BIAS RESISTORS ARE OPTIONAL, SHOWN FOR LVPECL OPERATION. REFER TO APPLICATION NOTES HFAN-01.0 AND HFAN-01.1 REGARDING LVPECL/CML INTERFACE.

THIS SYMBOL INDICATES A CONTROLLED-IMPEDANCE TRANSMISSION LINE OF CHARACTERISTIC IMPEDANCE $Z_0 = 50\Omega$.
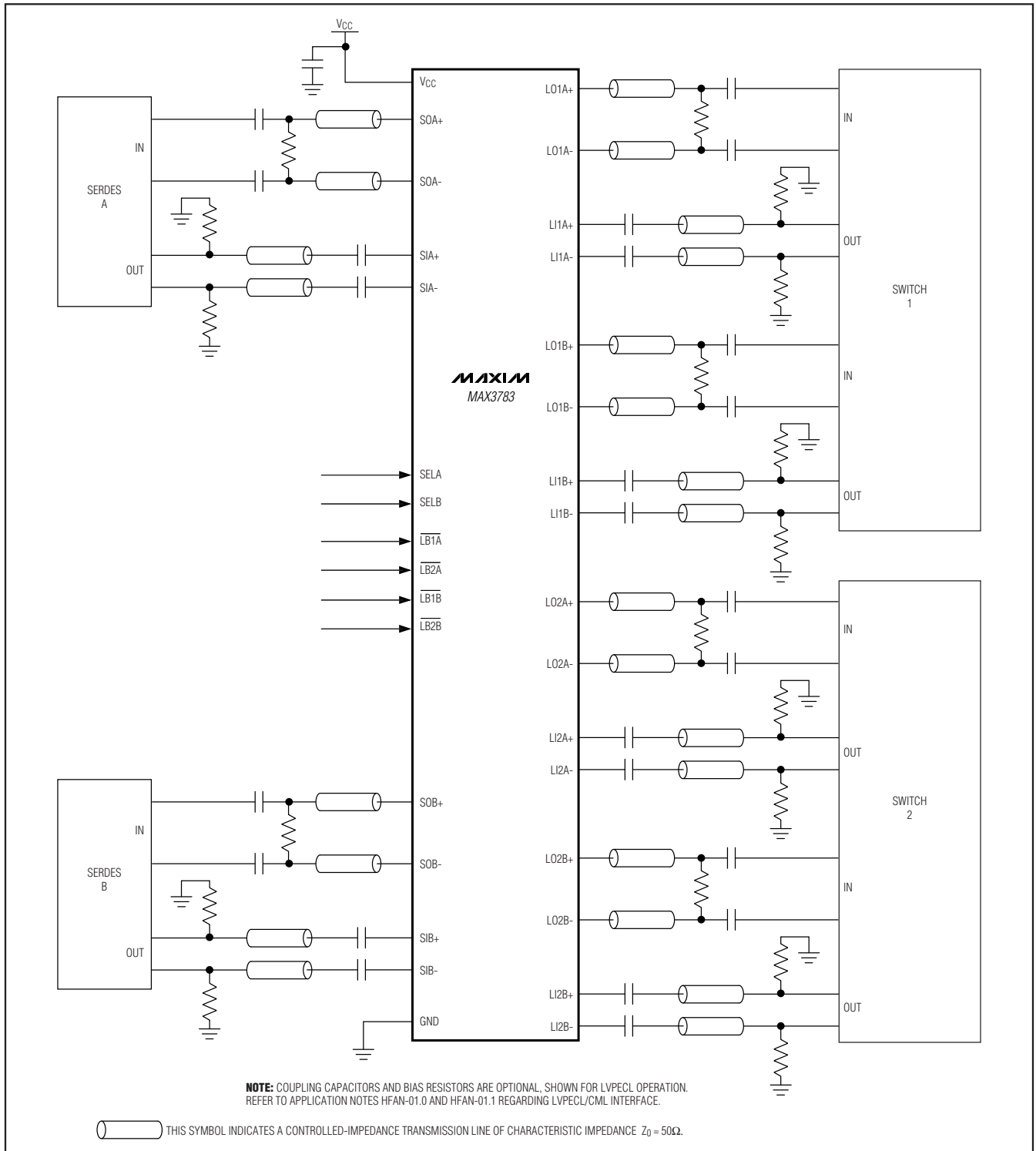
2.7Gbps Dual Mux/Buffer with Loopback

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/01	Initial release.	—
1	3/06	Added lead-free device to the Ordering Information table.	1
2	1/08	In the Electrical Characteristics table, modified Note 2 and added Note 6 for t_R, t_F; replaced package outline drawings with table.	2, 8, 9

MAX3783

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