Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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19-0406; Rev 2; 2/08

EVALUATION KIT AVAILABLE

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

General Description

The MAX3787 is a 1Gbps to 12.5Gbps equalization network that compensates for transmission medium losses encountered with FR4 and cables. The equalization network is composed entirely of passive components and functions equally well for 8b/10b or scrambled signals. It is packaged in a small 1.5mm x 1.5mm chip-scale package (UCSP™) that can be placed anywhere along the transmission medium to increase jitter margin for high-speed interconnects. Roughly the size of two 0603 components, the MAX3787 easily provides placement and routing flexibility.

At 8.5Gbps, the MAX3787 compensates for spans up to 18in of FR4 and 7m of cable. At 12.5Gbps, the MAX3787 compensates for spans up to 12in of FR4 and 3m of cable. Input and output impedance is 100Ω differential. The MAX3787 requires no power and operates over a -40°C to +125°C temperature range.

Applications

Backplane Interconnect Compensation

Cable Interconnect Compensation

Chip-to-Chip Link Extensions

Ethernet and Fibre-Channel Serial Modules

Chassis Life Extension

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

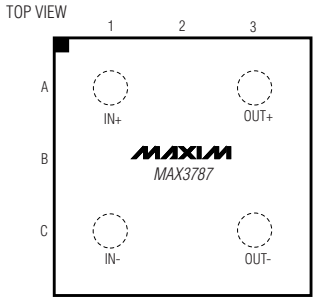
- **No Power Supply Required**
- **Small 1.5mm x 1.5mm Chip-Scale Package**
- **Passive Equalization Reduces ISI**
- **Operates from 1Gbps to 12.5Gbps**
- **Extends Board Link**
- **Extends Cable Link**
- **Coding Independent, 8b/10b or Scrambled**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3787ABL	-40°C to +125°C	4 UCSP	B9-7
MAX3787AWL+	-40°C to +125°C	4 WLP	W91B1+3

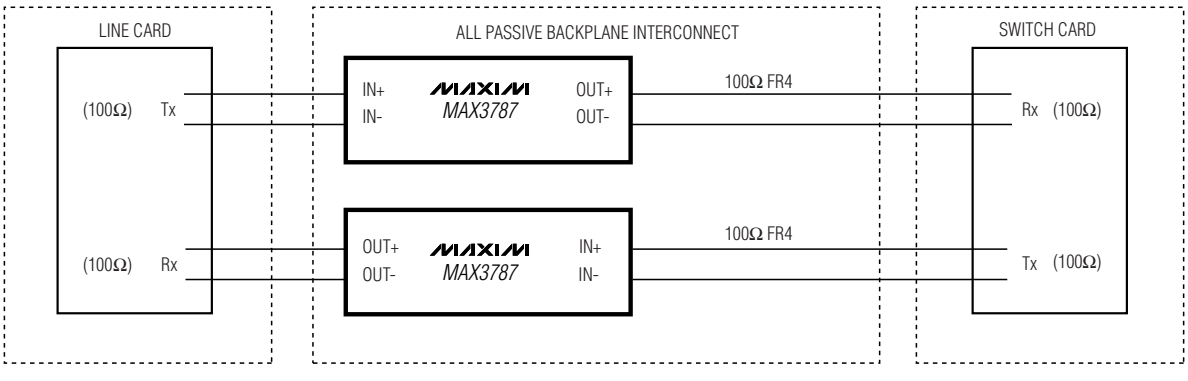
+Denotes a lead-free package.

Pin Configuration



UCSP/WLP

Typical Application Circuits



Typical Application Circuits continued at end of data sheet.

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

ABSOLUTE MAXIMUM RATINGS

Voltage between (IN+ and OUT+) or (IN- and OUT-).....+2V
Voltage between (IN+ and IN-) or (OUT+ and OUT-).....+4V
Voltage between (IN+ and OUT-) or (IN- and OUT+).....+4V

Continuous Power Dissipation (T_A = +70°C)
4-Bump UCSP (derate 3.0mW/°C above +70°C).....238mW
Operating Junction Temperature.....+150°C
Storage Ambient Temperature Range .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A		-40	+25	+125	°C
Bit Rate		NRZ data	1		12.5	Gbps
CID Tolerance		Consecutive identical digits			100	Bits

ELECTRICAL CHARACTERISTICS

(Specifications guaranteed over specified operating conditions. Typical values measured at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current				0.0		mA
Input Swing		Measured differentially at point A in Figure 1			3600	mV_{P-P}
Compensation		5GHz relative to 100MHz		6		dB
Input Impedance		Differential, Z_{LOAD} = 100Ω		100		Ω
Output Impedance		Differential, Z_{SOURCE} = 100Ω		100		Ω
Through Response		Relative to ideal load, see Figure 2 for setup		See Figure 3 for limits		
Input Return Loss		100MHz to 6GHz		15		dB
Output Return Loss		100MHz to 6GHz		15		dB
Resistance IN+ to IN- and OUT+ to OUT-		No load, high impedance on all ports	112		152	Ω
Resistance IN+ to OUT+ and IN- to OUT-		No load, high impedance on all ports	32		44	Ω
Resistance IN+ to OUT- and IN- to OUT+		No load, high impedance on all ports	112		152	Ω
DC Gain (OUT/IN)		Z_{LOAD} = 100Ω		0.5		
Residual Deterministic Jitter (Table 1, Notes 1, 2)		3.125Gbps and 6.25Gbps, 18in of 6mil microstrip FR4		0.05		UI
		8.5Gbps, 10.0Gbps, and 12.5Gbps, 18in of 6mil microstrip FR4		0.10		

Note 1: Signal applied differentially at point A as shown in Figure 1. The deterministic jitter at point B is from media-induced loss, not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

Note 2: Difference in deterministic jitter between reference points A and C in Figure 1. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 27 PRBS, 100 ones, 0, 1, 0, 1.

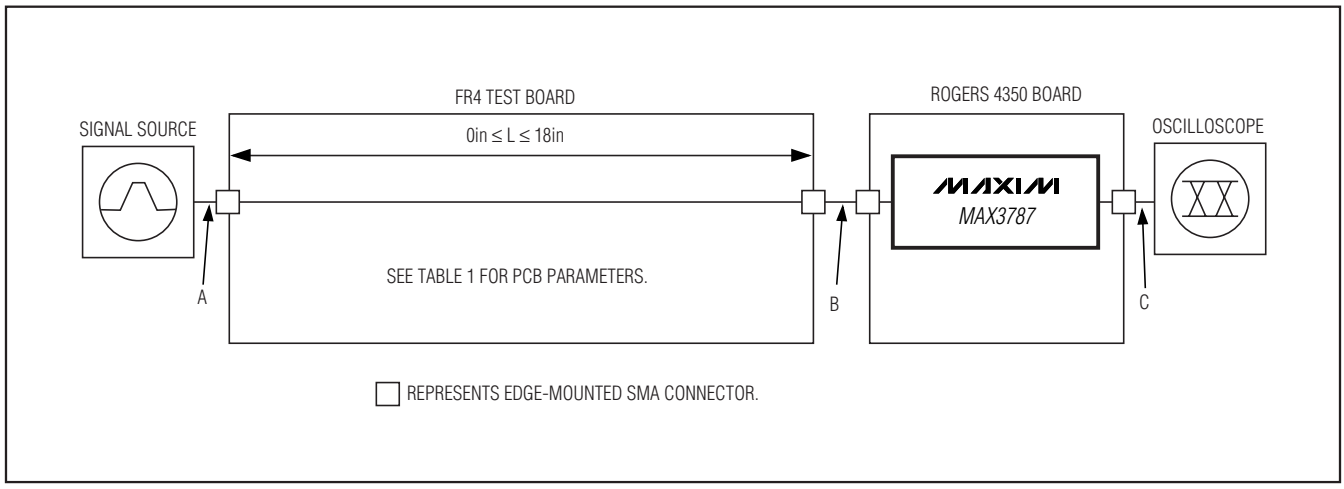


Figure 1. Residual Deterministic Jitter Test Circuit

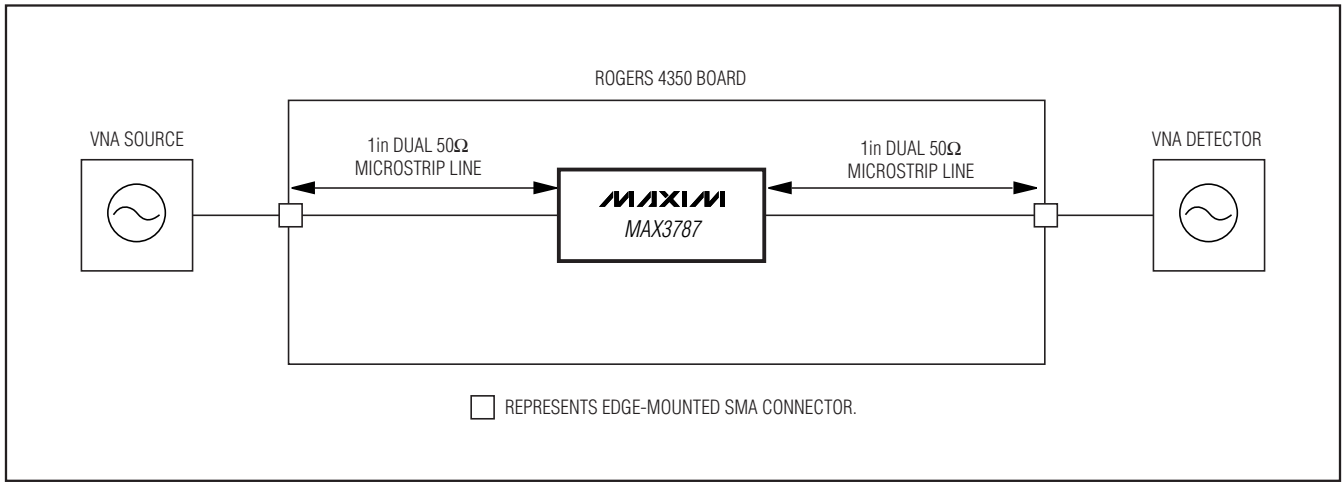


Figure 2. Frequency Response Test Circuit Using Vector Network Analyzer (VNA)

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

FREQUENCY	MIN (dB)	TYP (dB)	MAX (dB)
100MHz	-8.2	-7.4	-6.8
200MHz	-7.9	-7.0	-6.4
300MHz	-7.5	-6.6	-6.0
500MHz	-6.8	-6.0	-5.3
1.0GHz	-5.5	-4.8	-4.2
2.0GHz	-4.2	-3.2	-2.5
3.0GHz	-3.1	-2.2	-1.5
4.0GHz	-2.3	-1.5	-0.8
5.0GHz	-2.1	-1.3	-0.5
5.5GHz	-2.4	-1.6	-0.6
6.0GHz	-2.9	-2.1	-1.1
6.5GHz	—	-2.6	—
7.0GHz	—	-3.1	—
7.5GHz	—	-3.6	—
8.0GHz	—	-4.1	—
8.5GHz	—	-4.7	—
9.0GHz	—	-5.5	—
9.5GHz	—	-7.0	—
10.0GHz	—	-9.0	—

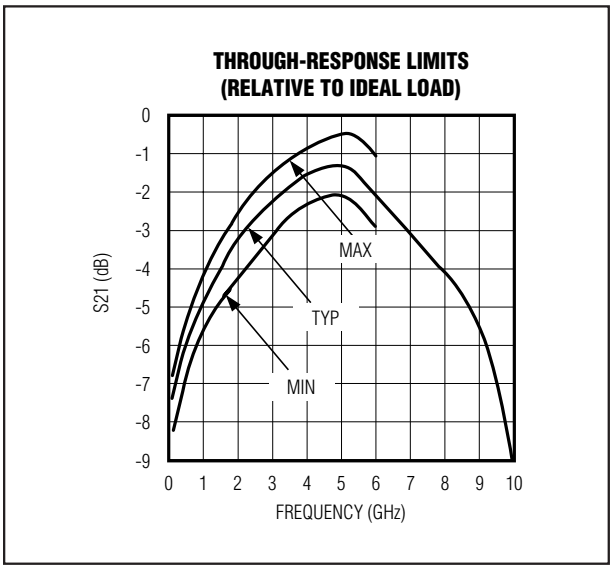


Figure 3. Through Response Limits

Table 1. PCB Assumptions (Board Material is FR4)

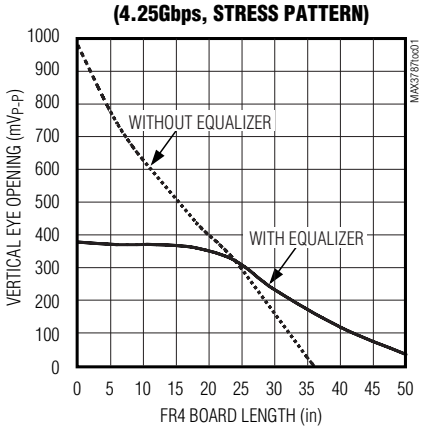
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmission Line	Edge-coupled microstrip line		6		mil
Relative Permittivity at 1GHz	FR4 or similar		4.0		—
Loss Tangent	FR4 or similar		0.02		—
Metal Thickness	1oz copper		1.4		mil
Impedance	Differential	90	100	110	Ω

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

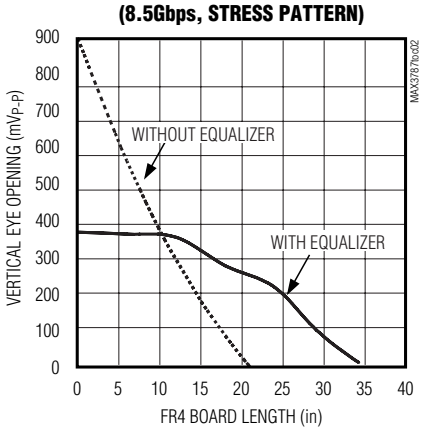
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

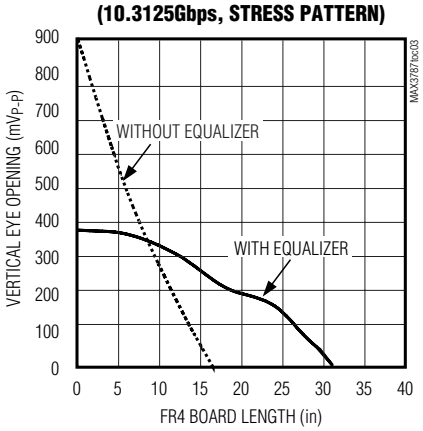
VERTICAL EYE OPENING vs. LENGTH (4.25Gbps, STRESS PATTERN)



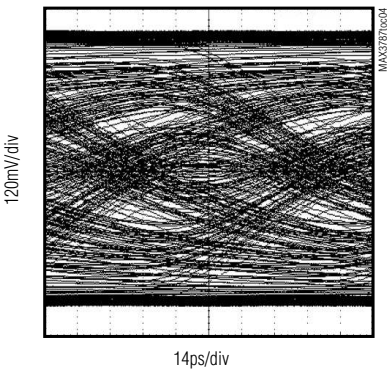
VERTICAL EYE OPENING vs. LENGTH (8.5Gbps, STRESS PATTERN)



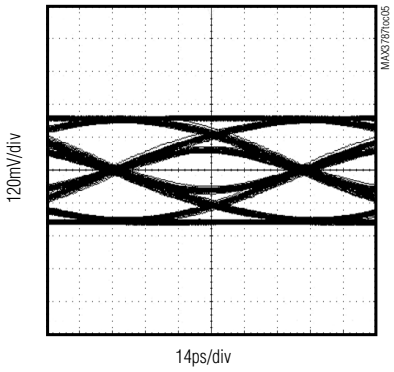
VERTICAL EYE OPENING vs. LENGTH (10.3125Gbps, STRESS PATTERN)



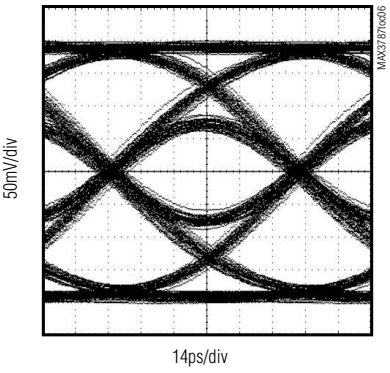
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



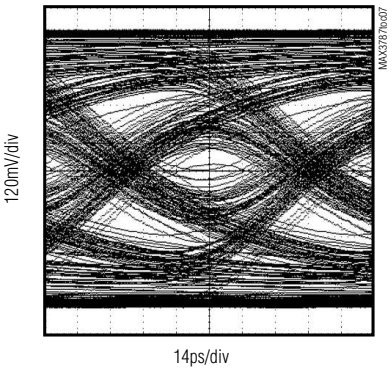
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



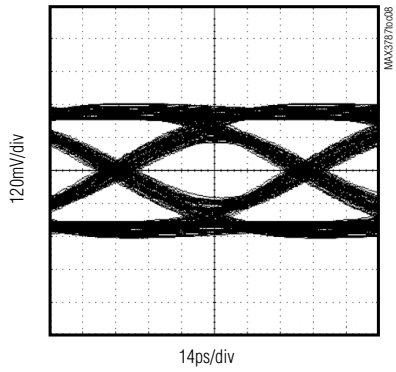
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 12.5Gbps, STRESS PATTERN)



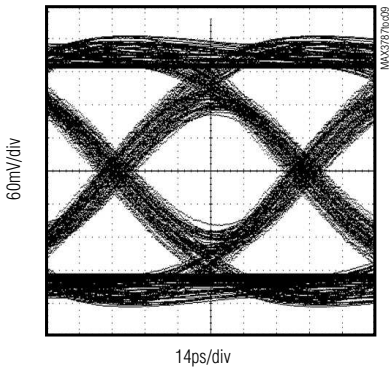
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 12.5Gbps, STRESS PATTERN)



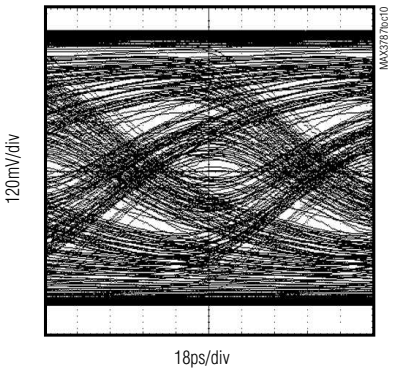
FrameScan is a registered trademark of Tektronix.
Spectra-Strip and Skewclear are registered trademarks of Amphenol.

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

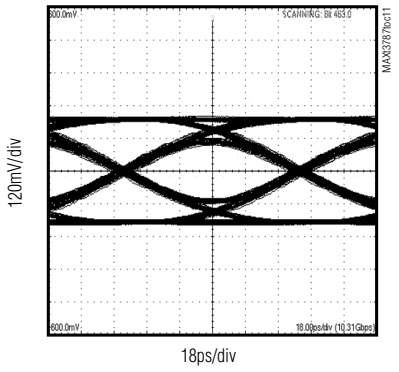
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

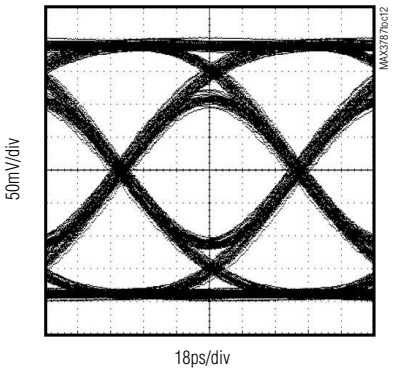
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



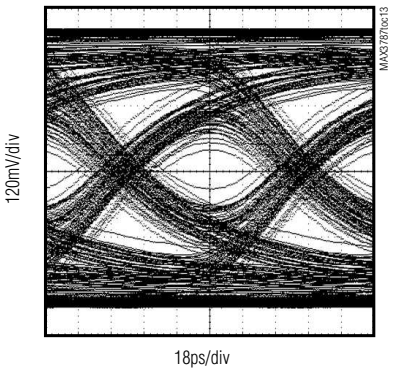
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



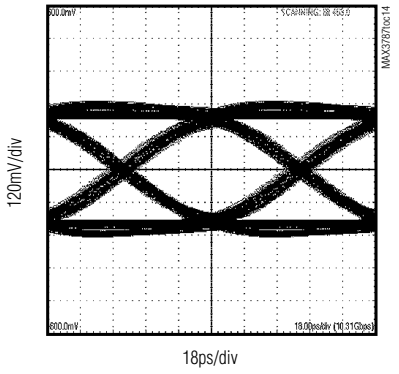
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 10.3125Gbps, STRESS PATTERN)



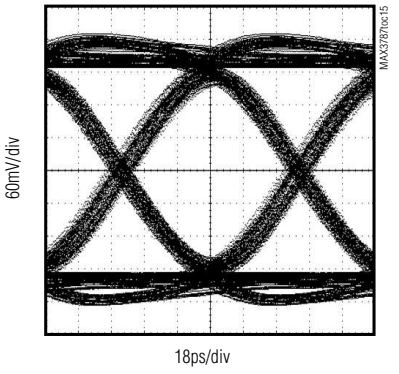
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



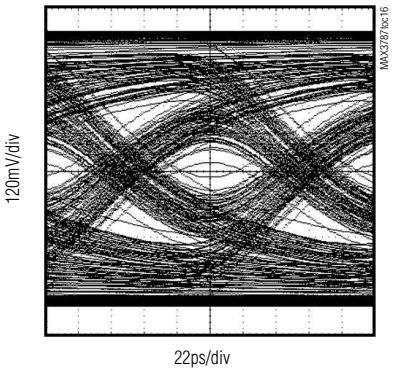
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



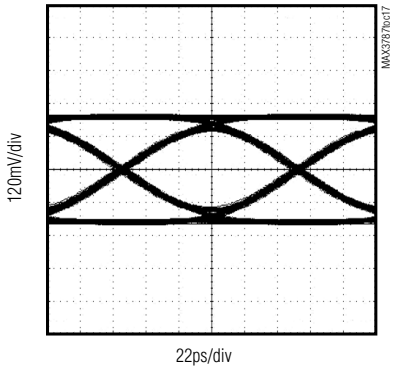
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 10.3125Gbps, STRESS PATTERN)



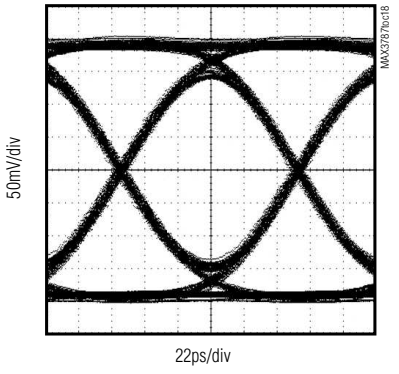
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



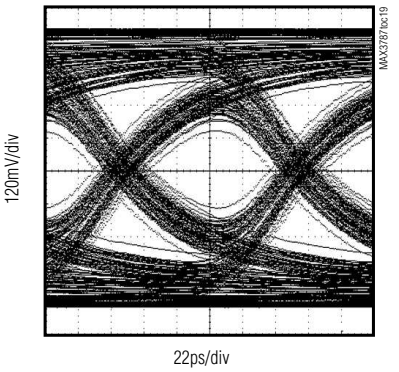
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 8.5Gbps, STRESS PATTERN)



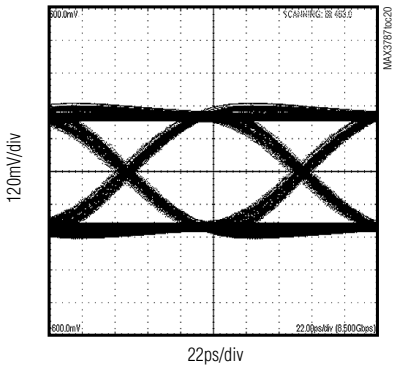
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

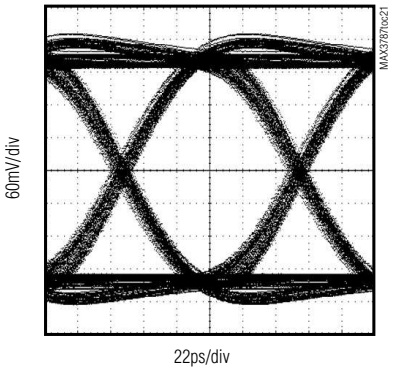
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



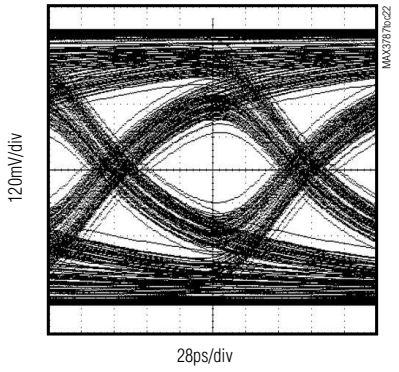
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



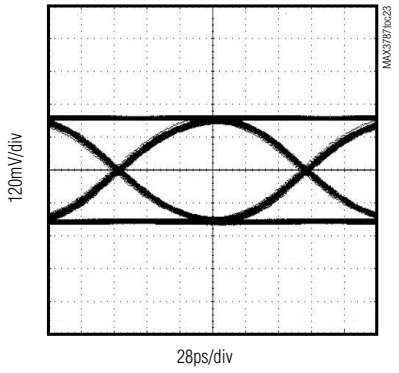
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 8.5Gbps, STRESS PATTERN)



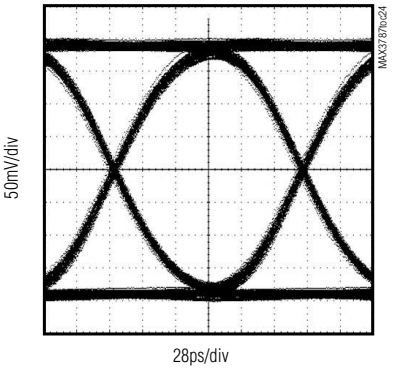
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



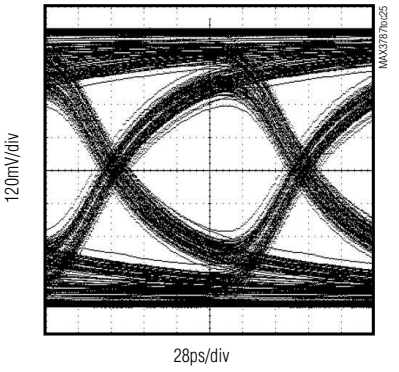
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



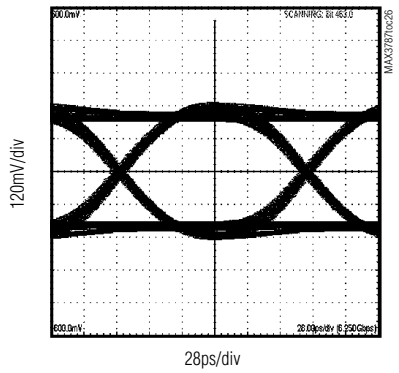
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 6.25Gbps, STRESS PATTERN)



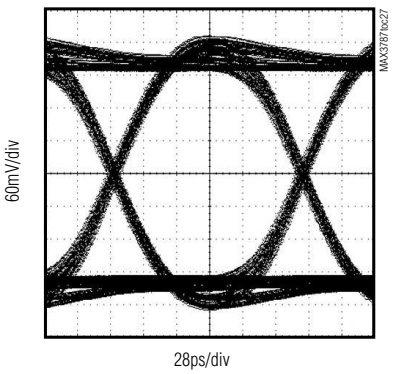
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 6.25Gbps, STRESS PATTERN)

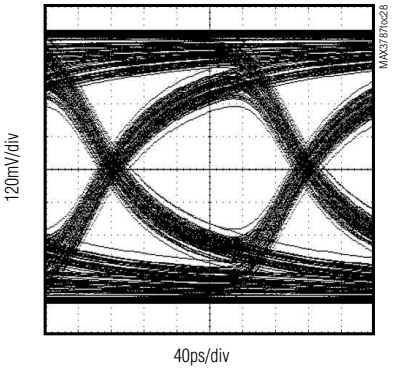


1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

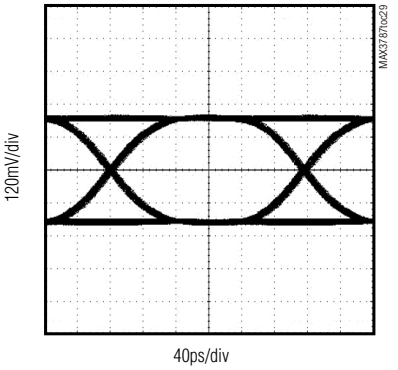
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

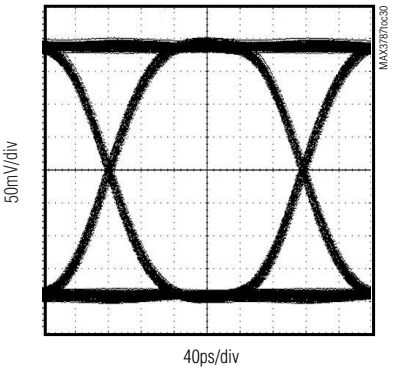
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



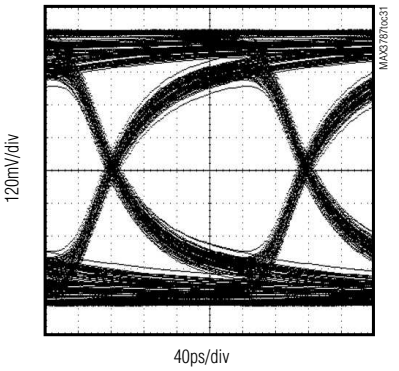
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



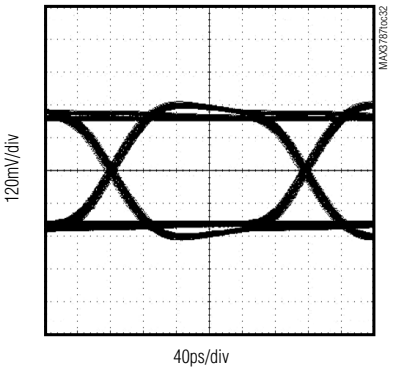
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 4.25Gbps, STRESS PATTERN)



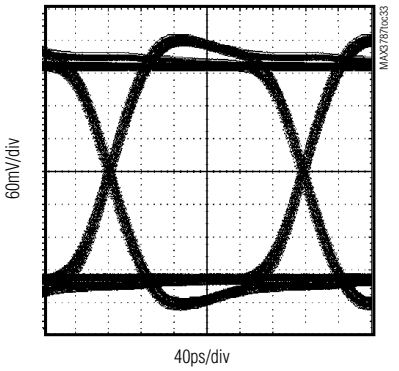
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



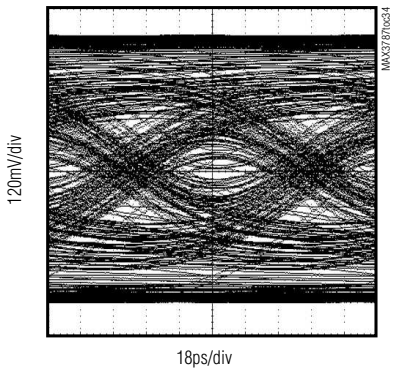
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



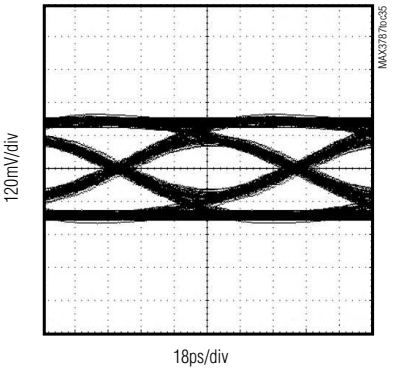
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 4.25Gbps, STRESS PATTERN)



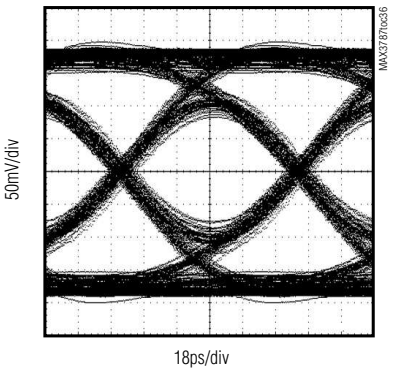
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



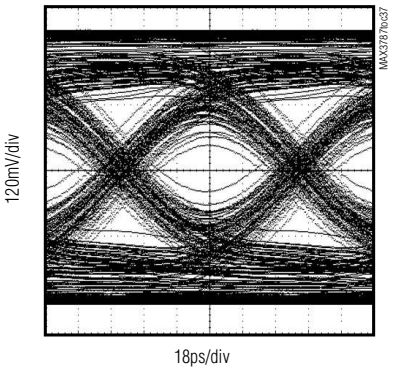
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



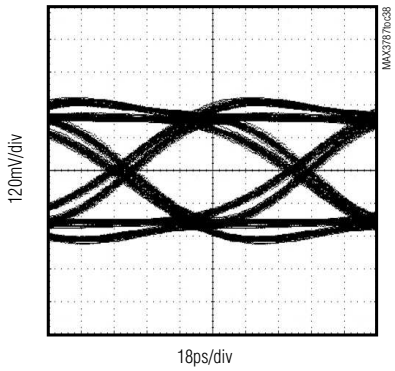
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan which include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

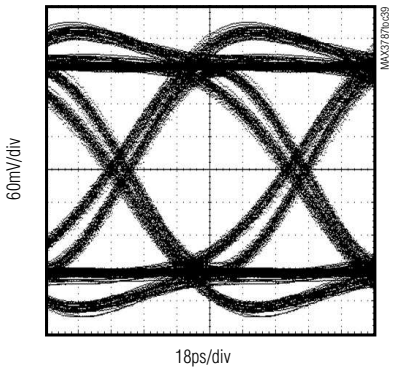
EYE DIAGRAM OF UNEQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



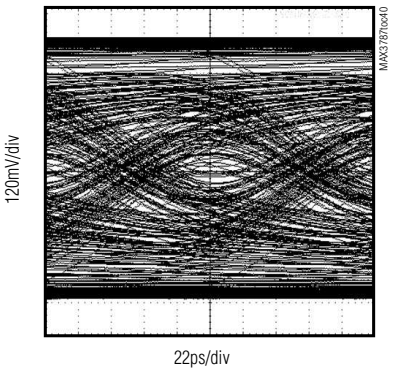
EYE DIAGRAM OF EQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



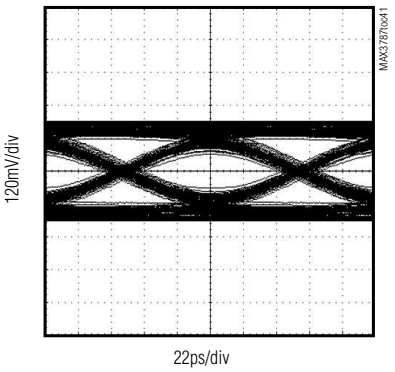
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



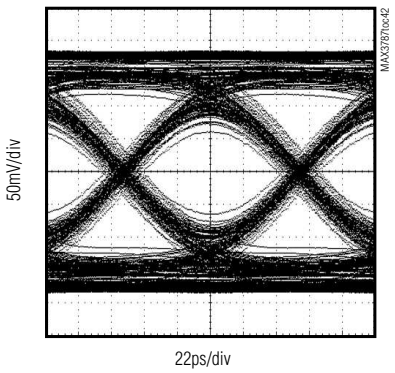
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



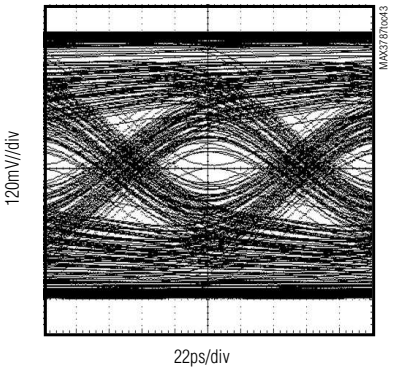
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



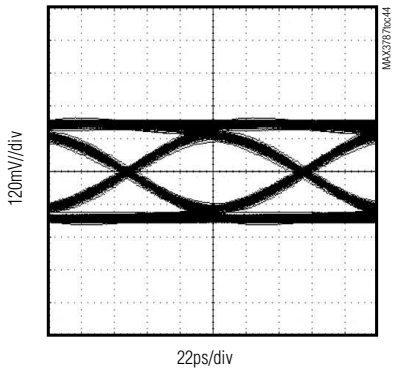
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



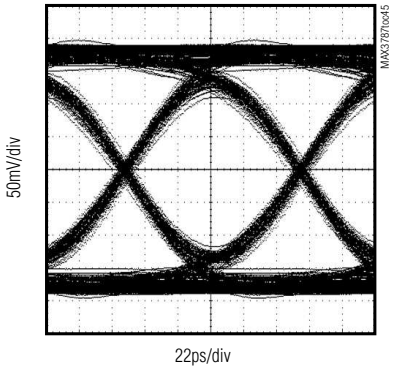
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)

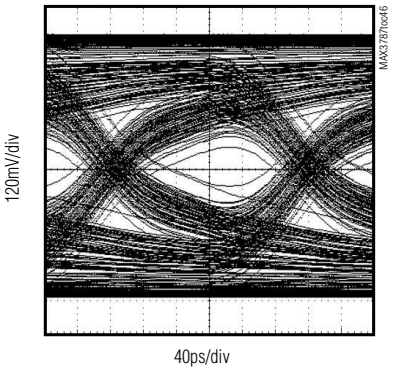


1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

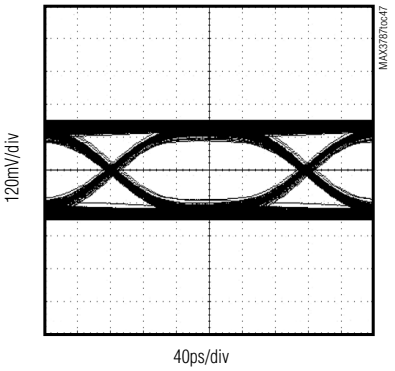
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

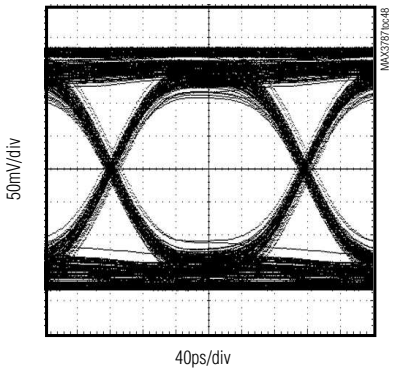
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



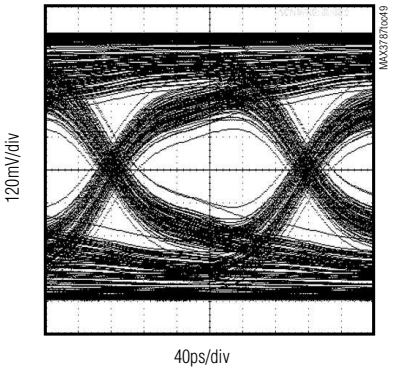
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



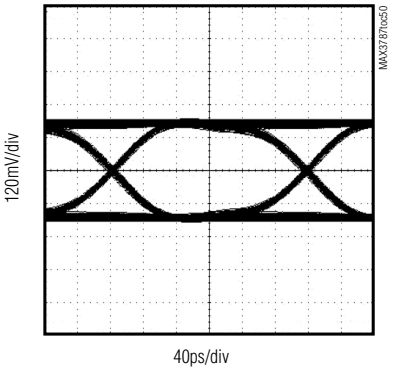
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



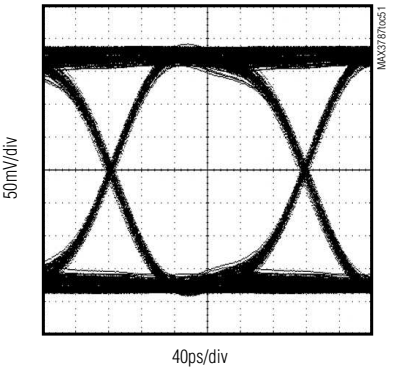
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



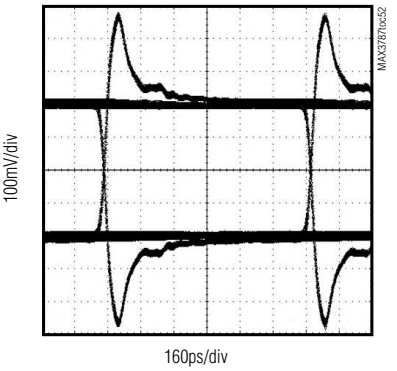
EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



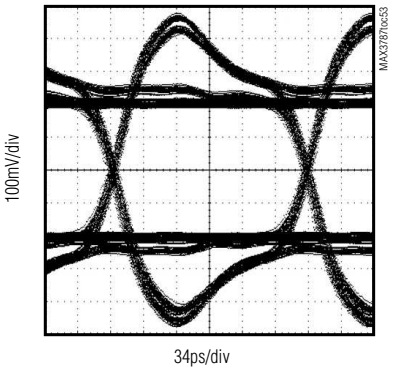
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



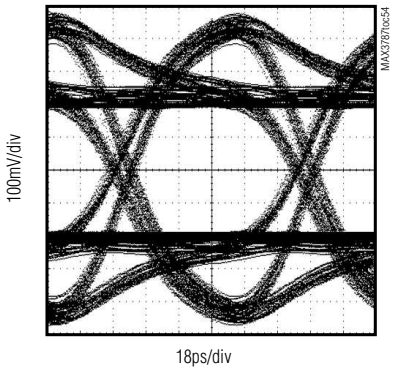
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 1Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 5Gbps, STRESS PATTERN)



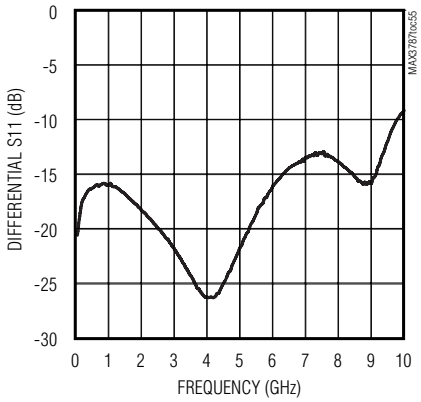
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 10Gbps, STRESS PATTERN)



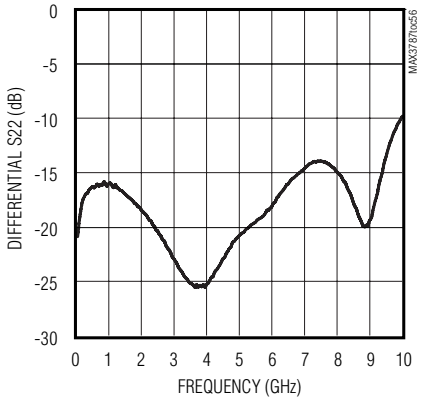
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

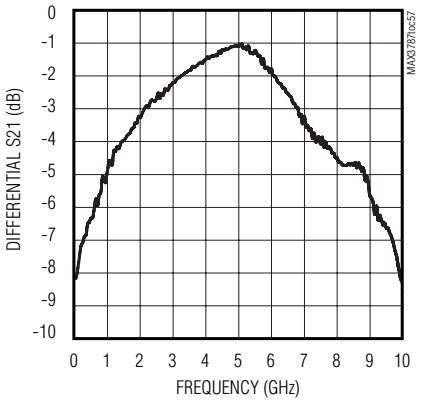
DIFFERENTIAL S11 vs. FREQUENCY



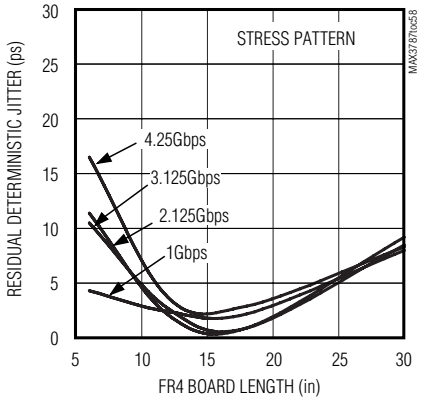
DIFFERENTIAL S22 vs. FREQUENCY



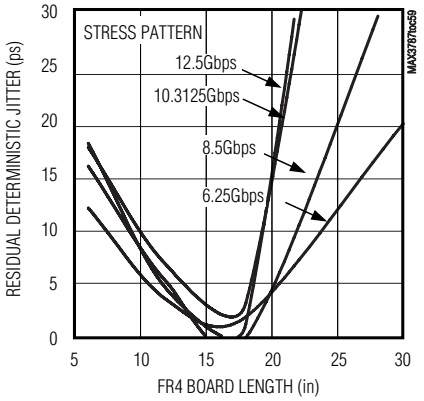
DIFFERENTIAL S21 vs. FREQUENCY



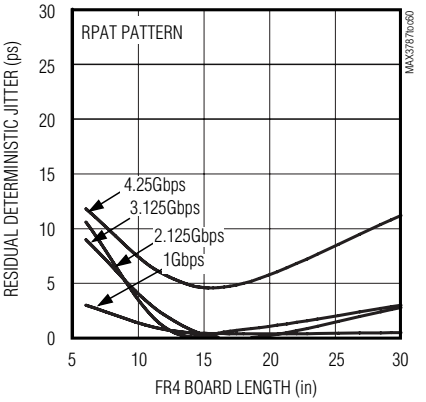
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



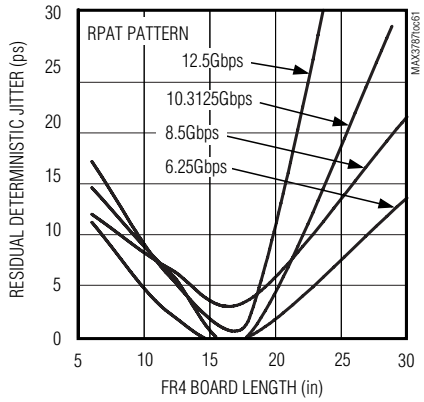
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH

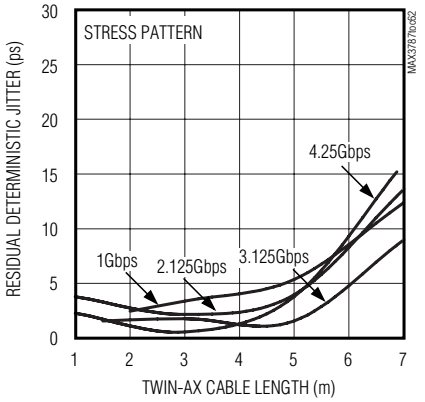


1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

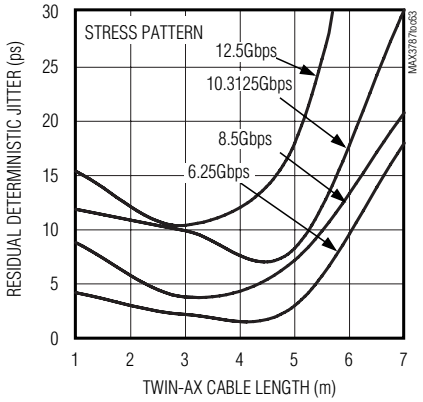
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

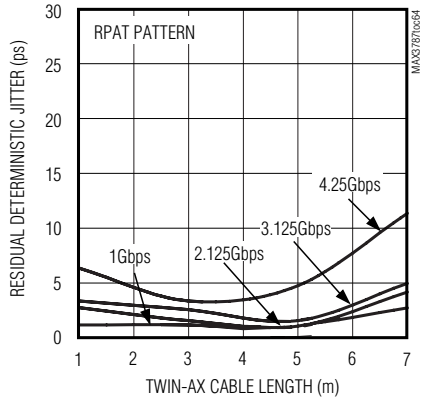
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



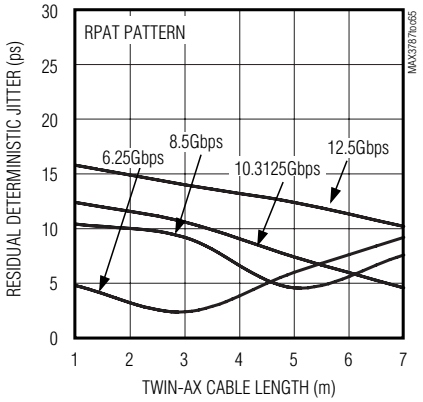
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



Pin Description

PIN	NAME	FUNCTION
A1	IN+	Positive Data Input
A3	OUT+	Positive Data Output
C1	IN-	Negative Data Input
C3	OUT-	Negative Data Output

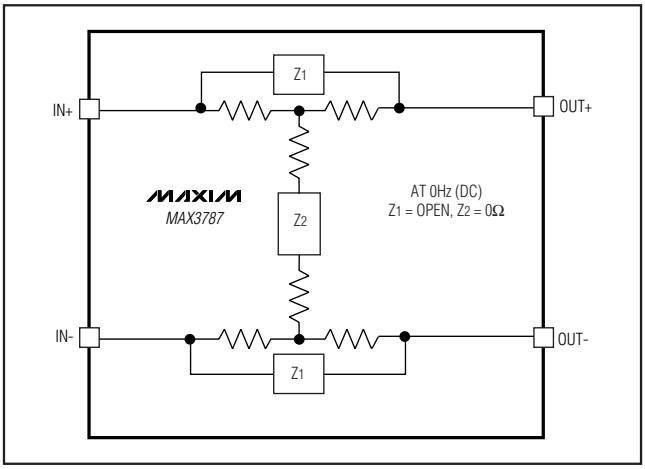


Figure 4. Functional Diagram

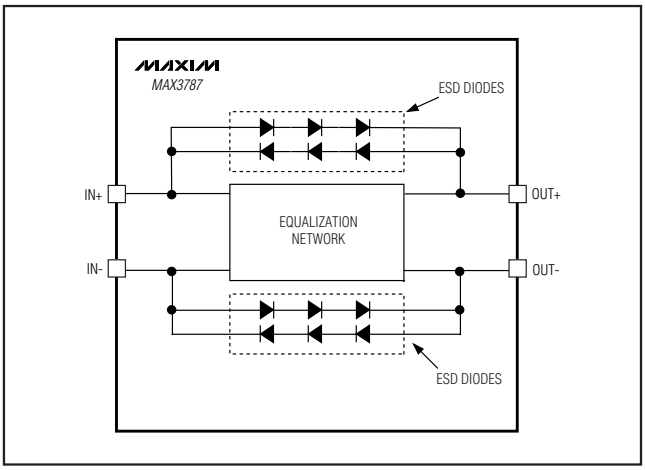


Figure 5. ESD Protection Diodes

Detailed Description

The MAX3787 is an entirely passive network composed of both resistive and reactive components (Figure 4). Two symmetric-T networks with bypassing for high-pass characteristics are used to create a differential symmetric-H network. The entire network acts as a filter specifically tuned to compensate for transmission medium losses encountered with FR4 and cables.

Input and Output Terminations

The MAX3787 input impedance is 100Ω differential with the output connected to a 100Ω differential load. The network is designed for 100Ω-balanced differential signals and is not intended for single-ended transmission.

ESD Protection Diodes

The MAX3787 contains ESD diodes that bypass the equalization network in case of static discharge (Figure 5).

Applications Information

Equalizer Integration and Placement

The MAX3787 is packaged in a small 1.5mm x 1.5mm UCSP that can be placed anywhere along the transmission medium. The small size allows placement and routing flexibility.

Due to the symmetry of the equalization network, signals can pass from IN to OUT or OUT to IN with the same compensation. The equalizer can also be placed at the beginning or end of the transmission medium and provide the same compensation at the receiving circuit. For example, two equalizers can be placed in one transceiver module, one for the transmit path and one for the receive path (see *Typical Application Circuits*).

UCSP Assembly Considerations

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *UCSP–A Wafer-Level Chip-Scale Package* available on Maxim's website at **www.maxim-ic.com/ucsp**.

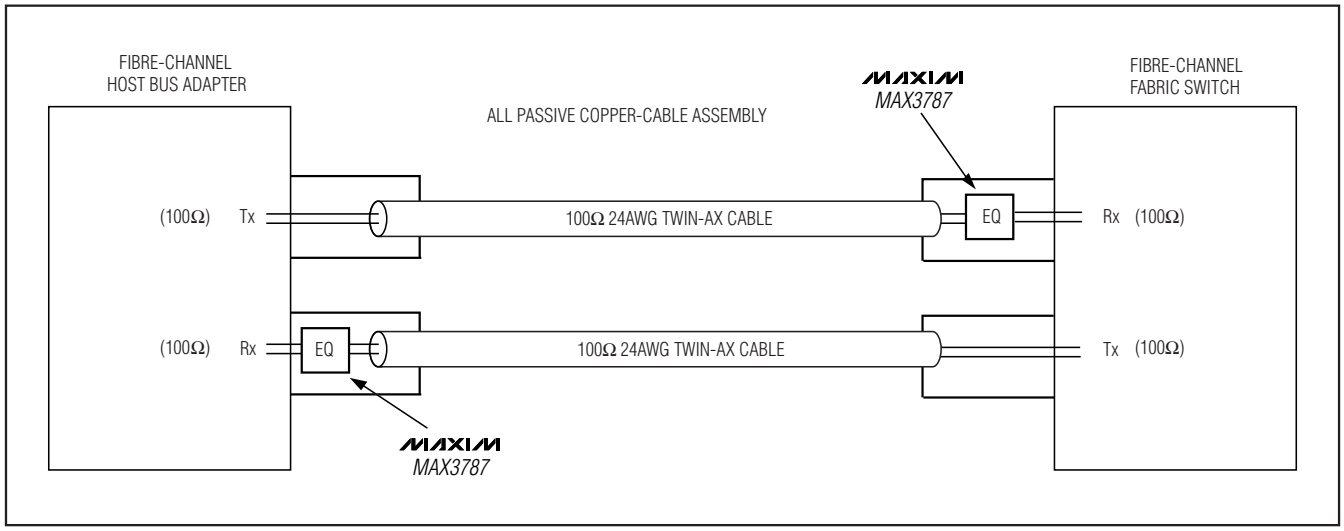
Chip Information

TRANSISTOR COUNT: 0

PROCESS: SiGe BiPOLAR

1Gbps to 12.5Gbps Passive Equalizer for Backplanes and Cables

Typical Application Circuits (continued)



Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
4 UCSP	B9-7	**21-0093**
4 WLP	W91B1+3	**21-0067**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/05	Initial release.	—
1	12/05	Added lead-free package to Ordering Information table.	1
2	2/08	In the Ordering Information table, changed lead-free part number from ABL+ to AWL+; added WLP package information.	1, 14