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19-2342; Rev 2; 2/05

EVALUATION KIT AVAILABLE

2.7Gbps Post Amp with Automatic Gain Control

General Description

The MAX3861 is a low-power amplifier with automatic gain control (AGC), designed for WDM transmission systems employing optical amplifiers and requiring a vertical threshold adjustment after the post amp. Operating from a single 3.3V supply, this AGC amplifier linearly amplifies/attenuates the input signal while maintaining a fixed output-voltage swing at data rates up to 2.7Gbps. The input and output are on-chip terminated to match 50Ω interfaces.

This amplifier has a small-signal bandwidth of 3.4GHz and an input-referred noise of 0.26mV$_{RMS}$. Over an input signal range of 6mV$_{P-P}$ to 1200mV$_{P-P}$ (46dB), the MAX3861 delivers a constant output amplitude adjustable from 400mV$_{P-P}$ to 920mV$_{P-P}$. Variation in output swing is controlled within 0.2dB over a 16dB input range. The MAX3861 provides a received-signal-strength indicator (RSSI) that is linear, within 2.5%, for input signal levels up to 100mV$_{P-P}$ and an input signal detect (SD) with programmable threshold.

Applications

OC-48/STM-16 Transmission Systems

WDM Optical Receivers

Long-Reach Optical Receivers

Continuous Rate Receivers

Features

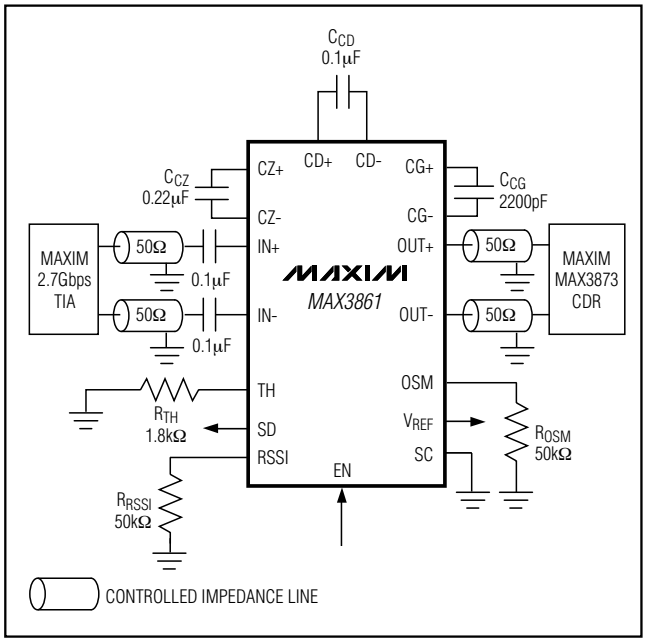
- **Single 3.3V Power Supply**
- **72mA Supply Current**
- **3.4GHz Small-Signal Bandwidth**
- **0.26mV$_{RMS}$ Input-Referred Noise**
- **6mV$_{P-P}$ to 1200mV$_{P-P}$ Input Range (46dB)**
- **Input Signal Detect with Programmable Threshold**
- **RSSI (Linear Up to 100mV$_{P-P}$)**
- **Adjustable Output Amplitude**
- **0.2dB Output Voltage Variation (Over 16dB Input Signal Variation)**

Ordering Information

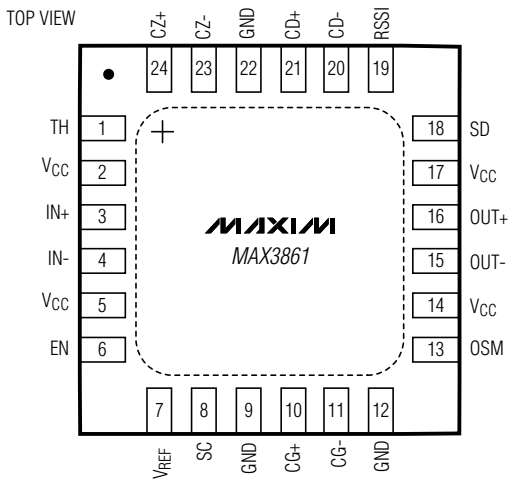
PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3861ETG+	-40°C to +85°C	24 Thin QFN-EP*	T2444-3
MAX3861EGG	-40°C to +85°C	24 QFN-EP*	G2444-1

+Denotes lead-free package.
**EP = Exposed pad.*

Typical Application Circuit



Pin Configurations



THIN QFN*

***NOTE:** MAXIM RECOMMENDS SOLDERING THE EXPOSED PAD TO GROUND.

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2.7Gbps Post Amp with Automatic Gain Control

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....-0.5V to +4.0V
Voltage at IN+, IN- .....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Voltage at CZ+, CZ-, CG+, CG-, CD+, CD- .....(V_{CC} - 3.5V) to (V_{CC} + 0.5V)
Voltage at SC, SD, EN, TH, OSM, V_{REF}, RSSI .....-0.5V to (V_{CC} + 0.5V)
CML Input Current at IN+, IN- 25mA
CML Output Current at OUT+, OUT- 25mA
Continuous Power Dissipation T_A = +85°C (24-Pin QFN and 24-Pin Thin QFN) (derate 20.8mW/°C above +85°C 1.35W
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	RSSI and SD enabled (Notes 2, 3)	At minimum gain		72	86	mA
			At maximum gain		94	112	
		RSSI and SD disabled (Notes 2, 3)	At minimum gain		57	69	
			At maximum gain		78	94	
Power-Supply Noise Rejection	PSNR	V_{NOISE} = 100mV_{P-P}, f_{NOISE} ≤ 10MHz, V_{SC} = 2V (Note 4)	V_{IN} = 1000mV_{P-P}		35		dB
			V_{IN} = 10mV_{P-P}		25		
Input Data Rate					2.7		Gbps
Input Resistance	R_{IN}	Single-ended to V_{CC}		40	50	60	Ω
Input Return Loss		≤2.7GHz			21		dB
		2.7GHz to 4.0GHz			15		
Input Common-Mode Level				V_{CC} - 0.3		V_{CC}	V
Input-Referred Noise		Up to 6GHz at max gain, C_{CZ} = 0.1µF			0.26	0.35	mV_{RMS}
Input Voltage Range	V_{IN}	Differential		6		1200	mV_{P-P}
Maximum Differential Input Voltage for Linear Operation		0.9 ≤ linearity ≤ 1.1	V_{SC} = 0		700		mV_{P-P}
			V_{SC} = 2V		650		
Output Resistance	R_{OUT}	Single-ended to V_{CC}		40	50	60	Ω
Output Return Loss		≤2.7GHz			16		dB
		2.7GHz to 4.0GHz			11		
Output Common-Mode Level		R_L = 50Ω to V_{CC}	V_{SC} = 0		V_{CC} - 0.13		V
			V_{SC} = 2V		V_{CC} - 0.28		
Maximum Differential Output Offset		V_{SC} = 0, R_L = 50Ω to V_{CC} (Note 5)	6mV_{P-P} ≤ V_{IN} ≤ 700mV_{P-P}		±3	±14	mV
			700mV_{P-P} ≤ V_{IN} ≤ 1200mV_{P-P}		±8		
		V_{SC} = 2V, R_L = 50Ω to V_{CC} (Note 5)	6mV_{P-P} ≤ V_{IN} ≤ 700mV_{P-P}		±5.5	±28	
			700mV_{P-P} ≤ V_{IN} ≤ 1200mV_{P-P}		±11		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Amplitude	V_{OUT}	R_L = 50Ω to V_{CC} (Note 6)	V_{SC} = 0	300	400	500	mV_{P-P}
			V_{SC} = 2V	760	920	1050	
Output Amplitude Variation	ΔV_{OUT}	$V_{IN} \geq 6mV_{P-P}$, R_L = 50Ω to V_{CC} (Notes 6, 7)			0.2	1.0	dB
Small Signal Bandwidth	BW	(Note 3)	At minimum gain	2.5	3.4	5.5	GHz
			At maximum gain	2.2	2.9	4.3	
Low-Frequency Cutoff		C_{CZ} = 0.1µF			7.6	13	kHz
Deterministic Jitter		(Note 8)			15	50	ps_{P-P}
Output Signal Monitor Voltage	V_{OSM}	$R_{OSM} \geq 2k\Omega$ (Note 6)	V_{OUT} = 920mV_{P-P}		2.0		V
			V_{OUT} = 400mV_{P-P}		0.9		
Output Signal Monitor Linearity		0V ≤ V_{SC} ≤ 2V (Note 6)			1.0		%
SC Input Range		(Note 9)		0		2.0	V
AGC Loop Constant		Without external capacitor C_{CG}, V_{SC} = 0 (Note 10)			16		µs
RSSI Output Voltage	RSSI	$R_{RSSI} \geq 2k\Omega$, V_{SC} = 0 (Note 6)	V_{IN} = 2mV_{P-P}		55		mV
			V_{IN} = 100mV_{P-P}		1800		
RSSI Linearity		2mV_{P-P} ≤ V_{IN} ≤ 100mV_{P-P} (Note 14)			±2.5	±12	%
		6mV_{P-P} ≤ V_{IN} ≤ 100mV_{P-P}			±2.5	±8	
Minimum SD Assert Input						2	mV_{P-P}
Maximum SD Assert Input				100			mV_{P-P}
SD Assert Time				10	70		µs
SD Deassert Time		CG+ and CG- are open (Note 11)		10	44		µs
SD Accuracy		(Note 12)			±10		%
SD Hysteresis		10mV_{P-P} ≤ V_{IN} ≤ 100mV_{P-P}		2.8	4.5	6.3	dB
		2mV_{P-P} ≤ V_{IN} ≤ 10mV_{P-P} (Note 13)			4.5		
SD Output High Voltage		Sourcing 20µA current		2.4			V
SD Output Low Voltage		Sinking 2mA current				0.44	V
EN Input Low Voltage	V_{IL}					0.8	V
EN Input High Voltage	V_{IH}			2.0			V
EN Input Low Current	I_{IL}	V_{IL} = 0				10	µA
EN Input High Current	I_{IH}	V_{IH} = 2.0V				10	µA
V_{REF} Output Voltage		$R_{VREF} \geq 40k\Omega$			2.0		V

Note 1: Electrical characteristics are measured or characterized using a 2^{23} - 1PRBS at 2.7Gbps with input edge speeds ≤200ps, unless otherwise noted. All AC specifications are guaranteed by design and characterization, unless otherwise noted.

Note 2: Supply current measurement is taken with AC-coupled inputs and excludes output currents into 50Ω loads.

Note 3: Minimum gain is defined as V_{IN} = 1200mV_{P-P} and V_{OUT} = 400mV_{P-P}. Maximum gain is defined as V_{IN} = 6mV_{P-P}, and V_{OUT} = 920mV_{P-P}. Reference gain is measured at 100MHz.

Note 4: Power-supply noise rejection is characterized with a 2.7Gbps 1100 pattern on the input. It is calculated by the equation PSNR = 20log(ΔV_{CC} / (ΔV_{OUT})), where ΔV_{OUT} is the change in differential output voltage because of power-supply noise. See the Power-Supply Noise Rejection vs. Frequency graph in the *Typical Operating Characteristics*.

2.7Gbps Post Amp with Automatic Gain Control

ELECTRICAL CHARACTERISTICS (continued)

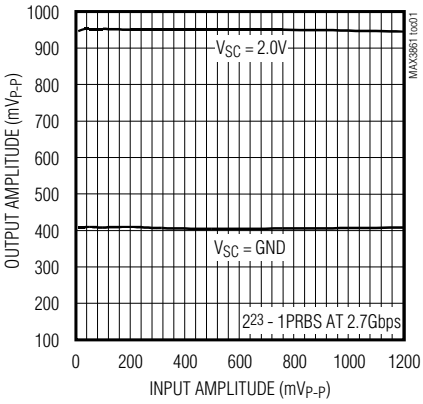
(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

Note 5: See the Distribution of Differential Output Offset (Worst-Case Conditions) graph in the *Typical Operating Characteristics*.
Note 6: Characterized with a 675Mbps 1-0 pattern.
Note 7: Measurements are taken over an input signal range of 16dB.
Note 8: Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Deterministic jitter is the difference between total jitter and random jitter, with system jitter calibrated out. It is measured with a 2^7 - 1PRBS, and 80CIDs with DC-coupled outputs.
Note 9: The typical input resistance of the SC pin is 40kΩ.
Note 10: AGC loop time constant is measured with a 20dB change in the input and V_{SC} held constant. With an external capacitor C_{CG} of 0.022µF connected between CG+ and CG-, a typical AGC loop time constant of 760µs is achieved.
Note 11: SD deassert time depends on the AGC loop time constant set by C_{CG}.
Note 12: SD accuracy is defined as the part-to-part variation of the SD threshold at a fixed R_{TH} value.
Note 13: See the Distribution of SD Hysteresis (Worst-Case Conditions) graph in the *Typical Operating Characteristics*.
Note 14: Measurements are taken over an input signal range of 20dB.

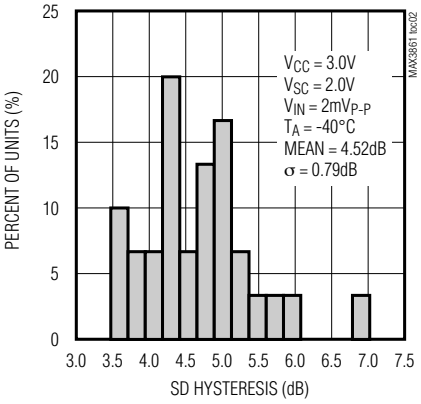
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

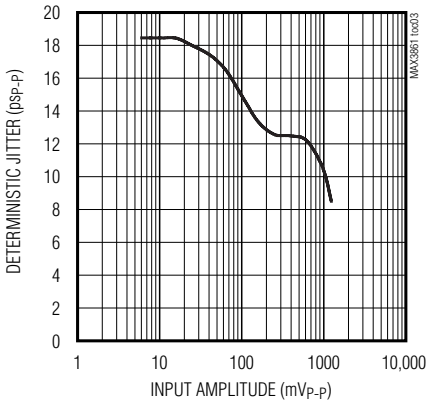
OUTPUT AMPLITUDE vs. INPUT AMPLITUDE



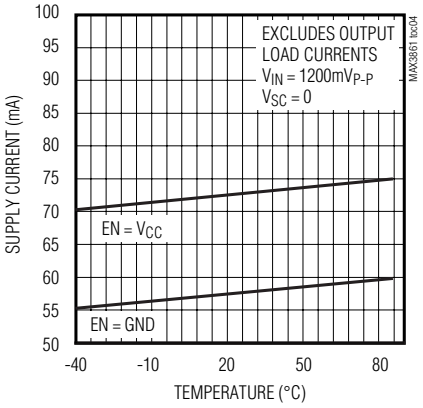
DISTRIBUTION OF SD HYSTERESIS (WORST-CASE CONDITIONS)



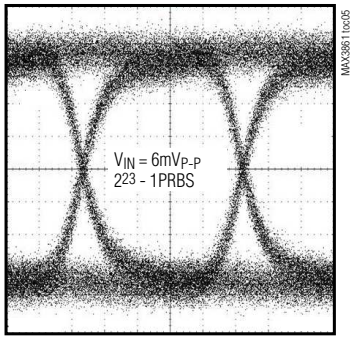
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



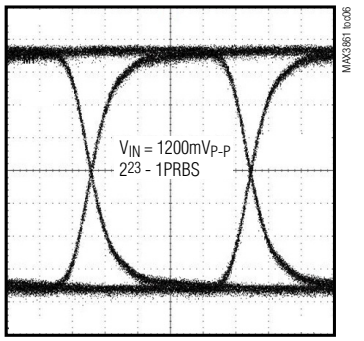
SUPPLY CURRENT vs. TEMPERATURE



EYE DIAGRAM, MINIMUM INPUT



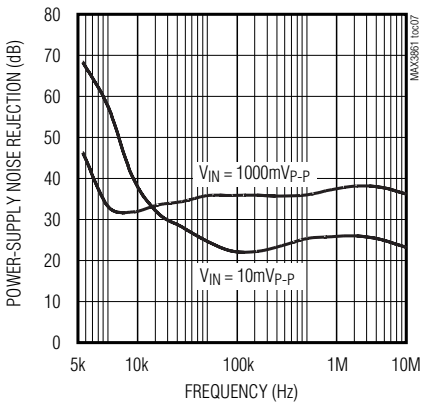
EYE DIAGRAM, MAXIMUM INPUT



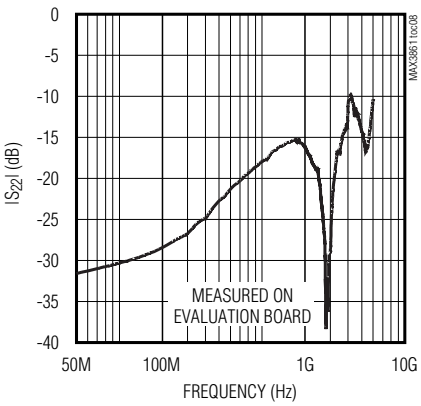
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

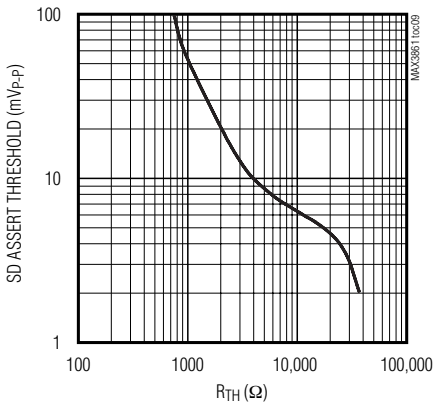
POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



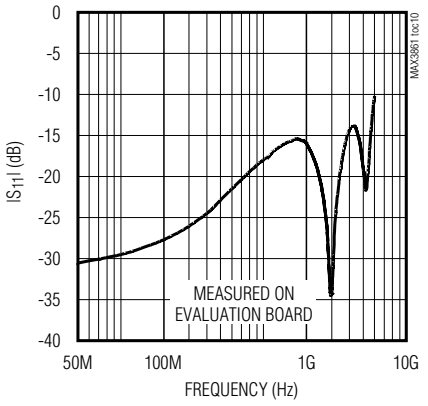
|S22| vs. FREQUENCY



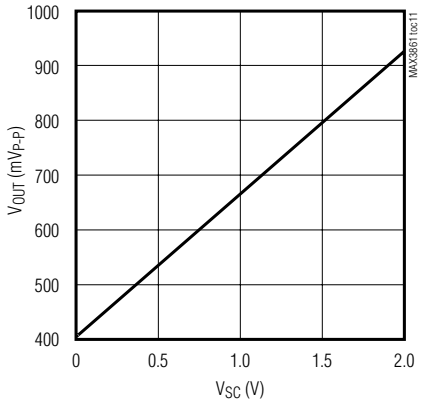
SIGNAL DETECT THRESHOLD vs. R_{TH}



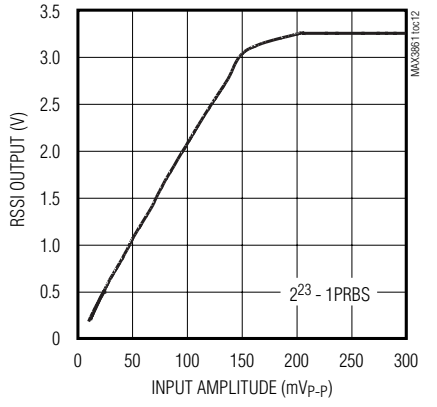
|S11| vs. FREQUENCY



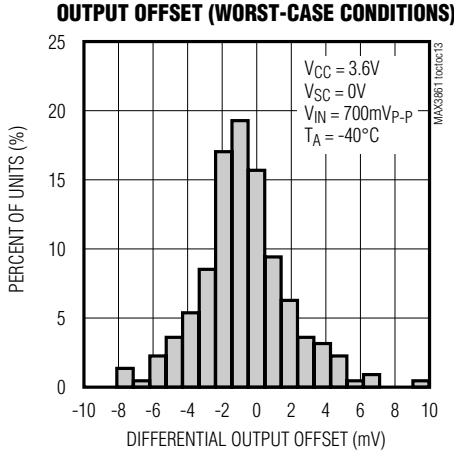
OUTPUT SIGNAL AMPLITUDE vs. SC PIN VOLTAGE (V_{IN} = 1.0V_{P-P})



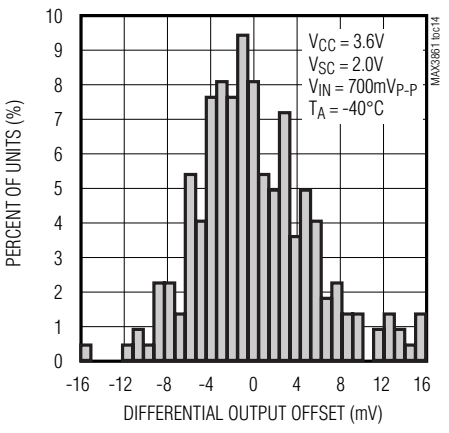
RSSI OUTPUT vs. INPUT AMPLITUDE



DISTRIBUTION OF DIFFERENTIAL OUTPUT OFFSET (WORST-CASE CONDITIONS)



DISTRIBUTION OF DIFFERENTIAL OUTPUT OFFSET (WORST-CASE CONDITIONS)



Pin Description

PIN	NAME	FUNCTION
1	TH	Input Signal Detect Threshold Programming Pin. Attach a resistor between this pin and ground to program the input signal detect assert threshold. Leaving this pin open sets the signal detect threshold to its absolute minimum value (<2mV$_{P-P}$). See the *Design Procedure* section.
2, 5, 14, 17	V_{CC}	Supply Voltage Connection. Connect all V_{CC} pins to the board V_{CC} plane.
3	IN+	Positive CML Signal Input with On-Chip Termination Resistor
4	IN-	Negative CML Signal Input with On-Chip Termination Resistor
6	EN	Signal Detect Enable. Set high (≥2.0V) or leave open to enable the input signal detection (RSSI and SD) circuitry. Set low (≤0.4V) to power down the input signal detection circuitry.
7	V_{REF}	Reference Voltage Output (2.0V). Connect this pin to the SC pin for maximum output signal swing.
8	SC	Output Amplitude External Control. Ground SC for minimum output amplitude. Apply 2.0V to SC or connect SC directly to V_{REF} for maximum output amplitude.
9, 12, 22	GND	Ground. Connect all GND pins to the board ground plane.
10	CG+	Connection for AGC Loop Capacitor. A capacitor connected between CG+ and CG- sets the AGC loop time constant.
11	CG-	Connection for AGC Loop Capacitor. A capacitor connected between CG+ and CG- sets the AGC loop time constant.
13	OSM	Output Signal Monitor. This DC signal is linearly proportional to the output signal amplitude.
15	OUT-	Negative CML Data Output with On-Chip Back-Termination Resistor
16	OUT+	Positive CML Data Output with On-Chip Back-Termination Resistor
18	SD	Input Signal Detect. Asserts logic low when the input signal level drops below the programmed threshold.
19	RSSI	Received Signal Strength Indicator. Outputs a DC signal linearly proportional to the input signal amplitude.
20	CD-	Connection for Signal Detect Capacitor. A capacitor connected between CD+ and CD- sets the offset-cancellation loop time constant of the input signal detection. See the *Detailed Description* section.
21	CD+	Connection for Signal Detect Capacitor. A capacitor connected between CD+ and CD- sets the offset-cancellation loop time constant of the input signal detection. See the *Detailed Description* section.
23	CZ-	Connection for Offset-Cancellation Loop Capacitor. A capacitor connected between CZ+ and CZ- sets the offset-cancellation loop time constant of the main signal path. See the *Detailed Description* section.
24	CZ+	Connection for Offset-Cancellation Loop Capacitor. A capacitor connected between CZ+ and CZ- sets the offset-cancellation loop time constant of the main signal path. See the *Detailed Description* section.
EP	Exposed Pad	Maxim recommends connecting the exposed pad to board ground.

Detailed Description

Figure 1 is a functional diagram of the MAX3861 automatic gain-control amplifier. The MAX3861 is divided into three sections: main signal path, input signal detection, and output signal detection.

Main Signal Path

The main signal path consists of variable gain amplifiers with CML output levels and an offset-cancellation loop. This configuration allows for overall gains from -9.5dB to 43.5dB.

Offset-Cancellation Loop

The offset-cancellation loop partially reduces additional offset at the input. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is partially removed by the offset-cancellation loop. An external capacitor is required between CZ+ and CZ- to compensate the offset-cancellation loop and determine the lower 3dB frequency of the signal path.

Input Signal Detection and SD Circuitry

The input signal detection circuitry consists of variable gain amplifiers and threshold voltages. Input signal detection information is compared to an internal reference and creates the RSSI voltage and an internal reference signal. The signal detect (SD) circuitry indicates when the input signal is below the programmed threshold by comparing a voltage proportional to the RSSI signal with internally generated control voltages. The SD threshold is set by a control voltage developed across the external TH resistor (R_{TH}). Two control voltages, V_{ASSERT} and $V_{DEASSERT}$, define the signal detect assert and deassert levels. To prevent SD chatter in the region of the programmed threshold, 2.8dB to 6.3dB of hysteresis is built into the SD assert/deassert function. Thus, once asserted, SD is not deasserted until sufficient gain is retained. When input signal detection (SD and RSSI) is not required, connect EN to a TTL low to power down this circuitry.

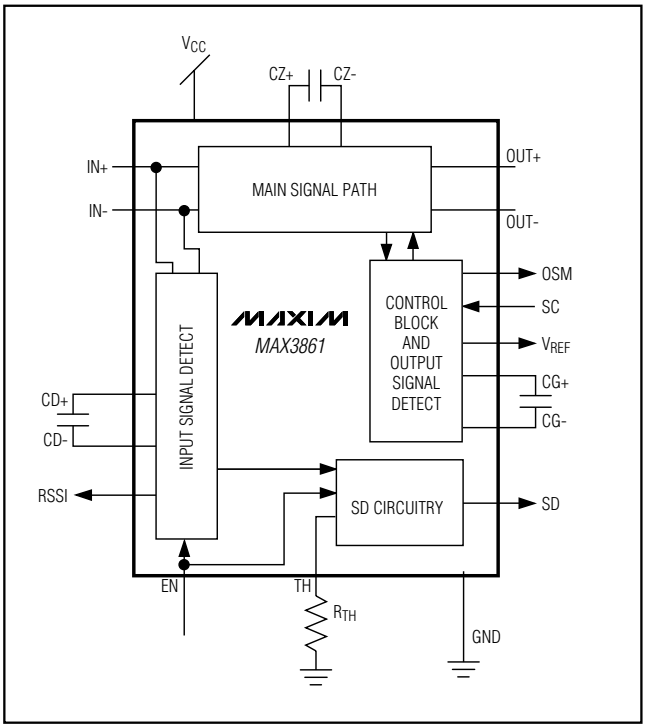


Figure 1. Functional Diagram

Output Signal Monitor and Amplitude Control

Output amplitude typically can be adjusted from 400mV$_{P-P}$ to 920mV$_{P-P}$ by applying a control voltage (0V to 2.0V) to the SC pin. See the Output Signal Amplitude vs. SC Pin Voltage graph in the *Typical Operating Characteristics*. Connect the V_{REF} pin (2.0V) to the SC pin for maximum output amplitude. The output signal monitor pin provides a DC voltage linearly proportional to the output signal.

Design Procedure

Program the SD Threshold

The SD threshold is programmed by an external resistor, R_{TH}, between the range of 2mV$_{P-P}$ to 100mV$_{P-P}$. The circuit is designed to have approximately 4.5dB of hysteresis over the full range. See the Signal Detect Threshold vs. R_{TH} graph in the *Typical Operating Characteristics* for proper sizing.

2.7Gbps Post Amp with Automatic Gain Control

Select the Coupling Capacitors

When AC-coupling is desired, select coupling capacitors C_{IN} and C_{OUT} to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased.

$$f_{IN} = \frac{1}{[2\pi(50)(C_{IN})]}$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1µF, which provides f_{IN} < 32kHz. For Fibre Channel, Gigabit Ethernet, and other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01µF, which provides f_{IN} < 320kHz.

Setting the Offset-Cancellation Loop Time Constant for Input Signal Detection Circuitry (Selecting C_{CD})

The capacitor between CD+ and CD- determines the time constant of the input signal detection DC offset-cancellation loop. A value of 0.1µF for C_{CD} provides a low-frequency cutoff (f_C) below 10kHz. If a lower cutoff frequency is desired, 0.22µF gives f_C = 4.5kHz and 0.47µF gives f_C = 2.1kHz. To guarantee stable operation, do not use a capacitor of less than 0.01µF.

Setting the Offset-Cancellation Loop Time Constant for the Main Signal Path (Selecting C_{CZ})

The capacitor between CZ+ and CZ- determines the time constant of the signal path DC offset-cancellation loop. To maintain stability, keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC offset-cancellation circuit. For SONET applications, f_{IN} < 32kHz, so f_{OCMAX} < 3.2kHz. Therefore, C_{CZ} = 0.22µF (f_{OC} = 2.99kHz), C_{CZ} = 0.47µF (f_{OC} = 1.4kHz), or a greater value can be used. To guarantee stable operation, do not use a capacitor of less than 0.01µF.

Setting the Automatic Gain-Control Loop Time Constant (Selecting C_{CG})

The automatic gain-control loop time constant is determined by the external capacitor connected between CG+ and CG-. Maxim recommends a value of at least 0.0022µF.

Programming the Output Amplitude (Programming the SC Pin)

Output amplitude can be programmed from 400mV$_{P-P}$ to 920mV$_{P-P}$ by applying a voltage to the SC pin. See the Output Signal Amplitude vs. SC Pin Voltage graph in the *Typical Operating Characteristics*.

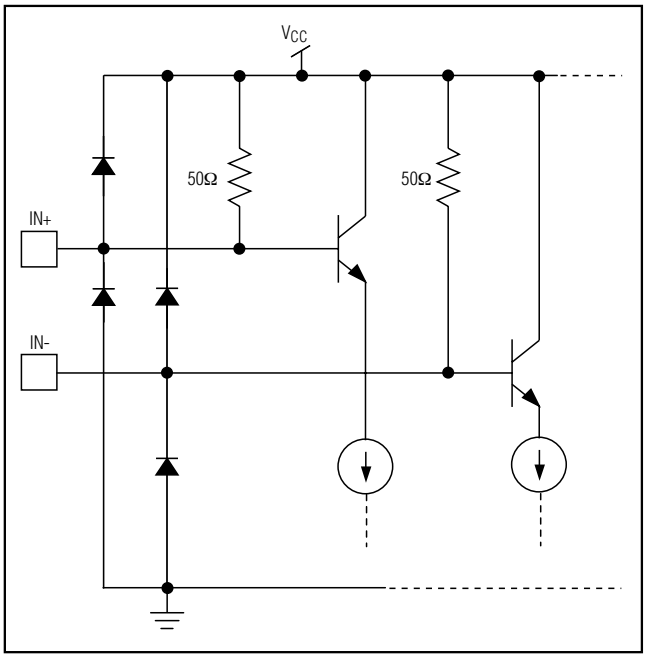


Figure 2. Input Interface

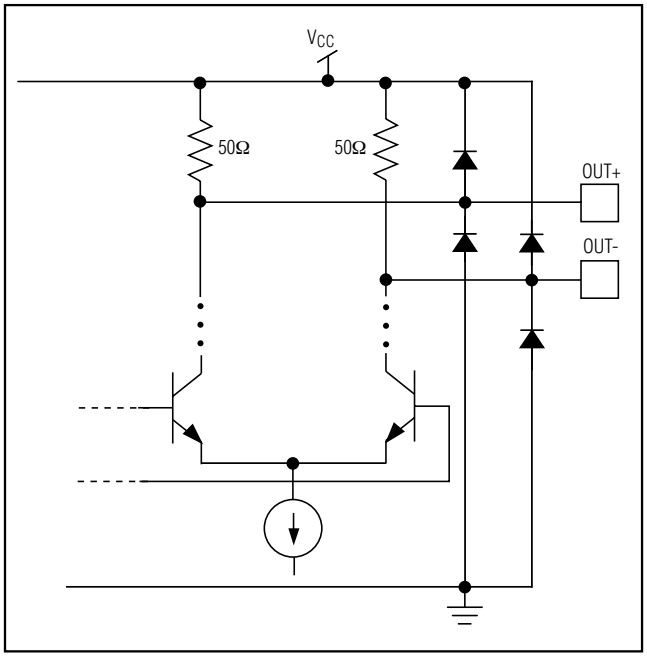


Figure 3. Output Interface

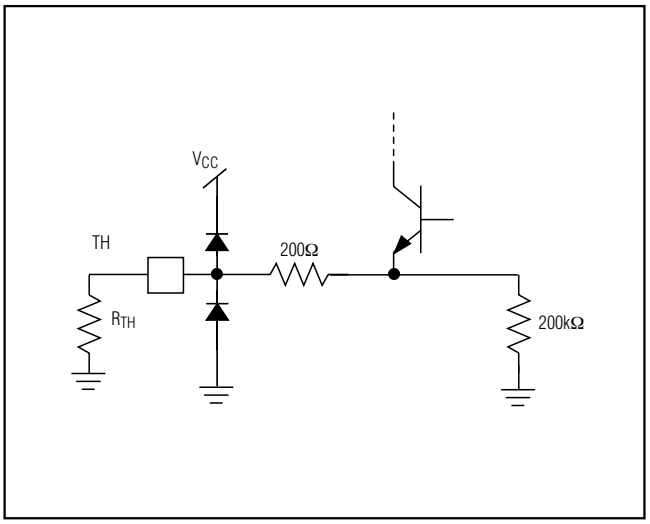


Figure 4. TH Interface

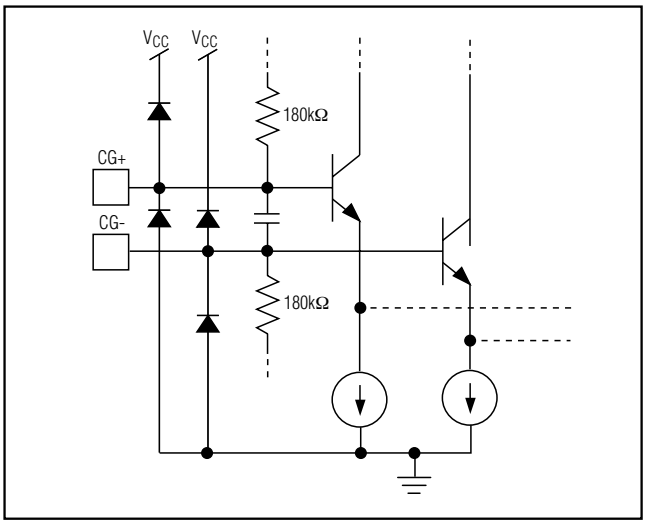


Figure 5. CG Interface

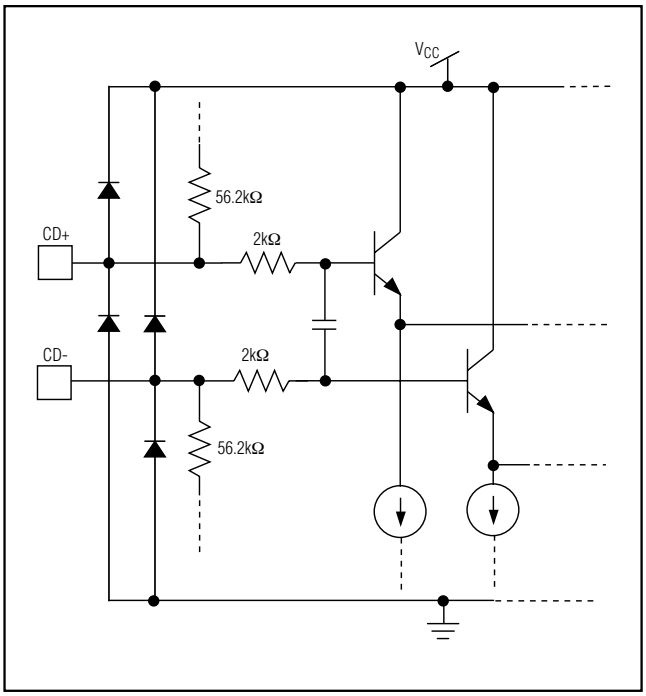


Figure 6. CD Interface

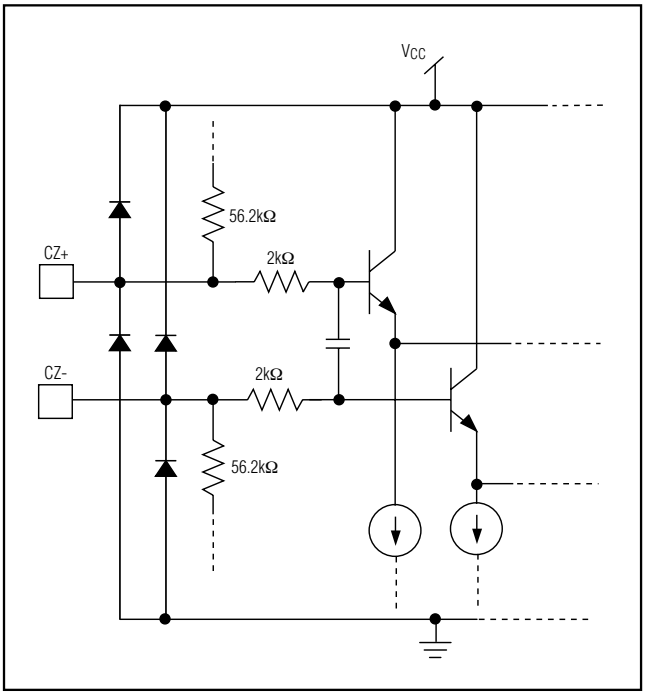
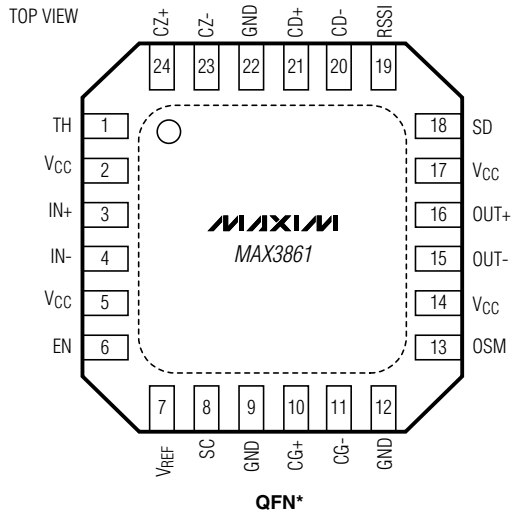


Figure 7. CZ Interface

2.7Gbps Post Amp with Automatic Gain Control

_____Pin Configurations (continued)



QFN*

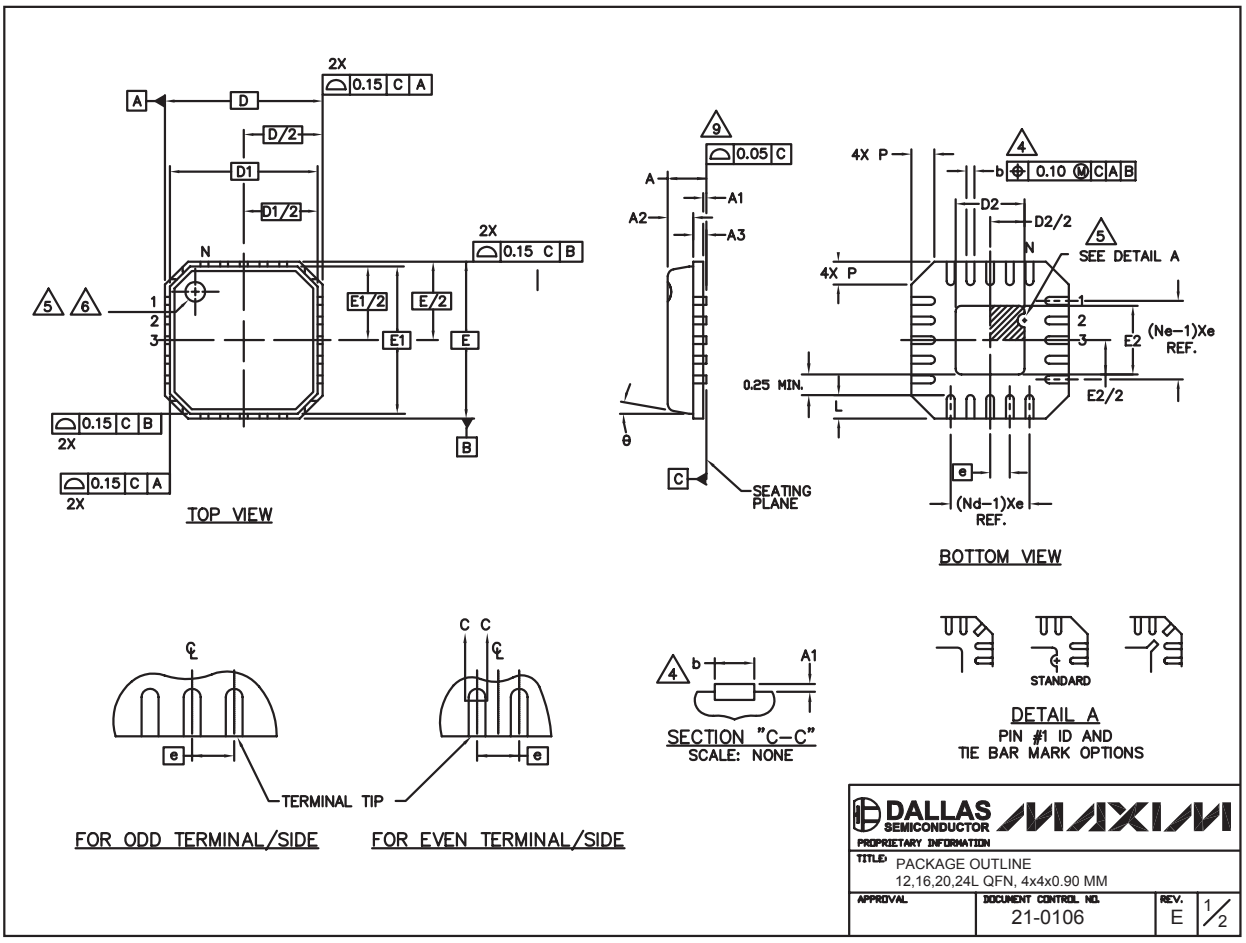
*__NOTE:__ MAXIM RECOMMENDS SOLDERING THE EXPOSED PAD TO GROUND.

2.7Gbps Post Amp with Automatic Gain Control

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



Chip Information

TRANSISTOR COUNT: 952

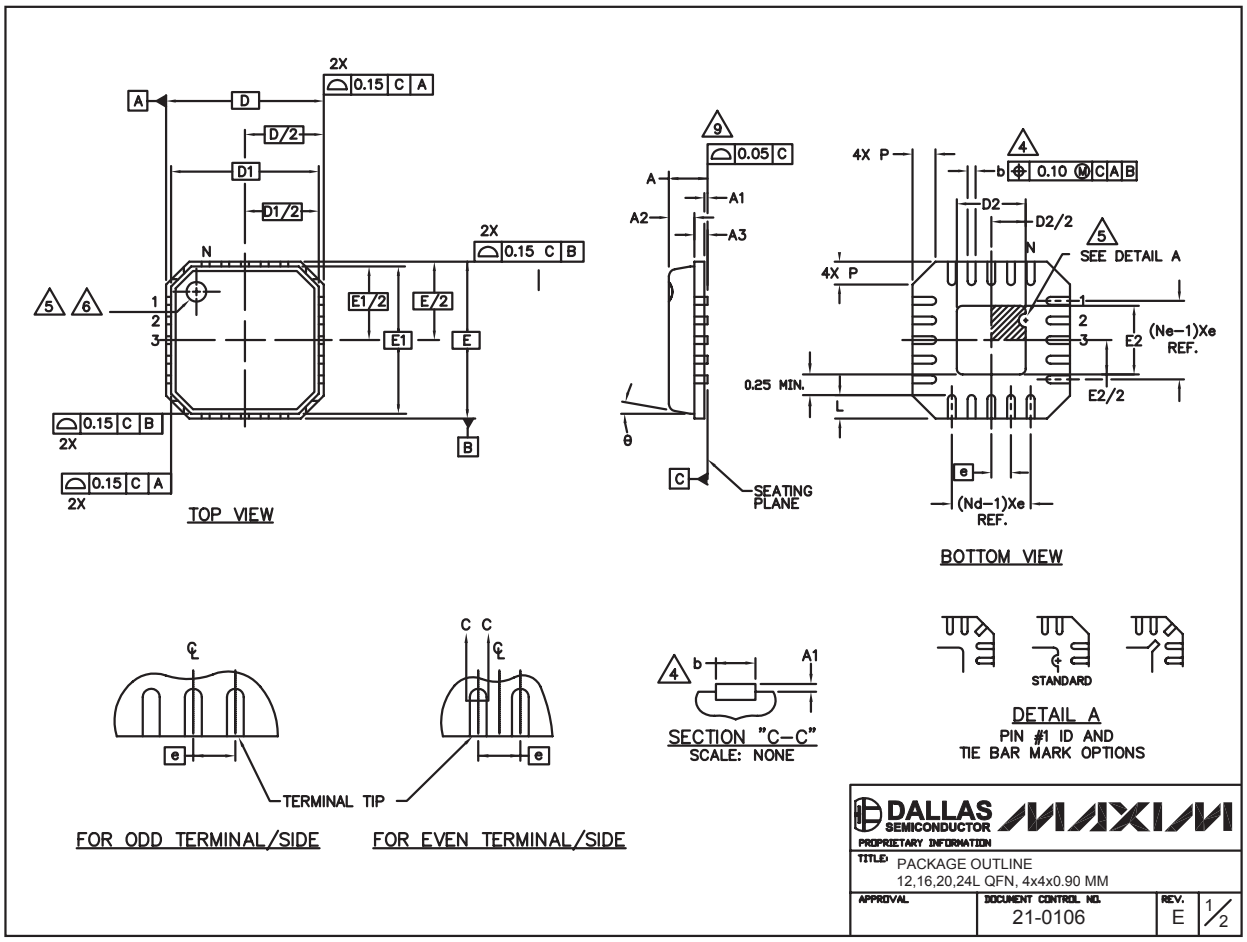
PROCESS: SiGe Bipolar

2.7Gbps Post Amp with Automatic Gain Control

Package Information (continued)

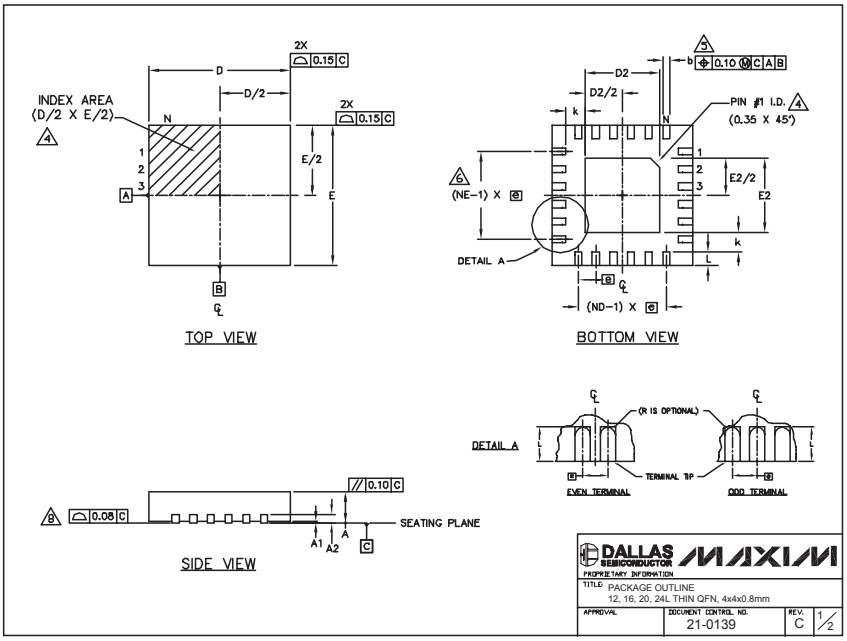
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. C
2/2

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