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MAX3949

11.3Gbps, Low-Power, AC-Coupled Laser Driver

General Description

The MAX3949 is a 3.3V, multirate, low-power laser diode driver designed for Ethernet, Fibre Channel, and SONET transmission systems at data rates up to 11.3Gbps. This device is optimized to drive a differential transmitter optical subassembly (TOSA) with a 25 Ω flex circuit. The unique design of the output stage enables use of unmatched TOSAs.

The device receives differential AC-coupled signals with on-chip termination. It can deliver laser modulation currents of up to 85mA at an edge speed of 22ps (20% to 80%) into a 5 Ω external differential load. The device is designed to have a high-bandwidth differential signal path with on-chip back termination resistors integrated into its outputs. An input equalization block can be activated to compensate for SFP+ host connector losses. The integrated bias circuit provides programmable laser bias currents up to 105mA. Both the laser bias current generator and the laser modulator can be disabled from a single pin.

The use of a 3-wire digital interface reduces the pin count while permitting adjustment of input equalization, polarity, output deemphasis, and modulation and bias currents without the need for external components. The device is available in a 3mm x 3mm, 16-pin TQFN package, and is specified for the -40°C to +95°C extended temperature range.

Benefits and Features

- ◆ **Low Power Consumption**
- ◆ **Saves Board Space**
 - ◇ **Small 3mm x 3mm Package**
- ◆ **Flexibility**
 - ◇ **Programmable Modulation Current Up to 85mA (5 Ω Load)**
 - ◇ **Programmable Bias Current Up to 105mA**
 - ◇ **Programmable Input Equalization and Output Deemphasis**
- ◆ **Safety**
 - ◇ **Supports SFF-8431 SFP+ MSA and SFF-8472 Digital Diagnostic**
 - ◇ **Integrated Eye Safety Features with Maskable Faults**
 - ◇ **Bias Current Monitor**

Applications

10GBASE-LR SFP+ Optical Transceivers
10GBASE-LRM SFP+ Optical Transceivers
OC192-SR SFP+ SDH/SONET Transceivers

[Ordering Information](#) appears at end of data sheet.

For related parts and recommended products to use with this part, refer to: www.maxim-ic.com/MAX3949.related

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ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{CCT}	-0.3V to +4.0V	Voltage Range at BIAS	0.4V to 2.5V
$ V_{CC} - V_{CCT} $	< 0.5V	Current into TOUTC and TOUTA	+150mA
Voltage Range at TIN+, TIN-, DISABLE, SDA, SCL, CSEL, VSEL, FAULT, and BMON.....	-0.3V to V_{CC}	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) TQFN (derate 20.8mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....	1666.7mW
Voltage Range at TOUTA, TOUTC	($V_{CCT} - 1.3\text{V}$) to ($V_{CCT} + 1.3\text{V}$)	Storage Temperature Range.....	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Current Range into TIN+ and TIN-.....	-20mA to +20mA	Die Attach Temperature	+400 $^\circ\text{C}$
Current Range into BIAS.....	0mA to +120mA	Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$
		Soldering Temperature (reflow)	+260 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	48 $^\circ\text{C}/\text{W}$
Junction-to-Case Thermal Resistance (θ_{JC})	10 $^\circ\text{C}/\text{W}$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{CCT} = 2.95\text{V}$ to 3.63V , $T_A = -40^\circ\text{C}$ to $+95^\circ\text{C}$; typical values are at $V_{CC} = V_{CCT} = 3.3\text{V}$, $T_A = +25^\circ\text{C}$, $I_{BIAS} = 60\text{mA}$, $I_{DMOD} = 40\text{mA}$, and 14Ω single-ended electrical output load, unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Excludes output current through the external pullup inductors (Note 3)		55	70	mA
Power-Supply Voltage	V_{CCT}, V_{CC}		2.95		3.63	V
POWER-ON RESET						
V_{CC} for Enable High				2.55	2.75	V
V_{CC} for Enable Low			2.3	2.45		V
DATA INPUT SPECIFICATION						
Input Data Rate			1	10.3	11.3	Gbps
Differential Input Voltage	V_{IN}	Launch amplitude into FR4 transmission line $\leq 12\text{in}$, SET_TXEQ[1:0] = 01b, SET_TXEQ[1:0] = 11b	0.2		0.8	V_{P-P}
		SET_TXEQ[1:0] = 01b, SET_TXEQ[1:0] = 11b, outside of optimized range	0.15		1.0	
		SET_TXEQ[1:0] = 00b	0.15		1.0	
Common-Mode Input Voltage	V_{CM}			2.15		V
Differential Input Resistance	R_{IN}		75	100	125	Ω

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{CCT} = 2.95V$ to $3.63V$, $T_A = -40^{\circ}C$ to $+95^{\circ}C$; typical values are at $V_{CC} = V_{CCT} = 3.3V$, $T_A = +25^{\circ}C$, $I_{BIAS} = 60mA$, $I_{DMOD} = 40mA$, and 14Ω single-ended electrical output load, unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input S-Parameters (Note 4)	SCD11	$0.1GHz \leq f \leq 11.3GHz$		-30		dB
	SDD11	$f \leq 4.1GHz$		-19		
		$4.1GHz \leq f \leq 11.3GHz$		-16		
	SCC11	$1GHz \leq f \leq 11.3GHz$, $Z_{CM_SOURCE} = 25\Omega$		-13		
BIAS CURRENT GENERATOR (Figure 3)						
Maximum BIAS DAC Current	$I_{BIASMAX}$	Current into BIAS pin	85	105		mA
Minimum BIAS DAC Current	$I_{BIASMIN}$	Current into BIAS pin			5	mA
BIAS-Off Current	$I_{BIAS-OFF}$				0.1	mA
BIAS DAC LSB Size				200		μA
BIAS DAC Integral Nonlinearity	INL	$5mA \leq I_{BIAS} \leq 85mA$		± 0.5		%FS
BIAS DAC Differential Nonlinearity	DNL	Guaranteed monotonic at 8-bit resolution, SET_IBIAS[8:1]		± 0.5		LSB
BIAS Current DAC Stability		$5mA \leq I_{BIAS} \leq 85mA$, $V_{BIAS} = 1.5V$ (Notes 5, 6)		1	4	%
BIAS Compliance Voltage			0.9	1.5	2.1	V
BMON Current Gain	G_{BMON}	$G_{BMON} = I_{BMON}/I_{BIAS}$, external resistor to GND defines voltage	8.5	9.6	11.8	mA/A
BMON Current Gain Stability		$5mA \leq I_{BIAS} \leq 85mA$, $V_{BIAS} = 1.5V$ (Notes 5, 6)		1.5	5	%
Compliance Voltage at BMON			0		1.8	V
LASER MODULATOR (Note 7)						
Maximum Laser Modulation Current	$I_{DMODMAX}$	Current into TOUTC pin, 5Ω laser load, 6.25% deemphasis	85			mA_{P-P}
Minimum Laser Modulation Current	$I_{DMODMIN}$	Current into TOUTC pin, 5Ω laser load, 6.25% deemphasis			10	mA_{P-P}
Modulation-Off Laser Current	$I_{DMOD-OFF}$	Current into TOUTC pin			0.1	mA
Modulation DAC Full-Scale Current	I_{MOD-FS}		99.7	130		mA
Modulation DAC LSB Size				247		μA
Modulation DAC Integral Nonlinearity	INL			± 1		%FS
Modulation DAC Differential Nonlinearity	DNL	Guaranteed monotonic at 8-bit resolution, SET_IMOD[8:1]		± 0.5		LSB
TOUTA and TOUTC Instantaneous Output Compliance Voltage		With external inductive pullup to V_{CCT}	$V_{CCT} - 1$		$V_{CCT} + 1$	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{CCT} = 2.95V$ to $3.63V$, $T_A = -40^{\circ}C$ to $+95^{\circ}C$; typical values are at $V_{CC} = V_{CCT} = 3.3V$, $T_A = +25^{\circ}C$, $I_{BIAS} = 60mA$, $LD_{MOD} = 40mA$, and 14Ω single-ended electrical output load, unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation Output Termination	R_{OUT}		19	25	31	Ω
Modulation Current DAC Stability		$10mA \leq LD_{MOD} \leq 85mA$, $V_{BIAS} = 1.5V$ (Notes 5, 6)		1.5	4	%
Modulation Current Rise/Fall Time	t_R, t_F	20% to 80%, $10mA \leq LD_{MOD} \leq 85mA$ (Note 5)		22	36	ps
Deterministic Jitter (Note 5)	DJ	$10mA \leq LD_{MOD} \leq 85mA$, 8.5Gbps with K28.5 pattern		4		psp-p
		$10mA \leq LD_{MOD} \leq 85mA$, 10.3125Gbps (Note 8)		6	12	
		$10mA \leq LD_{MOD} \leq 85mA$, 11.3Gbps (Note 8)		8	13	
Random Jitter	RJ	$10mA \leq LD_{MOD} \leq 85mA$ (Note 5)		0.19	0.55	psRMS
Differential S-Parameters (Note 4)	SCC22	$0.1GHz \leq f \leq 4.1GHz$, $Z_{CM_SOURCE} = 12.5\Omega$		-10		dB
		$4.1GHz < f \leq 11.3GHz$, $Z_{CM_SOURCE} = 12.5\Omega$		-5		
	SDD22	$0.1GHz < f \leq 11.3GHz$, $Z_{DIFF_SOURCE} = 50\Omega$		-13		
SAFETY FEATURES						
Threshold Voltage at BIAS		Fault never occurs for $V_{BIAS} \geq 0.55V$, fault always occurs for $V_{BIAS} < 0.35V$	0.35		0.55	V
Threshold Voltage at TOUTC		Fault never occurs for $V_{TOUTC} \geq V_{CCT} -$ 1.45, fault always occurs for $V_{TOUTC} <$ $V_{CCT} - 1.88$	$V_{CCT} -$ 1.88		$V_{CCT} -$ 1.45	V
Threshold Voltage at TOUTA		Fault never occurs for $V_{TOUTA} \geq V_{CCT} -$ 1.45V, fault always occurs for $V_{TOUTA} <$ $V_{CCT} - 1.88V$	$V_{CCT} -$ 1.88		$V_{CCT} -$ 1.45	V
Threshold Voltage at V_{CCT}		Fault never occurs for $V_{CCT} \geq V_{CC} - 0.27V$, fault always occurs for $V_{CCT} < V_{CC} - 0.6V$	$V_{CC} -$ 0.6		$V_{CC} -$ 0.27	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{CCT} = 2.95V$ to $3.63V$, $T_A = -40^{\circ}C$ to $+95^{\circ}C$; typical values are at $V_{CC} = V_{CCT} = 3.3V$, $T_A = +25^{\circ}C$, $I_{BIAS} = 60mA$, $LD_{MOD} = 40mA$, and 14Ω single-ended electrical output load, unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING REQUIREMENTS (Notes 5, 7)						
Initialization Time	t_{INIT}	$I_{BIAS} = 25mA$, $LD_{MOD} = 65mA$, bias and modulation DAC are both 0h, time from TX_EN = high to I_{BIAS} and LD_{MOD} at 90% of steady state		12		μs
DISABLE Assert Time	t_{OFF}	Time from rising edge of DISABLE input signal to I_{BIAS} and LD_{MOD} at 10% of steady state (Note 5)		3		μs
DISABLE Negate Time	t_{ON}	Time from falling edge of DISABLE to I_{BIAS} and LD_{MOD} at 90% of steady state (Note 5)		12		μs
FAULT Reset Time	$t_{RECOVER}$	Time from negation of latched fault using DISABLE to I_{BIAS} and LD_{MOD} at 90% of steady state		12		μs
FAULT Assert Time	t_{FAULT}	Time from fault to FAULT = high, $C_{FAULT} \leq 20pF$, $R_{FAULT} = 4.7k\Omega$		0.7	3	μs
DISABLE to Reset Time		Time DISABLE must be held high to reset fault	4			μs
DIGITAL I/O SPECIFICATIONS (SDA, SCL, CSEL, FAULT, DISABLE)						
Input High Voltage	V_{IH}		1.8		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Hysteresis	V_{HYST}			80		mV
Input Capacitance	C_{IN}				5	pF
DISABLE Input Resistance	R_{PULL}	Internal pullup resistor	4.7	7.5	10	$k\Omega$
Input Leakage Current (DISABLE)	I_{IH}	Input connected to V_{CC}			10	μA
	I_{IL}	Input connected to GND		440	775	
Input Leakage Current (SDA)	I_{IH}	Input connected to V_{CC}	-2		+2	μA
	I_{IL}	Input connected to GND, internal pullup is $75k\Omega$ typical	35		75	
Input Leakage Current (SCL, CSEL)	I_{IH}	Input connected to V_{CC} , internal pulldown is $75k\Omega$ typical	35		75	μA
	I_{IL}	Input connected to GND	-2		+2	
Output High Voltage (SDA, FAULT)	V_{OH}	External pullup is ($4.7k\Omega$ to $10k\Omega$) to V_{CC}	$V_{CC} - 0.1$			V
Output Low Voltage (SDA, FAULT)	V_{OL}	External pullup is ($4.7k\Omega$ to $10k\Omega$) to V_{CC}			0.4	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = V_{CCT} = 2.95V$ to $3.63V$, $T_A = -40^{\circ}C$ to $+95^{\circ}C$; typical values are at $V_{CC} = V_{CCT} = 3.3V$, $T_A = +25^{\circ}C$, $I_{BIAS} = 60mA$, $LD_{MOD} = 40mA$, and 14Ω single-ended electrical output load, unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (Figure 5)						
SCL Clock Frequency	f_{SCL}			400	1000	kHz
SCL Pulse-Width High	t_{CH}		500			ns
SCL Pulse-Width Low	t_{CL}		500			ns
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL Load	C_B	Total bus capacitance on one line with $4.7k\Omega$ pullup to V_{CC}			20	pF
VSEL FOUR-LEVEL DIGITAL INPUT (Table 2)						
Input Voltage High		3-wire address, ADDR[6:5] = 11b	$5/6V_{CC} + 0.2$		V_{CC}	V
Input Voltage Mid-High		3-wire address, ADDR[6:5] = 10b	$3/6V_{CC} + 0.2$	$2/3 \times V_{CC}$	$5/6V_{CC} - 0.2$	V
Input Voltage Mid-Low		3-wire address, ADDR[6:5] = 01b	$1/6V_{CC} + 0.2$	$1/3 \times V_{CC}$	$3/6V_{CC} - 0.2$	V
Input Voltage Low		3-wire address, ADDR[6:5] = 00b	0		$1/6V_{CC} - 0.2$	V

Note 2: Specifications at $T_A = -40^{\circ}C$ and $+95^{\circ}C$ are guaranteed by design and characterization.

Note 3: BIAS is connected to 1.9V. TOUTA and TOUTC are connected to V_{CCT} through pullup inductors.

Note 4: Measured with Agilent 8720ES + ATN-U112A and series RC (39Ω and $0.3pF$) between TOUTC and TOUTA ([Figure 1](#)).

Note 5: Guaranteed by design and characterization.

Note 6: Stability is defined as $[(I_{MEASURED}) - (I_{REFERENCE})]/(I_{REFERENCE})$ over the listed current/temperature range and $V_{CCT} = V_{CC} = V_{CCREF} \pm 5\%$, $V_{CCREF} = 3.3V$. Reference current measured at V_{CCREF} and $T_{REF} = +25^{\circ}C$.

Note 7: $LD_{MOD} = I_{MOD} \times (1 - DE) \times 50/(50 + R)$, where LD_{MOD} is the effective laser modulation current, I_{MOD} is the modulation DAC current, DE is the deemphasis percentage, and R is the differential laser load resistance. Example: For $R\Omega = 5$ and $DE = 6.25\%$, $LD_{MOD} = 0.852 \times I_{MOD}$.

Note 8: Equivalent $2^{23} - 1$ PRBS pattern = $2^7 - 1$ PRBS + 72 zeros + $2^7 - 1$ PRBS + 72 ones.

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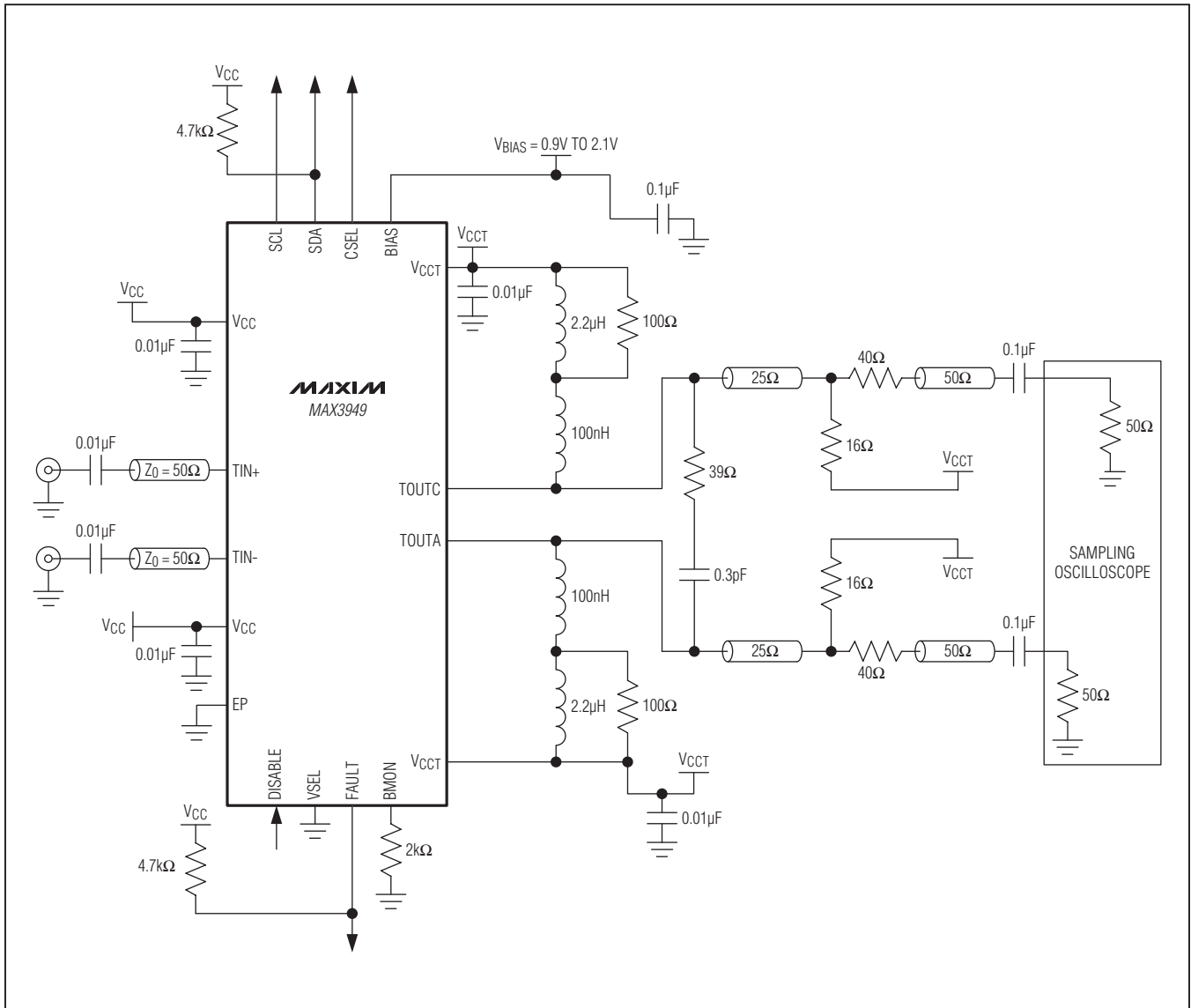


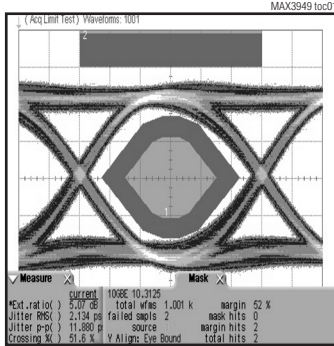
Figure 1. AC Test Setup

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Typical Operating Characteristics

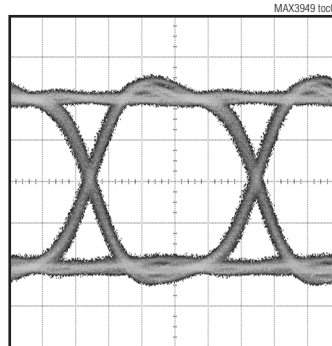
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10.3Gbps OPTICAL EYE DIAGRAM



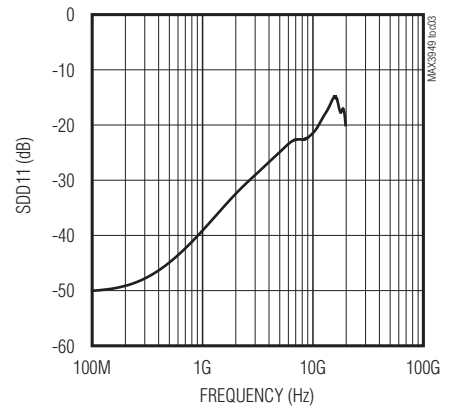
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10Gbps ELECTRICAL EYE DIAGRAM

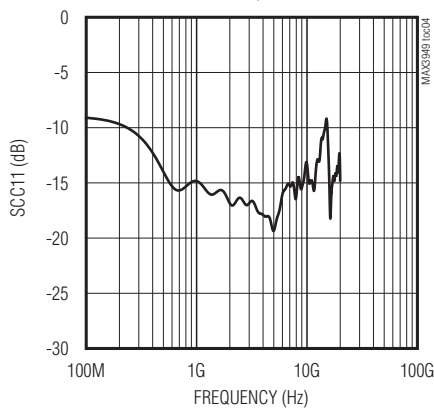


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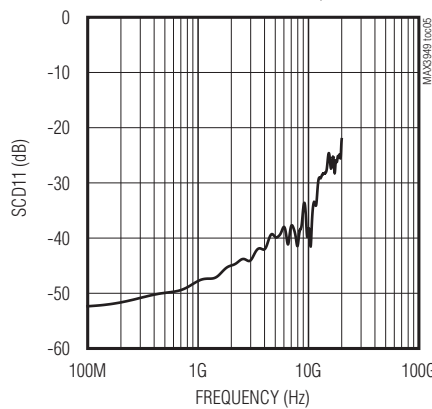
INPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



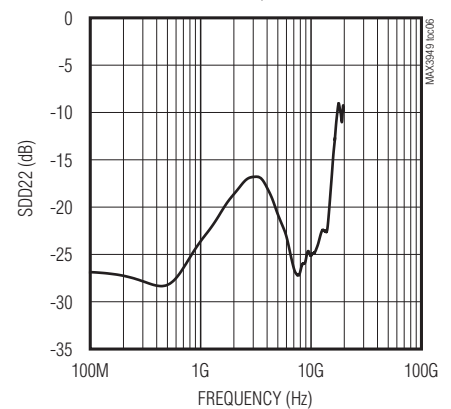
INPUT COMMON-MODE RETURN LOSS vs. FREQUENCY



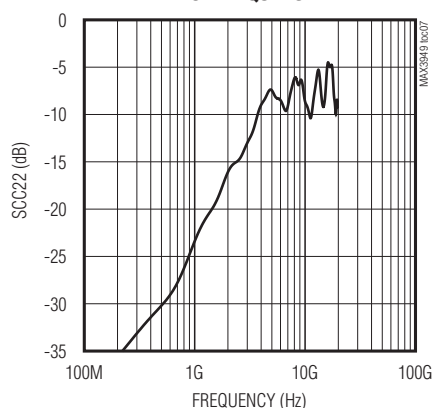
INPUT DIFFERENTIAL TO COMMON-MODE RETURN LOSS vs. FREQUENCY



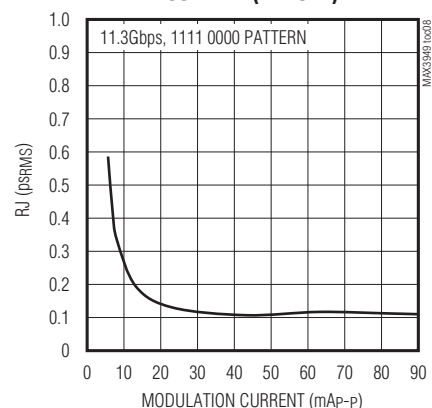
OUTPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



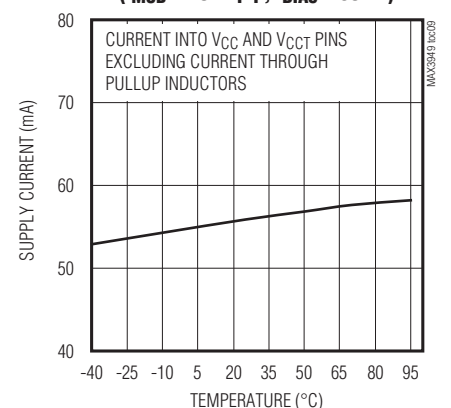
OUTPUT COMMON-MODE RETURN LOSS vs. FREQUENCY



RANDOM JITTER vs. MODULATION CURRENT (AT LOAD)



SUPPLY CURRENT vs. TEMPERATURE (I_{MOD} = 40mA_{P-P}, I_{BIAS} = 60mA)

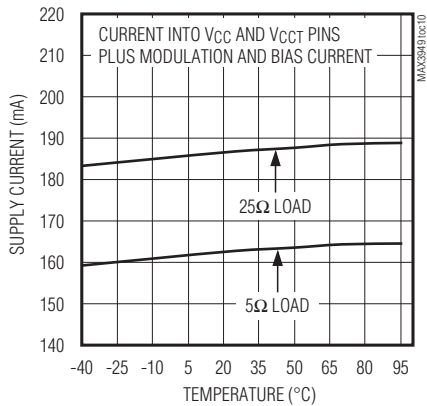


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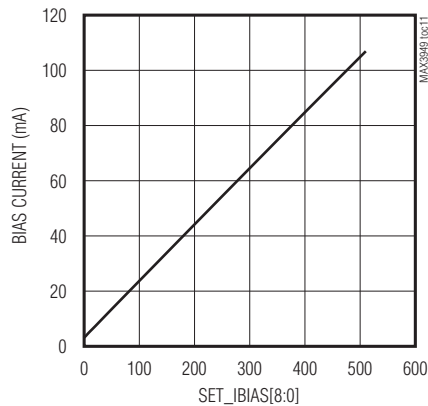
Typical Operating Characteristics (continued)

(Typical values are at $V_{CC} = V_{CCCT} = 3.3V$, $T_A = +25^\circ C$, data pattern = $2^7 - 1$ PRBS + 72 zeros + $2^7 - 1$ PRBS (inverted) + 72 ones, unless otherwise noted.)

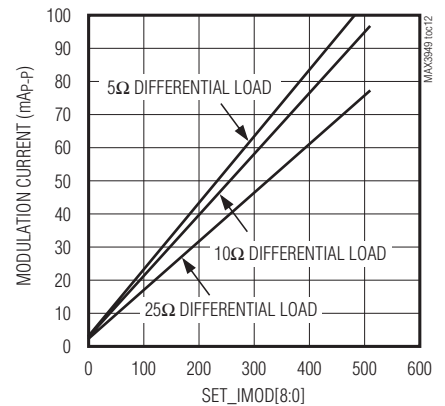
TOTAL CURRENT vs. TEMPERATURE
(I_{MOD} AT LOAD = 40mA-p-p, $I_{BIAS} = 60mA$)



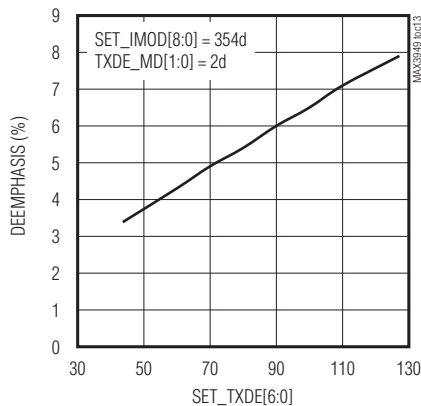
BIAS CURRENT vs. DAC SETTING



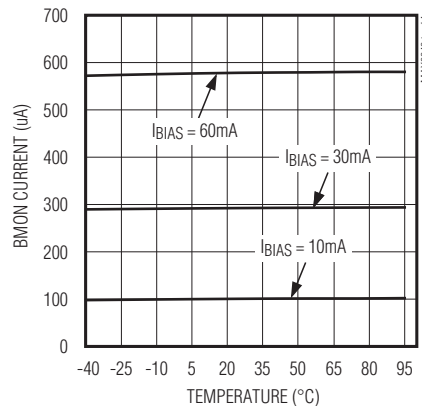
MODULATION CURRENT (AT LOAD) vs. DAC SETTING



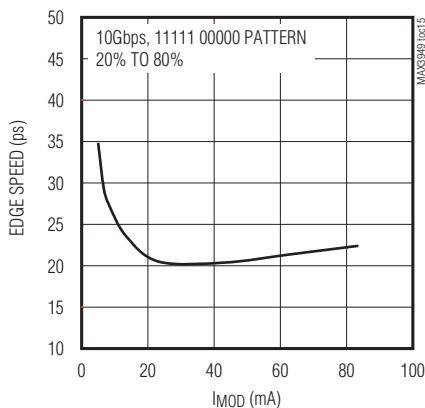
MODULATION CURRENT DEEMPHASIS vs. MANUAL DEEMPHASIS SETTING



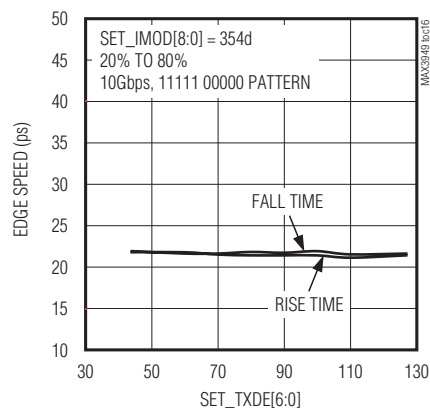
BIAS MONITOR CURRENT vs. TEMPERATURE



EDGE SPEED vs. MODULATION CURRENT



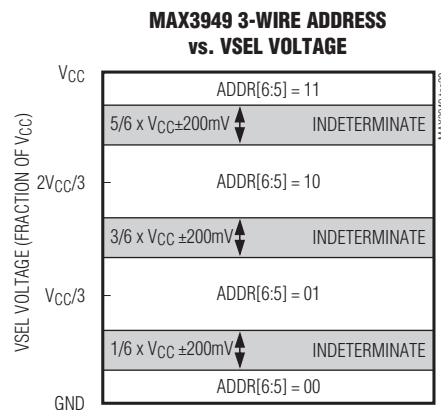
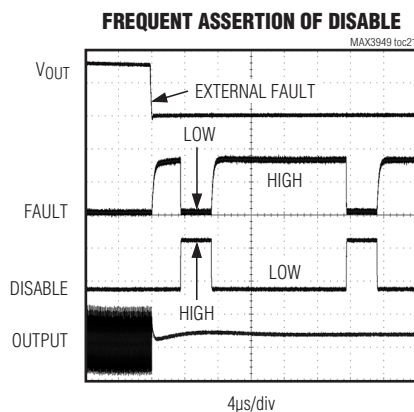
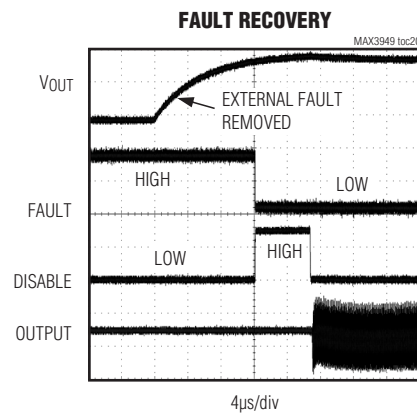
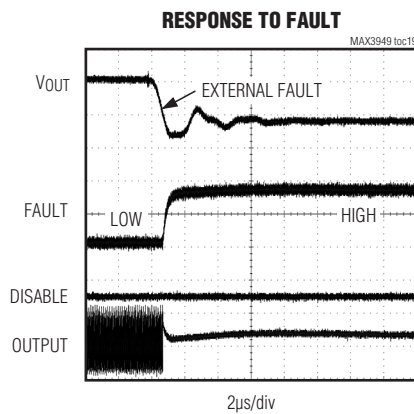
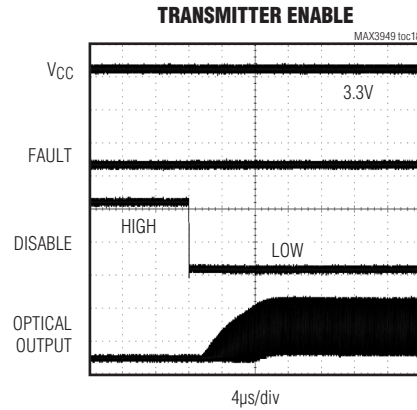
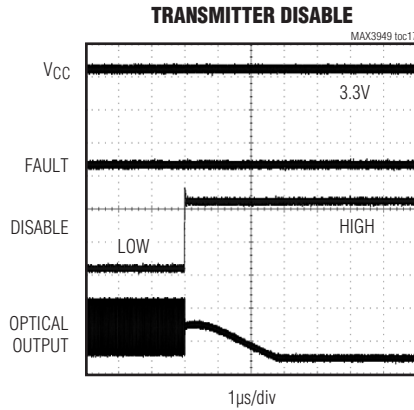
EDGE SPEED vs. DEEMPHASIS SETTING



11.3Gbps, Low-Power, AC-Coupled Laser Driver

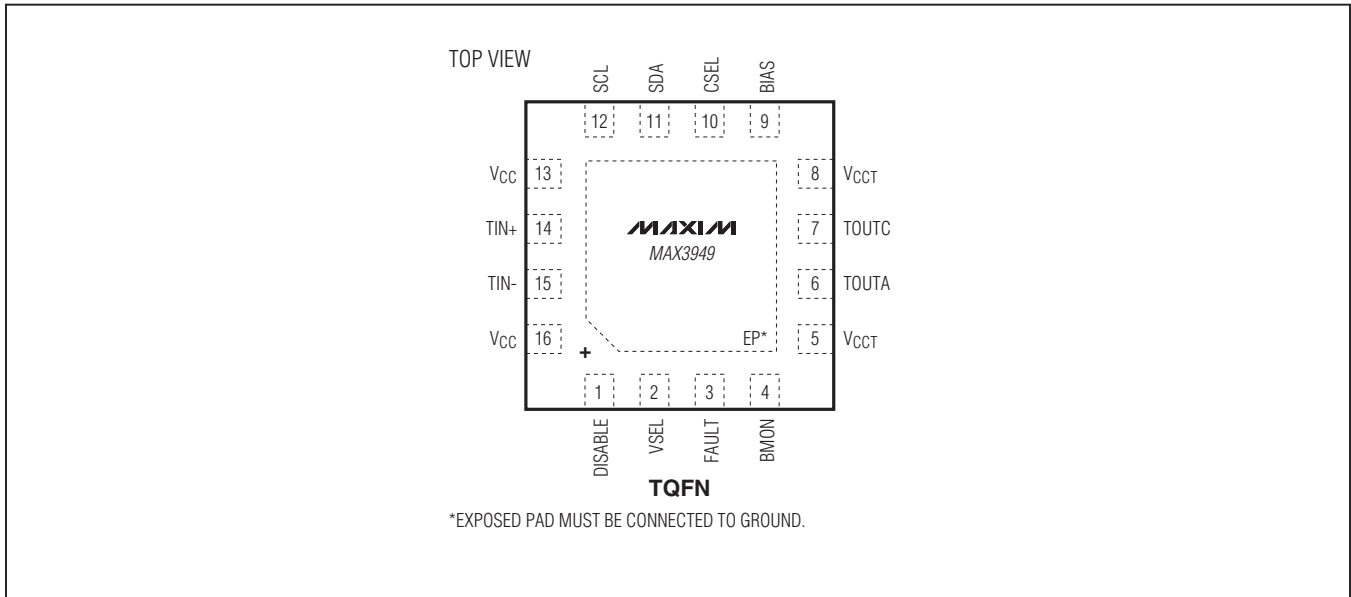
Typical Operating Characteristics (continued)

(Typical values are at $V_{CC} = V_{CCT} = 3.3V$, $T_A = +25^\circ C$, data pattern = $2^7 - 1$ PRBS + 72 zeros + $2^7 - 1$ PRBS (inverted) + 72 ones, unless otherwise noted.)



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Pin Configuration



Pin Description

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	DISABLE	Disable Input, CMOS. Set to logic-low for normal operation. Logic-high or open disables both the modulation current and the bias current. Internally pulled up by a 7.5kΩ resistor to V _{CC} .	
2	VSEL	4-Level Input for SPI Device Address Detection. Connecting to V _{CC} sets ADDR[6:5] to 11b, connecting to V _{CC} x 2/3 sets ADDR[6:5] to 10b, connecting to V _{CC} /3 sets ADDR[6:5] to 01b, and connecting to GND sets ADDR[6:5] to 00b.	

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Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
3	FAULT	Fault Output, Open Drain. Logic-high indicates a fault condition has been detected. It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by toggling DISABLE. FAULT should be pulled up to V_{CC} by a 4.7k Ω to 10k Ω resistor.	
4	BMON	Analog Laser Bias Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the BIAS pin current. The current sourced by this pin is typically 1/104 the BIAS pin current.	
5,8	V_{CCT}	Power Supply. Provides supply voltage to the output block.	—
6	TOUTA	Inverting Laser Diode Modulation Current Output. Connect this pin to the anode of the laser diode.	
7	TOUTC	Noninverting Laser Diode Modulation Current Output. Connect this pin to the cathode of the laser diode.	

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Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
9	BIAS	Combined Current Return Path and Laser BIAS Current Output	
10	CSEL	Chip-Select CMOS Input. Setting CSEL to logic-high starts a 3-wire command cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down to GND by a 75kΩ resistor.	
11	SDA	Serial Data Bidirectional CMOS Input. Also an open-drain output. This pin has a 75kΩ internal pullup, but requires an external 4.7kΩ to 10kΩ pullup resistor to VCC for proper operation.	
12	SCL	Serial-Clock CMOS Input. This pin has an internal 75kΩ pulldown resistor to GND.	

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Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
13, 16	V _{CC}	Power Supply. Provides supply voltage to core analog and digital circuitry.	—
14	TIN+	Noninverting Data Input. Input with internal 50Ω termination.	
15	TIN-	Inverting Data Input. Input with internal 50Ω termination.	
—	EP	Exposed Pad (Ground). This is the only electrical connection to ground on the MAX3949 and must be soldered to the circuit board ground for proper thermal and electrical performance (see the <i>Exposed-Pad Package</i> section).	—

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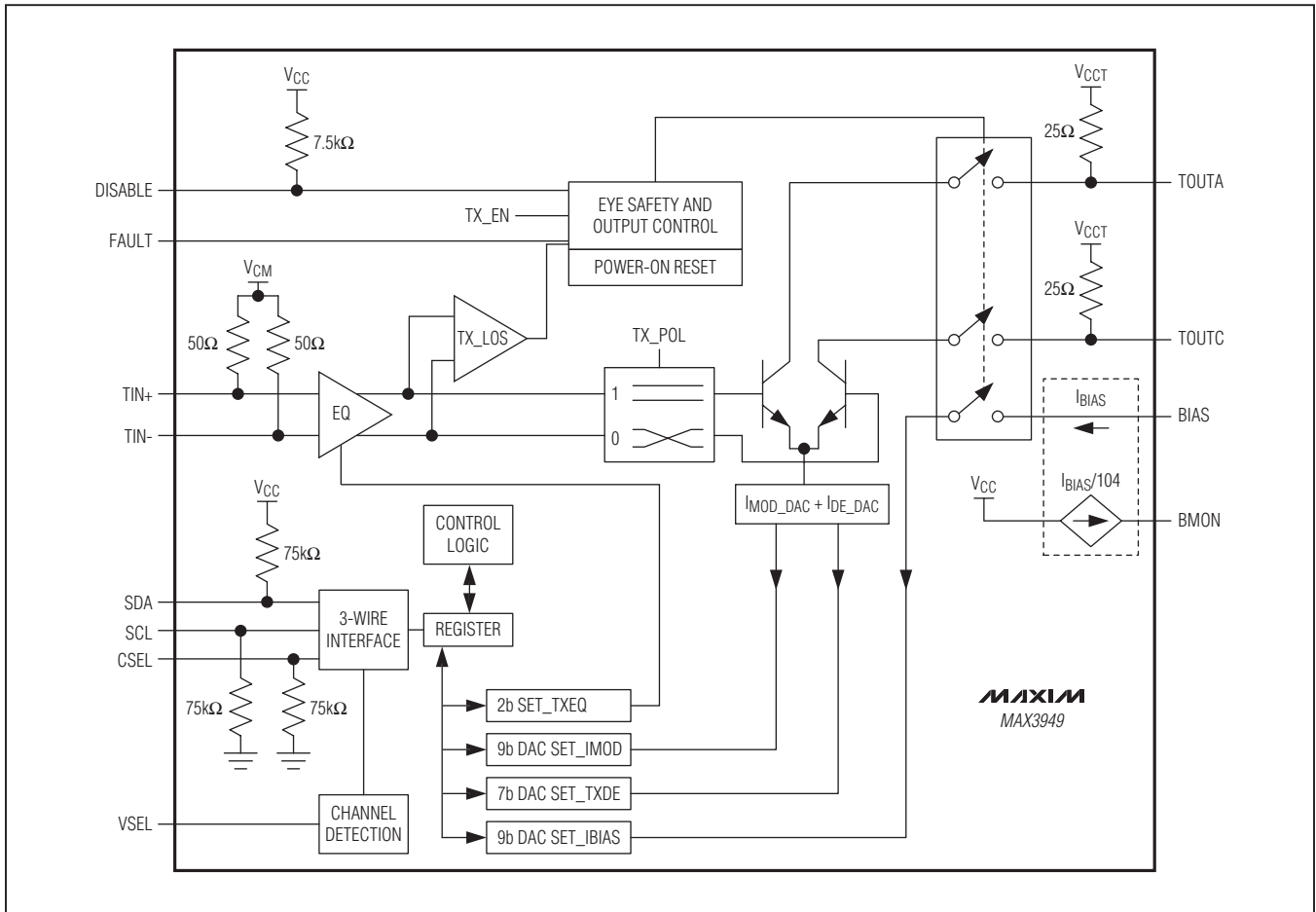


Figure 2. Functional Diagram

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Detailed Description

The MAX3949 SFP+/QSFP+ laser driver is designed to drive 5Ω to 10Ω TOSAs from 1Gbps to 11.3Gbps. It contains an input buffer with programmable equalization, bias and modulation current DACs, an output driver with adjustable deemphasis, power-on-reset circuitry, bias current monitor, programmable 3-wire address, and eye safety circuitry with maskable fault monitors. A 3-wire digital interface is used to control these functions.

Input Buffer with Programmable Equalization

The input is internally biased and terminated with 50Ω to a common-mode voltage. The first amplifier stage features a programmable equalizer for high-frequency losses including a SFP+/QSFP+ host connector. Equalization is controlled by the SET_TXEQ register (Table 1). The TX_POL bit in the TXCTRL register controls the polarity of TOUTA and TOUTC vs. TIN+ and TIN-. A status indicator bit (TXSTAT1 bit 5) monitors the presence of an AC input signal.

Table 1. Input Equalization Control Register Settings

SET_TXEQ[1:0]		BOOST AT 5.16GHz (dB)
0	0	1
0	1	3
1	1	5.5

Bias Current DAC

The bias current from the device is optimized to provide up to 105mA of bias current into a laser diode with 200μA resolution (Figure 3). The bias DAC current is controlled through the 3-wire digital interface using the SET_IBIAS[8:0], IBIASMAX[7:0], and BIASINC[4:0] bits.

For laser operation, the laser bias current can be set using the 9-bit SET_IBIAS DAC register. The upper 8 bits are set by the SET_IBIAS[8:1] register, commonly used during the initialization procedure after power-on reset (POR). The LSB (bit 0) of SET_IBIAS (BIASINC[7]) is initialized to zero after POR and can be updated using

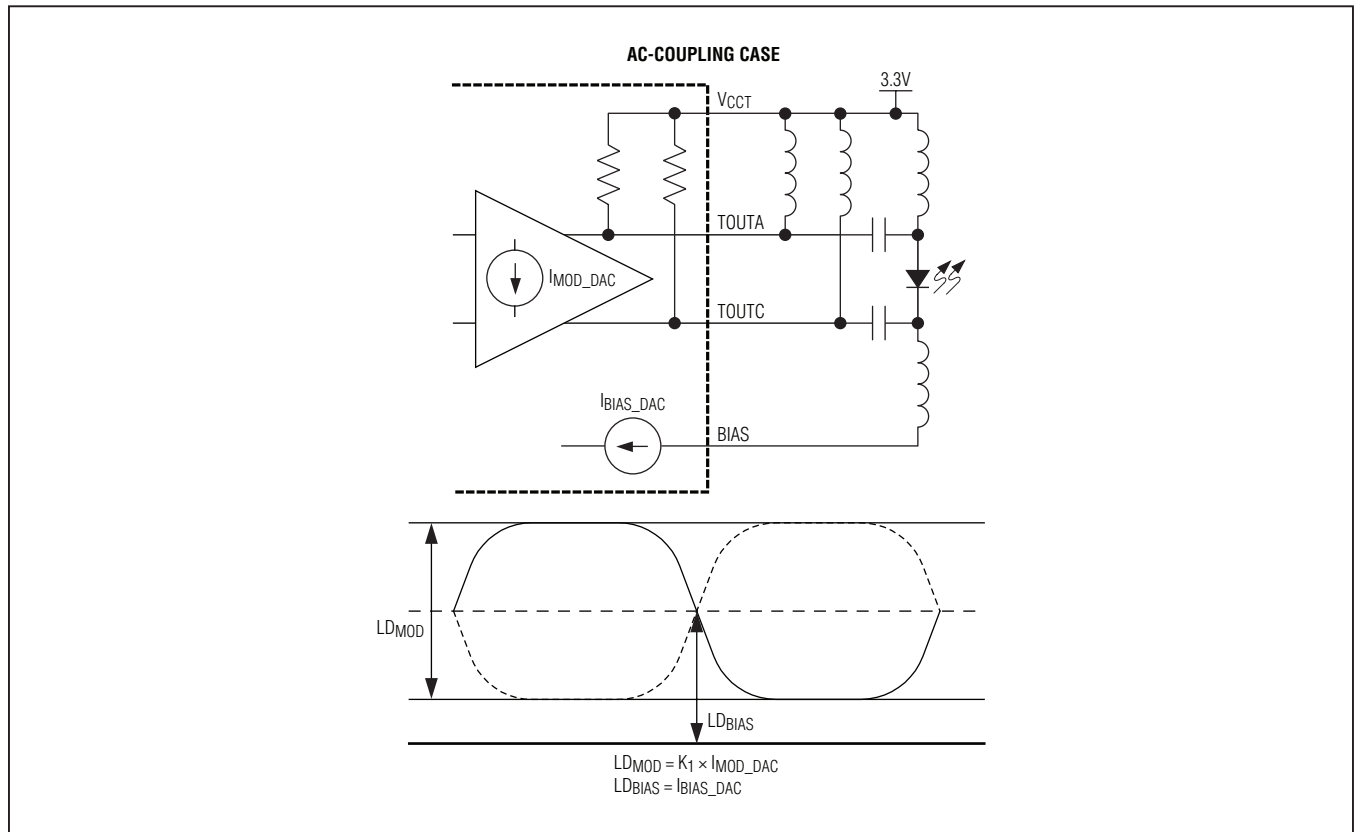


Figure 3. AC-Coupling Case

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the [BIASINC](#) register. The [IBIASMAX](#) register limits the maximum [SET_IBIAS](#)[8:1] DAC code.

After initialization the value of the [SET_IBIAS](#) DAC register should be updated using the [BIASINC](#) register to optimize cycle time and enhance laser safety. The [BIASINC](#) register is an 8-bit register. The first 5 bits of [BIASINC](#) contain the increment information in two's complement format. Increment values range from -16 to +15 LSBs. If the updated value of [SET_IBIAS](#)[8:1] exceeds [IBIASMAX](#)[7:0], the [IBIASERR](#) warning flag is set and [SET_IBIAS](#)[8:1] is set to [IBIASMAX](#)[7:0].

Modulation Current DAC

The modulation current from the MAX3949 is optimized to provide up to 85mA of modulation current into a 5Ω laser load with 210μA resolution. The modulation current is controlled through the 3-wire digital interface using the [SET_IMOD](#)[8:1], [IMODMAX](#)[7:0], [MODINC](#)[7:0], and [SET_TXDE](#) registers.

For laser operation, the laser modulation current can be set using the 9-bit [SET_IMOD](#) DAC. The upper 8 bits are programmed through the [SET_IMOD](#)[8:1] register, commonly used during the initialization procedure after POR. The LSB (bit 0) of [SET_IMOD](#) ([MODINC](#)[7]) is initialized to zero after POR and can be updated using the [MODINC](#) register. The [IMODMAX](#) register limits the maximum [SET_IMOD](#)[8:1] DAC code.

After initialization the value of the [SET_IMOD](#) DAC register should be updated using the [MODINC](#)[4:0] bits to optimize cycle time and enhance laser safety. The [MODINC](#) register is an 8-bit register. The first 5 bits of [MODINC](#) contain the increment information in two's complement format. Increment values range from -16 to +15 LSBs. If the updated value of [SET_IMOD](#)[8:1] exceeds [IMODMAX](#)[7:0], the [IMODERR](#) warning flag is set and [SET_IMOD](#)[8:1] is set to [IMODMAX](#)[7:0].

Effective modulation current seen by the laser is actually the combination of the DAC current generated by the [SET_IMOD](#)[8:0] register (I_{MOD}), deemphasis setting (DE), and differential laser load (R). It is calculated by the following formula:

$$LD_{MOD} = I_{MOD} \times 50 \times (1 - DE) / (50 + R)$$

Output Driver

This device is optimized to drive a differential TOSA with a 25Ω flex circuit. The unique design of the output stage

enables DC-coupling to unmatched TOSAs with laser diode impedances ranging from 5Ω to 10Ω. The output stage also features programmable deemphasis that can be set as a percentage of the modulation current. The deemphasis function is controlled by the [TXCTRL](#)[4:3] and the [SET_TXDE](#) registers.

Power-On Reset (POR)

Power-on reset ensures that the laser is off until the supply voltage has reached a specified threshold (2.75V). After power-on reset, [TX_EN](#) is 0 and bias current and modulation current DACs default to small codes. In the case of a POR, all registers are reset to their default values.

BMON Function

The current out of the [BMON](#) pin is typically 1/104th the value of the current into the [BIAS](#) pin. The total resistance to ground at [BMON](#) sets the voltage.

VSEL Function

The [VSEL](#) pin is an analog input that sets the 3-wire address for the MAX3949. The pin can be set to either V_{CC} , $V_{CC} \times 2/3$, $V_{CC}/3$, or to GND ([Table 2](#)). This allows up to four MAX3949s to be operated on a single 3-wire bus, each with their own address.

Table 2. 3-Wire Address Selection

VSEL	ADDR[6:5]
V_{CC}	11b
$V_{CC} \times 2/3$	10b
$V_{CC}/3$	01b
GND	00b

Eye Safety and Output Control Circuitry

The safety and output control circuitry includes the disable pin ([DISABLE](#)) and enable bit ([TX_EN](#)), along with a [FAULT](#) indicator and fault detectors ([Figure 4](#)). A fault condition triggers the [FAULT](#) pin to go high and a corresponding bit is set in the [TXSTAT1](#) register. The MAX3949 has two types of faults: hard faults and soft faults. Hard faults are maskable, trigger the [FAULT](#) pin (transitions high), disable the outputs and are stored in the [TXSTAT1](#) register. Soft faults serve as warnings, do not disable the outputs, and are stored in the [TXSTAT2](#) register.

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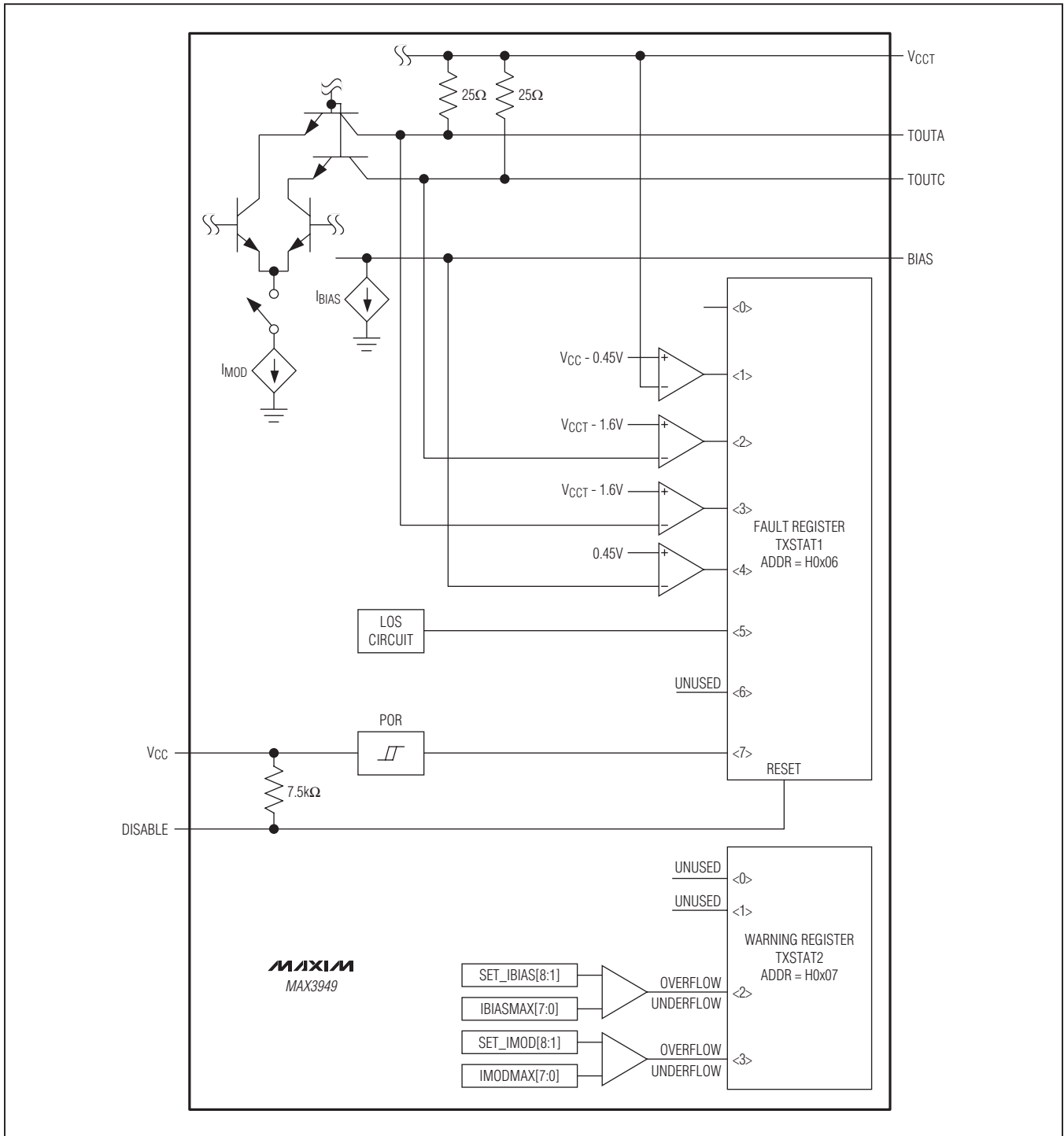


Figure 4. Eye Safety Circuitry

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The FAULT pin is a latched output that can be cleared by toggling the DISABLE pin. Toggling the DISABLE pin also clears the [TXSTAT1](#) and [TXSTAT2](#) registers. A single-point

failure can be a short to V_{CC} or GND. [Table 3](#) shows the circuit response to various single-point failures.

Table 3. Circuit Response to Single-Point Failure

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
1	DISABLE	Disabled	Normal (Note 1). Can only be disabled by other means.	Disabled
2	VSEL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
3	FAULT	Normal (Note 2)	Normal (Note 1)	Normal (Note 2)
4	BMON	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
5, 8	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 3)	Redundant path (Note 4)
6	TOUTA	Laser modulation current is reduced	Disabled (hard fault)	Laser modulation current is reduced or disabled (hard fault)
7	TOUTC	Laser modulation current is reduced or off	Disabled (hard fault)	Laser modulation current is reduced or disabled (hard fault)
9	BIAS	I_{BIAS} is on, but not delivered to the laser; no fault	Disabled (hard fault)	Disabled (hard fault)
10	CSEL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
11	SDA	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
12	SCL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
13, 16	V_{CC}	Normal	Disabled—Hard fault (external supply shorted) (Note 3)	Redundant path (Note 4)
14	TIN+	Disabled (hard fault)	Disabled (hard fault)	Normal (Note 2) or disabled (hard fault)
15	TIN-	Disabled (hard fault)	Disabled (hard fault)	Normal (Note 2) or disabled (hard fault)

Note 1: Normal operation—Does not affect the laser power.

Note 2: Pin functionality might be affected, which could affect laser power/performance.

Note 3: Supply-shortened current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.

Note 4: Normal in functionality, but performance could be affected.

Warning: Shorted to V_{CC} or shorted to ground on some pins can violate the [Absolute Maximum Ratings](#).

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3-Wire Interface

The MAX3949 implements a proprietary 3-wire digital interface. An external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, a SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. The master starts to generate a clock signal after the CSEL pin has been set to a logic-high. All data transfers are most significant bit (MSB) first.

Protocol

Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3949. The RWN bit determines if the cycle is read or write ([Table 5](#)).

Register Addresses

The MAX3949 contains 13 registers available for programming. [Table 6](#) shows the registers and addresses.

Write Mode (RWN = 0)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes

the transmission by setting CSEL to 0. [Figure 5](#) shows the interface timing.

Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. [Figure 5](#) shows the interface timing.

Mode Control

Normal mode allows read-only instruction for all registers. Only the [MODINC](#) and [BIASINC](#) registers can be updated during normal mode. Doing so speeds up the laser control update through the 3-wire interface by a factor of two. The normal mode is the default mode.

Setup mode allows the master to write unrestricted data into any register except the status ([TXSTAT1](#), [TXSTAT2](#)) registers. To enter the setup mode, the [MODECTRL](#) register (address = H0x0F) must be set to 12h. After the [MODECTRL](#) register has been set to 12h, the next operation is unrestricted. The setup mode is automatically exited after the operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

Broadcast mode allows for faster configuration of multiple MAX3949 ICs by causing the address selection bits (ADDR[6:5]) to be ignored so all MAX3949s on the bus can be written to simultaneously.

A block write in broadcast mode can start at any of the addresses in [Table 4](#). The block write is achieved by holding the CSEL pin high to lengthen the SPI cycle. The register address increments automatically through the sequence listed in [Table 4](#) and wraps from [TXCTRL](#) to [FMSK](#). The block write ends once the CSEL pin is asserted low.

Table 4. Broadcast Mode Register Initialization Sequence

ADDRESS	NAME
H0x0F	FMSK
H0x10	SET_TXDE
H0x11	SET_TXEQ
H0x0A	IMODMAX
H0x0B	IBIASMAX
H0x08	SET_IBIAS
H0x09	SET_IMOD
H0x05	TXCTRL

Table 5. Digital Communication Word Structure

BIT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[6:0]							RWN	DATA[7:0]							

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Table 6. Register Descriptions and Addresses

ADDRESS	NAME	FUNCTION
H0x05	TXCTRL	Transmitter Control Register
H0x06	TXSTAT1	Transmitter Status Register 1
H0x07	TXSTAT2	Transmitter Status Register 2
H0x08	SET_IBIAS	Bias Current Setting Register
H0x09	SET_IMOD	Modulation Current Setting Register
H0x0A	IMODMAX	Maximum Modulation Current Setting Register
H0x0B	IBIASMAX	Maximum Bias Current Setting Register
H0x0C	MODINC	Modulation Current Increment Setting Register
H0x0D	BIASINC	Bias Current Increment Setting Register
H0x0E	MODECTRL	Mode Control Register
H0x0F	FMSK	Fault Mask Register
H0x10	SET_TXDE	Transmitter Deemphasis Control Register
H0x11	SET_TXEQ	Transmitter Equalization Control Register

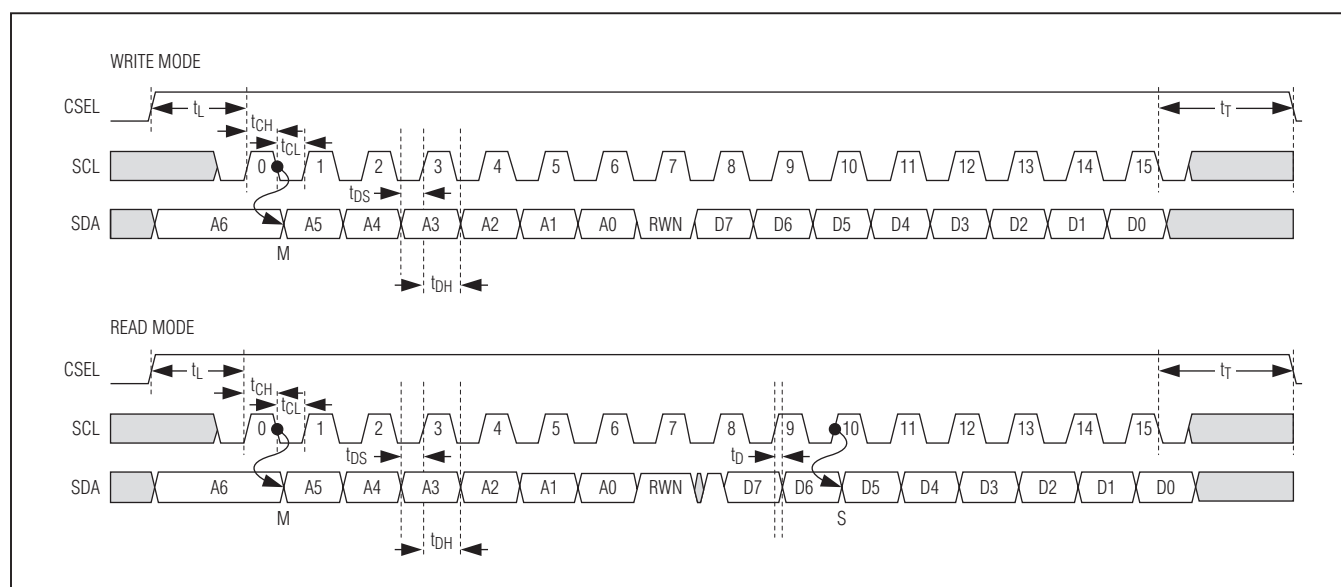


Figure 5. Timing for 3-Wire Digital Interface

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Register Descriptions

Transmitter Control Register (TXCTRL), Address: H0x05

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED	RESERVED	RESERVED	TXDE_MD[1]	TXDE_MD[0]	SOFTRES	TX_POL	TX_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	1	0

The TXCTRL register sets the device's operation.

BIT	NAME	DESCRIPTION
D[7:5]	RESERVED	Reserved Bits. The default state for these bits is 0 and they must be kept 0 when the register is accessed for a write operation.
D[4:3]	TXDE_MD	Controls the mode of the transmit output deemphasis circuitry. 00 = Deemphasis is fixed at 6% of the modulation amplitude 01 = Deemphasis is fixed at 3% of the modulation amplitude 10 = Deemphasis is programmed by SET_TXDE register setting (3% to 9%) 11 = Deemphasis is at its maximum of ~9%
D2	SOFTRES	Resets all registers to their default values (TXCTRL[1:0] must be = 10b during the write to SOFTRES for the registers to be set to their default values). 0 = Normal operation 1 = Reset
D1	TX_POL	Controls the polarity of the transmit signal path. 0 = Inverse 1 = Normal operation
D0	TX_EN	Enables or disables the transmit circuitry. 0 = Disabled 1 = Enabled

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Transmitter Status Register 1 (TXSTAT1), Address: H0x06

Bit	D7 (STICKY)	D6 (STICKY)	D5 (STICKY)	D4 (STICKY)	D3 (STICKY)	D2 (STICKY)	D1 (STICKY)	D0 (STICKY)
Bit Name	FST[7]	FST[6]	FST[5]	FST[4]	FST[3]	FST[2]	FST[1]	FST[0]
Read/Write	R	R	R	R	R	R	R	R
POR State	1	X	X	X	X	X	X	X
Reset Upon Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

The TXSTAT1 register is a device status register.

BIT	NAME	DESCRIPTION
D7	FST[7]	When the V_{CC} supply voltage is below 2.3V, the POR circuitry reports a FAULT and communication to the SPI cannot be performed . Once the V_{CC} supply voltage is above 2.75V, the POR resets all registers to their default values and the FAULT latch is cleared.
D6	FST[6]	Reserved.
D5	FST[5]	Indicates low or no AC signal at the inputs, a hard fault is reported unless masked.
D4	FST[4]	Indicates BIAS open or shorted to GND condition, threshold = 0.45V.
D3	FST[3]	Indicates TOUTA open or shorted to GND condition, threshold = $V_{CCT} - 1.6V$, a hard fault is reported unless masked.
D2	FST[2]	Indicates TOUTC open or shorted to GND condition, threshold = $V_{CCT} - 1.6V$, a hard fault is reported unless masked.
D1	FST[1]	Indicates V_{CCT} open or shorted to GND conditions, threshold (V_{CCT}) = $V_{CC} - 0.45V$, a hard fault is reported unless masked.
D0	FST[0]	Copy of a FAULT signal.

Transmitter Status Register 2 (TXSTAT2), Address: H0x07

Bit	D7	D6	D5	D4	D3 (STICKY)	D2 (STICKY)	D1	D0
Bit Name	X	X	X	X	IMODERR	IBIASERR	X	X
Read/Write	X	X	X	X	R	R	X	X
POR State	X	X	X	X	0	0	X	X
Reset Upon Read	X	X	X	X	Yes	Yes	X	X

The TXSTAT2 register is a device status register.

BIT	NAME	DESCRIPTION
D3	IMODERR	Modulation current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IMODMAX. In overflow condition, SET_IMOD[8:1] = IMODMAX[7:0]. Underflow occurs if result < 0. In underflow condition, SET_IMOD[8:0] = 0.
D2	IBIASERR	Bias current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IBIASMAX. In overflow condition, SET_IBIAS[8:1] = IBIASMAX[7:0]. Underflow occurs if result < 0. In underflow condition, SET_IBIAS[8:0] = 0.

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Bias Current Setting Register (SET_IBIAS), Address: H0x08

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IBIAS[8]	SET_IBIAS[7]	SET_IBIAS[6]	SET_IBIAS[5]	SET_IBIAS[4]	SET_IBIAS[3]	SET_IBIAS[2]	SET_IBIAS[1]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	1

The SET_BIAS register sets the laser bias current DAC.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IBIAS[8:1]	The bias current DAC is controlled by a total of 9 bits. The SET_IBIAS[8:1] bits are used to set the bias current with even denominations from 0 to 510 bits. The LSB (SET_IBIAS[0]) bit is controlled by the BIASINC register and is used to set the odd denominations in the SET_IBIAS[8:0]. Any direct write to SET_IBIAS[8:1] resets the LSB.

Modulation Current Setting Register (SET_IMOD), Address: H0x09

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IMOD[8]	SET_IMOD[7]	SET_IMOD[6]	SET_IMOD[5]	SET_IMOD[4]	SET_IMOD[3]	SET_IMOD[2]	SET_IMOD[1]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	1	0	0

The SET_IMOD register sets the laser modulation current DAC.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IMOD[8:1]	The mod current DAC is controlled by a total of 9 bits. The SET_IMOD[8:1] bits are used to set the modulation current with even denominations from 0 to 510 bits. The LSB (SET_IMOD[0]) bit is controlled by the MODINC register and is used to set the odd denominations in the SET_IMOD[8:0]. Any direct write to SET_IMOD[8:1] resets the LSB.

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Maximum Modulation Current Setting Register (IMODMAX), Address: H0x0A

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IMODMAX[7]	IMODMAX[6]	IMODMAX[5]	IMODMAX[4]	IMODMAX[3]	IMODMAX[2]	IMODMAX[1]	IMODMAX[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	0	0	0	0	0

The IMODMAX register sets the upper limit of modulation current.

BIT	NAME	DESCRIPTION
D[7:0]	IMODMAX[7:0]	The IMODMAX register is an 8-bit register that can be used to limit the maximum modulation current. IMODMAX[7:0] is continuously compared to SET_IMOD[8:1].

Maximum Bias Current Setting Register (IBIASMAX), Address: H0x0B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IBIASMAX[7]	IBIASMAX[6]	IBIASMAX[5]	IBIASMAX[4]	IBIASMAX[3]	IBIASMAX[2]	IBIASMAX[1]	IBIASMAX[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	0	0	0	0	0

The IBIASMAX register sets the upper limit of bias current.

BIT	NAME	DESCRIPTION
D[7:0]	IBIASMAX[7:0]	The IBIASMAX register is an 8-bit register that can be used to limit the maximum bias current. IBIASMAX[7:0] is continuously compared to SET_IBIAS[8:1].

Modulation Current Increment Setting Register (MODINC), Address: H0x0C

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IMOD[0]	X	X	MODINC[4]	MODINC[3]	MODINC[2]	MODINC[1]	MODINC[0]
Read/Write	R	X	X	R/W	R/W	R/W	R/W	R/W
POR State	0	X	X	0	0	0	0	0

The MODINC register increments/decrements the SET_IMOD register.

BIT	NAME	DESCRIPTION
D7	SET_IMOD[0]	LSB of SET_IMOD register
D[4:0]	MODINC	This string of bits is used to increment or decrement the modulation current. When written to, the SET_IMOD[8:0] bits are updated. MODINC[4:0] are a two's complement string.