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19-3496; Rev 2; 11/06

10Gbps Clock and Data Recovery with Equalizer

General Description

The MAX3992 is a 10Gbps clock and data recovery (CDR) with equalizer IC for XFP optical transmitters. The MAX3992 and the MAX3991 (CDR with limiting amplifier) form a signal conditioner chipset for use in XFP transceiver modules. The chipset is XFI compliant and offers multirate operation for data rates from 9.95Gbps to 11.1Gbps.

The MAX3992 recovers the data for up to 12 inches of FR-4 and one connector without the need for a standalone equalizer. The phase-locked loop is optimized for jitter tolerance in SONET, Ethernet, and Fibre-Channel applications. Low jitter generation of $4mUI_{RMS}$ leaves adequate margin for meeting SONET jitter requirements at the optical output.

An AC-based power detector asserts the loss-of-signal (LOS) output when the input signal is removed. An external reference clock, with frequency equal to 1/64 or 1/16 of the serial data rate, is used to aid in frequency acquisition. A loss-of-lock (LOL) indicator is provided to indicate the lock status of the receiver PLL.

The MAX3992 is available in a 4mm x 4mm, 24-pin QFN package. It consumes 356mW from a single +3.3V supply and operates over a 0°C to +85°C temperature range.

Applications

9.95Gbps to 11.1Gbps Optical XFP Modules

SONET OC-192/SDH STM-64 XFP Transceivers

10.3Gbps/11.1Gbps Ethernet XFP Transceivers

10.5Gbps Fibre-Channel XFP Transceivers

10Gbps DWDM Transceivers

10Gbps XFP Copper Modules

High-Speed Backplane Interconnects

Typical Application Circuit appears at end of data sheet.

Features

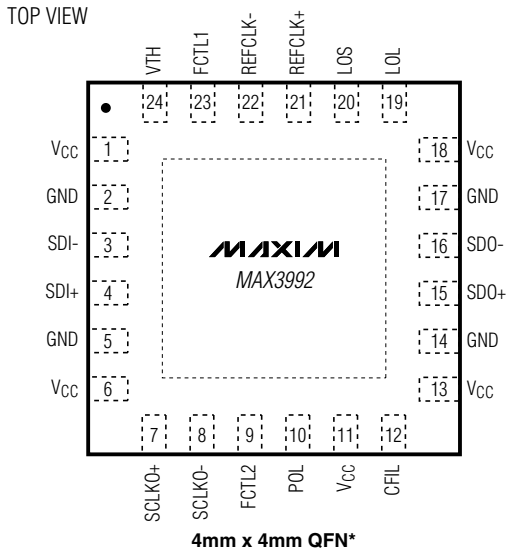
- **Multirate Operation from 9.95Gbps to 11.1Gbps**
- **Span Up to 300mm (12in) FR4 with One Connector**
- **Low-Output Jitter Generation: $4mUI_{RMS}$**
- **Low-Output Deterministic Jitter: $4.6ps_{P-P}$**
- **XFI-Compliant Input Interface**
- **LOS Indicator**
- **LOL Indicator**
- **Power Dissipation: 356mW**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3992UTG	0°C to +85°C	24 QFN	T2444-4
MAX3992UTG+*	0°C to +85°C	24 QFN	T2444-4

**Future product—contact factory for availability.*
+Denotes lead-free package.

Pin Configuration



4mm x 4mm QFN*

*THE EXPOSED PAD MUST BE CONNECTED TO CIRCUIT-BOARD GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

10Gbps Clock and Data Recovery with Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +4.0V
Input Voltage Levels
(SDI+, SDI-, REFCLK+, REFCLK-) .....(V_{CC} - 1.0V) to (V_{CC} + 0.5V)
CML Output Voltage
(SDO+, SDO-, SCLKO+, SLCKO-) .....(V_{CC} - 1.0V) to (V_{CC} + 0.5V)
Voltage at (CFIL, LOL, VTH, POL, LOS, FCTL1, FCTL2) .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
24-Pin QFN (derate 20.8mW/°C above +85°C) 1355mW
Junction Temperature Range .....-40°C to+150°C
Storage Temperature Range.....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			108	145	mA
DATA INPUT SPECIFICATION (SDI±)						
Single-Ended Input Resistance	R_{SE}		42	50	58	Ω
Differential Input Resistance	R_D		84	100	116	Ω
Single-Ended Input Resistance Matching					±5	%
Differential-Input Return Loss	SDD11	0.1GHz to 5.5GHz (Note 1)		15		dB
		5.5GHz to 12GHz (Note 1)		6		
Differential to Common-Mode Conversion	SCD11	0.1GHz to 15GHz		17		dB
Common-Mode Input Return Loss	SCC11	0.1GHz to 15GHz		7		dB
REFERENCE CLOCK SPECIFICATION (REFCLK±)						
Single-Ended Input Resisitance			84	100	116	Ω
Differential Input Resistance			168	200	232	Ω
CML OUTPUT SPECIFICATION (SDO±)						
SDO± Differential Output Swing		(Note 2)	575	650	725	mV_{P-P}
SDO± Output Common-Mode Voltage		RL = 50Ω to V_{CC}		V_{CC} - 0.16		V
SCLKO± Differential Output				380		mV_{P-P}
Single-Ended Output Resistance			42	50	58	Ω
Differential Output Resistance	R_O		84	100	116	Ω
Single-Ended Output Resistance Matching					±5	%
Differential-Output Return Loss	SDD22	0.1GHz to 5.5GHz (Note 1)		13		dB
		5.5GHz to 12GHz (Note 1)		8		
Rise/Fall Time		(20% to 80%) (Note 2)	18	23	30	ps
Power-Down Assert Time		(Note 3)			50	µs

ELECTRICAL CHARACTERISTICS (continued)

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JITTER SPECIFICATION							
Jitter Peaking	J_P	120kHz < f ≤ 8MHz (Notes 2, 4)			0.05	0.25	dB
		f ≤ 120kHz (Note 5)			0.03		
Jitter Transfer Bandwidth	J_{BW}	(Notes 2, 4)			5.6	8.0	MHz
Sinusoidal Jitter Tolerance		(Notes 2, 4, 7)	f = 400kHz	2.8	>2.8 (Note 6)		UI_{P-P}
			f = 4MHz	0.4	0.55		
			f = 80MHz	0.4	0.45		
Jitter Generation		(Notes 2, 4, 8)			4	5.5	mUI_{RMS}
Serial-Data Output Deterministic Jitter	DJ	PRBS 2^7 - 1 (Note 2)			4.6	13	ps_{P-P}
PLL ACQUISITION/LOCK SPECIFICATION							
Acquisition Time		Figures 1, 2 (Note 2)				200	µs
LOL Assert Time		Figure 1 (Note 2)				90	µs
Maximum Frequency Pullin Time		(Note 9)			2		ms
Frequency Difference at which LOL Is Asserted	$\Delta f/f_{REFCLK}$	$\Delta f = \lvert f_{VCO} / N - f_{REFCLK} \rvert$, N = 16 or 64			651		ppm
Frequency Difference at which LOL Is Deasserted	$\Delta f/f_{REFCLK}$	$\Delta f = \lvert f_{VCO} / N - f_{REFCLK} \rvert$, N = 16 or 64			500		ppm
LOSS-OF-SIGNAL (LOS) SPECIFICATION							
VTH Control Voltage Range	VTH			150		500	mV
LOS Gain Factor	VTH/V_{LOS_ASSERT}				10		V/V
Minimum LOS Assert Voltage	V_{LOS_ASSERT}				15		mV
Maximum LOS Assert Voltage	V_{LOS_ASSERT}				50		mV
LOS Gain-Factor Accuracy		(Notes 2, 10)		-1.5		+1.5	dB
LOS Hysteresis		(Notes 2, 11)		3.5	3.7	3.9	dB
LOS Gain-Factor Stability		(Note 2) Overtemperature and supply		-10		+10	%
LOS Assert Time		Figure 2 (Note 2)		3		90	µs
LOS Deassert Time		Figure 2 (Note 2)				90	µs
VTH Input Current				-5		+5	µA
LVTTL INPUT/OUTPUT SPECIFICATION (LOL, LOS, FCTL1, FCTL2)							
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Current				-30		+30	µA
Output High Voltage	V_{OH}	Sourcing 30µA		V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	Sinking 1mA				0.4	V

10Gbps Clock and Data Recovery with Equalizer

ELECTRICAL CHARACTERISTICS (continued)

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

Note 1: Measured with 100mV_{P-P} differential amplitude.
Note 2: Guaranteed by design and characterization.
Note 3: Measured from the time that the FCTL1 input goes high with FCTL2 = 0, to the time when the supply current drops to less than 40% of the nominal value.
Note 4: Measured with PRBS = 2^{31} - 1.
Note 5: Larger C_{FILT} can be used to reduce jitter peaking at ≤ 120kHz. A larger C_{FILT} will increase acquisition time. C_{FILT} should not exceed 200nF.
Note 6: Measurement limited by test equipment.
Note 7: Jitter tolerance is for BER ≤ 10^{-12}, measured with additional 0.1VI deterministic jitter through 15 inches of FR4. (See *Typical Operating Characteristics* 1.)
Note 8: Measured with 50kHz to 80MHz SONET filter.
Note 9: Applies on power-up or after standby.
Note 10: Over process, temperature and supply.
Note 11: Hysteresis is defined as 20Log($V_{LOS-DEASSERT}$/$V_{LOS-ASSERT}$).

Table 1. Operating Conditions (Unless otherwise noted, FCTL1 = FCTL2 = 0.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0		3.6	V
Ambient Temperature	T_A		0		+85	°C
Input Data Rate	Rb			(See Table 2)		Gbps
Differential Input Voltage to Transmission Line	V_D	0 to 12 inches FR-4	400		1000	mV_{P-P}
Output Load Resistance	RL	RL is AC-coupled		50		Ω
REFCLK± Differential Input Voltage Swing			300		1600	mV_{P-P}
REFCLK Duty Cycle			30		70	%
REFCLK Frequency	f_{REFCLK}			Rb / 16		GHz
				Rb / 64		
REFCLK Accuracy		Relative to Rb / 16 or Rb / 64	-100		+100	ppm
REFCLK Rise/Fall Times (20% to 80%)		F_{REFCLK} = Rb / 64			1200	ps
		f_{REFCLK} = Rb / 16			300	
REFCLK Random Jitter		Noise bandwidth < 100MHz			10	ps_{RMS}

Table 2. Serial Data Rate and Reference Clock Frequency

APPLICATION	DATA RATE (Rb) (Gbps)	/16 REFERENCE CLOCK FREQUENCY (MHz)	/64 REFERENCE CLOCK FREQUENCY (MHz)
OC-192 SONET – SDH64	9.95328	622.08	155.52
OC-192 SONET over FEC	10.664	666.5	166.625
ITU G.709	10.709	669.3125	167.328125
10Gbps Ethernet, IEEE 802.3ae	10.3125	644.53125	161.1328125
10Gbps Ethernet over ITU G.709	11.09573	693.483125	173.3707813
10Gbps Fibre Channel	10.51875	657.421875	164.355469

Note: *The part should be in standby mode when data rates are being switched.*

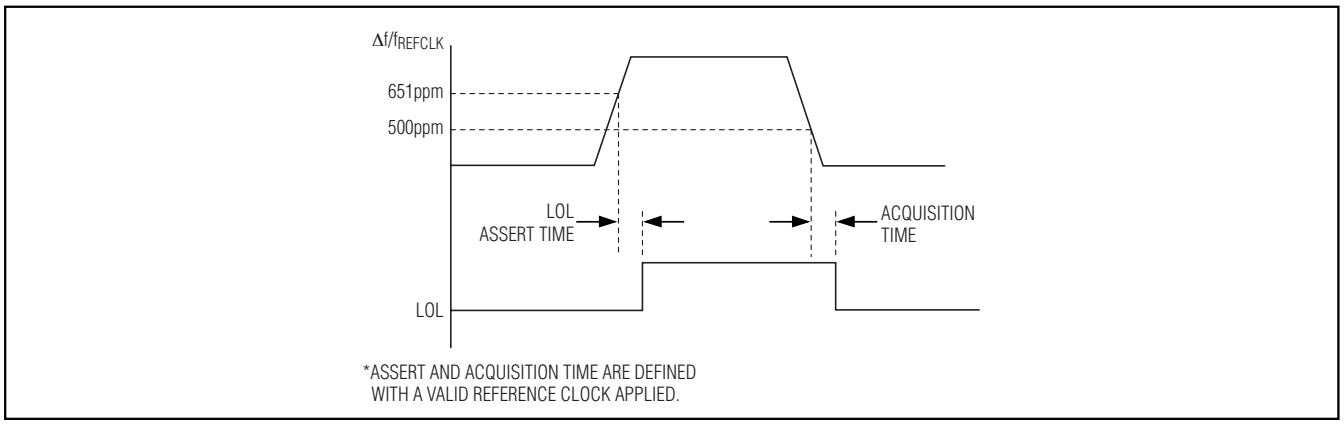


Figure 1. TX LOL Assert and PLL Acquisition Time

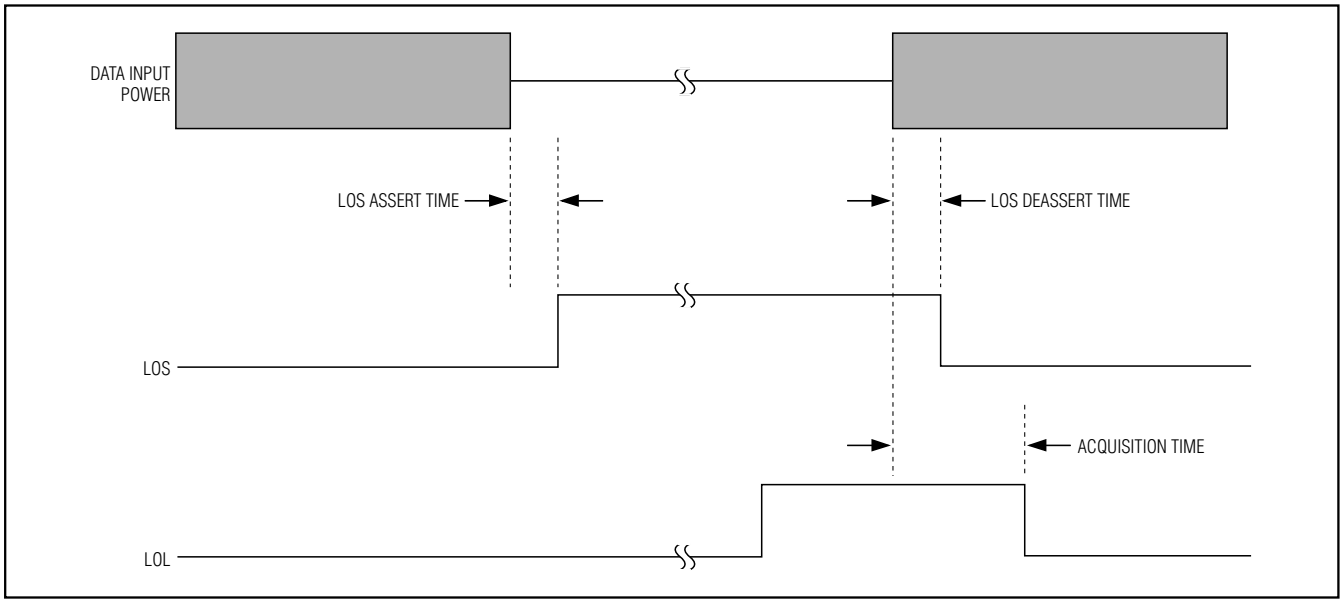


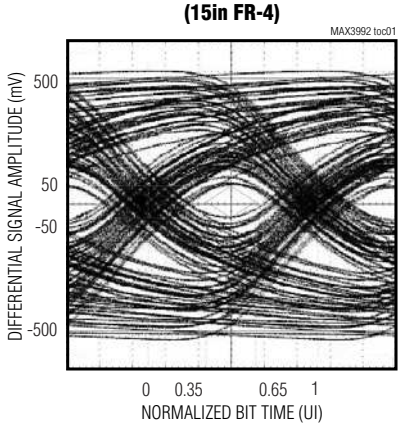
Figure 2. LOS Assert/Deassert Time

10Gbps Clock and Data Recovery with Equalizer

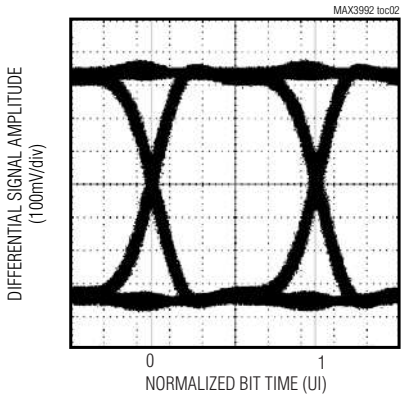
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

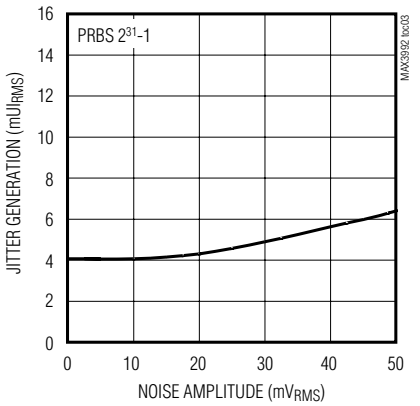
MAX3992 INPUT (15in FR-4)



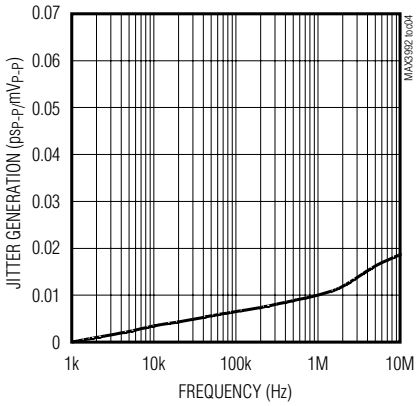
RECOVERED REFERENCE SIGNAL PRBS 2^31-1 15in FR-4



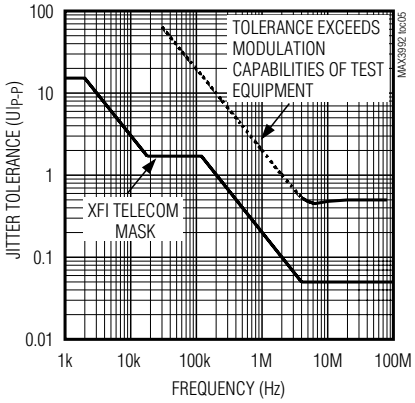
JITTER GENERATION vs. POWER-SUPPLY WHITE NOISE AMPLITUDE (BW < 100kHz)



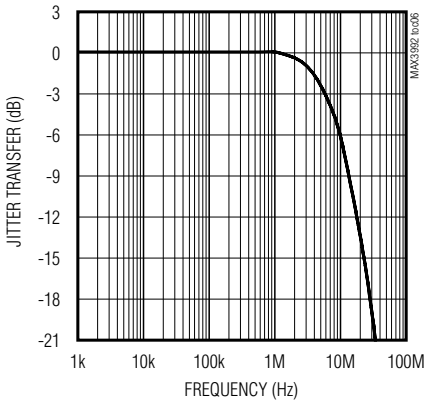
POWER-SUPPLY INDUCED OUTPUT JITTER vs. RIPPLE FREQUENCY



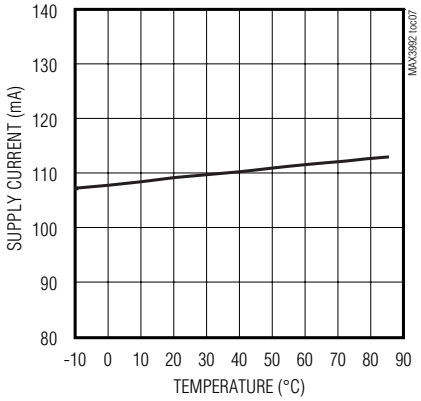
SINUSOIDAL JITTER TOLERANCE 12in FR-4 2^31-1 PRBS DATA



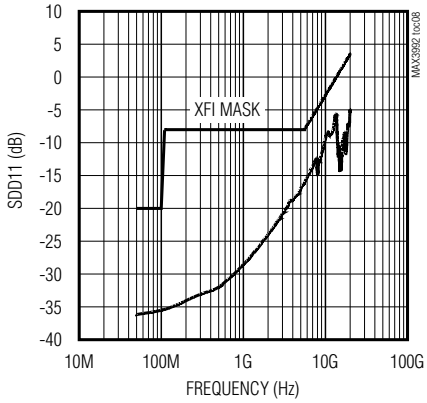
JITTER TRANSFER



MAX3992 SUPPLY CURRENT vs. TEMPERATURE



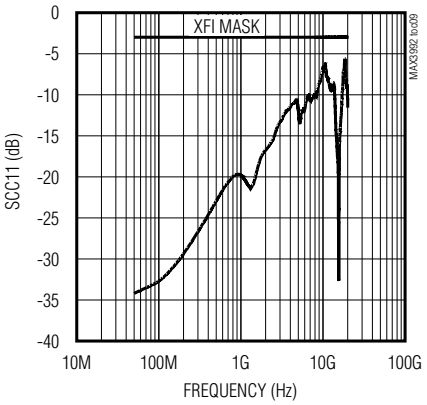
DIFFERENTIAL S11 SDD11



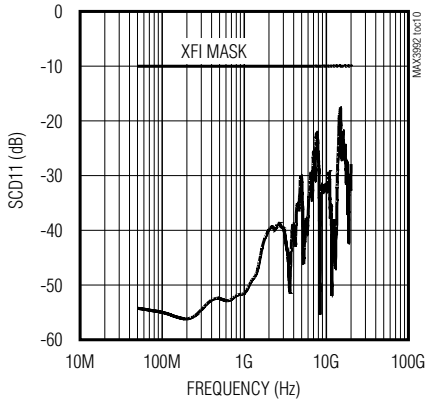
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

COMMON MODE S11
SCC11



DIFFERENTIAL TO COMMON MODE S11
SCD11



Pin Description

PIN	NAME	FUNCTION
1, 6, 11, 13, 18	V_{CC}	+3.3V Power Supply
2, 5, 14, 17	GND	Supply Ground
3	SDI-	Negative Serial Input, CML
4	SDI+	Positive Serial Input, CML
7	SCLKO+	Positive Clock Output, CML. See Table 3 for information about enabling the SCLKO output (for use in device testing).
8	SCLKO-	Negative Clock Output, CML. See Table 3 for information about enabling the SCLKO output (for use in device testing).
9	FCTL2	Function Control Input 2, TTL. See Table 3 for more information.
10	POL	Data Polarity Control Input, TTL. Connect to V_{CC} or leave open to maintain the same polarity as the input. Connect to GND to invert the polarity of the data.
12	CFIL	Loop-Filter Capacitor Connection. Connect a 0.047µF capacitor between CFIL and V_{CC}.
15	SDO+	Positive Serial Data Output, CML
16	SDO-	Negative Serial Data Output, CML
19	LOL	Lock Status Indicator, TTL. This output goes high to indicate the receiver is out of lock.
20	LOS	Receiver Loss-of-Signal Indicator, TTL . This output goes high when the input signal is removed.
21	REFCLK+	Positive Reference Clock Input, Digital. The REFCLK inputs are designed to be AC-coupled to the reference clock source. REFCLK± have a 200Ω differential impedance. See the *Detailed Description* section for more information. See Table 2.

10Gbps Clock and Data Recovery with Equalizer

Pin Description (continued)

PIN	NAME	FUNCTION
22	REFCLK-	Negative Reference Clock Input, Digital. The REFCLK inputs are designed to be AC-coupled to the reference clock source. REFCLK± have a 200Ω differential impedance. See the *Detailed Description* section for more information. See Table 2.
23	FCTL1	Function Control Input 1, TTL. See Table 3 for more information.
24	VTH	LOS Threshold Input, Analog. A voltage applied to this input sets the LOS assert threshold. The LOS power detector can be disabled if VTH is connected to V_{CC}, which forces LOS low.
EP	Exposed Pad	Supply Ground. The exposed pad must be soldered to the circuit-board ground for proper thermal and electrical performance. The MAX3992 uses exposed-pad variation T2444-4 in the package outline drawing. See the exposed-pad package.

Functional Diagram

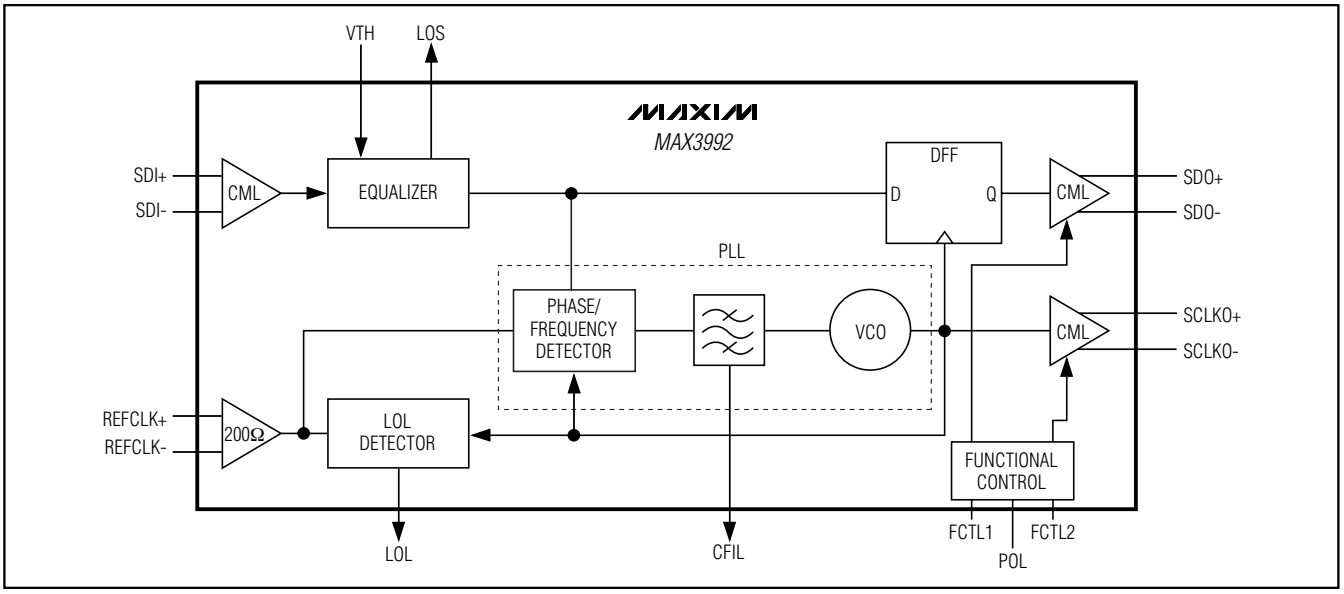


Figure 3. Functional Diagram

Detailed Description

The MAX3992 clock and data recovery with equalizer recovers data from the XFI interface. It consists of an equalizer with LOS power detector and a data retimer with LOL indicator. An optional recovered clock may also be enabled for performance testing.

Equalizer

The SDI inputs of the MAX3992 accept serial NRZ data from XFI standard interfaces. When signals from 400mV$_{P-P}$ to 1000mV$_{P-P}$ are applied to a transmission line from 0 to 12 inches of FR-4, the equalizer restores them for recovery by the CDR. The equalizer removes most of the deterministic jitter caused by frequency dependent skin effect and dielectric losses, as well as connector loss.

PLL Retimer

The integrated PLL recovers a synchronous clock that is used to retime the input data. Connect a 0.047µF capacitor between CFIL and V_{CC} to provide PLL dampening. The external reference connected to REFCLK aids in frequency acquisition. Because the reference clock is only used for frequency acquisition, an extremely low jitter generation can be achieved from a low-quality reference clock. The reference clock should be within ±100ppm of the bit rate divided by 16 or 64.

Loss-of-Lock Monitor

The LOL output indicates that the frequency difference between the recovered clock and the reference clock is excessive. LOL may assert due to excessive jitter at the data input, incorrect frequency, or loss of input data. The LOL detector monitors the frequency difference between the recovered clock and the reference clock. The LOL output is asserted high when the frequency difference exceeds 650ppm.

Loss-of-Signal Monitor

The LOS output indicates a loss of input data. Set VTH >500mV. When the input signal is removed (<50mV), LOS will be asserted high.

Reference Clock Input

The REFCLK inputs are internally terminated and self-biased to allow AC-coupling. The input impedance is 100Ω single-ended (200Ω differential). The REFCLK inputs of the MAX3991 and MAX3992 should be connected close together in parallel. The impedance looking into the parallel combination is 100Ω differential. This allows both the MAX3991 and MAX3992 to easily interface with one reference clock without using additional components. See Figure 4.

Design Procedure

Modes of Operation

The MAX3992 has a standby mode and jitter test mode in addition to its normal operating mode. Standby is used to conserve power. In the standby mode, the power consumption of the MAX3992 falls below 40% of the normal-operation power consumption. The jitter test mode enables the SCLK outputs to clock a BERT when testing jitter generation, jitter transfer, and jitter tolerance. The FCTL1 and FCTL2 TTL inputs are used to select the mode of operation as shown in Table 3.

Serial Data Rate and Reference Clock Frequency

Input Configuration

The SDI± inputs of the MAX3992 are current-mode logic (CML) compatible. The inputs have internal 50Ω terminations for minimum external components. See Figure 5 for the input structure. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML.*

Output Configuration

The MAX3992 uses CML for its high-speed digital outputs (SDO± and SCLKO±). The configuration of the output circuit includes internal 50Ω back terminations to V_{CC}. See Figure 6 for the output structure. CML outputs may be terminated by 50Ω to V_{CC}, or by 100Ω differential impedance. The relation of the output polarity to input can be reversed using the POL pin. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML.*

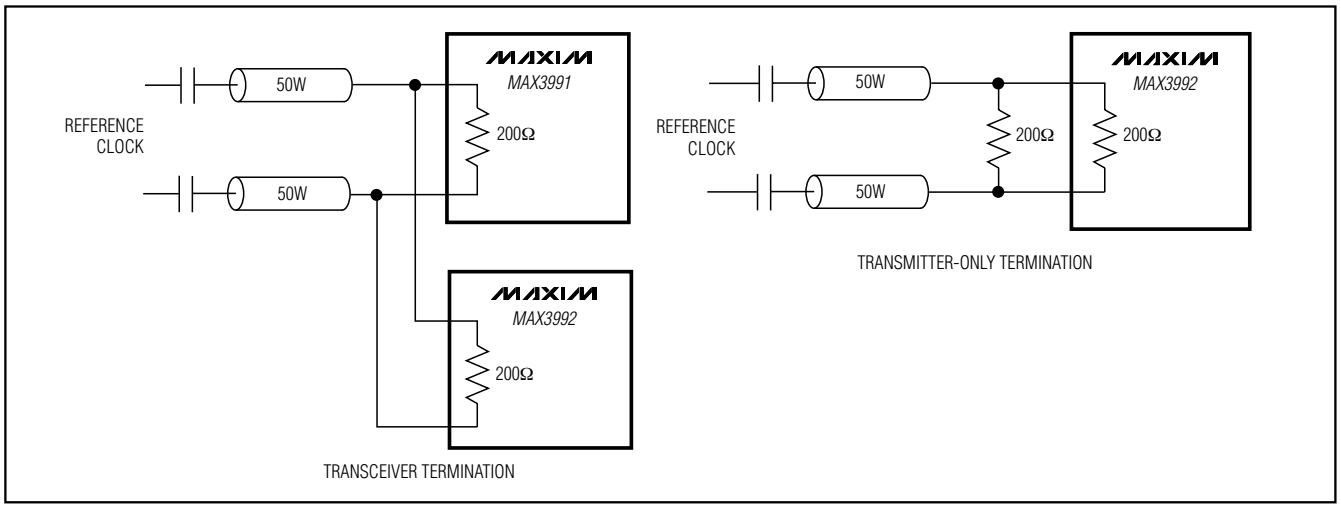


Figure 4. Reference Clock Termination

10Gbps Clock and Data Recovery with Equalizer

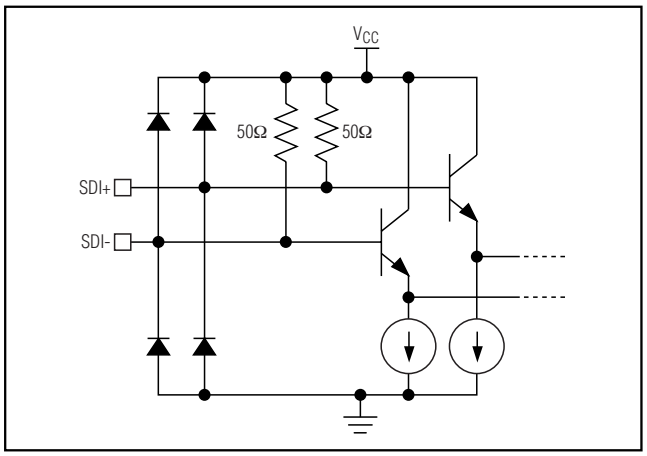


Figure 5. CML Input Model

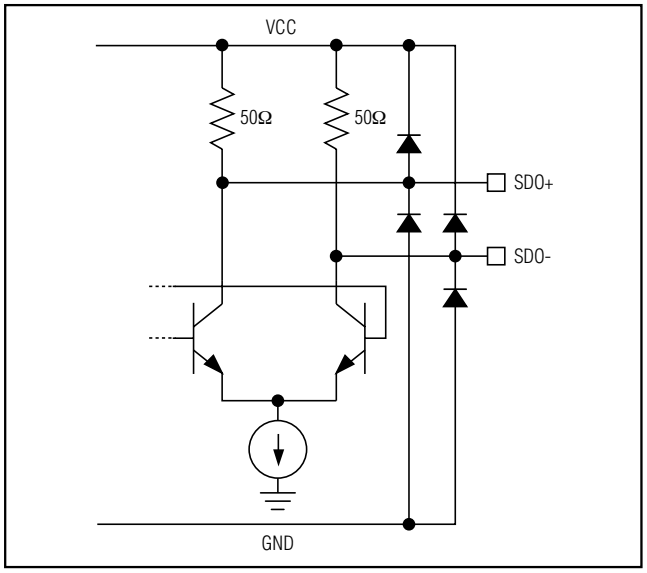


Figure 6. CML Output Model

Applications Information

Exposed Pad (EP) Package

The exposed pad, 24-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3992 and must be soldered to the circuit board for proper thermal and electrical performance.

Layout Considerations

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3992 high-speed inputs and outputs. Power-supply decoupling should be placed as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

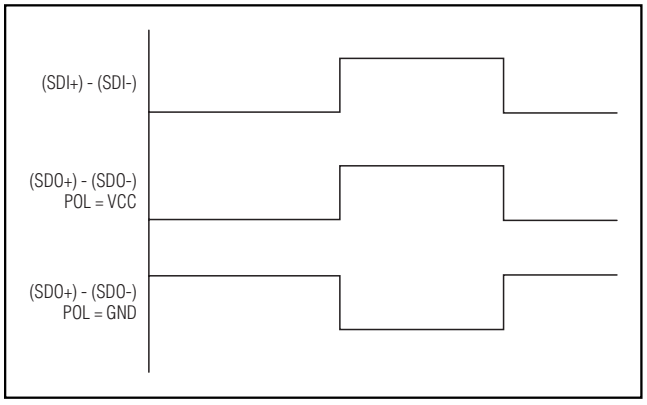


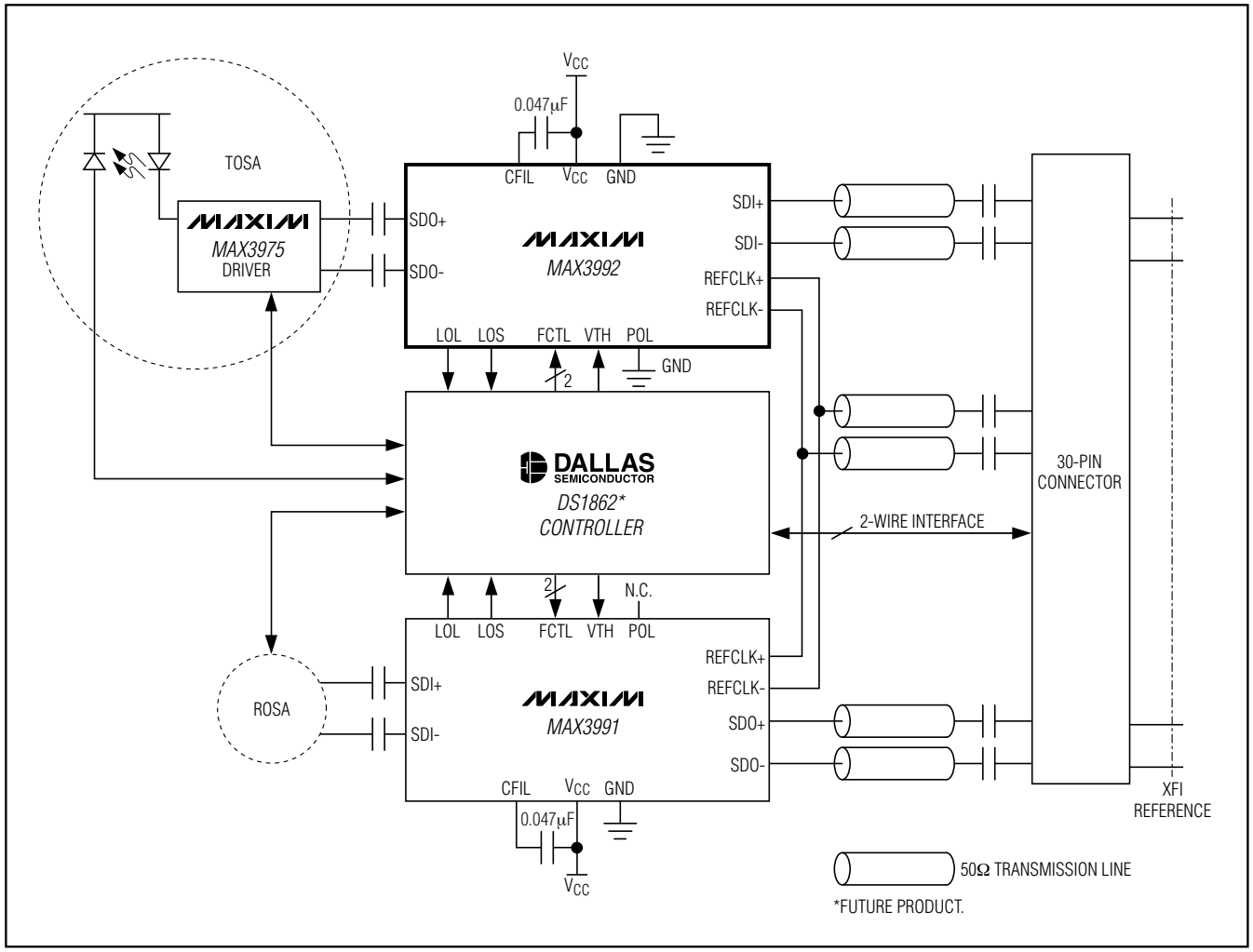
Figure 7. Polarity (POL) Function

Table 3. Functional Control

FCTL1	FCTL2	DESCRIPTION
0	0	Normal operation, serial clock output disabled.
1	0	Standby power-down mode.
0	1	Normal operation, serial clock output disabled.
1	1	Serial clock output enabled for jitter testing.

10Gbps Clock and Data Recovery with Equalizer

Typical Application Circuit



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Chip Information

TRANSISTOR COUNT: 10,300

PROCESS: SiGe bipolar

SUBSTRATE: SOI

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.) (QFN 4mm x 4mm x 0.8mm, package code: T2444-4)

Revision History

Rev 0;	11/04:	Initial data sheet release.
Rev 1;	11/05:	Changed Jitter Peaking max to typ (page 3); added new Note 5 (page 4); updated *Typical Application Circuit* (page 11).
Rev 2:	11/06:	Changed Jitter Tolerance min from 2.2UI_{P-P} to 2.8UI_{P-P}; changed Jitter Generation max from 6.9mUI_{RMS}, to 5.5mUI_{RMS} (page 3).