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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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EVALUATION KIT AVAILABLE

Audio/Video Switch for Three SCART Connectors

General Description

The MAX4399 audio/video switch is ideal for digital set-top box applications. The MAX4399 provides video and audio routing from the MPEG decoder source to the TV, VCR, and AUX SCART (peritelevision) connectors. In addition, the TV audio channel features clickless switching and programmable volume control from -56dB to +6dB in 2dB steps. The device can mix an auxiliary audio tone into the TV audio channel and can mix the stereo audio signal into a mono audio signal. The MAX4399 directly drives an external RF modulator with a composite video with blanking and sound (CVBS) signal created by an on-chip luma/chroma (Y/C) mixer and external RLC trap filter. The MAX4399 features a fast-mode I²C-compatible 2-wire interface allowing communication at data rates up to 400kbps. The MAX4399 operates with standard +5V and +12V single supplies and supports slow and fast switching.

All video and audio inputs are AC-coupled. The DC biases of all input and output signals are set to predefined levels. All video outputs, including the RF modulator, drive standard 150Ω loads. Red, green, and blue (RGB) outputs feature a programmable gain of +6dB ±1dB. All other video outputs have a fixed +6dB gain. The VCR and AUX audio output gains are programmable for -6dB, 0dB, and +6dB.

The MAX4399 is available in a compact 68-pin thin QFN package and is specified for the 0°C to +70°C commercial temperature range. The MAX4399 evaluation kit is available to help speed designs.

Applications

Satellite Receivers
Satellite Set-Top Boxes
Cable Set-Top Boxes
Terrestrial Set-Top Boxes
Game Consoles
TVs
Digital Television (DTV)
VCRs
DVD Players
DVD+R/W Players

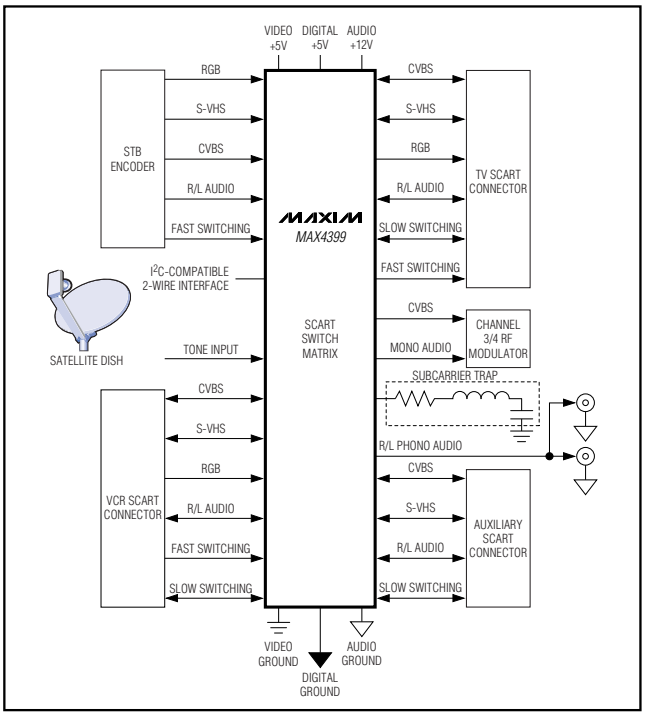
Features

- **Low -86dB Video Signal-to-Noise Ratio**
- **150Ω Driver on All Video Outputs, Including the RF Modulator**
- **Full CVBS Loop-Through on AUX SCART**
- **Programmable Audio Gain Control of -56dB to +6dB (TV Audio Outputs)**
- **Clickless Audio Switching (TV Audio Outputs)**
- **Programmable Clamp or Bias on Red/Chroma Video Inputs**
- **Programmable Video Gain of +6dB, ±1dB on RGB Outputs**
- **+5V and +12V Standard Supply Voltages**
- **27MHz -3dB Large-Signal Bandwidth on All Video Drivers**
- **Supports Three SCART Connectors**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4399CTK	0°C to +70°C	68 Thin QFN	T6800-3

Typical Operating Circuit



Audio/Video Switch for Three SCART Connectors

ABSOLUTE MAXIMUM RATINGS

Voltages
- V_VID to G_VID .....-0.3V to +6V
- V12 to G_AUD .....-0.3V to +14V
- V_DIG to G_DIG .....-0.3V to +6V
- G_AUD to G_DIG .....-0.1V to +0.1V
- G_VID to G_DIG .....-0.1V to +0.1V
- G_AUD to G_VID .....-0.1V to +0.1V
- Video Inputs, Video Outputs, ENC_FS_IN, VCR_FS_IN, VID_BIAS, TRAP .....-0.3V to (V_{V_VID} + 0.3V)
- V_AUD to G_AUD .....-0.3V to +9V
- Audio Inputs, Audio Outputs, AUD_BIAS .....-0.3V to (V_{V_AUD} + 0.3V)
- SDA, SCL, DEV_ADDR, INTERRUPT_OUT .....-0.3V to +6V
- AUX_SS, TV_SS, VCR_SS .....-0.3V to (V_{V12} + 0.3V)

Currents
- INTERRUPT_OUT .....+50mA
- TRAP .....±4mA

Output Short Circuit
- Video Outputs and TV_FS_OUT to V_VID, V_DIG, G_AUD, G_VID, or G_DIG .....Continuous
- Audio Outputs to V_AUD, V_VID, V_DIG, G_AUD, G_VID, or G_DIG .....Continuous
- AUX_SS, TV_SS, and VCR_SS to V12, V_AUD, V_VID, V_DIG, G_AUD, G_VID, or G_DIG .....Continuous

Continuous Power Dissipation (T_A = +70°C)
- 68-Pin Thin QFN (derate 41.7mW/°C above +70°C) 3333.3mW

Operating Temperature Range .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{V12} = 12V, V_{V_VID} = 5V, V_{V_DIG} = 5V, 0.47µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_AUD to G_AUD, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC							
V12 Supply Voltage Range		Inferred from the slow switch output levels		11.4	12	12.6	V
V_VID Supply Voltage Range		Inferred from the output swing of the video outputs		4.75	5	5.25	V
V_DIG Supply Voltage Range				4.75	5	5.25	V
V12 Quiescent Supply Current					17	35	mA
V_VID Quiescent Supply Current		All video output amplifiers are enabled, no load			51	116	mA
V_VID Standby Supply Current		All video output amplifiers are in shutdown, and TV_FS_OUT driver is in shutdown			19	34	mA
V_DIG Quiescent Supply Current					1	3	mA
VIDEO							
Voltage Gain		$1V_{P-P}$ input	CVBS and S-VHS	5.5	6	6.5	dB
			R, G, B, gain = 5dB	4.5	5	5.5	
			R, G, B, gain = 6dB	5.5	6	6.5	
			R, G, B, gain = 7dB	6.5	7	7.5	
Small-Signal Bandwidth, -3dB		$100mV_{P-P}$ input, gain = 6dB	CVBS and S-VHS		110		MHz
			R, G, B		110		
Large-Signal Bandwidth, -3dB		$1V_{P-P}$ input, gain = 6dB, T_A = +25°C (Note 2)	CVBS and S-VHS	15	27		MHz
			R, G, B		30		

ELECTRICAL CHARACTERISTICS (continued)

(V_{V12} = 12V, V_{V_VID} = 5V, V_{V_DIG} = 5V, 0.47µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_AUD to G_AUD, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	SR	1V_{P-P} input, gain = 6dB			170		V/µs
Gain Matching		1V_{P-P} input, between RGB or Y-C		-0.5	0	+0.5	dB
Differential Gain	DG	5-step modulated staircase	RF_CVBS_OUT		0.03		%
			All other video outputs		0.13		
Differential Phase	DP	5-step modulated staircase	RF_CVBS_OUT		0.09		degrees
			All other video outputs		0.36		
Signal-to-Noise Ratio	SNR	1V_{P-P} input			-86		dB
Group Delay		f = 0.1MHz to 6MHz	RF_CVBS_OUT		5		ns
			All other video outputs		3		
Bottom Level Clamp		RGB, composite and luma, no signal, no load			1.21		V
Chroma Bias		Chroma only, no signal, no load			1.88		V
Sync Crush		Percentage reduction in sync pulse (0.3V_{P-P}); inferred from input clamping current with a 0.1µF coupling capacitor		-2	0	+2	%
Power-Supply Rejection Ratio	PSRR	f = 100kHz, 0.5V_{P-P}			60		dB
Input Impedance		CVBS, Y, or RGB video input			4		MΩ
		Chroma video input			11		kΩ
Input Clamp Current		V_{IN} = 1.75V		2.5	4.2	8.0	µA
Output Bias Voltage		No signal, no load	RGB, composite, and luma		1.05		V
			Chroma		2.24		
Pulldown Resistance		VCR_R/C_OUT, AUX_R/C_OUT, TV_R/C_OUT			10		Ω
Crosstalk		f = 4.43MHz, 1V_{P-P} input, between any two active inputs			-63		dB
Mute Suppression		f = 4.43MHz, 1V_{P-P} input, on one input			-65		dB
AUDIO							
V_AUD Voltage		Generated by internal linear regulator			8.1		V
Voltage Gain		1.414V_{P-P} input, gain = 0dB		-0.25	0	+0.25	dB
Gain Matching Between Channels		1.414V_{P-P} input, gain = 0dB		-0.5	0	+0.5	dB
Gain Flatness		f = 20Hz to 20kHz, 0.5V_{RMS} input, gain = 0dB			0.005		dB
Frequency Bandwidth		0.5V_{RMS} input; frequency where output is -3dB with 1kHz serving as 0dB			210		kHz

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ELECTRICAL CHARACTERISTICS (continued)

(V_{V12} = 12V, V_{V_VID} = 5V, V_{V_DIG} = 5V, 0.47µF X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_AUD to G_AUD, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Level		Gain = 0dB			V_AUD/2		V
Input Signal Amplitude		Inferred through total harmonic distortion specification, f = 1kHz			2		V_{RMS}
Input Resistance					100		kΩ
Output DC Level					V_AUD/2		V
Signal-to-Noise Ratio	SNR	f = 1.0kHz, 1V_{RMS}, gain = 0dB, 20Hz to 20kHz			105		dB
Total Harmonic Distortion	THD	R_{LOAD} = 10kΩ	f = 1.0kHz, 0.5V_{RMS}		0.002		%
			f = 1.0kHz, 2V_{RMS}		0.005		
Output Impedance					0.5		Ω
Volume Attenuation Step		1.414V_{P-P} input	TV audio, volume control range extends from -56dB to +6dB	1.5	2	2.5	dB
			VCR, AUX audio	5.5	6	6.5	
Power-Supply Rejection Ratio	PSRR	f = 1kHz, 0.5V_{P-P}			110		dB
Mute Suppression		f = 1kHz, 0.5V_{RMS} input			105		dB
Audio Limiter Level		f = 1kHz, 2.5V_{RMS} input			6.7		V_{P-P}
Crosstalk		f = 1kHz, 0.5V_{RMS}, gain = 0dB			105		dB
DIGITAL INTERFACE: SDA and SCL							
Low-Level Input Voltage	V_{IL}					0.8	V
High-Level Input Voltage	V_{IH}			2.6			V
Hysteresis of Schmitt Trigger Input					0.2		V
SDA Low-Level Output Voltage	V_{OL}	I_{SINK} = 3mA		0		0.4	V
		I_{SINK} = 6mA		0		0.6	
Output Fall Time for SDA Line		400pF bus load				250	ns
Spike Suppression					50		ns
Input Current		V_{IL} = 0V, V_{IH} = 5V		-10		+10	µA
Input Capacitance					5		pF
SCL Clock Frequency				0		400	kHz
Hold Time	$t_{HD,STA}$	Repeated start condition		0.6			µs
Low Period of SCL Clock	t_{LOW}			1.3			µs
High Period of SCL Clock	t_{HIGH}			0.6			µs
Setup Time for a Repeated Start Condition	$t_{SU,STA}$			0.6			µs
Data Hold Time	$t_{HD,DAT}$			0		0.9	µs
Data Setup Time	$t_{SU,DAT}$			100			ns
Maximum Receive SCL/SDA Rise Time	t_R	(Note 3)			300		ns

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Receive SCL/SDA Rise Time (Note 3)	t_R			20 + 0.1C_B		ns
Maximum Receive SCL/SDA Fall Time (Note 3)	t_F			300		ns
Minimum Receive SCL/SDA Fall Time (Note 3)	t_F			20 + 0.1C_B		ns
Setup Time for Stop Condition	$t_{SU,STO}$		0.6			µs
Bus Free Time Between a Stop and Start	t_{BUF}		1.3			µs
OTHER DIGITAL PINS						
DEV_ADDR Low Level					0.8	V
DEV_ADDR High Level			2.6			V
INTERRUPT_OUT Low Voltage		INTERRUPT_OUT sinking 1mA		0.15	0.4	V
INTERRUPT_OUT High Leakage Current		$V_{INTERRUPT\_OUT}$ = 5V		1	10	µA
SLOW SWITCHING						
Input Low Level			0		2	V
Input Medium Level			4.5		7.0	V
Input High Level			9.5		12.0	V
Input Current				50	100	µA
Output Low Level		R_{LOAD} = 10kΩ to ground	0		1.5	V
Output Medium Level (External 16/9)		R_{LOAD} = 10kΩ to ground	5.0		6.5	V
Output High Level (External 4/3)		R_{LOAD} = 10kΩ to ground	10		12	V
FAST SWITCHING						
Input Low Level			0		0.4	V
Input High Level			1		3	V
Input Current				1	10	µA
Output Low Level		I_{SINK} = 0.5mA	0	0.01	0.2	V
Output High Level		V_VID - V_{OH}, I_{SOURCE} = 20mA		0.75	2	V
Fast-Switching Output to RGB Skew		Difference in propagation delays of fast-switching signal and RGB signals; measured from 50% input transition to 50% output transition		30		ns
Fast-Switching Output Rise Time		R_{LOAD} = 150Ω to ground		30		ns
Fast-Switching Output Fall Time		R_{LOAD} = 150Ω to ground		30		ns

Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Parameter guaranteed by design.
Note 3: C_B = total capacitance of one bus line in pF. Tested with C_B = 400pF.

Audio/Video Switch for Three SCART Connectors

Typical Operating Characteristics

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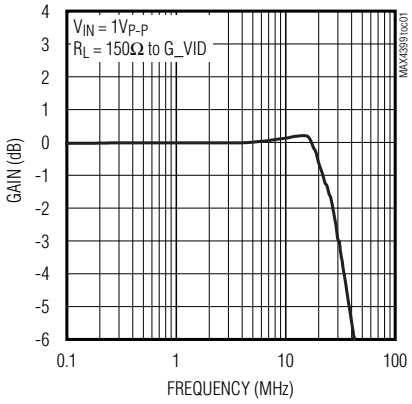
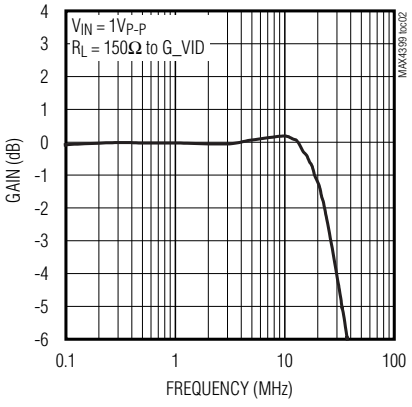
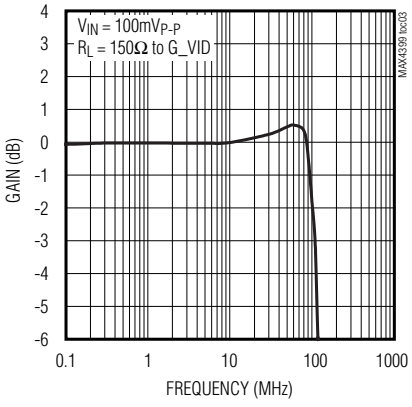
RGB VIDEO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



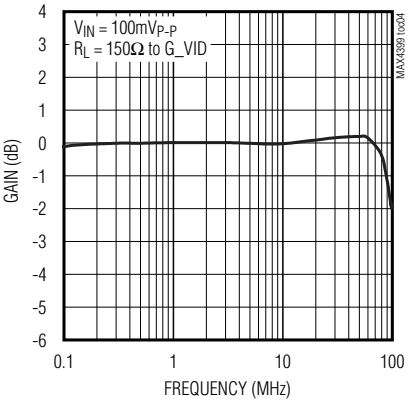
Y VIDEO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



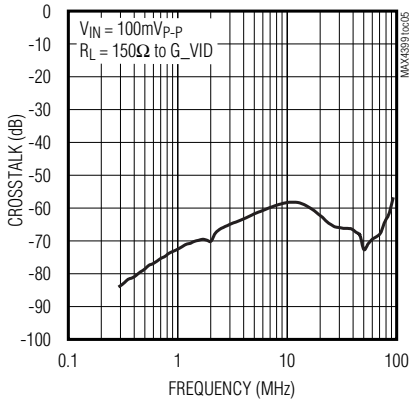
RGB VIDEO SMALL-SIGNAL BANDWIDTH vs. FREQUENCY



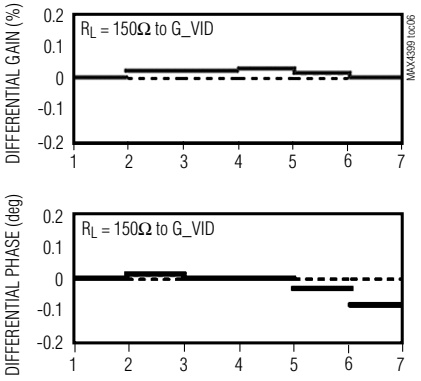
Y VIDEO SMALL-SIGNAL BANDWIDTH vs. FREQUENCY



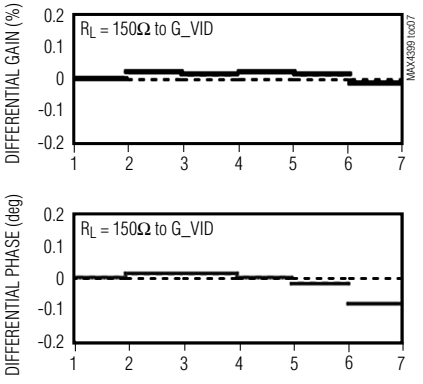
VIDEO CROSSTALK vs. FREQUENCY



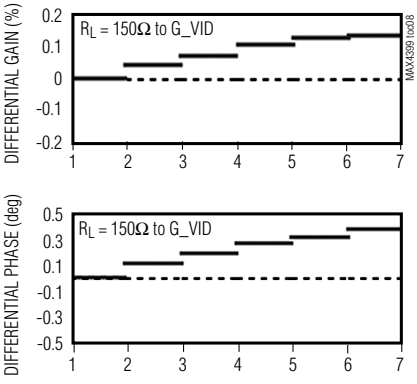
RF_CVBS_OUT (WITH TRAP FILTER)



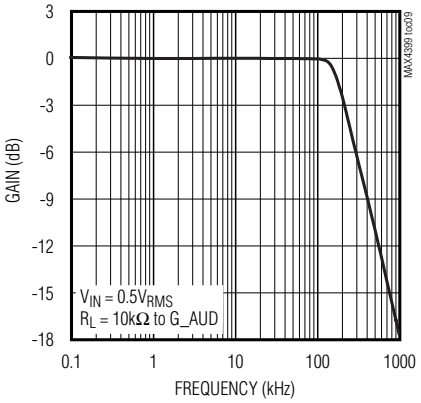
RF_CVBS_OUT (WITHOUT TRAP FILTER)



TV_Y/CVBS_OUT



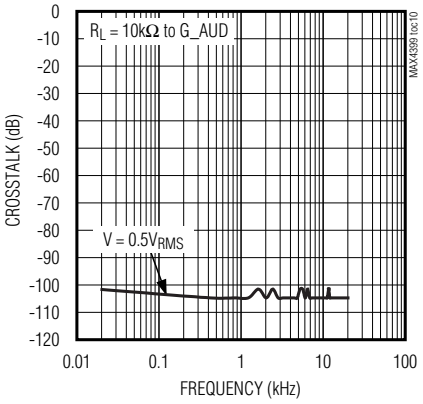
AUDIO LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



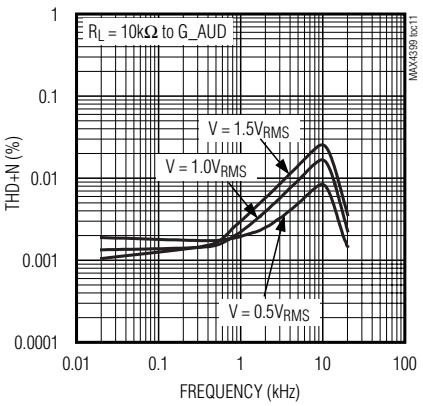
Typical Operating Characteristics (continued)

(V_{V12} = 12V, V_{V_VID} = 5V, V_{V_DIG} = 5V, 0.47µF ceramic X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_AUD to G_AUD, no load, T_A = +25°C, unless otherwise noted.)

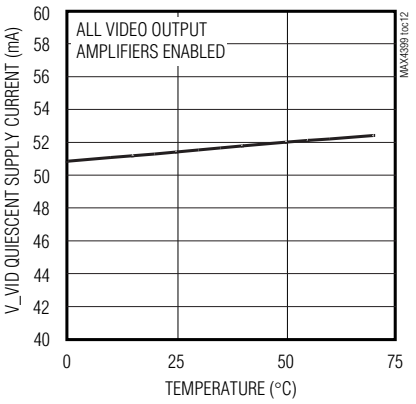
AUDIO CROSSTALK vs. FREQUENCY



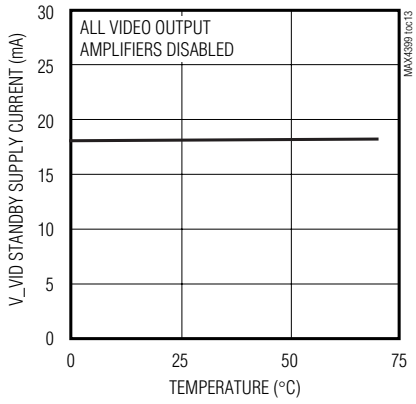
AUDIO THD+N vs. FREQUENCY



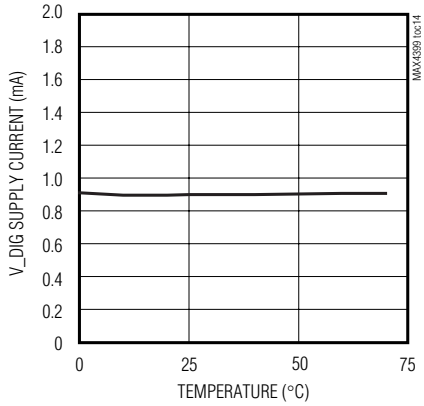
V_VID QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



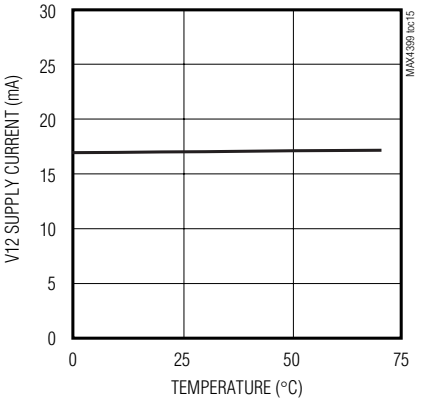
V_VID STANDBY QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



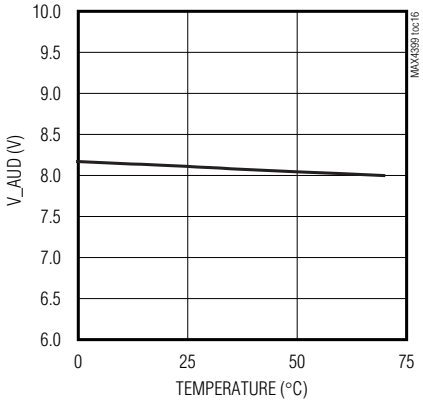
V_DIG QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



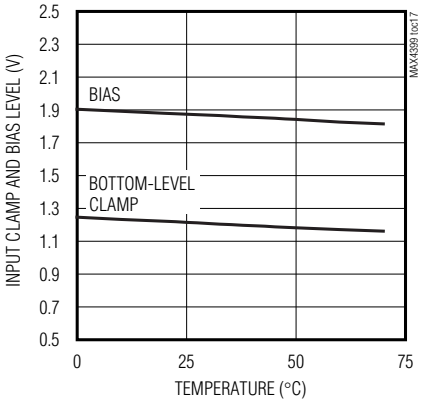
V12 QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



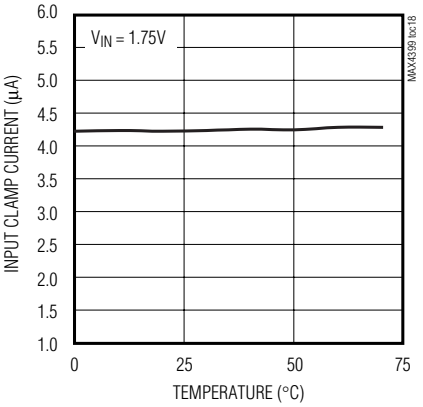
V_AUD vs. TEMPERATURE



INPUT CLAMP AND BIAS LEVEL vs. TEMPERATURE



INPUT CLAMP CURRENT vs. TEMPERATURE

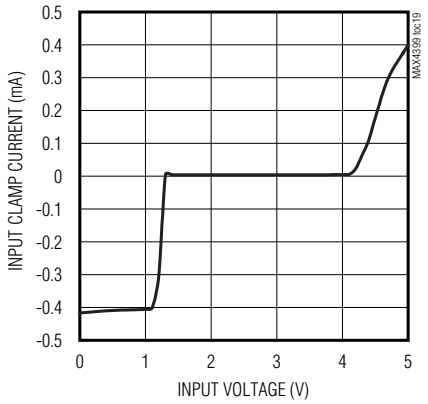


Audio/Video Switch for Three SCART Connectors

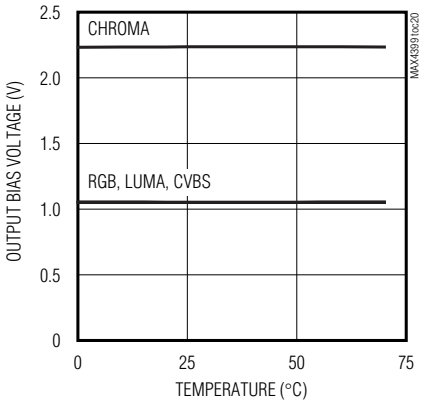
Typical Operating Characteristics (continued)

(V_{V12} = 12V, V_{V_VID} = 5V, V_{V_DIG} = 5V, 0.47µF ceramic X5R capacitor in parallel with a 10µF aluminum electrolytic capacitor from V_AUD to G_AUD, no load, T_A = +25°C, unless otherwise noted.)

INPUT CLAMP CURRENT vs. INPUT VOLTAGE



OUTPUT BIAS VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_DIG	Digital Supply Voltage. Connect to 5V.
2	DEV_ADDR	Device Address Set Input. Connect to G_DIG to set write and read addresses of 94h and 95h, respectively. Connect to V_DIG to set write and read addresses of 96h and 97h, respectively.
3	SDA	Bidirectional Data I/O. I^2C-compatible, 2-wire interface data input/output. Output is open drain.
4	SCL	Clock Input. I^2C-compatible, 2-wire interface clock.
5	INTERRUPT_OUT	Interrupt Output. INTERRUPT_OUT is an open-drain output that goes high impedance to indicate a change in the slow switch lines, AUX_SS, TV_SS, or VCR_SS.
6	G_DIG	Digital Ground
7	ENC_L_IN	Digital Encoder Left-Channel Audio Input
8	ST_AUX_IN	Satellite Dish Tone Input
9	ENC_R_IN	Digital Encoder Right-Channel Audio Input
10	AUD_BIAS	Audio Input Bias Voltage. Bypass AUD_BIAS with a 10µF capacitor and a 0.1µF capacitor to G_AUD.
11, 22, 30	V_AUD	Audio Supply Voltage. Connect all V_AUD together. An on-board linear regulator creates the +8V audio supply voltage from V12. Bypass pin 30 with a 10µF aluminum electrolytic capacitor in parallel with a 0.47µF low-ESR ceramic capacitor to audio ground, and bypass pins 11 and 22 with 0.1µF capacitors to audio ground.
12	AUX_L_IN	AUX SCART Left-Channel Audio Input
13	AUX_R_IN	AUX SCART Right-Channel Audio Input
14	VCR_R_IN	VCR SCART Right-Channel Audio Input
15	VCR_L_IN	VCR SCART Left-Channel Audio Input
16	TV_R_IN	TV SCART Right-Channel Audio Input

Pin Description (continued)

PIN	NAME	FUNCTION
17	TV_L_IN	TV SCART Left-Channel Audio Input
18, 26	G_AUD	Audio Ground
19	AUX_L_OUT	AUX SCART Left-Channel Audio Output
20	AUX_R_OUT	AUX SCART Right-Channel Audio Output
21	VCR_R_OUT	VCR SCART Right-Channel Audio Output
23	VCR_L_OUT	VCR SCART Left-Channel Audio Output
24	PHONO_R_OUT	Hi-Fi Right-Channel Audio Output
25	PHONO_L_OUT	Hi-Fi Left-Channel Audio Output
27	RF_MONO_OUT	RF Modulator Mono Audio Output
28	TV_L_OUT	TV SCART Left-Channel Audio Output
29	TV_R_OUT	TV SCART Right-Channel Audio Output
31	V12	+12V Supply. Bypass V12 with a 10µF capacitor in parallel with a 0.1µF capacitor to ground.
32	AUX_SS	AUX SCART Bidirectional Slow-Switch Signal
33	TV_SS	TV SCART Bidirectional Slow-Switch Signal
34	VCR_SS	VCR SCART Bidirectional Slow-Switch Signal
35	TRAP	Trap Filter. Connect a series RLC trap filter to eliminate the color subcarrier frequency (4.43MHz) from the luma signal. The filter prevents cross-mixing of the color subcarriers when the luma and chroma signals are added together to form a composite signal. Internally biased at +0.5V.
36, 42, 50	G_VID	Video Ground
37	TV_FS_OUT	TV SCART Fast-Switching Output. This signal is used to switch the TV to its RGB inputs for on-screen display purposes.
38, 46, 61	V_VID	Video Supply. Bypass each V_VID with a 0.01µF capacitor to V_GND. Connect a 200nH ferrite bead from V_VID to a 5V supply.
39	RF_CVBS_OUT	RF Modulator Composite Video Output. Internally biased at 1.0V.
40	TV_Y/CVBS_OUT	TV SCART Luma/Composite Video Output. Internally biased at 1.0V.
41	TV_R/C_OUT	TV SCART Red/Chroma Video Output. Internally biased at 1.0V for red video signal and 2.1V for chroma video signal.
43	TV_G_OUT	TV SCART Green Video Output. Internally biased at 1.0V.
44	TV_B_OUT	TV SCART Blue Video Output. Internally biased at 1.0V.
45	AUX_R/C_OUT	AUX SCART Red/Chroma Video Output. Internally biased at 1.0V for red video signal and 2.1V for chroma video signal.
47	AUX_Y/CVBS_OUT	AUX SCART Luma/Composite Video Output. Internally biased at 1.0V.
48	VCR_Y/CVBS_OUT	VCR SCART Luma/Composite Video Output. Internally biased at 1.0V.
49	VCR_R/C_OUT	VCR SCART Red/Chroma Video Output. Internally biased at 1.0V for red video signal and 2.1V for chroma video signal.
51	VID_BIAS	Video Bias Voltage Output. VID_BIAS sets video bias level for chroma signals. Bypass VID_BIAS with a low-ESR 0.1µF capacitor to G_VID.
52	TV_R/C_IN	TV SCART Red/Chroma Video Input. Internally biased at 1.22V for red, or 1.8V for chroma.

Audio/Video Switch for Three SCART Connectors

Pin Description (continued)

PIN	NAME	FUNCTION
53	TV_Y/CVBS_IN	TV SCART Luma/Composite Video Input. Internally biased at 1.22V.
54	AUX_R/C_IN	AUX SCART Red/Chroma Video Input. Internally biased at 1.22V for red, or 1.8V for chroma.
55	AUX_Y/CVBS_IN	AUX SCART Luma/Composite Video. Internally biased at 1.22V.
56	VCR_Y/CVBS_IN	VCR SCART Luma/Composite Video Input. Internally biased at 1.22V.
57	VCR_FS_IN	VCR SCART Fast-Switching Input
58	VCR_R/C_IN	VCR SCART Red/Chroma Video Input. Internally biased at 1.22V for red, or 1.8V for chroma.
59	VCR_G_IN	VCR SCART Green Video Input. Internally biased at 1.22V.
60	VCR_B_IN	VCR SCART Blue Video Input. Internally biased at 1.22V.
62	ENC_Y/CVBS_IN	Digital Encoder Luma/Composite Video Input. Internally biased at 1.22V.
63	ENC_R/C_IN	Digital Encoder Red/Chroma Video Input. Internally biased at 1.22V for red, or 1.8V for chroma.
64	ENC_G_IN	Digital Encoder Green Video Input. Internally biased at 1.22V.
65	ENC_B_IN	Digital Encoder Blue Video Input. Internally biased at 1.22V.
66	ENC_Y_IN	Digital Encoder Luma Video Input. Internally biased at 1.22V.
67	ENC_C_IN	Digital Encoder Chroma Video Input. Internally biased at 1.8V.
68	ENC_FS_IN	Digital Encoder Fast-Switching Input

Detailed Description

The MAX4399 audio/video switch matrix connects audio and video signals between different ports. In the case of a set-top box, the ports consist of the MPEG decoder and three SCART connectors. For DVD+RW recorders and some televisions, the ports consist of the main board, front panel, tuner, and two SCART connectors.

The video section consists of input buffers, a crosspoint switch, and output drivers that can be disabled. There is also a mixer, which creates a composite video signal from S-video. The video inputs can be set in either clamp or bias mode. The red/chroma outputs have pull-downs that connect the outputs to video ground as described in the *Video Inputs* section.

The audio section features input buffers, a crosspoint switch, and output drivers. The TV audio path has volume control from -56dB to +6dB in 2dB steps. The VCR and AUX audio paths have volume control from -6dB to +6dB in 6dB steps. The MAX4399 can be configured to switch inputs during a zero crossing to reduce clicks. The MAX4399 can also switch volume levels during a zero crossing to reduce zipper noise. The audio outputs can operate in different modes. For instance, left and right audio channels can be swapped (see the *Audio Outputs* section).

The MAX4399 has two fast-switching inputs and one fast-switching output. Fast switching is used for creating on-screen displays by switching between the CVBS and RGB signals. Under I²C-compatible control, the fast-switching output can follow either of the fast-switching inputs or be set high or low.

The MAX4399 features three slow-switching input/outputs to support slow switching, which sets the screen aspect ratio or video source of the display device. The slow switching relies on tri-level logic in which the levels are 0V, 6V, and 12V. The status of the slow-switching input is continuously read and stored in register 0Eh. If INTERRUPT_OUT is enabled, then INTERRUPT_OUT changes to a high-impedance state if any of the slow-switching inputs change logic levels. The slow-switching outputs can be set to a logic level or high impedance by writing to registers 07h, 09h, or 0Bh.

The MAX4399 can be configured through an I²C-compatible interface. DEV_ADDR sets the I²C-compatible address.

SCART Video Switching

The MAX4399 triple SCART audio/video switch includes multiplexed video amplifiers and a Y-C mixer-driver with a trap filter to drive an RF modulator. The MAX4399 switches video from an MPEG decoder output and TV, VCR, and AUX SCART connectors.

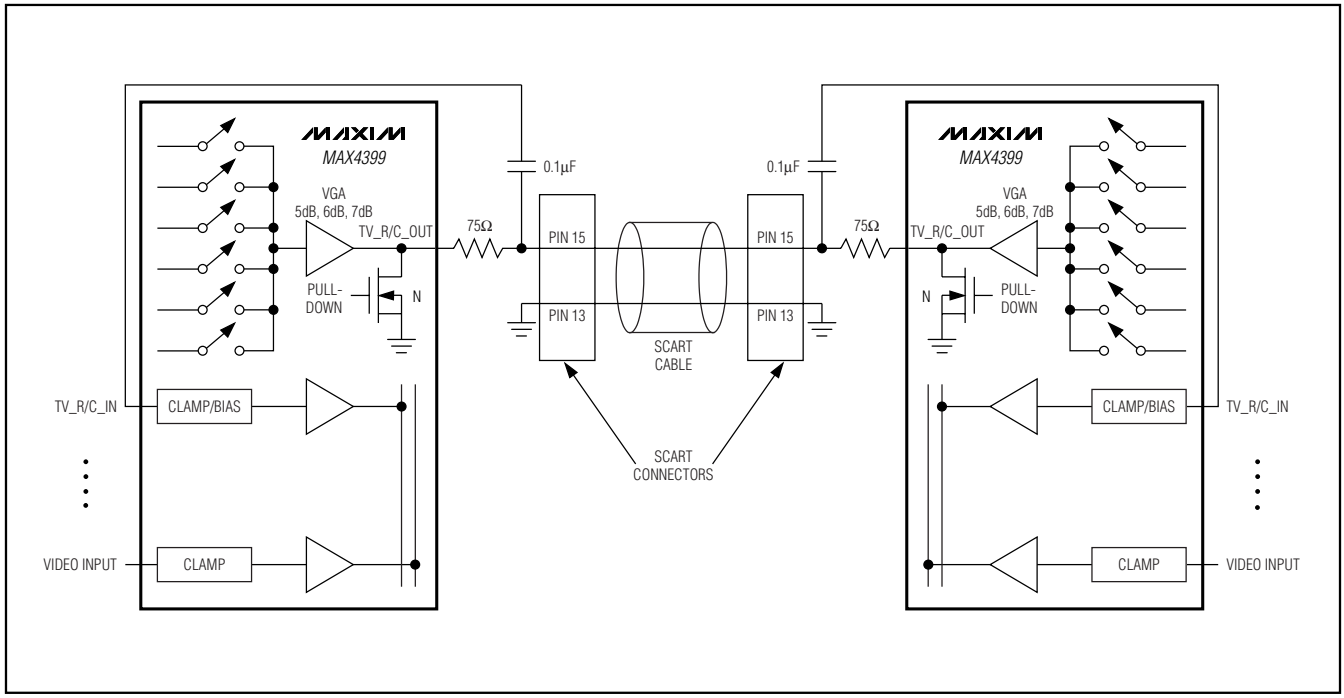


Figure 1. Bidirectional SCART Pins

The inputs and outputs are grouped by SCART connectors: TV, VCR, and AUX. While the SCART connector supports RGB, S-video, and composite formats, RGB and S-video share a bidirectional set of SCART connector pins. The MAX4399 supports connection of auxiliary devices (DVD players, DVD+R/W recorders, game consoles, camcorders, etc.) by including full I/O support for an auxiliary (AUX) SCART connector.

Video Inputs

All of the video amplifier inputs are AC-coupled with an external 0.1µF capacitor. Either a clamp or bias circuit sets the DC input level of the video signals. The clamp circuit positions the sync tip of the CVBS, RGB, or luma (S-VHS) signals. If the signal does not have sync, then the clamp positions the minimum of the signal at the clamp voltage. The bias circuit positions the chroma signal (S-VHS) at its midlevel. On the video inputs that can receive either a chroma or a red video signal, the 2-wire interface sets whether the clamp or bias circuit is active.

Red/chroma signals, such as TV_R/C_OUT signals are bidirectional. When the red/chroma signal is being used as an input, then the red/chroma output must connect the 75Ω back-termination resistor to ground, as shown in Figure 1, so the transmitting device can see the proper termination on the receiving side. The MAX4399 provides an active pulldown to G_VID on all red/chroma outputs (AUX_R/C_OUT, TV_R/C_OUT, and VCR_R/C_OUT).

The MPEG decoder and VCR uses the RGB format to insert an on-screen display (OSD), usually text, onto the TV. A fast-switching signal controls whether the RGB signals or composite video signal appear on the TV. The MAX4399 supports RGB as an input from either the VCR or the MPEG decoder and as an output only to the TV. The red video signal of the RGB format and the chroma video signal of the S-VHS format share the same SCART connector pin; therefore RGB signals and S-VHS signals cannot be present at the same time. Loop-through is possible with a composite video signal but not with RGB signals because the RGB SCART pins are used for both input and output.

The VCR, MPEG decoder, auxiliary device, and TV use the S-VHS format, which is the high-quality format for the home today. The MAX4399 supports S-VHS as an input from the VCR, MPEG decoder, auxiliary device, and TV, and as a separately switchable output to the TV, VCR, and AUX SCART connectors. Because S-VHS support was not included in the original specification of the SCART connector, the Y signal of S-VHS and the CVBS signal share the same SCART connector pins. If S-VHS is present, then a composite signal must be created

Audio/Video Switch for Three SCART Connectors

from the Y and C signals to drive the legacy RF_CVBS_OUT output. The circuit is shown as a summing point with bias in Figure 2. The MAX4399 sums Y and C to get CVBS, and the bias provides the DC levels for offsetting the chroma signal. Again, loop-through is not possible with S-VHS because the chroma SCART pin is used for both input and output.

The MAX4399 supports the CVBS format, with inputs from the VCR, MPEG decoder, TV, and auxiliary device. Full loop-through is possible to all devices except the MPEG decoder because the SCART connector has separate input and output pins for the CVBS format.

Slow Switching

The MAX4399 supports the tri-level slow switching of IEC 933-1, Amendment 1, which selects the aspect ratio for the display device. Under I²C-compatible control, the MAX4399 sets the slow-switching output levels. Table 1 shows the valid output levels of the slow-switching signal and the corresponding operating modes of the display device.

The slow-switching SCART pins are bidirectional. The MAX4399 can set the slow-switch output drivers to high-impedance mode to receive signals. When enabled, INTERRUPT_OUT becomes high impedance if the voltage level changes on TV_SS, VCR_SS, or AUX_SS.

The VCR or MPEG decoder outputs a fast-switching signal to the display device. The fast-switching signal can also be set to a constant high or low through the 2-wire interface. The pass-through delay from VCR to TV or MPEG decoder to TV matches that of the RGB signals facilitating proper OSD insertion.

Video Outputs

The DC level at the video outputs is controlled so coupling capacitors are not required, and all of the video outputs are capable of driving a 150Ω, back-terminated coax load directly with respect to ground. Since some televisions and VCRs use the horizontal sync height for automatic gain control, the MAX4399 accurately reproduces the sync height to within ±2%.

Y/C Mixer and Trap Filter

The MAX4399 includes an on-chip mixer to produce CVBS from Y and C. The Y signal input to the mixer has an external trap filter connection, TRAP, to eliminate the color subcarrier frequency (4.43MHz), preventing cross-mixing of the subcarriers in the mixer. TRAP is internally biased at 0.5V. Connect a series RLC filter to G_VID, or leave TRAP unconnected if not used.

Table 1. Slow Switch Modes

SLOW-SWITCHING SIGNAL VOLTAGE (V)	MODE
0 to 2	Display device uses an internal source such as a built-in tuner to provide a video signal
4.5 to 7	Display device uses a video signal from the SCART connector and sets the display to 16:9 aspect ratio
9.5 to 12.6	Display device uses a signal from a SCART connector and sets the display to 4:3 aspect ratio

SCART Audio Switching

Audio Inputs

The audio block has four stereo audio inputs from the TV, VCR, and AUX SCART connectors, plus the MPEG decoder. Additionally, the MAX4399 provides a satellite tone input. Each input has a 100kΩ resistor connected to an internally generated voltage equal to 0.5 x V_AUD. There are three main sections—the TV channel, the VCR channel, and the AUX channel.

Audio Outputs

Each channel has a stereo output and the TV channel has an additional phono output and a mono output. The phono outputs always follow the TV audio input selection. The mono output, a mix of the TV right and left channels, drives the channel 3/4 RF modulator. The three stereo outputs can be configured to normal mode, swap mode, mono, both channels to right input, and both channels to left input. The latter two modes are useful if the left audio channel carries one language and the right audio channel carries another language. The phono output is ideal for connection to a hi-fi, and carries the same signals as the TV output when switched to normal mode.

The mono mixer, a resistor summer, attenuates the amplitude of each of the two signals by 6dB. The 3dB gain block, which follows the mono mixer (Figures 3 and 4), is a compromise between a 0dB gain block and a 6dB gain block. If the left and right audio channels were completely uncorrelated, then a 6dB gain block could be used. If the left and right channels were completely correlated, then a 0dB block would have to be used. In reality, most stereo audio channels are partially correlated and hence a 3dB gain block was used.

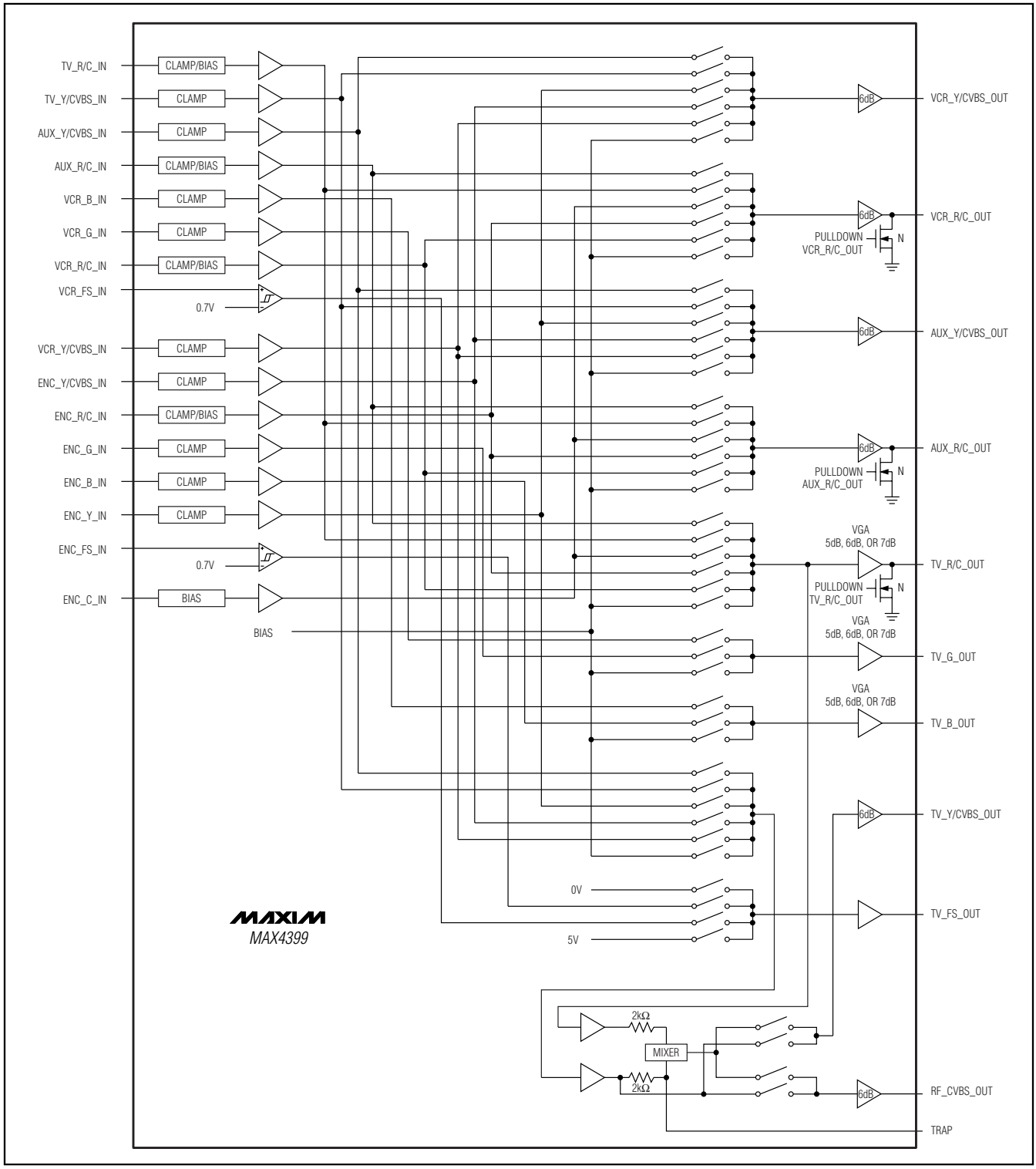


Figure 2. MAX4399 Video Section Functional Diagram

Audio/Video Switch for Three SCART Connectors

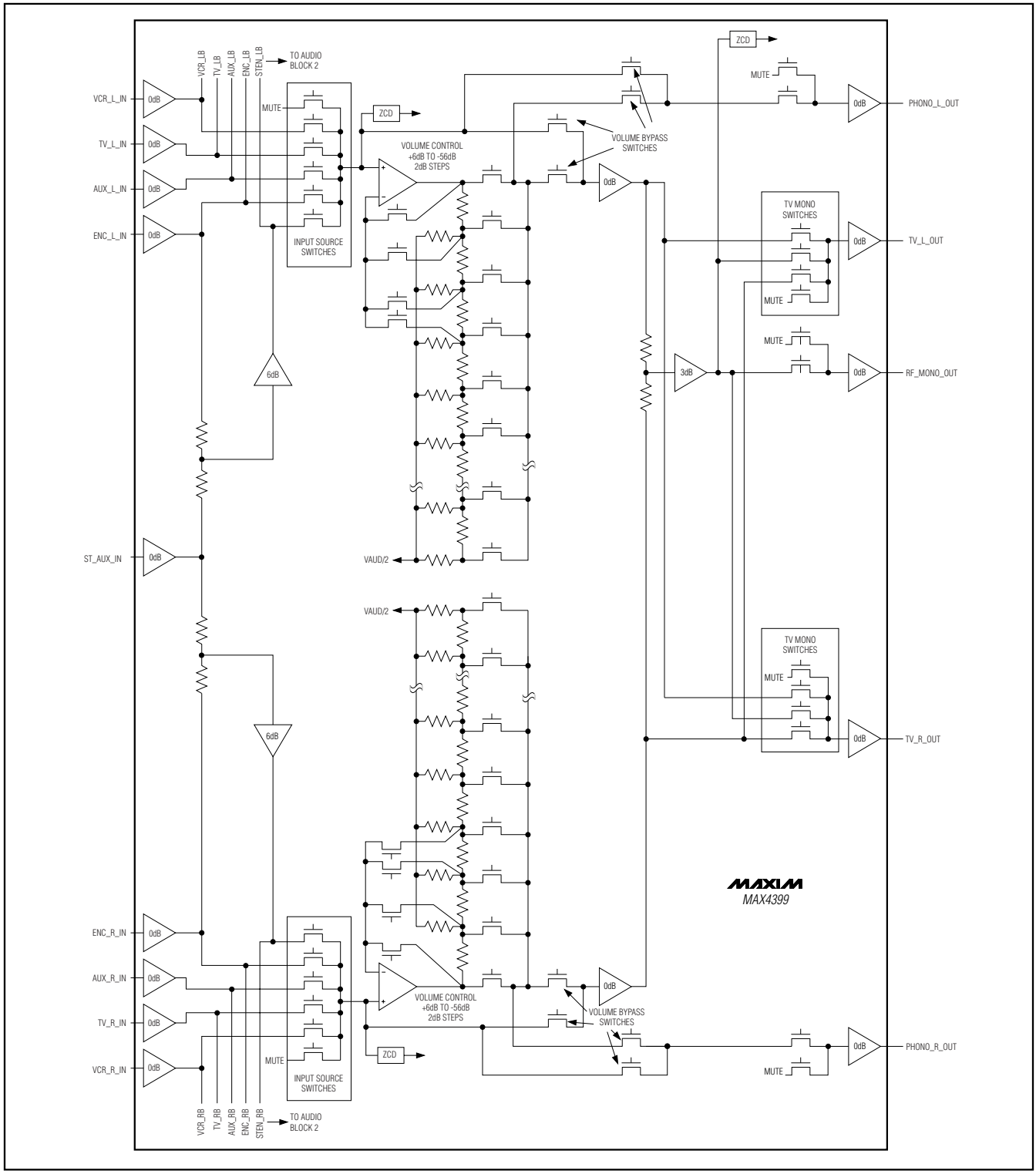


Figure 3. MAX4399 Audio Functional Diagram (AUDIO BLOCK 1)

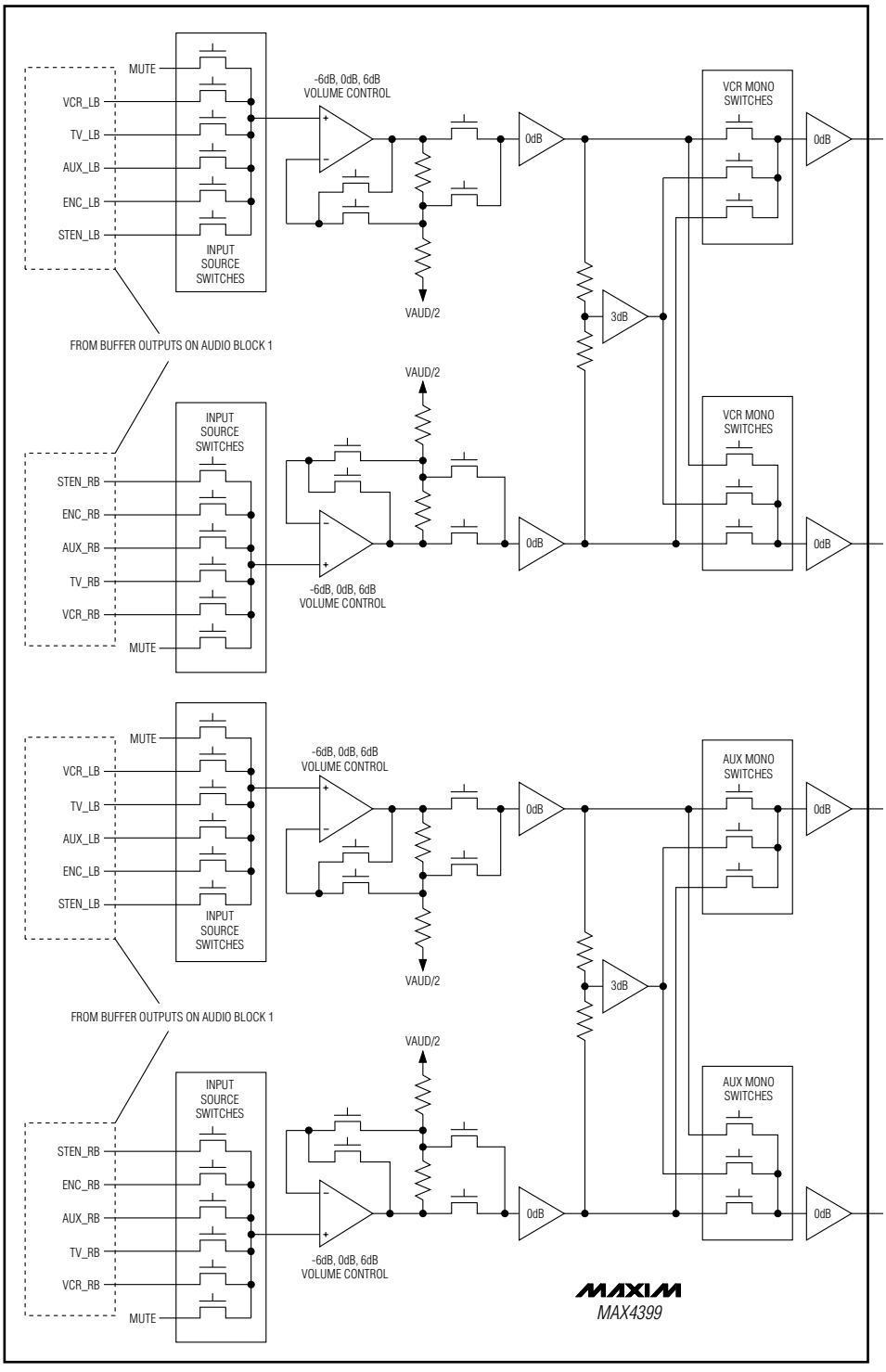


Figure 4. Audio Functional Diagram (AUDIO BLOCK2)

Audio/Video Switch for Three SCART Connectors

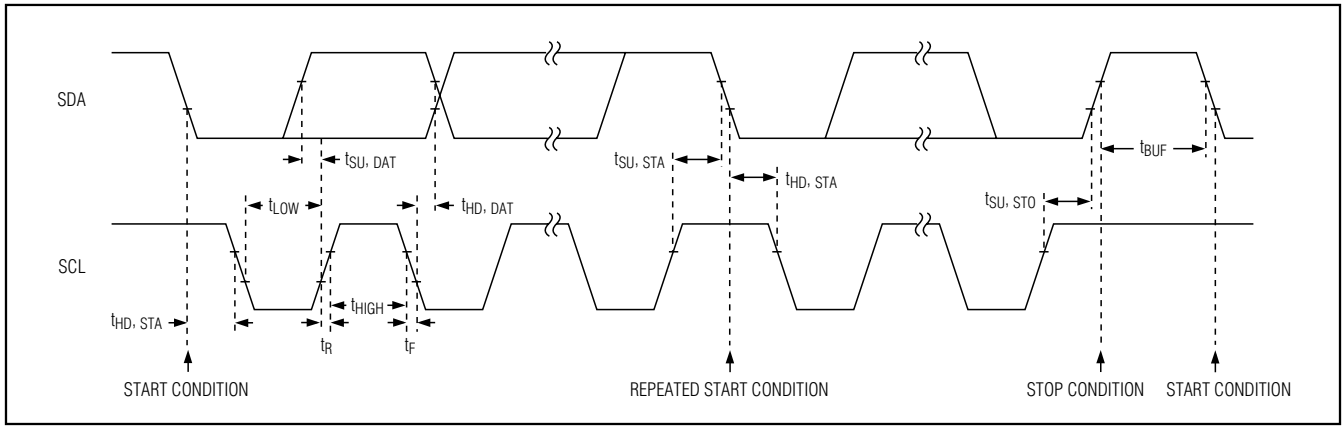


Figure 5. Timing Diagram for SDA and SCL Signals

Zero-Cross (Clickless) Switching

The TV channel incorporates a zero-crossing detect (ZCD) circuit that minimizes click noise due to abrupt signal level changes that occur when switching between audio signals at an arbitrary moment in time.

To implement the zero-cross function when switching audio signals, set the ZCD bit by loading register 00h through the I²C-compatible interface (if the ZCD bit is not already set). Then set the mute bit high by loading register 00h. Next, wait for a period of time long enough for the audio signal to cross zero. This period is a function of the audio signal path's low frequency 3dB corner (f_{L3dB}). For example, if f_{L3dB} = 20Hz, the time period to wait for zero cross is 1/20Hz or 50ms. Next, set the appropriate TV switches using register 01h. Finally, clear the mute bit (while leaving the ZCD bit high) using register 00h. The MAX4399 switches the signal out of mute at the next zero crossing.

To implement the zero-cross function for TV volume changes, or for TV and phono volume bypass switching, simply ensure the ZCD bit in register 00h is set.

Volume Control

The TV channel volume control ranges from -56dB to +6dB in 2dB increments. The VCR and AUX volume control settings are programmable for -6dB, 0dB, and +6dB. With the ZCD bit set, the TV volume control switches only at zero crossings, thus minimizing click noise. The TV outputs can bypass the volume control. While the phono outputs always follow the TV audio input selection, the phono outputs can either be processed through the TV volume control or they can bypass the TV volume control.

Digital Section

Serial Interface

The MAX4399 uses a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (µP) port. The fast-mode I²C-compatible serial interface allows communication at data rates up to 400kbps. Figure 5 shows the timing diagram for signals on the 2-wire bus.

The two bus lines (SDA and SCL) must be high when the bus is not in use. The MAX4399 is a slave device and must be controlled by a bus master device. Figure 6 shows a typical application where multiple devices can be connected to the bus provided they have different address settings. External pullup resistors are not necessary on these lines (when driven by push-pull drivers), though the MAX4399 can be used in applications where pullup resistors are required to maintain compatibility with existing circuitry. The serial interface operates at SCL rates up to 400kHz. The SDA state is allowed to change only while SCL is low, with the exception of START and STOP conditions as shown in Figure 7.

SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer each byte to the MAX4399. Release SDA during the 9th clock cycle as the selected device acknowledges the receipt of the byte, by pulling SDA low during this time. A series resistor on the SDA line may be needed if the master's output is forced high while the selected device acknowledges (Figure 6).

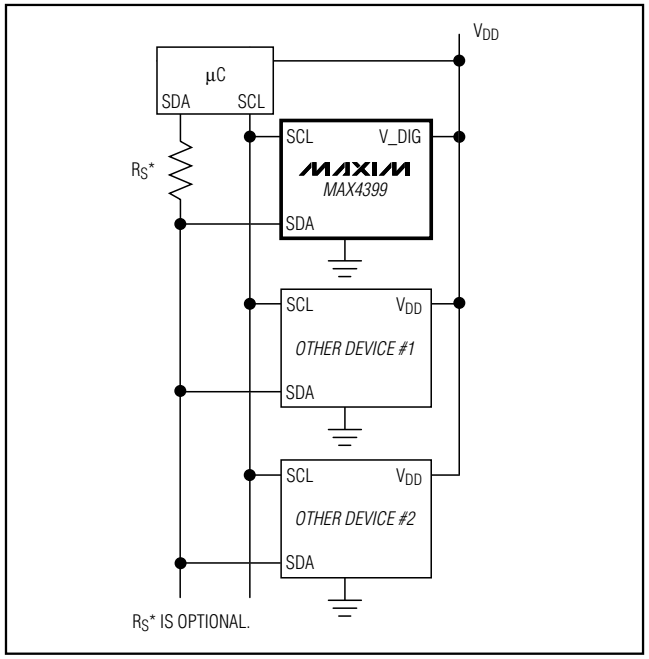


Figure 6. Multiple Devices Controlled by a 2-Wire Interface

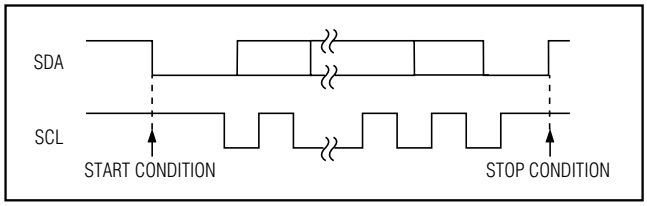


Figure 7. Start and Stop Conditions on a 2-Wire Interface

I²C Compatibility

The MAX4399 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs. SDA has an open drain that pulls the data line low during the 9th clock pulse. Figure 8 shows a typical I²C interface application. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The MAX4399 address is compatible with the 7-bit I²C addressing protocol only. No 10-bit formats are supported. RESTART protocol is supported, but an immediate STOP condition is necessary to update the MAX4399.

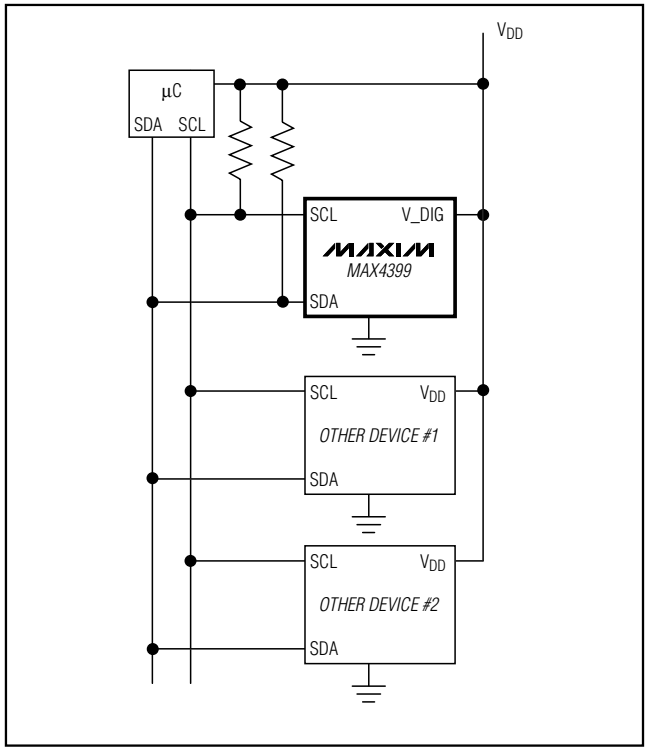


Figure 8. A Typical I²C Interface Application

Digital Inputs and Interface Logic

The I²C-compatible, 2-wire interface has logic levels defined as V_{OL} = 0.8V and V_{OH} = 2.0V. All of the inputs include Schmitt-trigger buffers to accept slow-transition interfaces. The digital inputs are compatible with 3V CMOS logic levels.

INTERRUPT_OUT Signal

INTERRUPT_OUT is an open-drain output that becomes high impedance when a change in any of the slow-switch signals occurs. Clear INTERRUPT_OUT by setting bit 3 of register 04h low.

Data Format of the 2-Wire Interface

Write mode

S	Slave Address	A	Register Address	A	Data	A	P

Read mode

S	Slave Address	A	Register Address	A	Data	A	P

Where S = Start Condition, A = Acknowledge, P = Stop Condition.

Audio/Video Switch for Three SCART Connectors

2-Wire Interface Slave Address Programming

Connect DEV_ADDR to G_DIG or V_DIG to set the MAX4399 write and read addresses as shown in Table 2.

Data Register Writing and Reading

Program the SCART video and audio switches by writing to registers 00h through 0Dh (Tables 3 through 18). Registers 00h through 0Dh can also be read, allowing read-back of data after programming and facilitating system debugging. The status register is read-only and can be read from address 0Eh (Table 19).

Table 2. Slave Address Programming

DEV_ADDR CONNECTION	WRITE ADDRESS	READ ADDRESS
G_DIG	94h	95h
V_DIG	96h	97h

Applications Information

Filtering of Encoder Outputs

The DAC outputs of encoder chips need to be processed through a lowpass filter (reconstruction filter) to attenuate out-of-band noise. Figure 9 shows how the MAX7440 provides an integrated, convenient solution for reconstruction filtering.

Table 3. Write Mode Input Data Format

REGISTER ADDRESS	POR VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	47h	Not used	ZCD	Volume control					TV audio mute
01h	07h	Not used	Not used	TV mono switch			TV audio selection		
02h	07h	VCR volume control		VCR mono switch			VCR audio selection		
03h	07h	AUX volume control		AUX mono switch			AUX audio selection		
04h	01h	Not used	Not used	Not used	Not used	Interrupt enable	TV volume bypass	Phono volume bypass	Not used
05h	00h	ENC_R/C_IN Clamp	Not used	Not used	Not used	Not used	Not used	Not used	Not used
06h	1Fh	TV_R/C_IN clamp	RGB gain		TV G and B video switch		TV video switch		
07h	20h	Not used	RF_CVBS_OUT switch	TV_Y/CVBS_ OUT switch	TV fast switch		TV_R/C_OUT ground	Set TV slow switch	
08h	07h	VCR_R/C_IN clamp	Not used	Not used	Not used	Not used	VCR video switch		
09h	00h	Not used	Not used	Not used	Not used	Not used	VCR_R/C_ OUT ground	Set VCR slow switch	
0Ah	07h	AUX_R/C_IN clamp	Not used	Not used	Not used	Not used	AUX video switch		
0Bh	00h	Not used	Not used	Not used	Not used	Not used	AUX_R/C_ OUT ground	Set AUX slow switch	
0Ch	00h	Not used	Not used	Not used	Not used	Not used	Not used	VCR_Y/ CVBS_ OUT enable	VCR_R/ C_OUT enable
0Dh	00h	AUX_Y/CVBS_ OUT enable	AUX_R/C_OUT enable	TV_R/C_OUT enable	TV_G_OUT enable	TV_B_OUT enable	TV_Y/CVBS_ OUT enable	TV_FB_ OUT enable	RF_CVBS_ OUT enable

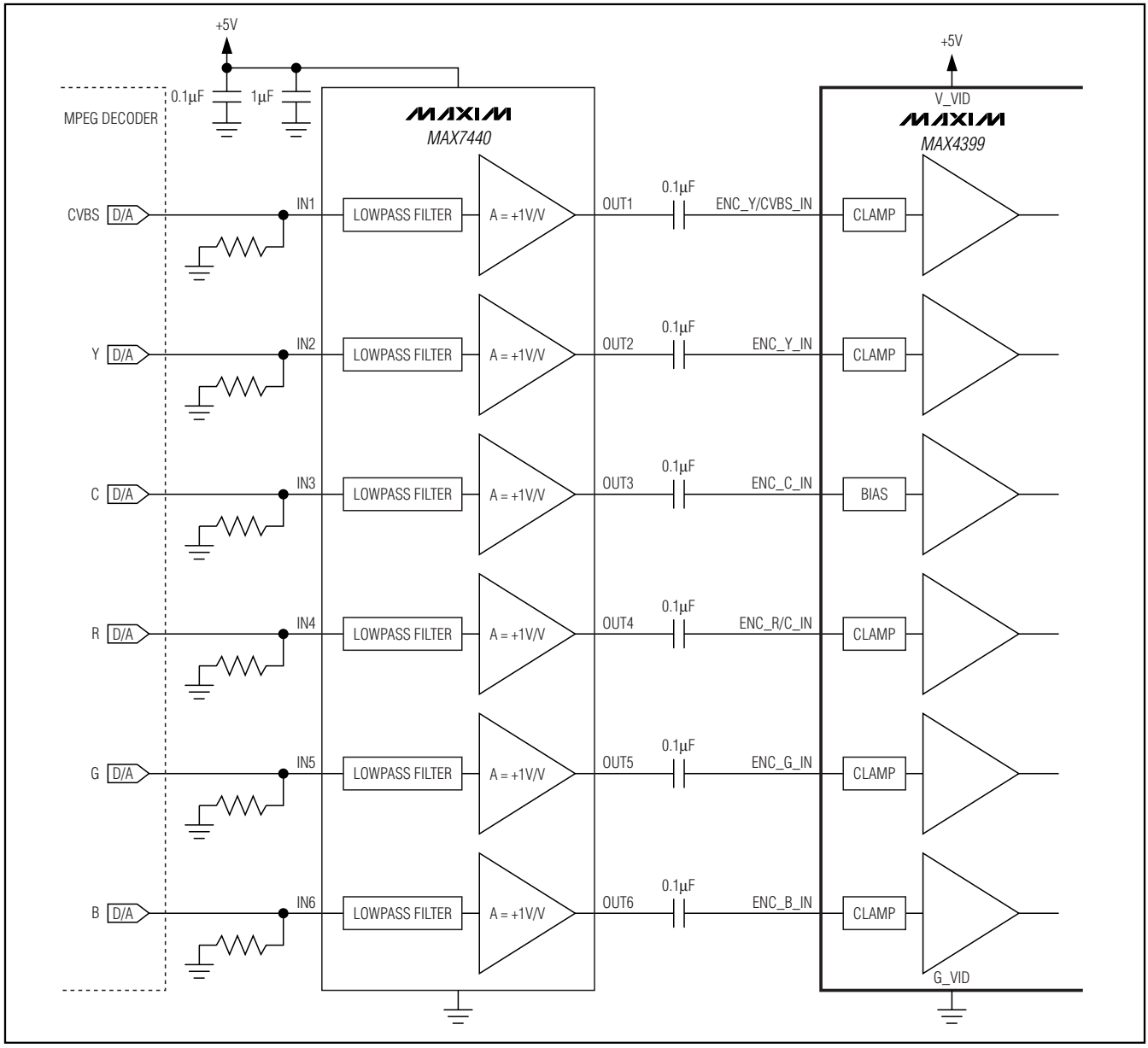
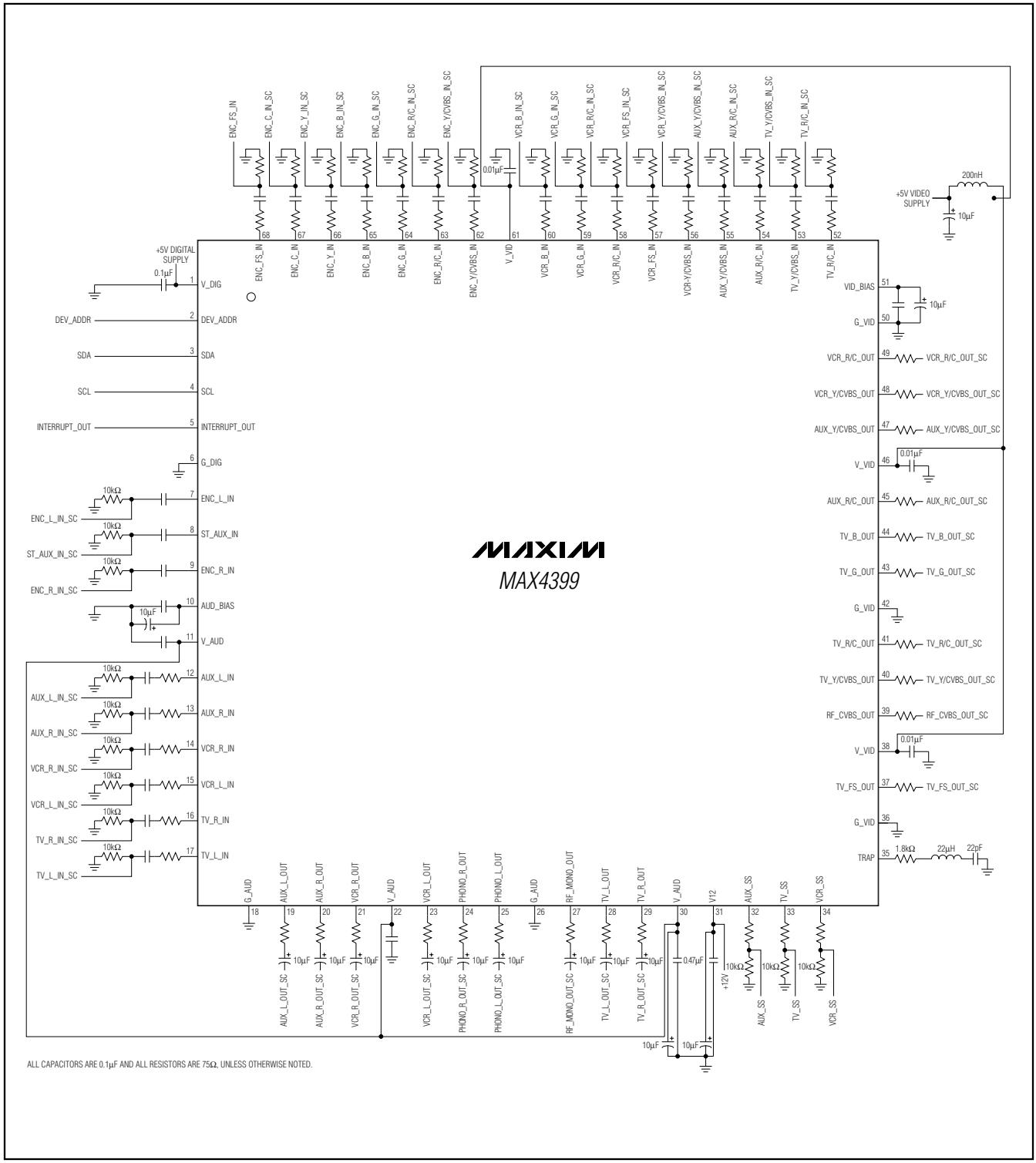


Figure 9. MPEG Decoder Outputs Filtered by the MAX7440 Before Being Passed to the MAX4399

Hot-Plug of SCART Connectors—Floating Chassis Discharge

The MAX4399 features high-ESD protection on all SCART inputs and outputs, and requires no external transient voltage suppressor (TVS) devices to protect against floating chassis discharge. Some set-top boxes have a floating chassis problem in which the chassis is not connected to earth ground. As a result, the chassis can charge up to 500V. When a SCART cable is connected to the SCART connector, the charged chassis can discharge through a signal pin. The equivalent circuit is a 2200pF capacitor charged to 311V connected through less than 0.1Ω to a signal pin. The MAX4399 is soldered on the PC board when it experiences such a discharge. Therefore, the current spike flows through the ESD protection diodes and is absorbed by the supply bypass capacitors, which have high capacitance and low ESR.

Audio/Video Switch for Three SCART Connectors



ALL CAPACITORS ARE 0.1µF AND ALL RESISTORS ARE 75Ω, UNLESS OTHERWISE NOTED.

Figure 10. Floating Chassis Discharge Protection Circuit

Read Mode: Output Data Format

Table 4. Read Mode Output Data Format

REGISTER ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0Eh	Not used	Power-on reset	AUX slow switch status		VCR slow switch status		TV slow switch status	

Write Mode: Description of Registers

Table 5. Register 00h: Audio Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Audio Mute	—	—	—	—	—	—	—	0	Off
	—	—	—	—	—	—	—	1	On (power-on default)
Volume Control	—	—	0	0	0	0	0	—	+6dB gain
	—	—	0	0	0	0	1	—	+4dB gain
	—	—	0	0	0	1	0	—	+2dB gain
	—	—	0	0	0	1	1	—	0dB gain (power-on default)
	—	—	0	0	1	0	0	—	-2dB gain
	—	—	0	0	1	0	1	—	-4dB gain
	—	—	—	—	—	—	—	—	—
	—	—	1	1	1	1	0	—	-54dB gain
	—	—	1	1	1	1	1	—	-56dB gain
Zero-Crossing Detector	—	0	—	—	—	—	—	—	Off
	—	1	—	—	—	—	—	—	On (power-on default)

To better protect the MAX4399 against excessive voltages during the cable discharge event, additional 75Ω resistors should be placed in series with all inputs and outputs that go to the SCART connector (Figure 10). For harsh environments needing ±15kV protection, the MAX4385E and MAX4386E single and quad high-speed op amps feature the industry's first integrated ±15kV ESD protection on video inputs and outputs.

Power Supplies and Bypassing

The MAX4399 features single +5V and +12V supply operation, and requires no negative supply. The +12V supply provides voltage for SCART function switching, and provides power for the internally generated audio supply, V_AUD. Place all bypass capacitors as close as possible to the MAX4399. Bypass V12 to ground with a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. Connect all V_AUD pins together and bypass pin 30 with a 10µF electrolytic capacitor in parallel with a 0.47µF low-ESR ceramic capacitor to audio ground. Bypass V_AUD pins 11 and 22 each with a 0.1µF capacitor to audio ground. Bypass AUD_BIAS to audio ground with a 10µF electrolytic in parallel with a 0.1µF ceramic capacitor.

Bypass V_DIG with a 0.1µF ceramic capacitor to digital ground. Bypass each V_VID to video ground with a 0.01µF ceramic capacitor. Connect V_VID in series with a 200nH ferrite bead to the +5V supply. Bypass the internally generated video bias, VID_BIAS with a 0.1µF low-ESR ceramic capacitor to G_VID.

Layout and Grounding

For optimal performance, use controlled-impedance traces for video signal paths, and place input termination resistors and output back-termination resistors close to the MAX4399. Avoid running video traces parallel to high-speed data lines.

The MAX4399 provides separate ground connections for video, audio, and digital supplies. For best performance use separate ground planes for each of the ground returns, and connect all three ground planes together at a single point. Refer to the MAX4399 evaluation kit for a proven circuit board layout example.

Audio/Video Switch for Three SCART Connectors

Table 6. Register 01h: TV Audio

DESCRIPTION	BIT								COMMENTS		
	7	6	5	4	3	2	1	0			
Input Source for TV Audio	—	—	—	—	—	0	0	0	Encoder audio		
	—	—	—	—	—	0	0	1	VCR audio		
	—	—	—	—	—	0	1	0	AUX audio		
	—	—	—	—	—	0	1	1	TV audio		
	—	—	—	—	—	1	0	0	Encoder audio + tones		
	—	—	—	—	—	1	0	1	Mute		
	—	—	—	—	—	1	1	0	Mute		
	—	—	—	—	—	1	1	1	Mute (power-on default)		
TV Mono Switch Settings	—	—	—	—	—	—	—	—	L CHANNEL OUTPUT	R CHANNEL OUTPUT	—
	—	—	0	0	0	—	—	—	L	R	Normal (power-on default)
	—	—	0	0	1	—	—	—	R+L	R+L	Mono mix
	—	—	0	1	0	—	—	—	R	L	Swap
	—	—	0	1	1	—	—	—	R	R	R channel only
	—	—	1	0	0	—	—	—	L	L	L channel only
	—	—	1	0	1	—	—	—	L	R	Normal
	—	—	1	1	0	—	—	—	L	R	Normal
	—	—	1	1	1	—	—	—	L	R	Normal

Table 7. Register 02h: VCR Audio

DESCRIPTION	BIT								COMMENTS		
	7	6	5	4	3	2	1	0			
Input Source for VCR Audio	—	—	—	—	—	0	0	0	Encoder audio		
	—	—	—	—	—	0	0	1	VCR audio		
	—	—	—	—	—	0	1	0	AUX audio		
	—	—	—	—	—	0	1	1	TV audio		
	—	—	—	—	—	1	0	0	Encoder audio + tones		
	—	—	—	—	—	1	0	1	Mute		
	—	—	—	—	—	1	1	0	Mute		
	—	—	—	—	—	1	1	1	Mute (power-on default)		
VCR Mono Switch Settings	—	—	—	—	—	—	—	—	L CHANNEL OUTPUT	R CHANNEL OUTPUT	—
	—	—	0	0	0	—	—	—	L	R	Normal (power-on default)
	—	—	0	0	1	—	—	—	R+L	R+L	Mono mix
	—	—	0	1	0	—	—	—	R	L	Swap
	—	—	0	1	1	—	—	—	R	R	R-channel only
	—	—	1	0	0	—	—	—	L	L	L-channel only
	—	—	1	0	1	—	—	—	L	R	Normal
	—	—	1	1	0	—	—	—	L	R	Normal
	—	—	1	1	1	—	—	—	L	R	Normal
VCR Volume Control	0	0	—	—	—	—	—	—	0dB (power-on default)		
	0	1	—	—	—	—	—	—	+6dB		
	1	0	—	—	—	—	—	—	0dB		
	1	1	—	—	—	—	—	—	-6dB		

Audio/Video Switch for Three SCART Connectors

Table 8. Register 03h: AUX Audio

DESCRIPTION	BIT								COMMENTS		
	7	6	5	4	3	2	1	0			
Input Source for AUX Audio	—	—	—	—	—	0	0	0	Encoder audio		
	—	—	—	—	—	0	0	1	VCR audio		
	—	—	—	—	—	0	1	0	AUX audio		
	—	—	—	—	—	0	1	1	TV audio		
	—	—	—	—	—	1	0	0	Encoder audio + tones		
	—	—	—	—	—	1	0	1	Mute		
	—	—	—	—	—	1	1	0	Mute		
	—	—	—	—	—	1	1	1	Mute (power-on default)		
AUX Mono Switch Settings	—	—	—	—	—	—	—	—	L CHANNEL OUTPUT	R CHANNEL OUTPUT	—
	—	—	0	0	0	—	—	—	L	R	Normal (power-on default)
	—	—	0	0	1	—	—	—	R+L	R+L	Mono mix
	—	—	0	1	0	—	—	—	R	L	Swap
	—	—	0	1	1	—	—	—	R	R	R channel only
	—	—	1	0	0	—	—	—	L	L	L channel only
	—	—	1	0	1	—	—	—	L	R	Normal
	—	—	1	1	0	—	—	—	L	R	Normal
	—	—	1	1	1	—	—	—	L	R	Normal
AUX Volume Control	0	0	—	—	—	—	—	—	0dB (power-on default)		
	0	1	—	—	—	—	—	—	+6dB		
	1	0	—	—	—	—	—	—	0dB		
	1	1	—	—	—	—	—	—	-6dB		

Table 9. Register 04h: Volume Control Bypass

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Phono Volume Bypass	—	—	—	—	—	—	0	—	Phono audio passes through volume control (power-on default)
	—	—	—	—	—	—	1	—	Phono audio bypasses volume control
TV Volume Bypass	—	—	—	—	—	0	—	—	TV audio passes through volume control (power-on default)
	—	—	—	—	—	1	—	—	TV audio bypasses volume control
Interrupt Enable	—	—	—	—	0	—	—	—	Clear INTERRUPT_OUT (power-on default)
	—	—	—	—	1	—	—	—	Enable INTERRUPT_OUT

Table 10. Register 05h: Encoder Video Input Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
ENC_R/C_IN Clamp/Bias	0	—	—	—	—	—	—	—	DC restore clamp active at input (power-on default)
	1	—	—	—	—	—	—	—	Chroma bias applied at input

Table 11. Register 06h: TV Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for TV Video	—	—	—	—	—	—	—	—	TV_Y/CVBS_OUT	TV_R/C_OUT
	—	—	—	—	—	0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
	—	—	—	—	—	0	0	1	ENC_Y_IN	ENC_C_IN
	—	—	—	—	—	0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
	—	—	—	—	—	0	1	1	AUX_Y/CVBS_IN	AUX_R/C_IN
	—	—	—	—	—	1	0	0	TV_Y/CVBS_IN	TV_R/C_IN
	—	—	—	—	—	1	0	1	Mute	Mute
	—	—	—	—	—	1	1	0	Mute	Mute
	—	—	—	—	—	1	1	1	Mute (power-on default)	Mute (power-on default)
Input Sources for TV_G_OUT and TV_B_OUT	—	—	—	—	—	—	—	—	TV_G_OUT	TV_B_OUT
	—	—	—	0	0	—	—	—	ENC_G_IN	ENC_B_IN
	—	—	—	0	1	—	—	—	VCR_G_IN	VCR_B_IN
	—	—	—	1	0	—	—	—	Mute	Mute
	—	—	—	1	1	—	—	—	Mute (power-on default)	Mute (power-on default)
RGB Gain	—	0	0	—	—	—	—	—	6dB (power-on default)	
	—	0	1	—	—	—	—	—	7dB	
	—	1	0	—	—	—	—	—	5dB	
	—	1	1	—	—	—	—	—	5dB	
TV_R/C_IN Clamp/Bias	0	—	—	—	—	—	—	—	DC restore clamp active at input (power-on default)	
	1	—	—	—	—	—	—	—	Chroma bias applied at input	