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# MAX4484/MAX4486/ MAX4487

# Single/Dual/Quad, Low-Cost, Single-Supply 7MHz, Rail-to-Rail Op Amps

## General Description

The MAX4484/MAX4486/MAX4487 single/dual/quad low-cost general-purpose op amps operate from a single +2.7V to +5.5V supply. The op amps are unity-gain stable with a 7MHz gain-bandwidth product, capable of driving an external 2kΩ load with rail-to-rail output swing. The amplifiers are stable with capacitive loads of up to 100pF. The MAX4484/MAX4486/MAX4487 are specified from -40°C to +125°C, making them suitable for a variety of harsh environments.

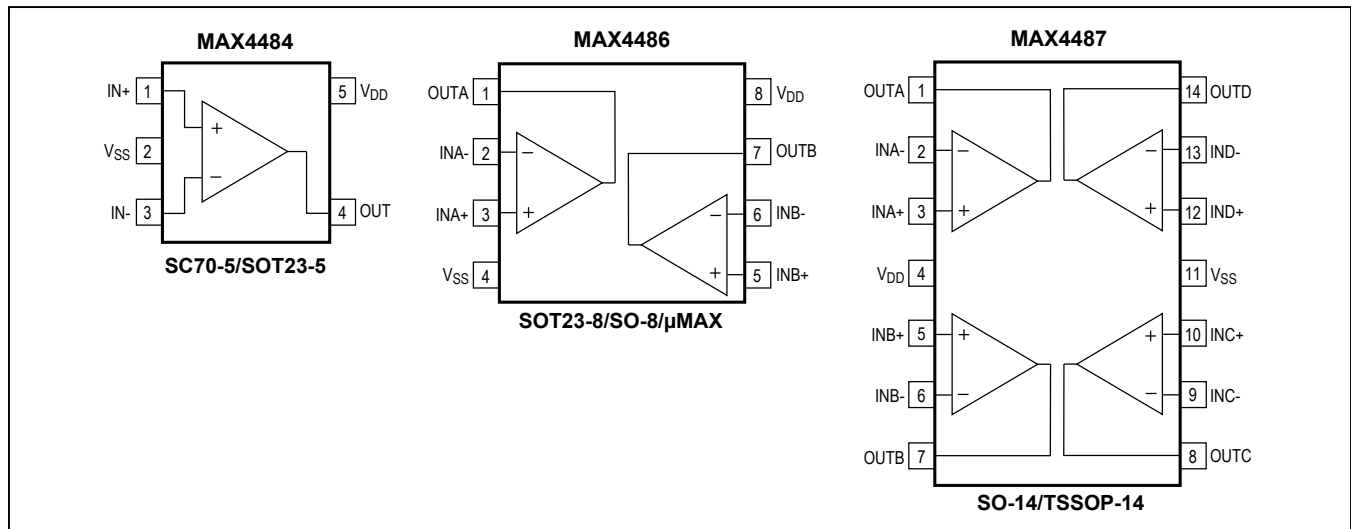
The single MAX4484 is available in the ultra-small 5-pin SC70, while the dual MAX4486 is packaged in the space-saving 8-pin SOT23 and μMAX® packages. The quad MAX4487 is available in the 14-pin SO and TSSOP packages.

## Applications

- Single-Supply Zero-Crossing Detector
- Instruments and Terminals
- Portable Communicators
- Electronic Ignition Modules
- Infrared Receivers for Remote Controls
- Sensor Signal Detection

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## Pin Configurations/Functional Diagrams



## Features

- 7MHz Unity-Gain Stable Bandwidth
- Stable for Capacitive Loads Up to 100pF
- +2.7V to +5.5V Single-Supply Voltage Range
- Ground-Sensing Inputs
- Outputs Swing Rail-to-Rail
- No Phase Reversal for Overdriven Inputs
- 85dB A<sub>VOL</sub> with 2kΩ Load
- 0.01% THD with 2kΩ Load
- Available in Space-Saving Packages
  - 5-Pin SC70 (MAX4484)
  - 8-Pin SOT23 (MAX4486)

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4484AXK-T	-40°C to +125°C	5 SC70-5	ABQ
MAX4484AUK-T	-40°C to +125°C	5 SOT23-5	ADPE
MAX4486AKA-T	-40°C to +125°C	8 SOT23-8	AAEP
MAX4486ASA	-40°C to +125°C	8 SO	—
MAX4486AUA	-40°C to +125°C	8 μMAX	—
MAX4487AUD	-40°C to +125°C	14 TSSOP	—
MAX4487ASD	-40°C to +125°C	14 SO	—

### Absolute Maximum Ratings

Power Supply Voltage ( $V_{DD}$ to $V_{SS}$ ).....	-0.3V to +6V	8-Pin $\mu$ MAX (derate 4.5mW/°C above +70°C).....	362mW
All Other Pins .....	( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )	14-Pin TSSOP (derate 9.1mW/°C above +70°C).....	727mW
Output Short-Circuit Duration (OUT shorted to $V_{DD}$ or $V_{SS}$ ) .....	Continuous	14-Pin SO (derate 8.33mW/°C above +70°C).....	667mW
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )		Operating Temperature Range.....	-55°C to +125°C
5-Pin SC70 (derate 3.1mW/°C above +70°C).....	247mW	Junction Temperature.....	+150°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C) .....	571mW	Storage Temperature Range.....	-65°C to +150°C
8-Pin SOT23 (derate 9.1mW/°C above +70°C) .....	727mW	Lead Temperature (soldering, 10s) .....	+300°C
8-Pin SO (derate 5.88mW/°C above +70°C).....	471mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Electrical Characteristics— $T_A = +25^\circ\text{C}$

( $V_{DD} = +5.0V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	Inferred from PSRR test	2.7		5.5	V
Supply Current per Amplifier	$I_{DD}$	$V_{DD} = +2.7V$		1.9		mA
		$V_{DD} = +5.0V$		2.2	3.5	
Input Offset Voltage	$V_{OS}$	MAX4484		$\pm 0.3$	$\pm 5.0$	mV
		MAX4486		$\pm 0.3$	$\pm 7.0$	
		MAX4487		$\pm 0.3$	$\pm 9.0$	
Input Bias Current	$I_B$	(Note 1)		$\pm 0.1$	100	pA
Input Offset Current	$I_{OS}$	(Note 1)		$\pm 0.1$	100	pA
Input Resistance	$R_{IN}$	Differential or common mode		1000		G $\Omega$
Input Common-Mode Voltage Range	$V_{CM}$	Inferred from CMRR test	$V_{SS}$		$V_{DD} - 1.3$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq V_{DD} - 1.3V$	67	83		dB
Power-Supply Rejection Ratio	PSRR	$+2.7V \leq V_{DD} \leq +5.5V$	70	85		dB
Large-Signal Voltage Gain	$A_{VOL}$	$V_{SS} + 0.3V \leq V_{OUT} \leq V_{DD} - 0.3V$ , $R_L = 1k\Omega$	$R_L = 100k\Omega$		98	dB
			$R_L = 2k\Omega$	76	85	
Output Voltage High	$V_{OH}$	Specified as $ V_{DD} - V_{OH} $	$R_L = 100k\Omega$		3	mV
			$R_L = 2k\Omega$		15	
Output Voltage Low	$V_{OL}$	Specified as $ V_{OL} - V_{SS} $	$R_L = 100k\Omega$		1	mV
			$R_L = 2k\Omega$		20	
Output Short-Circuit Current	$I_{SC}$	Sourcing		27		mA
		Sinking		33		
Gain-Bandwidth Product	GBW			7		MHz
Phase Margin	$\phi_m$			55		degrees
Gain Margin	Gm			12		dB
Slew Rate	SR			20		V/ $\mu$ s



### Electrical Characteristics— $T_A = +25^\circ\text{C}$

( $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage-Noise Density	$e_n$	$f = 10\text{kHz}$		29		$\text{nV}/\sqrt{\text{Hz}}$
Input Current-Noise Density	$i_n$	$f = 10\text{kHz}$		1		$\text{fA}/\sqrt{\text{Hz}}$
Capacitive-Load Stability	$C_{LOAD}$	$A_V = +1\text{V/V}$ (Note 1)	100			pF
Power-On Time	$t_{ON}$			1		$\mu\text{s}$
Input Capacitance	$C_{IN}$			2		pF
Total Harmonic Distortion	THD	$f = 10\text{kHz}$ , $V_{OUT} = 2V_{P-P}$ , $A_V = +1\text{V/V}$	$R_L = 100\text{k}\Omega$	0.006		%
			$R_L = 2\text{k}\Omega$	0.01		
Settling Time to 0.01%	$t_S$	$V_{OUT} = 4\text{V}$ step, $A_V = +1\text{V/V}$		450		ns

### Electrical Characteristics— $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

( $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ , unless otherwise noted.) (Note 2)

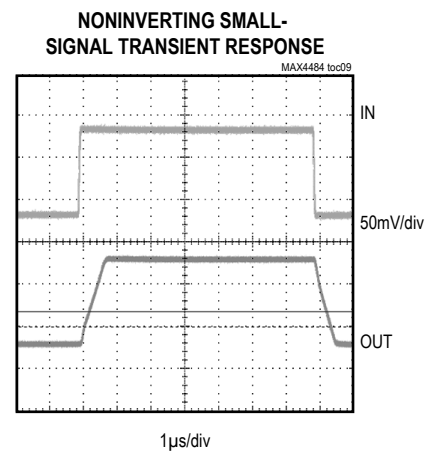
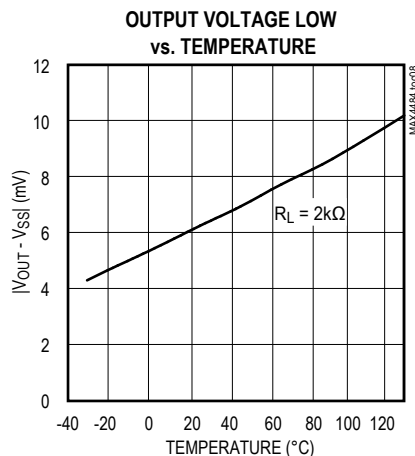
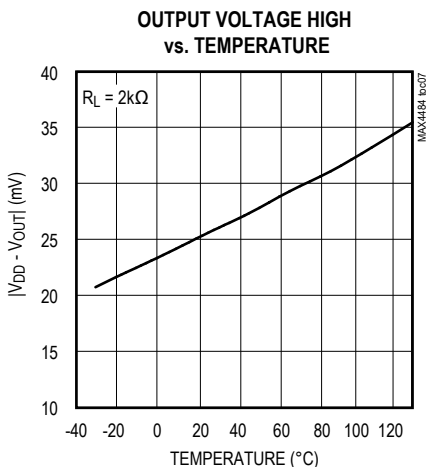
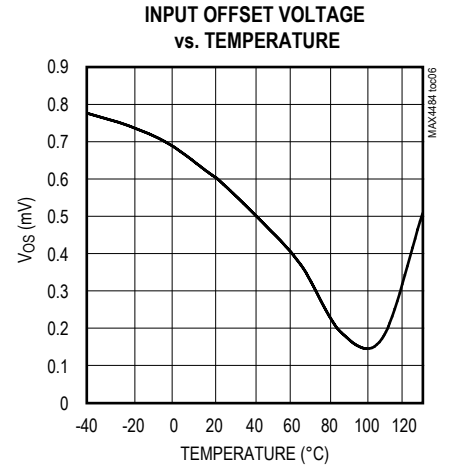
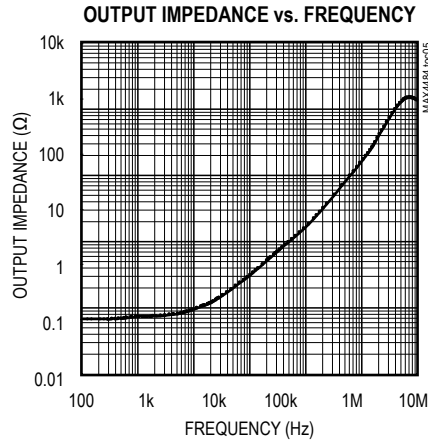
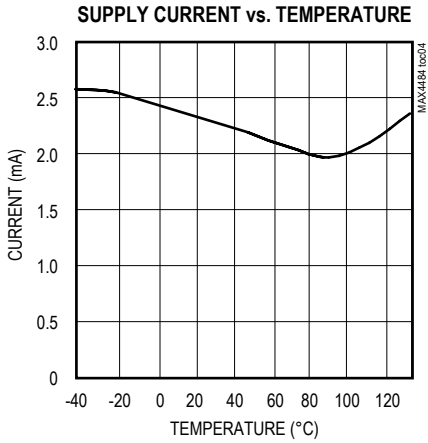
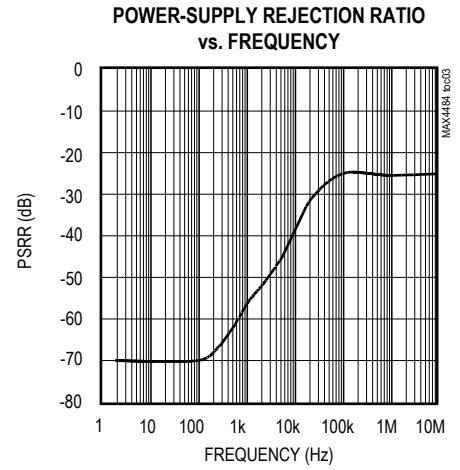
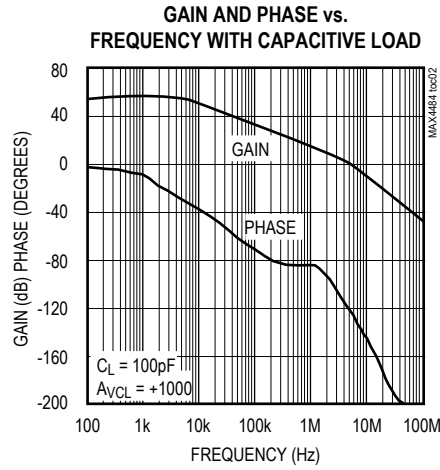
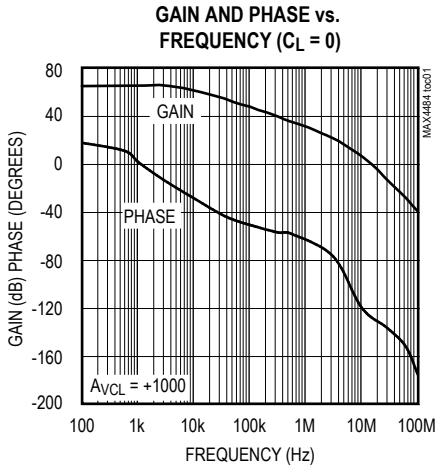
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	Inferred from PSRR test	2.7		5.5	V
Supply Current per Amplifier	$I_{DD}$				4.0	mA
Input Offset Voltage	$V_{OS}$	MAX4484			$\pm 8.5$	mV
		MAX4486			$\pm 10.0$	
		MAX4487			$\pm 11.0$	
Input Offset Voltage Drift	$TC_{VOS}$			$\pm 6$		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	(Note 1)			$\pm 100$	pA
Input Offset Current	$I_{OS}$	(Note 1)			$\pm 100$	pA
Input Common-Mode Voltage Range	$V_{CM}$	Inferred from CMRR test	$V_{SS}$		$V_{DD} - 1.4$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq V_{DD} - 1.4\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	65		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	62		
Power-Supply Rejection Ratio	PSRR	$+2.7\text{V} \leq V_{DD} \leq +5.5\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	67		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	64		
Large-Signal Voltage Gain	$A_{VOL}$	$V_{SS} + 0.3\text{V} \leq V_{OUT} \leq V_{DD} - 0.3\text{V}$ , $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	66		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	62		
Output Voltage High	$V_{OH}$	$ V_{DD} - V_{OUT} $ , $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	100		
Output Voltage Low	$V_{OL}$	$ V_{OUT} - V_{SS} $ , $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	250		

**Note 1:** Guaranteed by design.

**Note 2:** Specifications are 100% tested at  $T_A = +25^\circ\text{C}$  (exceptions marked). All temperature limits are guaranteed by design.

Typical Operating Characteristics

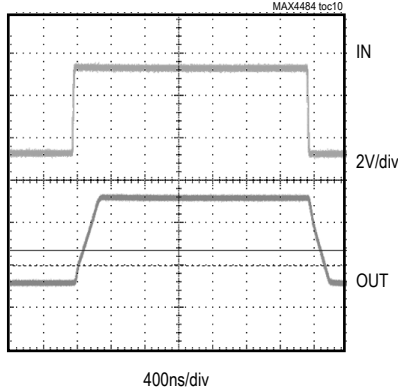
( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ , unless otherwise noted.)



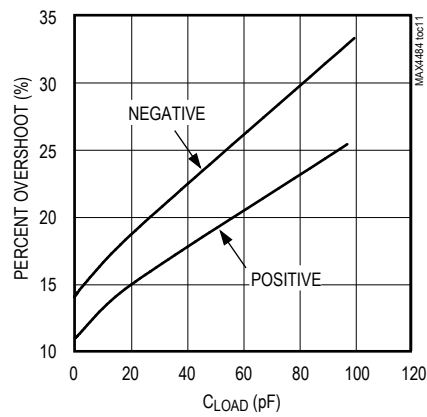
Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ , unless otherwise noted.)

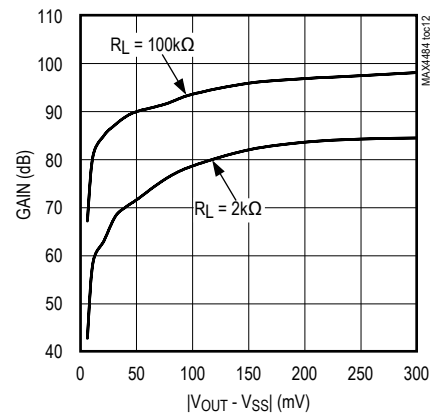
NONINVERTING LARGE-SIGNAL  
TRANSIENT RESPONSE



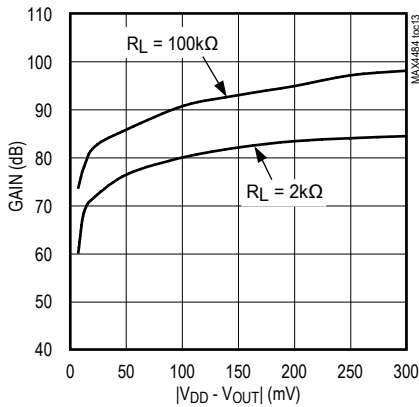
PERCENT OVERSHOOT  
vs. CAPACITIVE LOAD



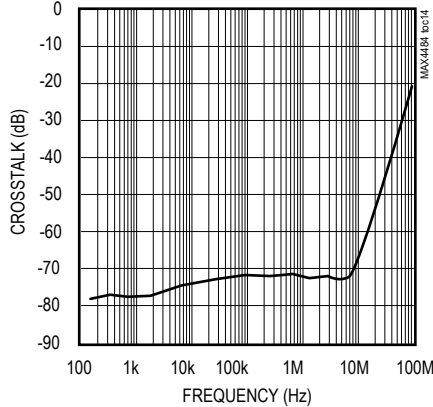
LARGE-SIGNAL GAIN  
vs. OUTPUT VOLTAGE LOW



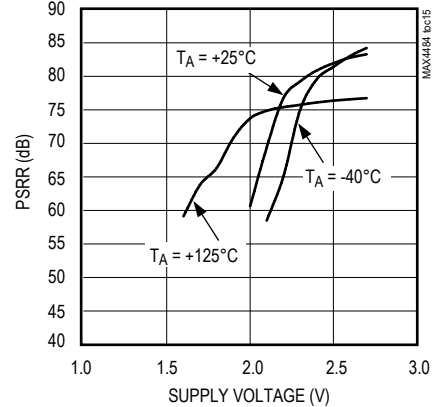
LARGE-SIGNAL GAIN  
vs. OUTPUT VOLTAGE HIGH



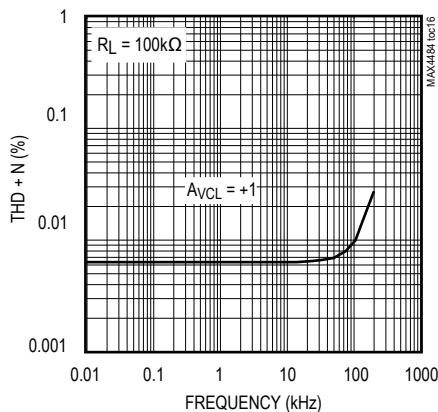
CROSSTALK vs. FREQUENCY



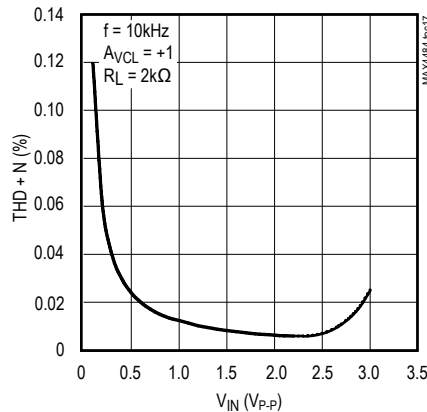
POWER-SUPPLY REJECTION RATIO  
vs. OPERATING VOLTAGE



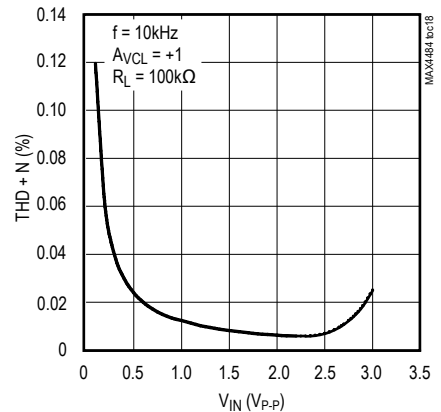
TOTAL HARMONIC DISTORTION  
PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION  
PLUS NOISE vs. AMPLITUDE



TOTAL HARMONIC DISTORTION  
PLUS NOISE vs. AMPLITUDE



## Pin Description

PIN			NAME	FUNCTION
MAX4484	MAX4486	MAX4487		
3	—	—	IN-	Inverting Amplifier Input
1	—	—	IN+	Noninverting Amplifier Input
4	—	—	OUT	Amplifier Output
—	2	2	INA-	Inverting Amplifier Input (Channel A)
—	3	3	INA+	Noninverting Amplifier Input (Channel A)
—	1	1	OUTA	Amplifier Output (Channel A)
—	6	6	INB-	Inverting Amplifier Input (Channel B)
—	5	5	INB+	Noninverting Amplifier Input (Channel B)
—	7	7	OUTB	Amplifier Output (Channel B)
—	—	9	INC-	Inverting Amplifier Input (Channel C)
—	—	10	INC+	Noninverting Amplifier Input (Channel C)
—	—	8	OUTC	Amplifier Output (Channel C)
—	—	13	IND-	Inverting Amplifier Input (Channel D)
—	—	12	IND+	Noninverting Amplifier Input (Channel D)
—	—	14	OUTD	Amplifier Output (Channel D)
2	4	11	V <sub>SS</sub>	Negative Power-Supply Voltage
5	8	4	V <sub>DD</sub>	Positive Power-Supply Voltage

## Detailed Description

### Rail-to-Rail Output Stage

The MAX4484/MAX4486/MAX4487 can drive a 2kΩ load and still swing within 50mV of the supply rails. Figure 1 shows the output swing of the MAX4484 configured with  $A_V = +1V/V$ .

### Driving Capacitive Loads

Driving a capacitive load can cause instability in many op amps, especially those with low quiescent current. The MAX4484/MAX4486/MAX4487 are unity-gain stable for a range of capacitive loads up to 100pF. Figure 2 shows the response of the MAX4484 with an excessive capacitive load. Adding a series resistor between the output and the load capacitor (Figure 3) improves the circuit's response by isolating the load capacitance from the op amp's output.

## Applications Information

### Power Supplies and Layout

The MAX4484/MAX4486/MAX4487 operate from a single +2.7V to +5.5V power supply. Bypass the power supply with 0.1μF capacitor to ground. Good layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins. Use surface-mount components for best results.

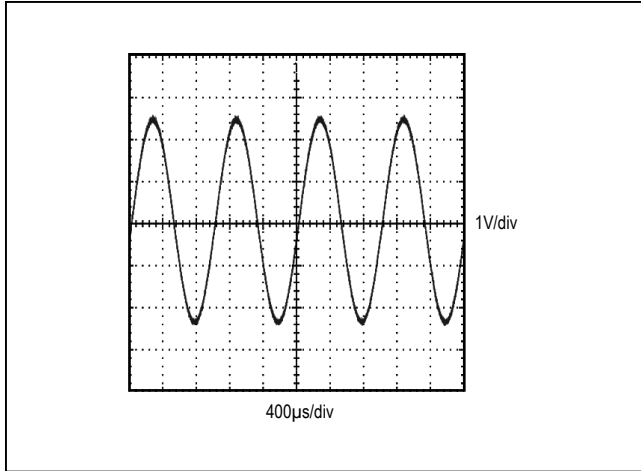


Figure 1. Rail-to-Rail Output Operation

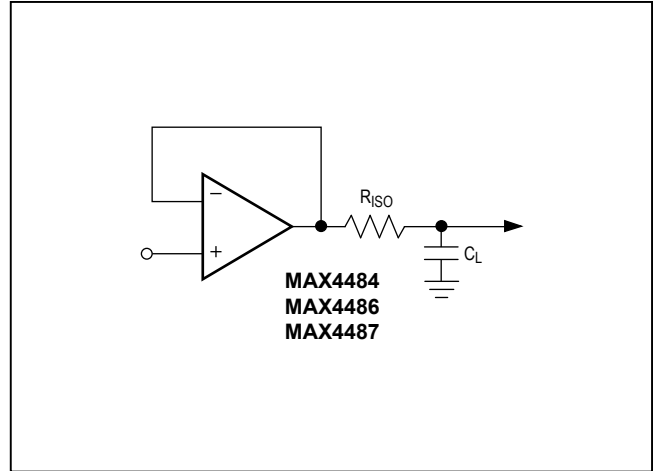


Figure 3. Capacitive-Load-Driving Circuit

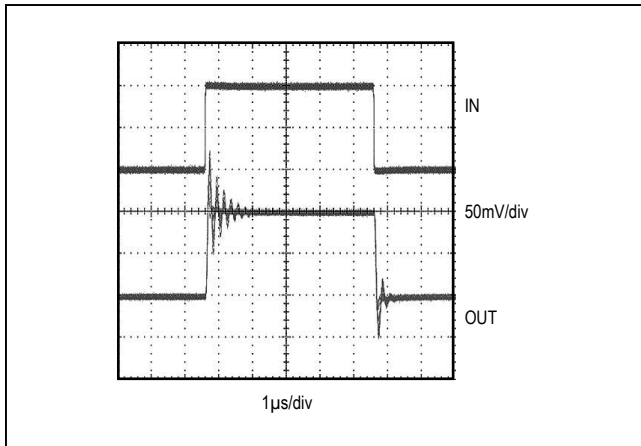


Figure 2. Small-Signal Transient Response with Excessive Capacitive Load ( $C_L = 270\text{pF}$ )

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
5 SC70	X5-1	21-0076	90-0188
5 SOT23	U5-1	21-0057	90-0174
8 SOT23	U8-1	21-0036	90-0092
8 SO	S8-2	21-0041	90-0096
8 µMAX	K8-5	21-0078	90-0176
14 TSSOP	U14-1	21-0066	90-0113
14 SO	S14-1	21-0041	90-0112



MAX4484/MAX4486/  
MAX4487

Single/Dual/Quad, Low-Cost, Single-Supply  
7MHz, Rail-to-Rail Op Amps

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/00	Initial release	—
1	5/14	Updated <i>General Description</i>	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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