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19-1136; Rev 6; 7/07

MAXIM

Quad, Low-Voltage, SPST Analog Switches

General Description

The MAX4521/MAX4522/MAX4523 are quad, low-voltage, single-pole/single-throw (SPST) analog switches. On-resistance (100Ω max) is matched between switches to 4Ω max, and is flat (12Ω max) over the specified signal range. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

The MAX4521 has four normally closed (NC) switches, and the MAX4522 has four normally open (NO) switches. The MAX4523 has two NC switches and two NO switches.

These CMOS switches can operate with dual power supplies ranging from ±2V to ±6V or a single supply between +2V and +12V. They are fully specified for single +2.7V operation.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment

Data Acquisition

Test Equipment

Avionics

Audio Signal Routing

Networking

Features

- **+2V to +12V Single Supply ±2V to ±6V Dual Supplies**
- **100Ω Signal Paths with ±5V Supplies**
- **Low Power Consumption, <1µW**
- **4 Separately Controlled SPST Switches**
- **Rail-to-Rail Signal Handling**
- **Pin Compatible with Industry-Standard DG211/DG212/DG213**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with ±5V or Single +5V Supply**

Ordering Information

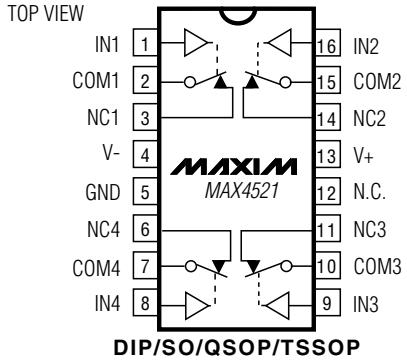
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4521CPE	0°C to +70°C	16 Plastic DIP	P16-1
MAX4521CSE	0°C to +70°C	16 Narrow SO	S16-2
MAX4521CEE	0°C to +70°C	16 QSOP	E16-4
MAX4521CUE	0°C to +70°C	16 TSSOP	U16-2
MAX4521CGE	0°C to +70°C	16 QFN-EP**	G1644-1
MAX4521C/D	0°C to +70°C	Dice*	—

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

***EP = Exposed pad.*

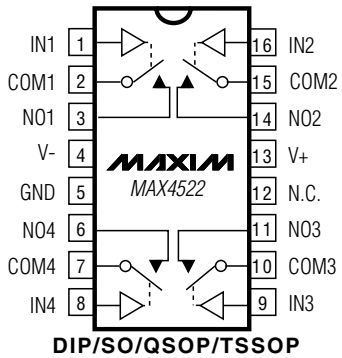
Pin Configurations/Functional Diagrams/Truth Tables



DIP/SO/QSOP/TSSOP

MAX4521	
LOGIC	SWITCH
0	ON
1	OFF

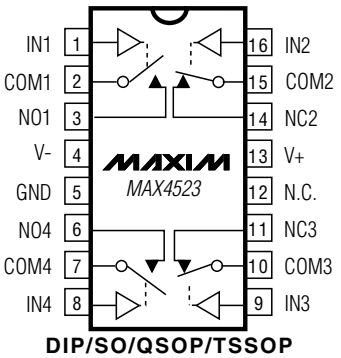
N.C. = NOT CONNECTED



DIP/SO/QSOP/TSSOP

MAX4522	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO/QSOP/TSSOP

MAX4523		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +13.0V
V- .....-13.0V to +0.3V
V+ to V- .....-0.3V to +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±10mA
Peak Current into Any Terminal
(pulsed at 1ms,10% duty cycle) .....±20mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 9.52mW/°C above +70°C) 762mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
TSSOP (derate 6.7mW/°C above +70°C) 457mW
QFN (derate 16.9mW/°C above +70°C) 1349mW
Operating Temperature Ranges
MAX452_C_E .....0°C to +70°C
MAX452_E_E .....-40°C to +85°C
MAX452_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.
Note 2: All leads are soldered or welded to PC boards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 4)	C, E, M	V-		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 5V, V- = -5V, $V_{COM\_}$ = ±3V, $I_{COM\_}$ = 1mA	+25°C		65	100	Ω
			C, E, M			125	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 5V, V- = -5V, $V_{COM\_}$ = ±3V, $I_{COM\_}$ = 1mA	+25°C		1	4	Ω
			C, E, M			6	
COM_ to NO_, COM_ to NC_ On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, $V_{COM\_}$ = ±3V, $I_{COM\_}$ = 1mA	+25°C		7	12	Ω
			C, E, M			15	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ∓4.5V, $V_{N\_}$ = ±4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ Off-Leakage Current (Note 7)	$I_{COM\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{N\_}$ = ∓ 4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	
			M	-200		200	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = ±3V, V+ = 4.5V, V- = -4.5V, Figure 1	+25°C		45	80	ns
			C, E, M			100	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = ±3V, V+ = 4.5V, V- = -4.5V, Figure 1	+25°C		15	30	ns
			C, E, M			40	
Break-Before-Make Time Delay (MAX4523 only)	t_{BBM}	$V_{COM\_}$ = ±3V, V+ = 5.5V, V- = -5.5V, Figure 2	+25°C	5	20		ns
Charge Injection (Note 4)	Q	C_L = 1nF, $V_{NO\_}$ = 0, R_S = 0Ω, Figure 3	+25°C		1	5	pC
NO_, NC_ Off-Capacitance	$C_{N\_(OFF)}$	$V_{NO\_}$ = GND, f = 1MHz, Figure 6	+25°C		2		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz, Figure 6	+25°C		2		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	$V_{COM\_}$ = $V_{NO\_}$ = GND, f = 1MHz, Figure 7	+25°C		5		pF
Off-Isolation (Note 8)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 100kHz, Figure 4	+25°C		< -90		dB
Channel-to-Channel Crosstalk (Note 9)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 100kHz, Figure 5	+25°C		< -90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	-6		6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN\_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = -5.5V	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 4)	C, E, M	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM\_}$ = 3.5V, $I_{COM\_}$ = 1mA	+25°C		125	200	Ω
			C, E, M			250	
COM_ to NO_, COM_ to NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 5V, $V_{COM\_}$ = 3.5V, $I_{COM\_}$ = 1mA	+25°C		2	8	Ω
			C, E, M			10	
NO_, NC_ Off-Leakage Current (Notes 7, 10)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{N\_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ Off-Leakage Current (Notes 7, 10)	$I_{COM\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{N\_}$ = 4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
			M	-100		100	
COM_ On-Leakage Current (Notes 7, 10)	$I_{COM\_(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V	+25°C	-2	0.01	2	nA
			C, E,	-20		20	
			M	-200		200	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 3V, V+ = 4.5V, Figure 1	+25°C		60	100	ns
			C, E, M			150	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 3V, V+ = 4.5V, Figure 1	+25°C		20	50	ns
			C, E, M			75	
Break-Before-Make Time Delay (MAX4523 only)	t_{BBM}	$V_{COM\_}$ = 3V, V+ = 5.5V, Figure 2	+25°C	10	30		ns
Charge Injection (Note 4)	Q	C_L = 1nF, $V_{NO\_}$ = 0, R_S = 0Ω, Figure 3	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN\_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = 0	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 4)	C, E, M	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM\_}$ = 1.0V, $I_{COM\_}$ = 0.1mA	+25°C		260	500	Ω
			C, E, M			600	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 4)							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		120	250	ns
			C, E, M			300	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		40	80	ns
			C, E, M			100	
Break-Before-Make Time Delay (MAX4523 only)	t_{BBM}	$V_{COM\_}$ = 1.5V, V+ = 3.6V, Figure 2	+25°C	15	50		ns
Charge Injection	Q	C_L = 1nF, $V_{NO\_}$ = 0, R_S = 0Ω, Figure 3	+25°C		0.5	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN\_}$ = 0 or V+	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	
V- Supply Current	I-	V- = 0	+25°C	-1	0.05	1	µA
			C, E, M	-1		1	

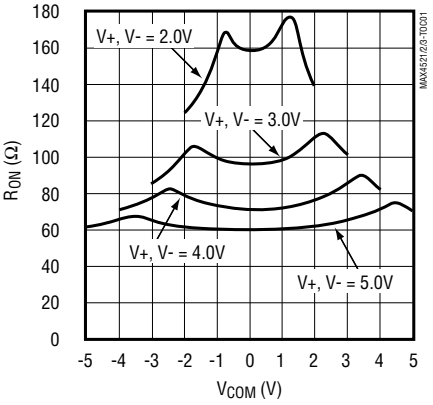
Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: Guaranteed by design.
Note 5: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 6: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 7: Leakage parameters are 100% tested at maximum rated temperature, and guaranteed by correlation at T_A = +25°C.
Note 8: Off-Isolation = $20\log_{10}$ [$V_{COM\_}$ / ($V_{NC\_}$ or $V_{NO\_}$)], $V_{COM\_}$ = output, $V_{NC\_}$ or $V_{NO\_}$ = input to off switch.
Note 9: Between any two switches.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad, Low-Voltage, SPST Analog Switches

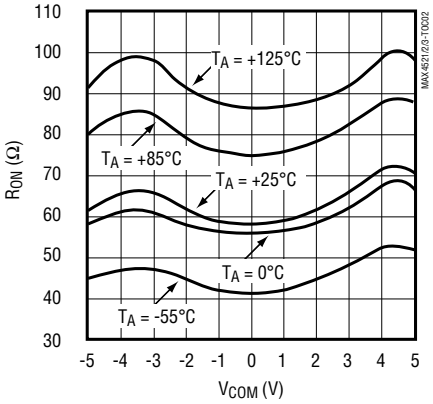
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0, T_A = +25°C, unless otherwise noted.)

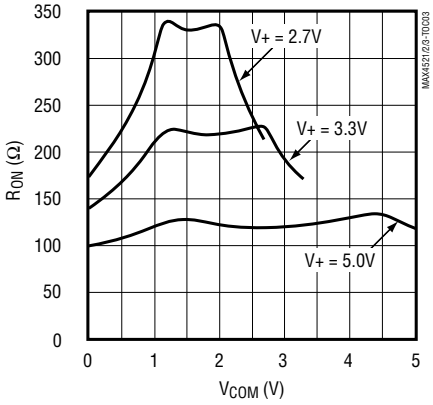
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



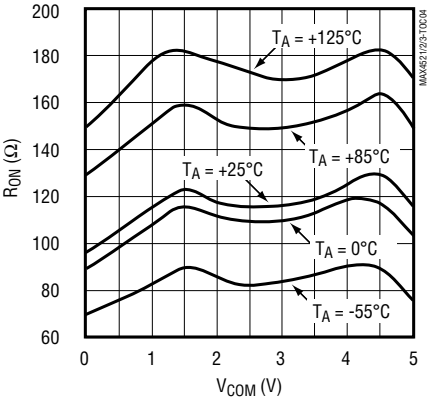
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



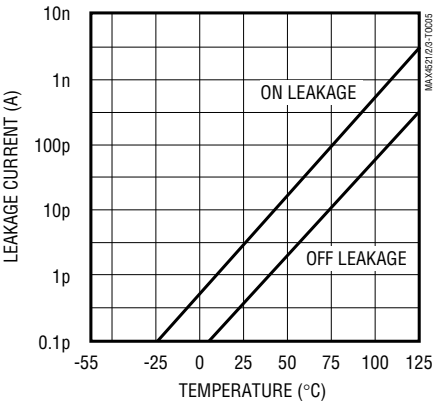
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



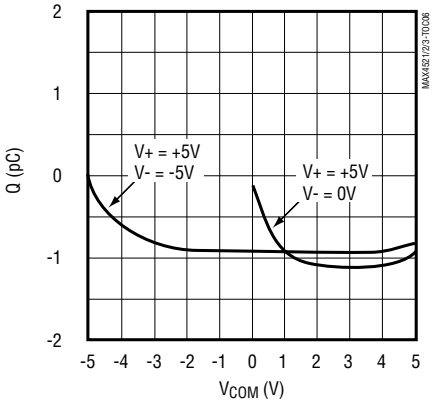
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



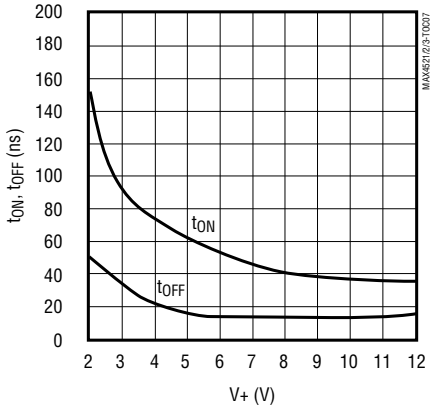
ON- AND OFF-LEAKAGE CURRENT vs. TEMPERATURE



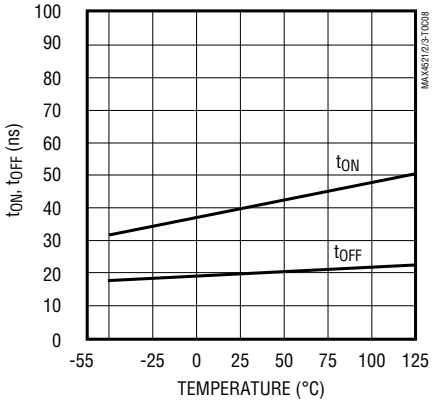
CHARGE INJECTION vs. V_{COM}



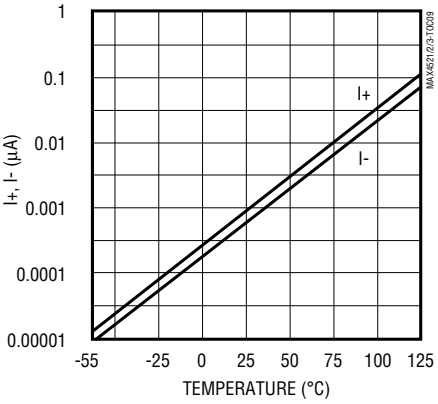
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



TURN-ON/OFF TIME vs. TEMPERATURE



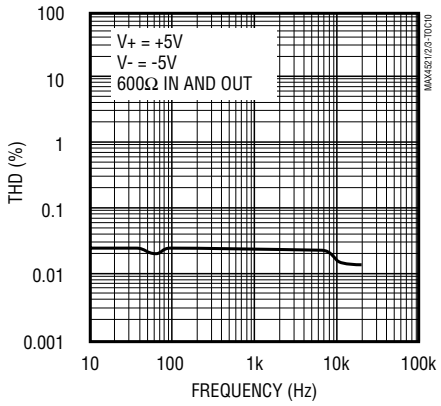
POWER-SUPPLY CURRENT vs. TEMPERATURE



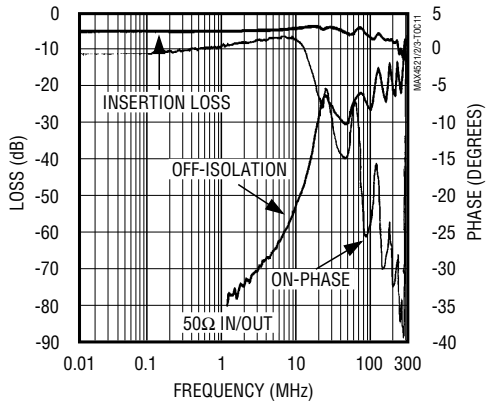
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION vs. FREQUENCY



FREQUENCY RESPONSE



Pin Description

PIN						NAME	FUNCTION
MAX4521		MAX4522		MAX4523			
TSSOP/SO	QFN	TSSOP/SO	QFN	TSSOP/SO	QFN		
1, 16, 9, 8	15, 14, 7, 6	1, 16, 9, 8	15, 14, 7, 6	1, 16, 9, 8	15, 14, 7, 6	IN1–1N4	Logic-Control Digital Input
2, 15, 10, 7	16, 13, 8, 5	2, 15, 10, 7	16, 13, 8, 5	2, 15, 10, 7	16, 13, 8, 5	COM1–COM4	Analog Switch Common* Terminals
3, 14, 11, 6	1, 12, 9, 4	—	—	—	—	NC1–NC4	Analog Switch Normally Closed Terminals
—	—	3, 14, 11, 6	1, 12, 9, 4	—	—	NO1–NO4	Analog Switch Normally Open Terminals
—	—	—	—	3, 6	1, 4	NO1, NO4	Analog Switch Normally Open Terminals
—	—	—	—	14, 11	12, 9	NC2, NC3	Analog Switch Normally Closed Terminals
4	2	4	2	4	2	V-	Negative Analog Supply-Voltage Input. Connect to GND for single supply operation.
5	3	5	3	5	3	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
12	10	12	10	12	10	N.C.	No Connection. Not internally connected.
13	11	13	11	13	11	V+	Positive Analog and Digital Supply-Voltage Input. Internally connected to substrate.
—	EP	—	EP	—	EP	EP	Exposed Pad. Connect EP to V+.

**NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.*

Applications Information

Power-Supply Considerations

Overview

The MAX4521/MAX4522/MAX4523 construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches, and they set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes conducts. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled, and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level thresholds are CMOS/TTL compatible when V+ = +5V. The threshold increases slightly as V+ is raised, and when V+ reaches +12V, the level threshold is about 3.1V. This is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4521/MAX4522/MAX4523 operate with bipolar supplies between ±2V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4521/MAX4522/MAX4523 V+ to +3V, and then connect the logic-level-input pins to TTL logic-level signals. TTL logic-level outputs in excess of the absolute maximum ratings can damage the part and/or external circuits.**

Caution: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or 12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4521/MAX4522/MAX4523. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single Supply

The MAX4521/MAX4522/MAX4523 operate from a single supply between +2V and +12V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -52dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

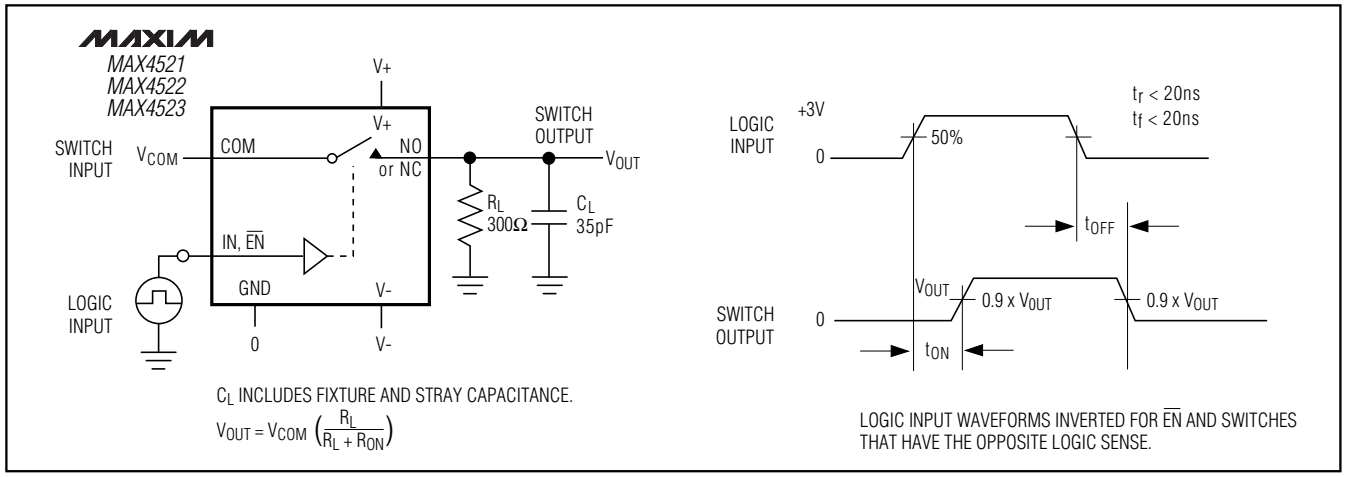


Figure 1. Switching Time

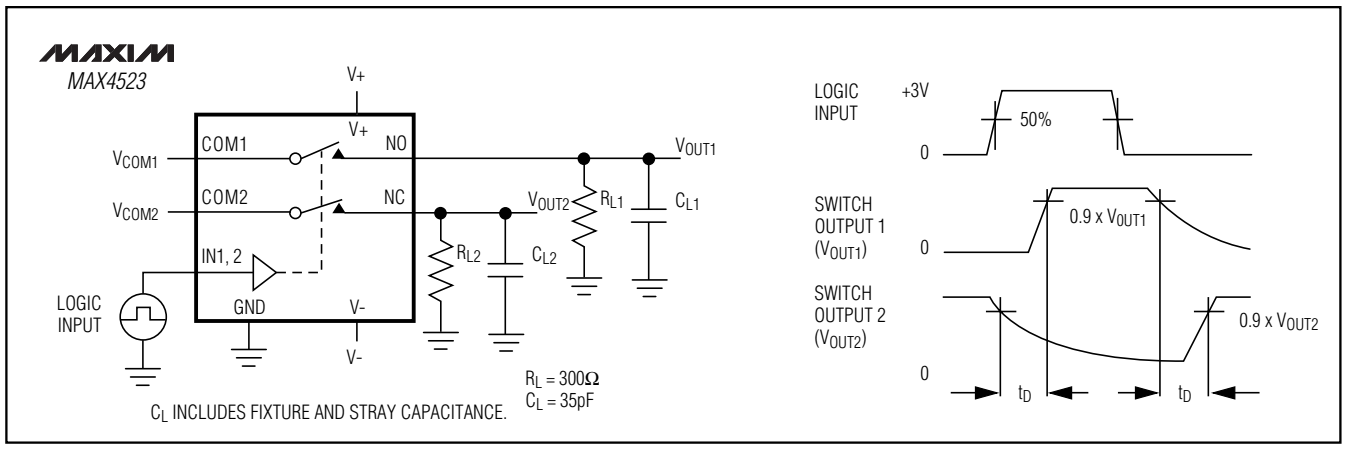


Figure 2. Break-Before-Make Interval (MAX4523 only)

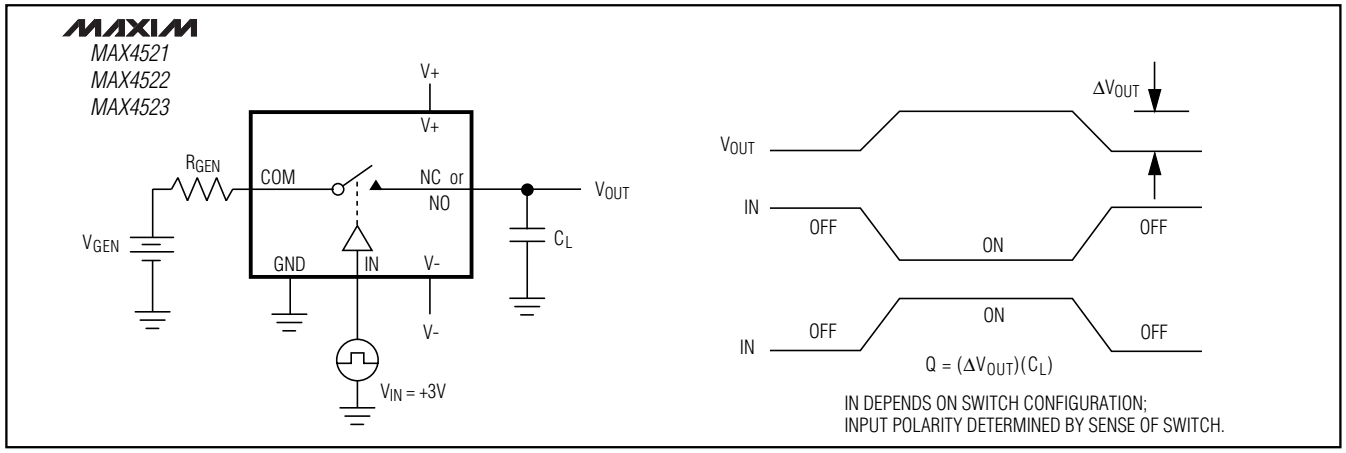


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

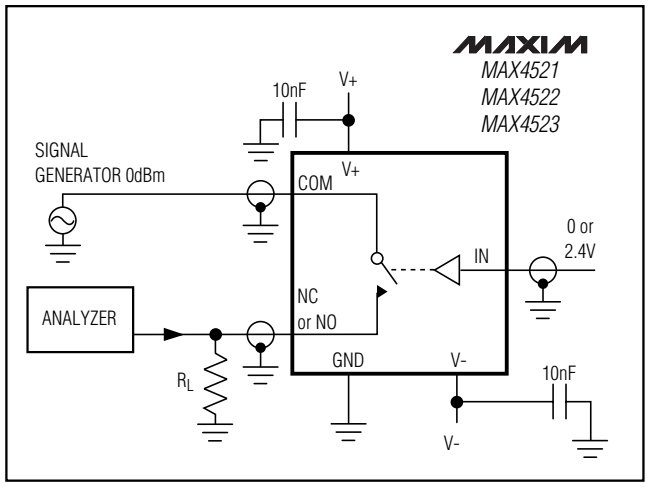


Figure 4. Off-Isolation

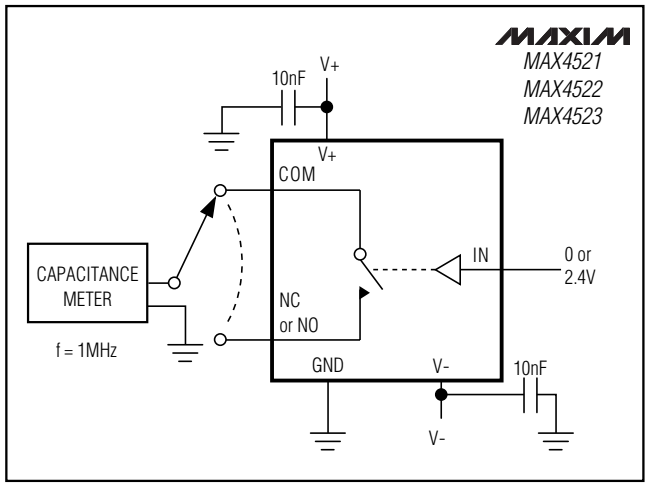


Figure 6. Channel Off-Capacitance

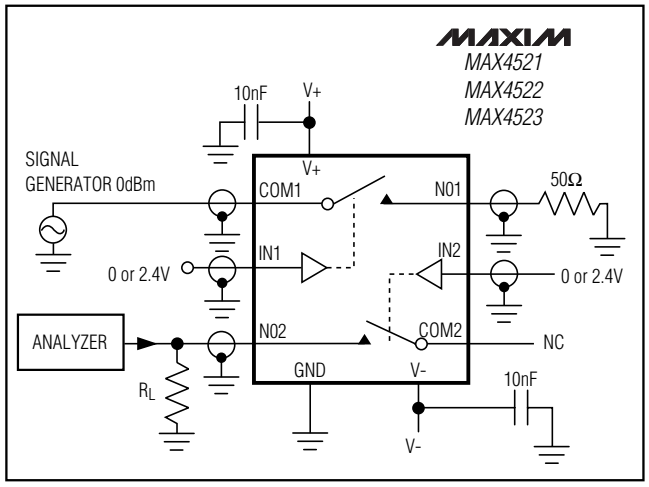


Figure 5. Crosstalk

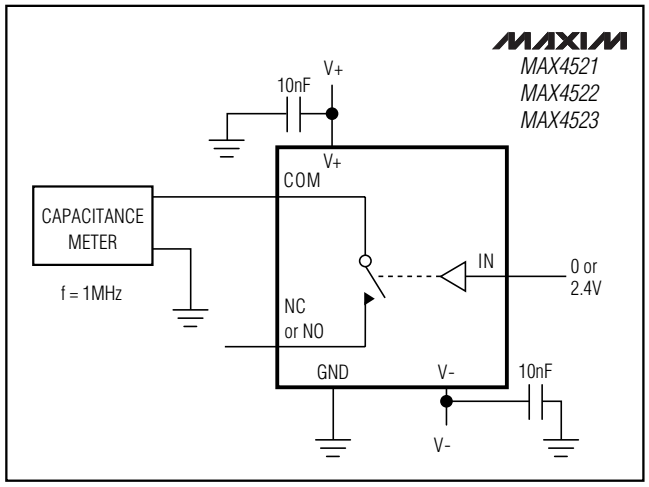


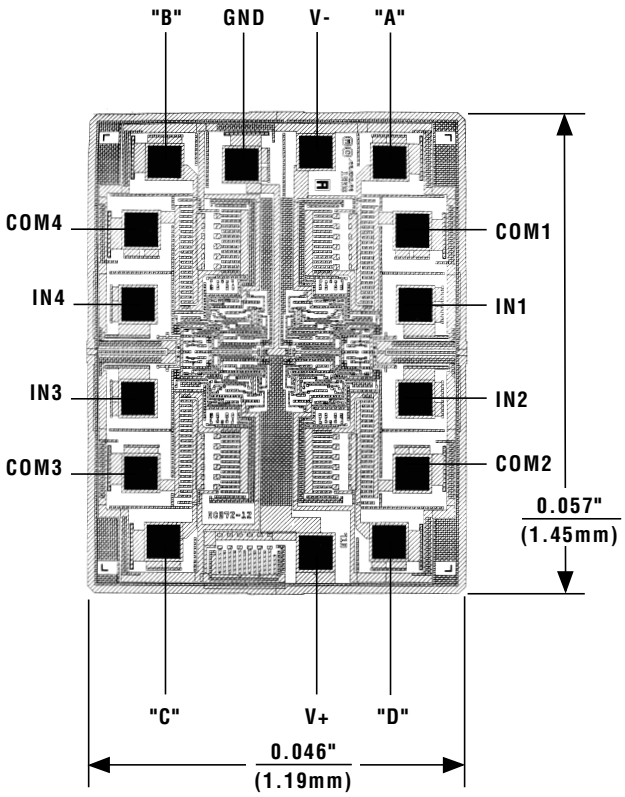
Figure 7. Channel On-Capacitance

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4521EPE	-40°C to +85°C	16 Plastic DIP	P16-1
MAX4521ESE	-40°C to +85°C	16 Narrow SO	S16-2
MAX4521EEE	-40°C to +85°C	16 QSOP	E16-4
MAX4521EUE	-40°C to +85°C	16 TSSOP	U16-2
MAX4521EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4521MJE	-55°C to +125°C	16 CERDIP***	J16-3
MAX4522CPE	0°C to +70°C	16 Plastic DIP	P16-1
MAX4522CSE	0°C to +70°C	16 Narrow SO	S16-2
MAX4522CEE	0°C to +70°C	16 QSOP	E16-4
MAX4522CUE	0°C to +70°C	16 TSSOP	U16-2
MAX4522CGE	0°C to +70°C	16 QFN-EP**	G1644-1
MAX4522C/D	0°C to +70°C	Dice*	—
MAX4522EPE	-40°C to +85°C	16 Plastic DIP	P16-1
MAX4522ESE	-40°C to +85°C	16 Narrow SO	S16-2
MAX4522EEE	-40°C to +85°C	16 QSOP	E16-4
MAX4522EUE	-40°C to +85°C	16 TSSOP	U16-2
MAX4522EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4522MJE	-55°C to +125°C	16 CERDIP***	J16-3
MAX4523CPE	0°C to +70°C	16 Plastic DIP	P16-1
MAX4523CSE	0°C to +70°C	16 Narrow SO	S16-2
MAX4523CEE	0°C to +70°C	16 QSOP	E16-4
MAX4523CUE	0°C to +70°C	16 TSSOP	U16-2
MAX4523CGE	0°C to +70°C	16 QFN-EP**	G1644-1
MAX4523C/D	0°C to +70°C	Dice*	—
MAX4523EPE	-40°C to +85°C	16 Plastic DIP	P16-1
MAX4523ESE	-40°C to +85°C	16 Narrow SO	S16-2
MAX4523EEE	-40°C to +85°C	16 QSOP	E16-4
MAX4523EUE	-40°C to +85°C	16 TSSOP	U16-2
MAX4523EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4523MJE	-55°C to +125°C	16 CERDIP***	J16-3

**Contact factory for dice specifications.*
***EP = Exposed pad.*
****Contact factory for availability.*

Chip Topography

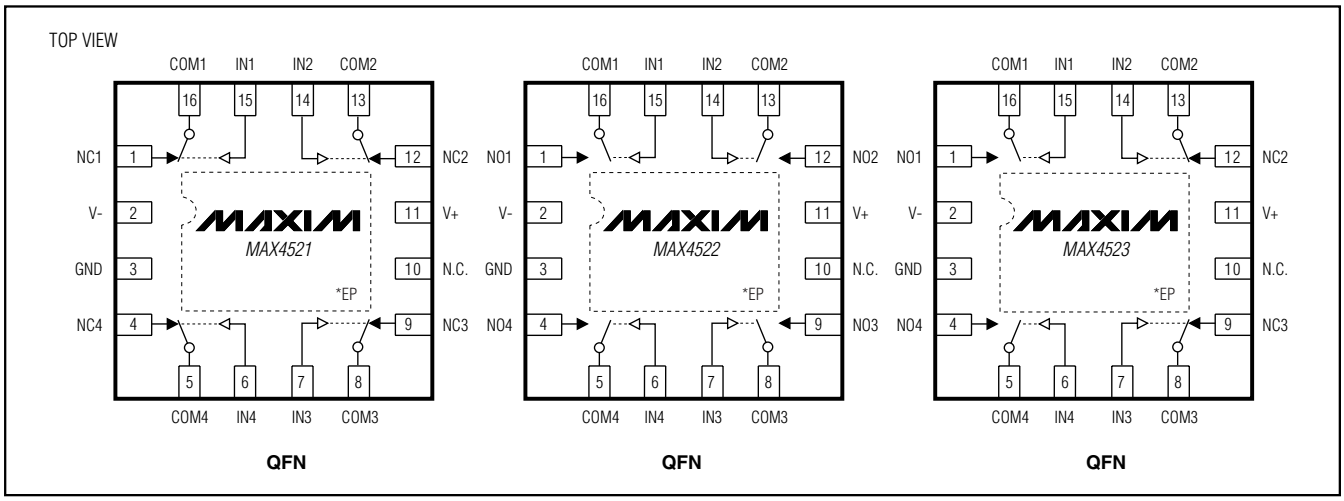


MAX4521		MAX4522		MAX4523	
PIN	NAME	PIN	NAME	PIN	NAME
A	NC1	A	NO1	A	NO1
B	NC4	B	NO4	B	NO4
C	NC3	C	NO3	C	NC3
D	NC2	D	NO2	D	NC2

SUBSTRATE CONNECTED TO V+

Quad, Low-Voltage, SPST Analog Switches

Pin Configurations

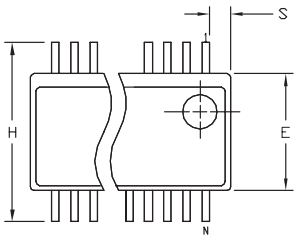


*EP = Exposed Pad, connect EP to V+

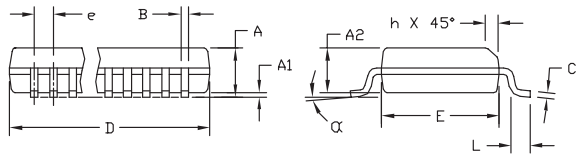
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



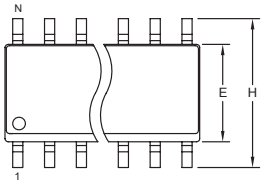
VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV. F | 1/1

SOICN .EPS

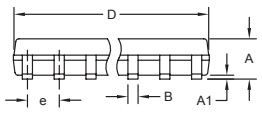


TOP VIEW

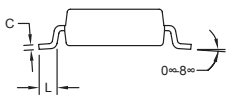
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

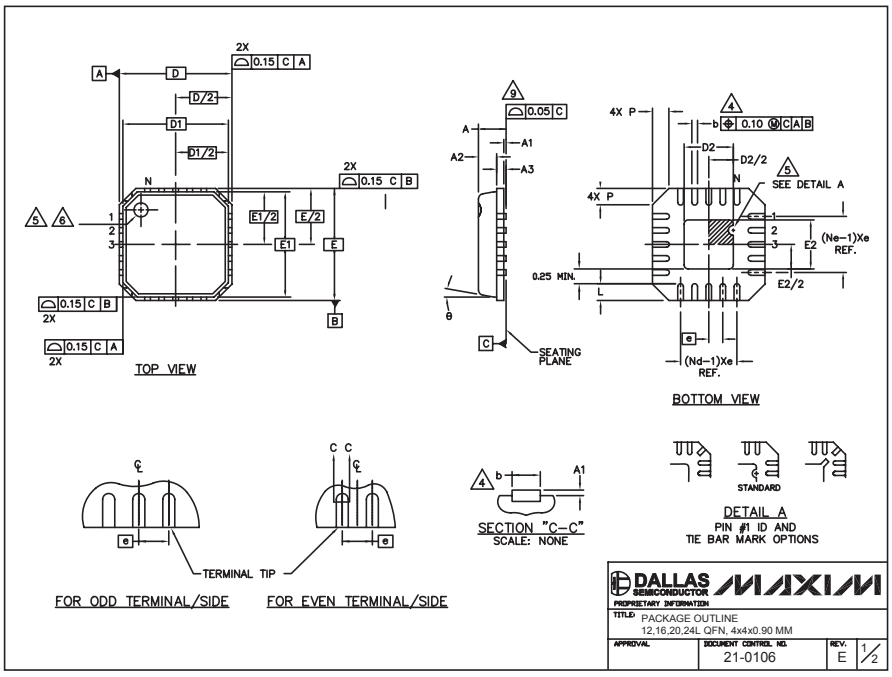
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, .150" SOIC
APPROVAL | DOCUMENT CONTROL NO. 21-0041 | REV. B | 1/1

Quad, Low-Voltage, SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A			NOTE	PITCH VARIATION B			NOTE	PITCH VARIATION C			NOTE	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
e		0.80 BSC				0.65 BSC				0.50 BSC				0.50 BSC		
N		12		3		16		3		20		3		24		3
Nd		3		3		4		3		5		3		6		3
Ne		3		3		4		3		5		3		6		3
L	0.50	0.60	0.75		0.50	0.60	0.75		0.50	0.60	0.75		0.30	0.40	0.50	
b	0.28	0.33	0.40	4	0.23	0.28	0.35	4	0.18	0.23	0.30	4	0.18	0.23	0.30	4

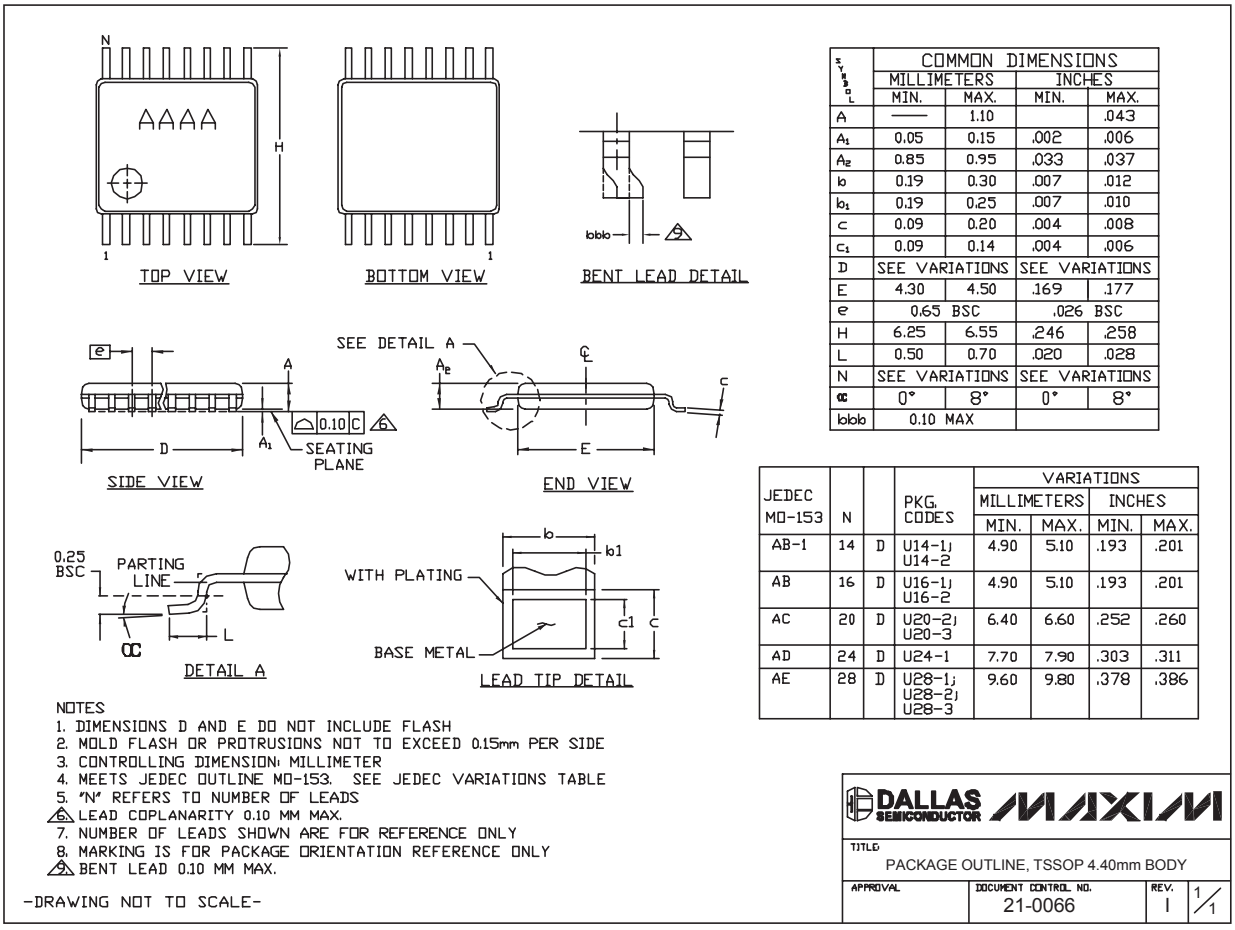
PKG. CODE	EXPOSED PAD VARIATION D2 MIN.	D2 NOM.	D2 MAX.	E2 MIN.	E2 NOM.	E2 MAX.
G1244-2	1.95	2.10	2.25	1.95	2.10	2.25
G1644-1	1.95	2.10	2.25	1.95	2.10	2.25
G2044-3	1.95	2.10	2.25	1.95	2.10	2.25
G2044-4	1.55	1.70	1.85	1.55	1.70	1.85
G2444-1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN, 4x4x0.90 MM
APPROVAL
DOCUMENT CONTROL NO. 21-0106
REV. E
2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
loblo	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

Revision History

Pages changed at Rev 6: 1, 7, 11, 12, 15

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.