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19-0258; Rev 3; 8/99

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

8x4 Video Crosspoint Switches with Buffers

General Description

The MAX458/MAX459 are crosspoint switches with eight input channels and four high-speed, buffered output channels. The MAX458 output buffer is configured with a gain of one, while the MAX459 buffer has a gain of two. In each device, any one of eight input lines can be connected to any of four output amplifiers. The output buffers are capable of driving loads of 75Ω.

Data interface can be accomplished by either a 16-bit serial or a 6-bit parallel connection. In the serial mode, the MAX458/MAX459 are SPI™, QSPI™, and Microwire™ compatible. In parallel mode, the MAX458/MAX459 are compatible with most microprocessor buses. Three-state amplifier output capability makes it possible to multiplex MAX458/MAX459s to form larger switch networks. The output buffers can be disabled individually or the entire device can be shut down to conserve power.

Applications

Video Test Equipment
Video Security Systems
Video Editing

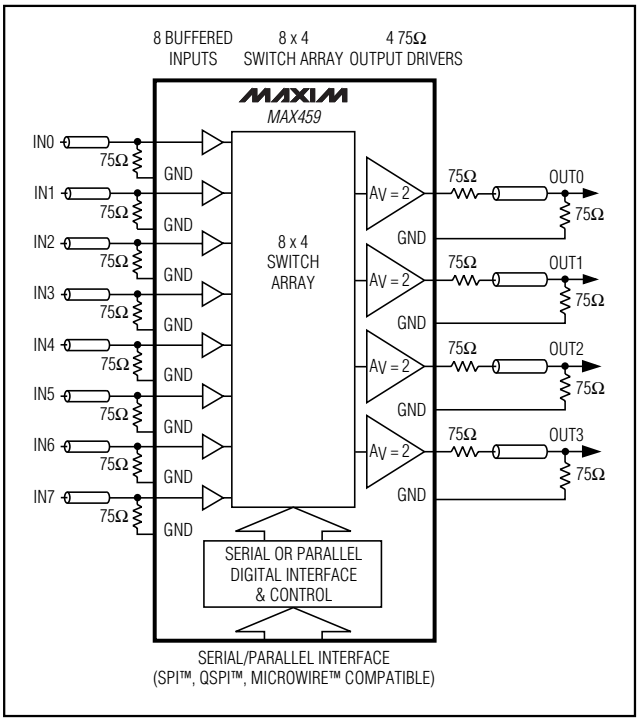
Features

- **100MHz Unity-Gain Bandwidth**
- **300V/µs Slew Rate**
- **Low 0.05° Differential Phase Error**
- **Low 0.01% Differential Gain Error**
- **Directly Drives 75Ω Cables**
- **Fast 60ns Switching Time**
- **High-Z Amplifier Output Capability**
- **Shutdown Capability**
- **16-Bit Serial and 6-Bit Parallel Address Modes**
- **40-Pin DIP and 44-Pin PLCC Packages**

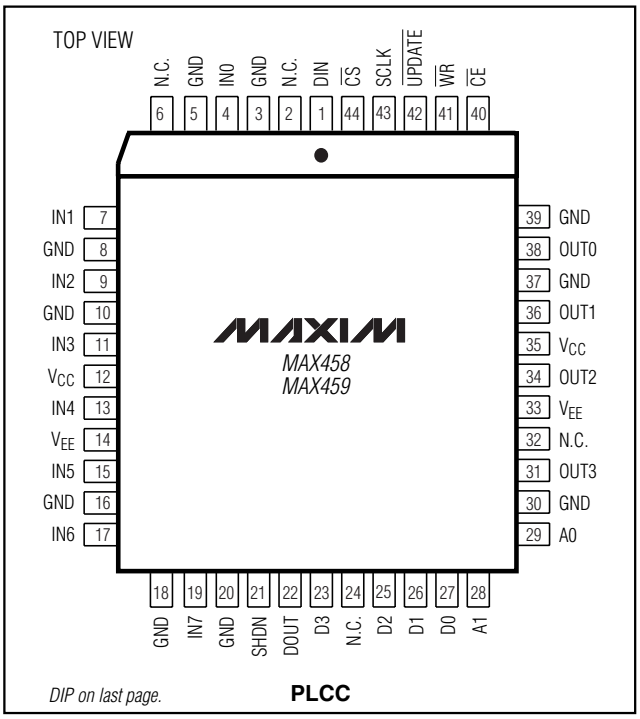
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX458CPL	0°C to +70°C	40 Plastic DIP
MAX458CQH	0°C to +70°C	44 PLCC
MAX458EPL	-40°C to +85°C	40 Plastic DIP
MAX459CPL	0°C to +70°C	40 Plastic DIP
MAX459CQH	0°C to +70°C	44 PLCC
MAX459EPL	-40°C to +85°C	40 Plastic DIP

Block Diagram



Pin Configurations



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PLCC

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8x4 Video Crosspoint Switches with Buffers

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{CC} to V_{EE}) 12V
Positive Supply Voltage (V_{CC} to GND).....6V
Negative Supply Voltage (V_{EE} to GND) 6V
Analog Input/Output Voltage .....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Digital Input Voltage.....(V_{CC} + 0.3V) to -0.3V
Duration of Output Short Circuit to GND (Note 1).....Continuous
Continuous Power Dissipation
  Plastic DIP (derate 17mW/°C above +70°C) 1333mW
  PLCC (derate 13mW/°C above +70°C) 1067mW
Operating Temperature Ranges
  MAX45_C_ _ .....0°C to +70°C
  MAX45_E_ _.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Outputs may be shorted to any supply pin or ground as long as package power dissipation ratings are not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS							
Input Voltage Range				-2		+2	V
Input Offset Voltage	V_{OS}	Any channel	T_A = +25°C		5	15	mV
			T_A = T_{MIN} to T_{MAX}			20	
Input Offset Voltage Match	ΔV_{OS}	V_{IN} = 0V (Note 2)			3	10	mV
Power-Supply Rejection Ratio	PSRR	V_S = ±4.75V to ±5.25V		50	60		dB
On Input Bias Current	I_{IN}	V_{IN} = 0V, input programmed to one output			±1	±5	µA
On Input Resistance	R_{IN}	Input programmed to one output		0.50	5.0		MΩ
Input Capacitance	C_{IN}	Input channel on or off			7		pF
DC Voltage Gain Accuracy		MAX458 (Note 3)	T_A = +25°C		0.1	0.5	%
			T_A = T_{MIN} to T_{MAX}			1.0	
		MAX459 (Note 4)	T_A = +25°C		0.1	1.0	
			T_A = T_{MIN} to T_{MAX}			2.0	
Output Voltage Swing	V_{OUT}			±2	±3		V
Enabled Output Resistance	R_{OUT}	V_{IN} = 1kHz sine wave			0.05		Ω
		V_{IN} = 10MHz sine wave			4.0		
Disabled Output Resistance	R_{OUT}	MAX458		0.25	1.0		MΩ
		MAX459		0.70	1.0		kΩ
Disabled Output Capacitance	C_{OUT}				12		pF
Positive Power-Supply Current	I_{CC}	V_{IN} = 0V, all amplifiers enabled	T_A = +25°C	60	75	85	mA
			T_A = T_{MIN} to T_{MAX}	50		100	
Negative Power-Supply Current	I_{EE}	V_{IN} = 0V, all amplifiers enabled	T_A = +25°C	50	65	75	mA
			T_A = T_{MIN} to T_{MAX}	40		90	
Positive Supply Current in Shutdown					15	26	mA
Negative Supply Current in Shutdown					7	12	mA
Logic Input High Voltage	V_{IH}	(Note 5)				2.0	V
Logic Input Low Voltage	V_{IL}	(Note 5)		0.8			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input High Current	I_{IH}	(Note 3)				10	µA
Logic Input Low Current	I_{IL}	(Note 3)				10	µA
Logic Output High Voltage	V_{OH}	I_{SOURCE} = 400µA (Note 5)		4.0			V
Logic Output Low Voltage	V_{OL}	I_{SINK} = 700µA (Note 5)				0.5	V
DYNAMIC SPECIFICATIONS							
Differential Gain Error (Note 6)	DG	MAX458			0.01		%
		MAX459			0.13		
Differential Phase Error (Note 6)	DG	MAX458			0.05		degrees
		MAX459			0.14		
Slew Rate	SR	MAX458	Positive transition		200		V/µs
			Negative transition		150		
		MAX459	Positive transition		300		
			Negative transition		250		
Bandwidth (-3dB)	BW	MAX458, R_L = 75Ω			100		MHz
		MAX459, R_L = 150Ω			90		
Input Noise Density	e_n	f = 10kHz			20		nV/√Hz
Settling Time	t_S	To 0.1% of final value (Note 7)			40		ns
Amplifier Disable Time	t_{AOFF}				100		ns
Amplifier Enable Time	t_{AON}				120		ns
Channel Switching Time	t_{CSW}				60		ns
Channel Switching Propagation Delay	t_{CPD}				50		ns
Switching Transient Glitch		See *Typical Operating Characteristics*			100		mV_{p-p}
Adjacent Channel Crosstalk		(Note 8)			-65		dB
Non-Adjacent Channel Crosstalk		(Note 9)			-65		dB
All-Hostile Crosstalk		(Note 10)			-55		dB
All-Hostile Off Isolation		(Note 11)			-60		dB

Note 2: Defined as the DC offset shift when switching between input channels for a given output.

Note 3: Voltage Gain Accuracy for MAX458 calculated as $\frac{(V_{OUT} - V_{IN})\ @\ (V_{IN} = +2V) - (V_{OUT} - V_{IN})\ @\ (V_{IN} = -2V)}{4V}$

Note 4: Voltage Gain Accuracy for MAX459 calculated as $\frac{(V_{OUT}/2 - V_{IN})\ @\ (V_{IN} = +1V) - (V_{OUT}/2 - V_{IN})\ @\ (V_{IN} = -1V)}{2V}$

Note 5: All logic levels are guaranteed over the range of V_S = ±4.75V to ±5.25V.

Note 6: Differential phase and gain measured with a 40 IRE (285.7mV), 3.58MHz sine wave superimposed on a linear ramp of 0 IRE to 100 IRE (714.3mV). "The IRE scale is a linear scale for measuring, in arbitrary IRE units, the relative amplitudes of the various components of a television signal" (from the "Television Engineering Handbook", edited by K. Blair Benson, McGraw Hill). This system defines 100 IRE as reference white, 0 IRE as the blanking level, and -40 IRE as the sync peak. The equipment used for the test signal generated 714.3mV (100 IRE) as reference white and -285.7mV (-40 IRE) as sync. The modulation used was 285.7mV (40 IRE), which conforms to the EIA color signal standards.

Note 7: For MAX458, step input from +2V to 0V; for MAX459, step input from +1V to 0V. All unused channels grounded and all unused amplifiers disabled.

Note 8: Test input channel programmed to an output and grounded through a 75Ω resistor. Adjacent input is programmed to an adjacent output and driven by a 10MHz, 4Vp-p sine wave.

Note 9: Same as Note 6 above, except driven input and output are not adjacent to test input/output.

Note 10: All inputs but the test input are driven by a 10MHz 4Vp-p sine wave. All outputs except the test output are connected to driven inputs.

Note 11: Same as Note 9 above, except with test channel programmed off.

TIMING CHARACTERISTICS (Note 12)

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

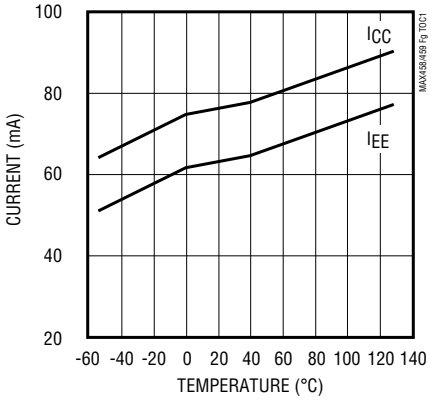
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
PARALLEL-MODE TIMING (see Figure 1)					
Address to $\overline{WR}$ Fall Setup Time	t_{ADS}		20		ns
Address to $\overline{WR}$ Rise Hold Time	t_{ADH}		0		ns
$\overline{CE}$ Fall to $\overline{WR}$ Fall Setup Time	t_{CES}		0		ns
$\overline{CE}$ Rise to $\overline{WR}$ Rise Hold Time	t_{CEH}		0		ns
$\overline{WR}$ Pulse Width Low	t_{WR}		40		ns
Data to $\overline{WR}$ Rise Setup Time	t_{DS}		50		ns
Data to $\overline{WR}$ Rise Hold Time	t_{DH}		0		ns
$\overline{WR}$ Rise to $\overline{UPDATE}$ Fall Setup Time	t_{WRS}		0		ns
$\overline{UPDATE}$ Pulse Width Low	t_{UP}		40		ns
$\overline{UPDATE}$ Rise to $\overline{WR}$ Fall Setup Time	t_{UPS}		25		ns
SERIAL-MODE TIMING (see Figure 6)					
SCLK to $\overline{CS}$ Fall	t_{CSO}		0		ns
$\overline{CS}$ Fall to SCLK Rise	t_{CSS}		35		ns
SCLK Pulse Width High	t_{CH}		50		ns
SCLK Pulse Width Low	t_{CL}		30		ns
DIN to SCLK Rise Setup Time	t_{DS}		50		ns
DIN to SCLK Rise Hold Time	t_{DH}		0		ns
SCLK Fall to DOUT	t_{DO}			200	ns
SCLK Rise to $\overline{CS}$ Rise	t_{CSH}		30		ns
$\overline{CS}$ Rise to SCLK Rise	t_{CS1}		20		ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100		ns

Note 12: Timing Characteristics are guaranteed by design.

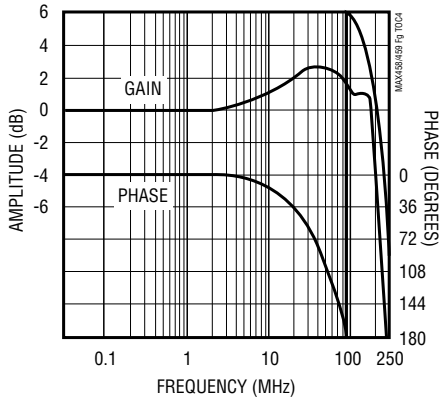
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

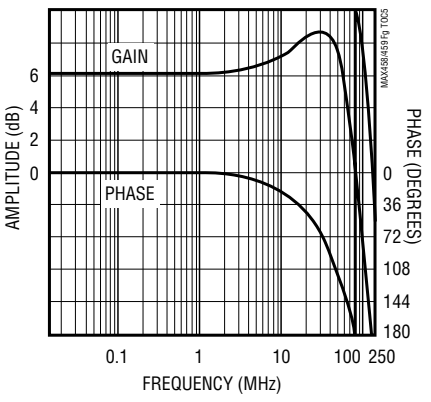
POWER SUPPLY CURRENT vs. TEMPERATURE



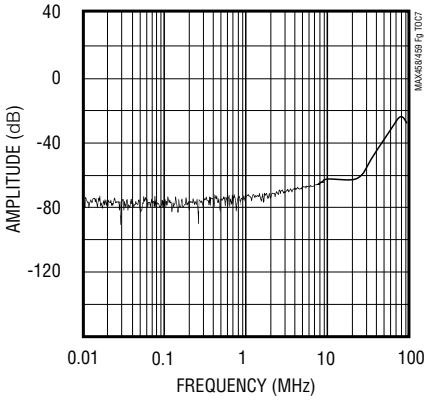
MAX458 GAIN vs. FREQUENCY



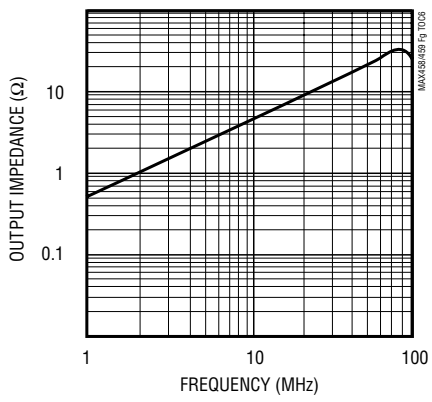
MAX459 GAIN vs. FREQUENCY



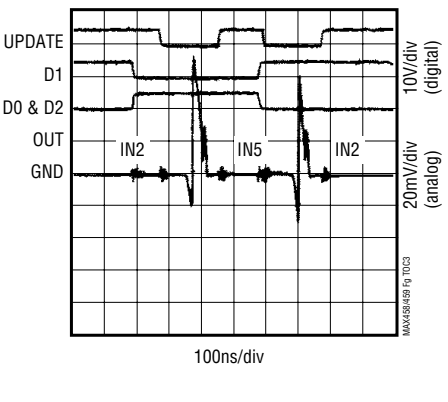
CROSSTALK vs. FREQUENCY



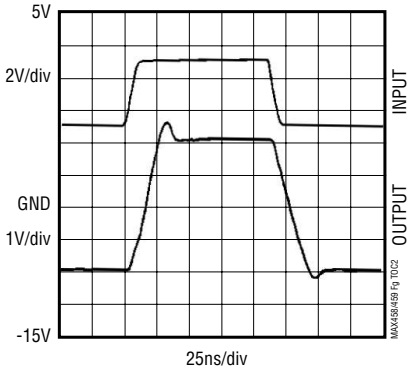
OUTPUT IMPEDANCE vs. FREQUENCY



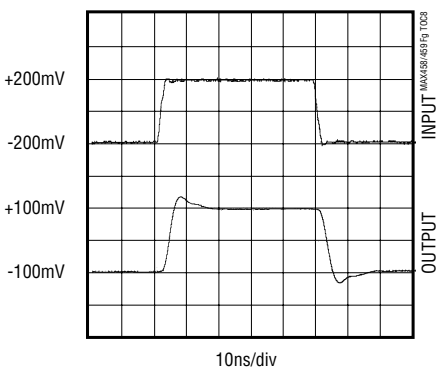
CHANNEL SWITCH TRANSIENT



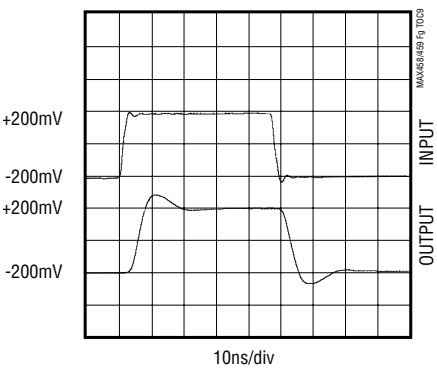
MAX458 LARGE-SIGNAL PULSE RESPONSE



MAX458 SMALL-SIGNAL PULSE RESPONSE



MAX459 SMALL-SIGNAL PULSE RESPONSE



8x4 Video Crosspoint Switches with Buffers

Pin Description

PIN		NAME	FUNCTION
DIP	PLCC		
1	1	DIN	Serial Data Input
2, 4, 6, 8, 14, 16, 18, 27, 33, 35	3, 5, 8, 10, 16, 18, 20, 30, 37, 39	GND	Ground
3	4	IN0	Analog Input Channel 0
5	7	IN1	Analog Input Channel 1
7	9	IN2	Analog Input Channel 2
9	11	IN3	Analog Input Channel 3
10, 31	12, 35	V_{CC}	Positive Power Supply (+5V). Connect both V_{CC} pins to the positive supply.
11	13	IN4	Analog Input Channel 4
12, 29	14, 33	V_{EE}	Negative Power Supply (-5V). Connect both V_{EE} pins to the negative supply.
13	15	IN5	Analog Input Channel 5
15	17	IN6	Analog Input Channel 6
17	19	IN7	Analog Input Channel 7
19	21	SHDN	Shutdown, active high. Connect to GND if not used.
20	22	DOUT	Serial Data Output used for daisy-chaining devices.
21	23	D3	Parallel Digital Channel Input Address Bit 3
22	25	D2	Parallel Digital Channel Input Address Bit 2
23	26	D1	Parallel Digital Channel Input Address Bit 1
24	27	D0	Parallel Digital Channel Input Address Bit 0
25	28	A1	Parallel Digital Amplifier Output Address Bit 1
26	29	A0	Parallel Digital Amplifier Output Address Bit 0
28	31	OUT3	Amplifier 3 Analog Output
30	34	OUT2	Amplifier 2 Analog Output
32	36	OUT1	Amplifier 1 Analog Output
34	38	OUT0	Amplifier 0 Analog Output
36	40	$\overline{CE}$	Chip Enable, used in parallel mode. Keep high for serial operation.
37	41	$\overline{WR}$	Write Low, latches input registers in parallel mode. Hold high for serial operation.
38	42	$\overline{UPDATE}$	Update Low, latches amplifier registers in parallel mode. Hold high for serial operation.
39	43	SCLK	Serial Clock
40	44	$\overline{CS}$	Chip Select, used in serial operation. Hold high for parallel mode of operation.
—	2, 6, 24, 32	N.C.	Not Internally Connected

Note: All GND pins must be grounded for optimum crosstalk performance.

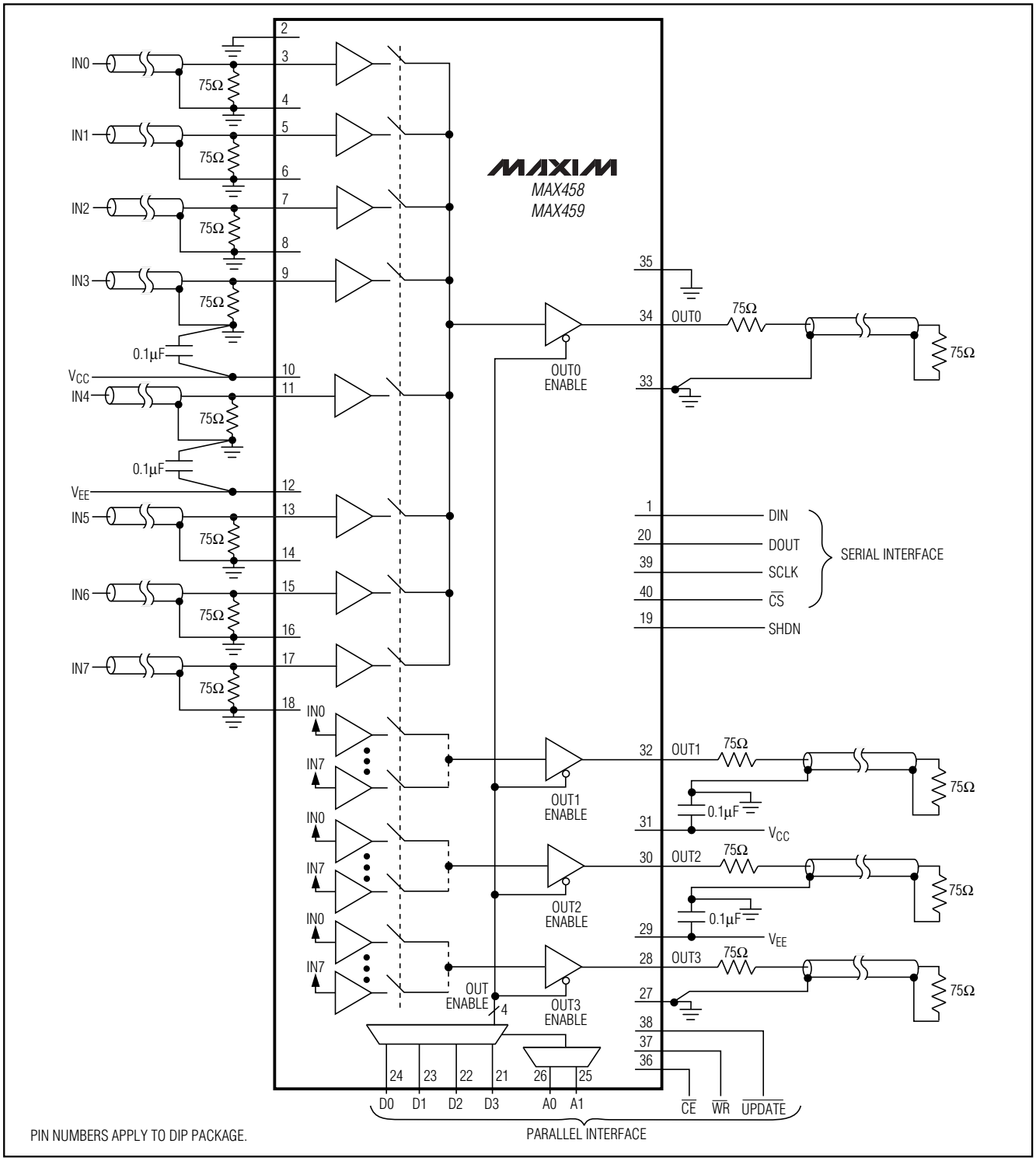


Figure 1. Block Diagram and Typical Operating Circuit

8x4 Video Crosspoint Switches with Buffers

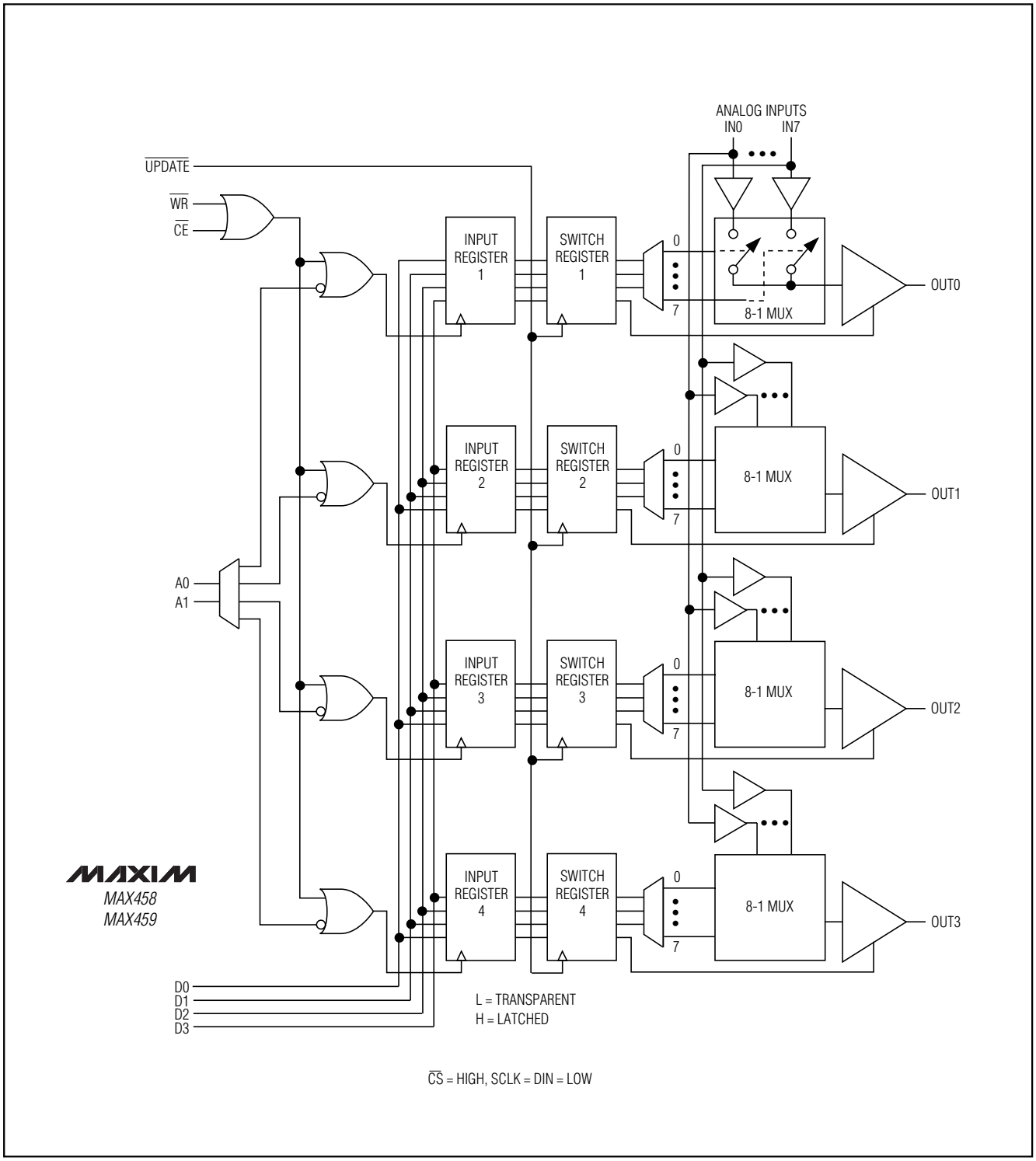


Figure 2. Parallel-Logic Block Diagram

Detailed Description

Analog Section

The MAX458/MAX459 video crosspoint switches consist of a high-speed 32 (8x4) switch array with wide-bandwidth line drivers (Figure 1). This design allows make-before-break switching to reduce output noise and glitches, but the inputs will not short together. It also provides high input impedance and low input capacitance, so no input buffer amplifier is needed. However, because different transistors provide gain depending on the input selection, the DC offset voltage shifts slightly when a new input is switched in. The change in offset voltage is typically 3mV.

All output buffers will drive back-terminated 50Ω, 75Ω, or higher impedance lines with up to 100pF capacitance. The amplifier outputs can be disabled, which is useful for creating large arrays. When disabled, the MAX458 presents an output impedance of approximately 1MΩ. The MAX459 disabled output impedance is 1kΩ (to ground), due to the internal feedback resistors used to achieve the gain of two.

During power-on, if $\overline{CS}$ and $\overline{UPDATE}$ are held high, all output amplifiers are disabled. In a large array, this feature prevents two ON paralleled amplifiers from distorting each other's signals. The amplifiers can be programmed to come up in any state simultaneously at any time after power-on. See the *Creating Large Arrays* section.

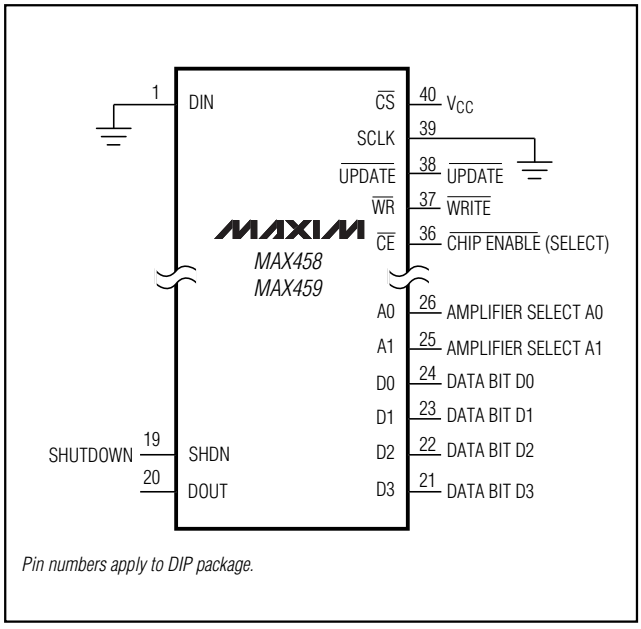


Figure 3. Parallel Connection (only logic pins shown)

Digital Section—Parallel Mode

The MAX458/MAX459 have two register banks—an input register and a switch register (Figure 2). Each of these registers is either latched (when the control input is high) or transparent (when the control input is low). The input register is controlled by $\overline{WR}$ and $\overline{CE}$ and is selected by the decode of A0 and A1. If both $\overline{WR}$ and $\overline{CE}$ are low, the input register selected by A0 and A1 is transparent, and the state of D0–D3 is presented to the switch register. The other three input registers remain latched. If D0–D3 change before $\overline{UPDATE}$ is asserted (goes low), the new data (the changed D0–D3) will then be latched in the switch register. If $\overline{WR}$ or $\overline{CE}$ is high, all input registers are latched and their data is presented

Table 1. Amplifier Selection

A1	A0	Output Amplifier Selected
L	L	0
L	H	1
H	L	2
H	H	3

Table 2. Input Selection

D3	D2	D1	D0	Input Channel Selected
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	Disable output amplifier selected by A0, A1.

Table 3. Writing Data

$\overline{CE}$	$\overline{WR}$	$\overline{UPDATE}$	FUNCTION
H X	X H	H H	Device not selected or is operating in serial mode. Both registers are latched.
H X	X H	L L	Data in input registers passes through switch registers. Output reflects data in input registers.
L	L	H	Input register of selected amplifier is transparent. Switch registers are latched. Other input registers are latched.
L	L	L	All switch registers and selected input register are transparent. Selected amplifier (chosen by state of A0, A1) reflects input data. Other amplifiers reflect data that had been latched into the input registers previously.

8x4 Video Crosspoint Switches with Buffers

to their switch registers. As long as either $\overline{WR}$ or $\overline{CE}$ is high, the input register will not change. The switch register will pass any new data on the falling transition of $\overline{UPDATE}$.

Each register of the switch-register bank controls the inputs to one amplifier. With $\overline{UPDATE}$ low, the switch registers are transparent and switch connection is controlled by the input register. However, if $\overline{UPDATE}$ is high, the switch register is latched and any change in data by the input register will not affect the amplifier output state. Two register banks are used so that data can be loaded into input registers without affecting the switch/amplifier selection. This allows amplifiers to be programmed and then changed simultaneously. When the registers are not latched, they are made transparent.

Use data bit D3 to disable the amplifier selected by A0–A1 and place its output in high-impedance mode. As an example, the code to disable OUT0 is as follows:

Pin Name:	D3	D2	D1	D0	A1	A0
Input Code:	1	X	X	X	0	0

When operating in parallel mode, $\overline{CS}$ must be wired high and SCLK and DIN should be grounded, as shown in Figure 3. Refer to Figure 4 for the correct timing relationships.

Digital Section—Serial Mode

The MAX458/MAX459 use a three-wire serial interface that is compatible with SPI, QPSI and Microwire interfaces. Serial mode, shown in Figure 5, is enabled when $\overline{WR}$, $\overline{UPDATE}$, and $\overline{CE}$ are held high and $\overline{CS}$ goes low. Figures 6 and 7 show serial-mode timing. Figure 8 shows the MAX458/MAX459 configured for serial operation. Figure 9 shows the Microwire connection, and Figure 10 shows the SPI/QSPI connection.

The serial output, DOUT, allows cascading of two or more crosspoint switches to create larger arrays. The data at DOUT is delayed by 16 cycles plus one clock pulse width at DIN. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

The MAX458/MAX459 input data in 16-bit blocks. SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data. The QSPI interface allows variable word lengths from 8 to 16 bits and can be loaded into the crosspoint in one write cycle. SPI and Microwire limit clock rates to 2MHz, while the QSPI maximum clock rate is 4MHz.

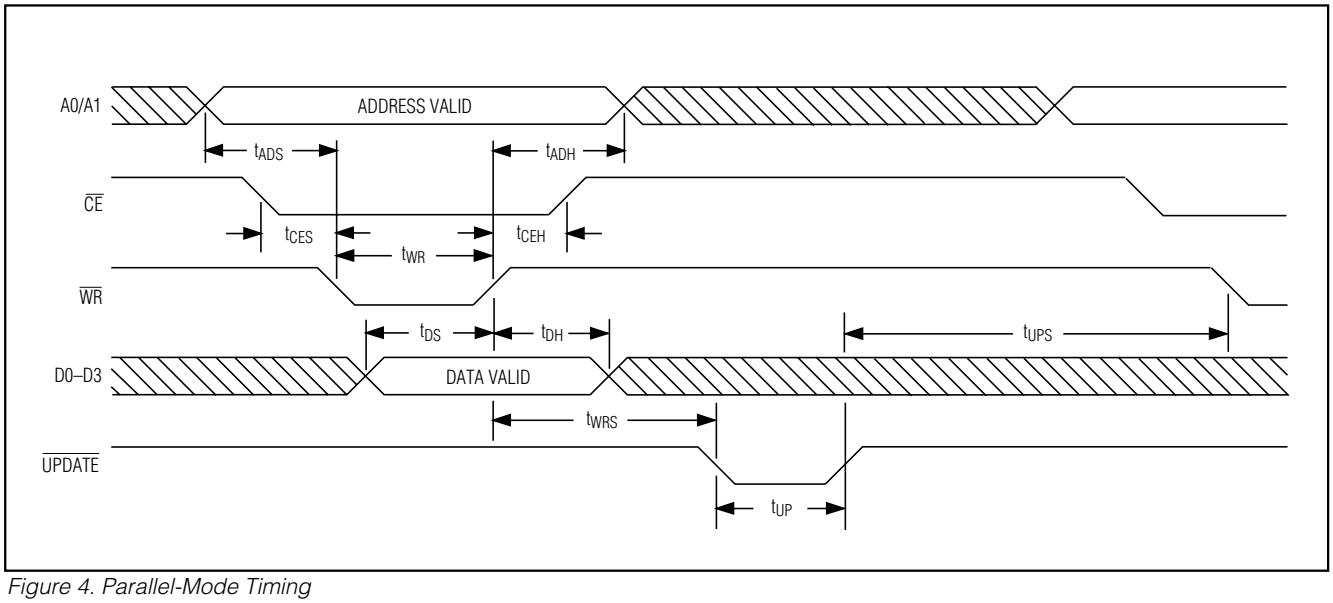


Figure 4. Parallel-Mode Timing

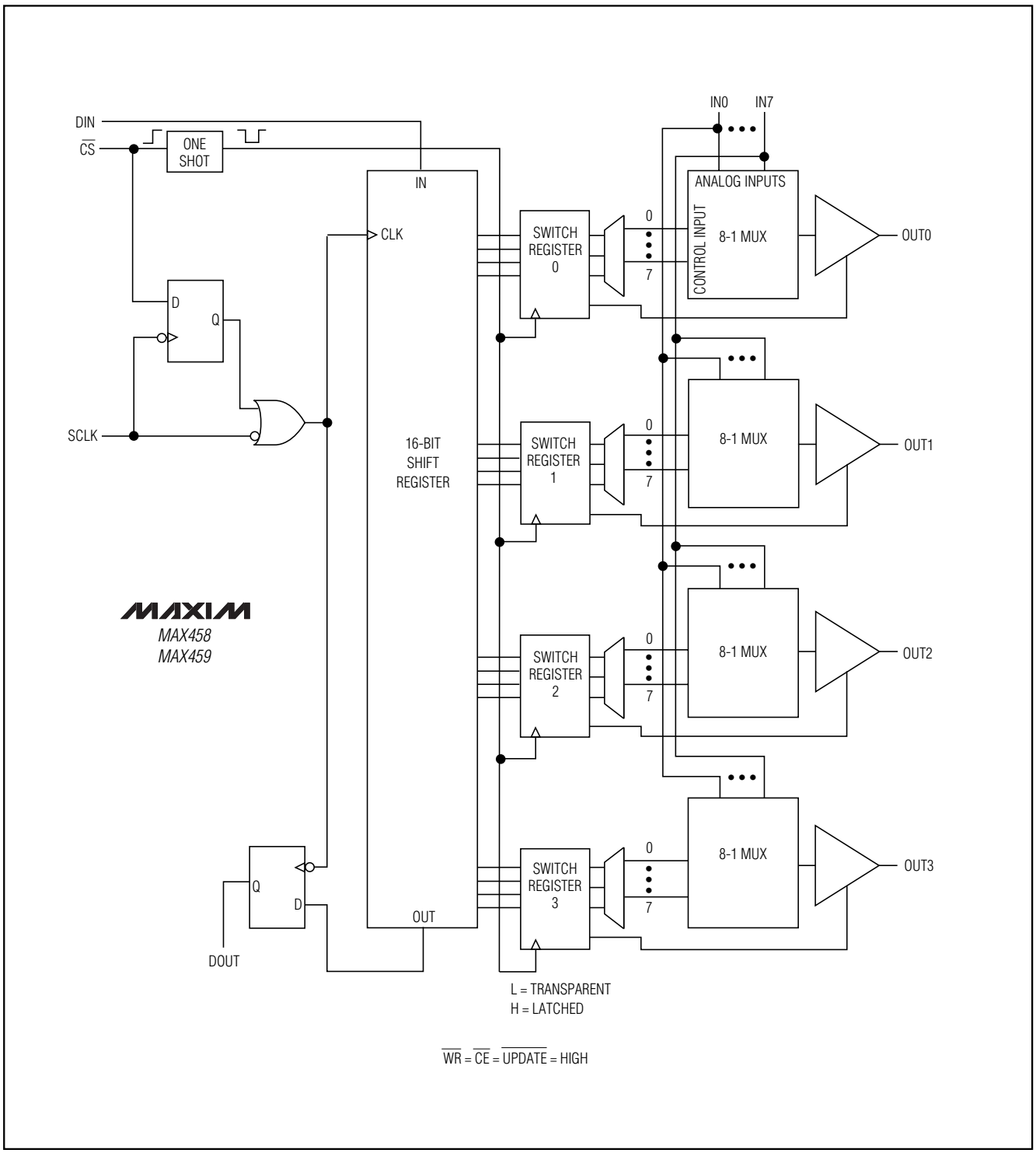


Figure 5. Serial-Mode Logic Block Diagram

8x4 Video Crosspoint Switches with Buffers

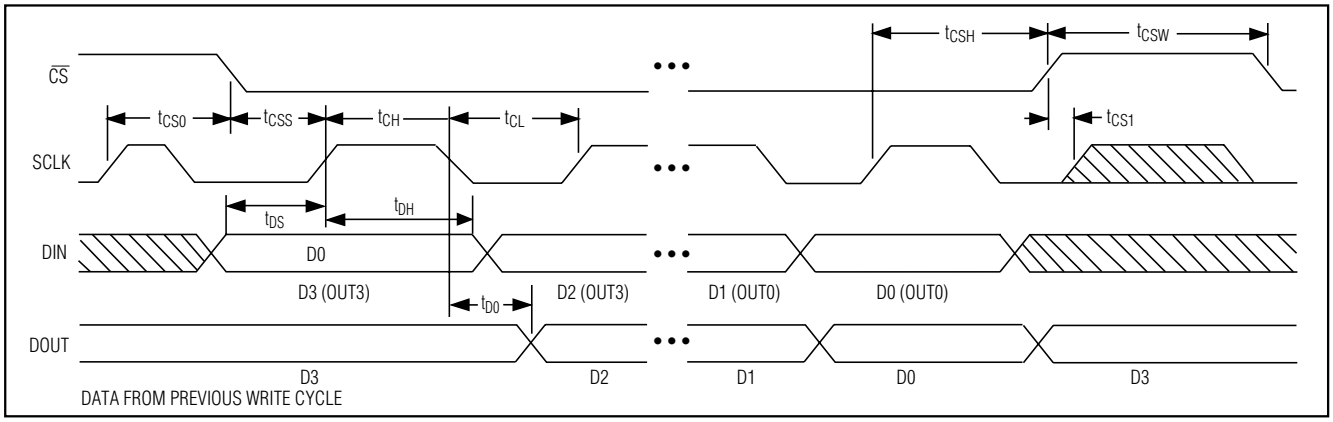


Figure 6. Serial-Mode Timing

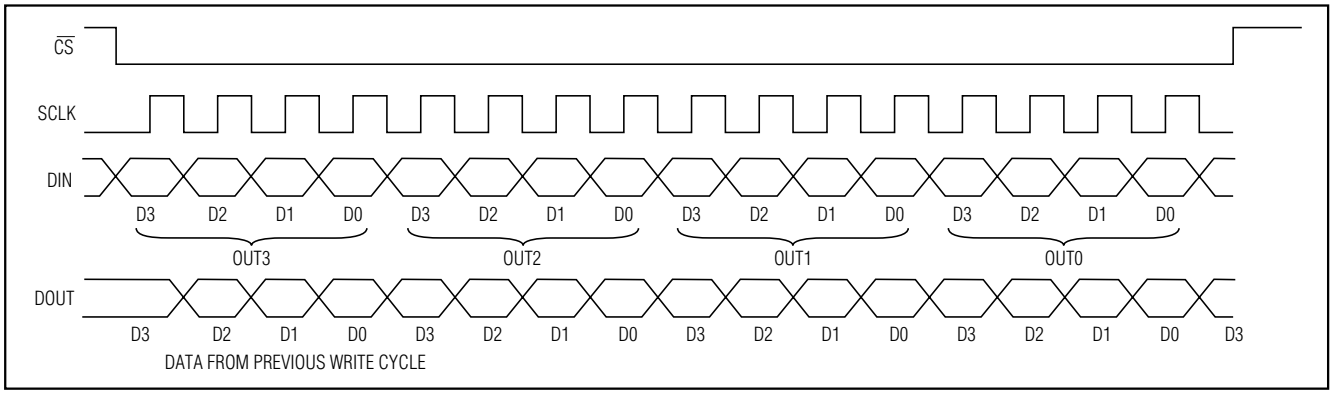


Figure 7. Serial-Mode Data Sequence

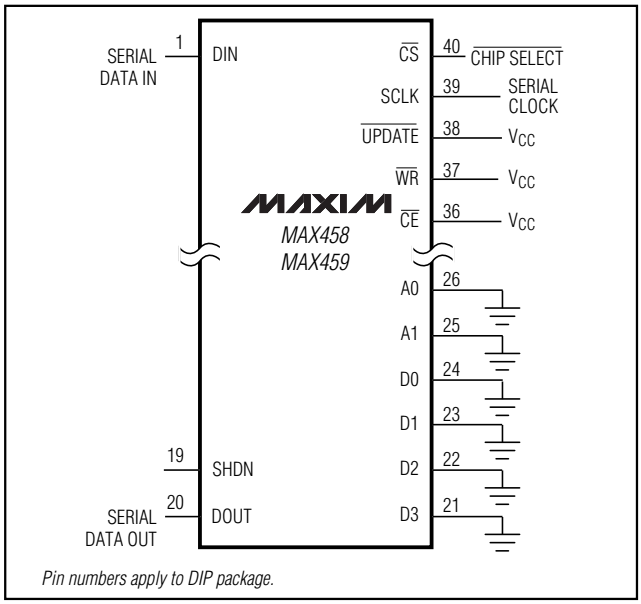


Figure 8. Serial Connection (only logic pins shown)

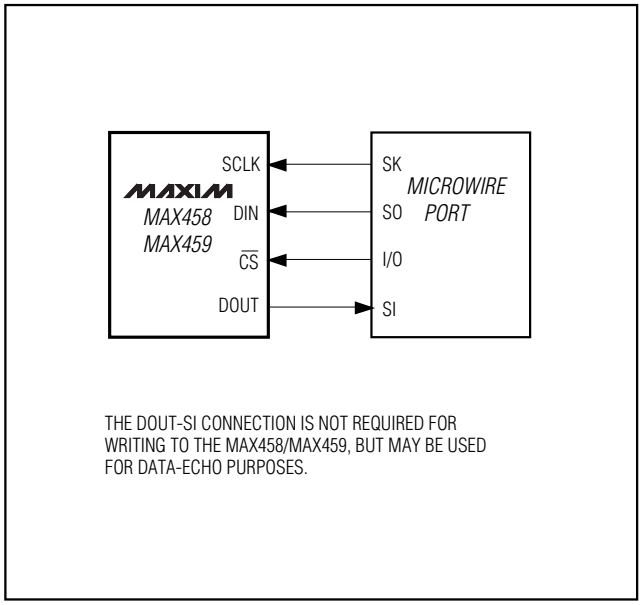


Figure 9. Microwire Connection

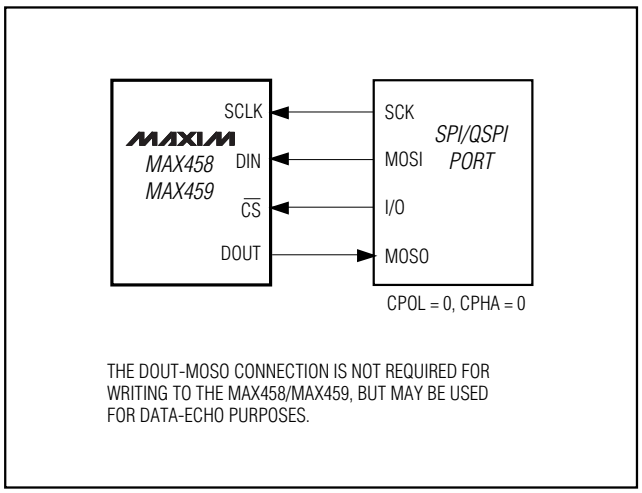


Figure 10. SPI/QSPI Connection

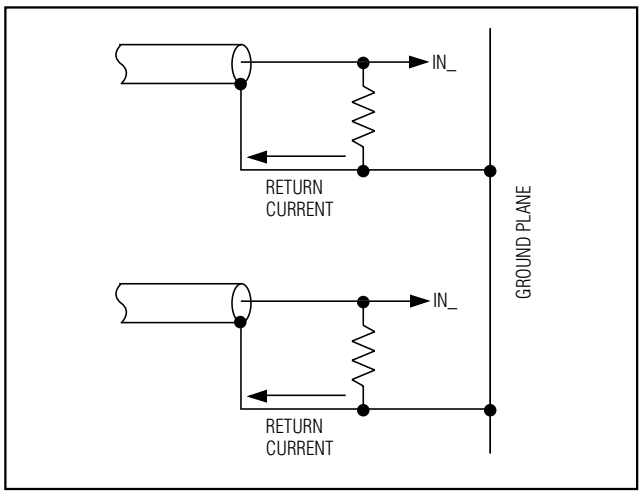


Figure 11. Low-Crosstalk Layout. Return current from termination resistor does not flow through the ground plane.

Applications Information

Grounding and Bypassing, PC Board Layout

As with all analog circuits, good PC board layout, proper grounding, and careful component selection are crucial for realizing the full AC performance of high-speed amplifiers such as the MAX458/MAX459. For optimal performance:

1) Use a large, low-impedance analog ground plane. With multilayer boards, the ground plane(s) should be located on the layer that does not contain signal traces. Connect all GND pins to the analog ground plane.
2) Minimize trace area at the circuit's critical high-impedance nodes to prevent unwanted signal coupling. Surround analog inputs with an AC ground trace (bypassed DC power supply, etc.). The analog input pins of the MAX458/MAX459 have been separated with AC ground pins (GND, V_{CC}, V_{EE}) to minimize parasitic coupling, which can degrade crosstalk.
3) Connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane to further reduce crosstalk (Figure 11).
4) Bypass all power-supply pins directly to the ground plane with 0.1µF ceramic capacitors placed as close to the supply pins as possible. For high-current loads, you may need 10µF tantalum or aluminum-electrolytic capacitors in parallel with the 0.1µF ceramics. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount chip capacitors are ideal.

Creating Larger Arrays

The MAX458/MAX459 assume a high-impedance state on power-up if the inputs are not being programmed to any particular state during that time. They also are in a high-impedance state when disabled. This feature makes it possible to create larger arrays than 8x4 without special programming, other than ensuring that your program doesn't turn on two paralleled outputs simultaneously. Testing has shown no degradation of differential gain or phase when the outputs are connected in parallel.

The MAX458/MAX459's input registers remain active during shutdown, which allows the crosspoint to be programmed while the devices are shut down. As a result, all outputs may be simultaneously brought to any state, including disabled. Just program all of the MAX458/MAX459s into shutdown, and enter the program of your choice by selecting the desired inputs and outputs. Taking SHDN low takes the device(s) out of shutdown.

A power-on reset circuit causes the output amplifiers to power up in the disabled mode, whether or not SHDN is applied, if $\overline{UPDATE}$ and $\overline{CS}$ are high.

The number of MAX458s that can be paralleled is limited by capacitive loading on each output, which must not exceed 100pF. Each input presents approximately 7pF of load, and each output presents approximately 12pF. Therefore, the MAX458/MAX459 will drive a maximum of 14 inputs, or 7 outputs and 2 inputs, or any other combination resulting in less than a 100pF load. Adding isolation resistors enables more MAX458s to be paralleled (see the *Driving Capacitive Loads* section).

8x4 Video Crosspoint Switches with Buffers

Driving Capacitive Loads

When driving loads greater than 100pF, you may need a capacitance compensating resistor in series with the output of each affected amplifier. The required resistor will depend on load as well as capacitance. For 150Ω or higher load resistances and capacitance up to 1000pF, use a 2.4Ω resistor. For 100Ω loads, use a 4.7Ω resistor.

If an output amplifier is loaded with a pure capacitance or with the inputs of other MAX458/MAX459s, the resistors will cause no degradation of gain or other performance because of the high impedance of the crosspoints. However, resistive loads may cause a reduction in gain.

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more crosspoint switches to create larger arrays. The data at DOUT is the DIN data delayed by 16 cycles plus one clock width. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX458/MAX459 crosspoint switches can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain, as shown in Figure 12. For proper timing, ensure that both t_{CSS} ($\overline{CS}$ low to SCLK high) and t_{CL} are greater than $t_{DO} + t_{DS}$.

DOUT is a TTL-compatible output with an active pull-up. It does not become high impedance when $\overline{CS}$ is high.

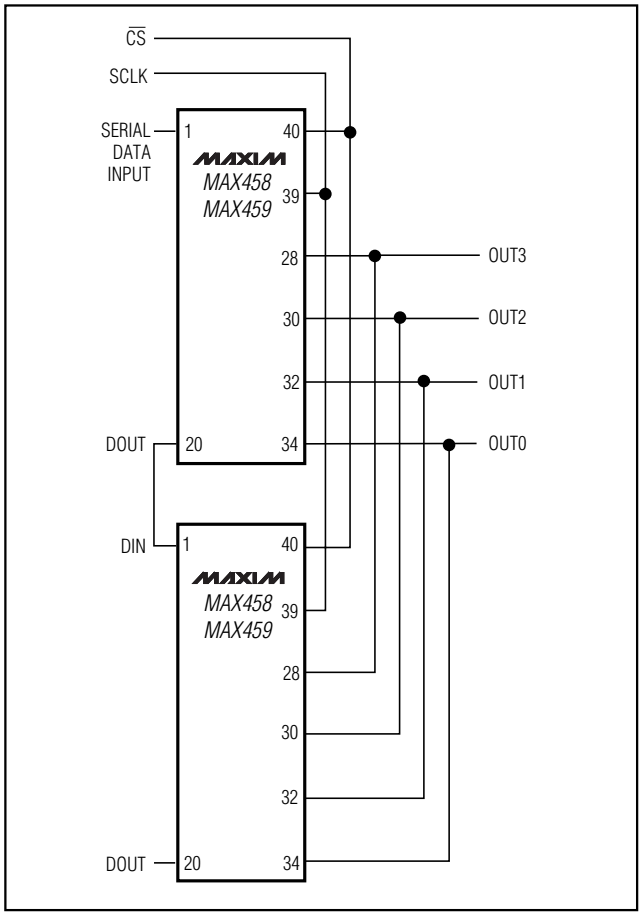
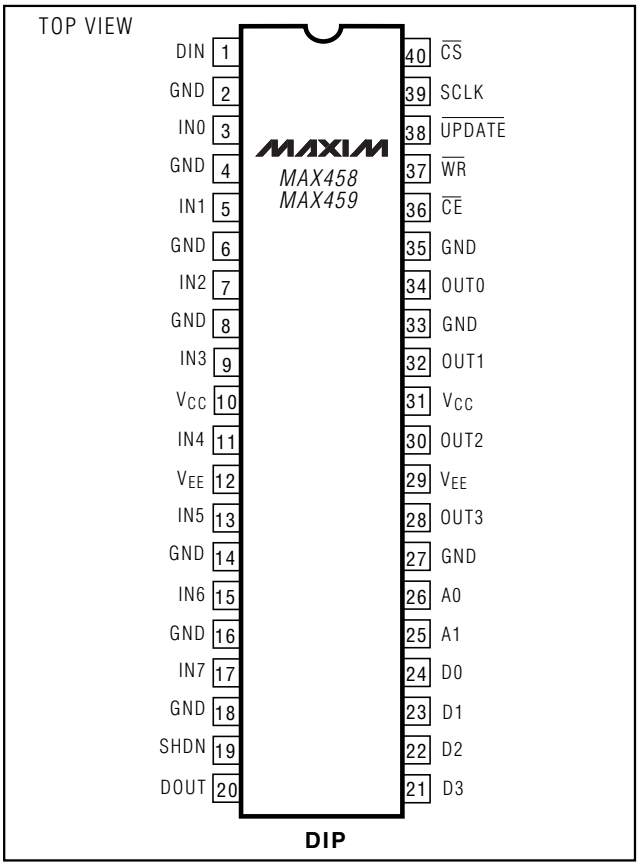


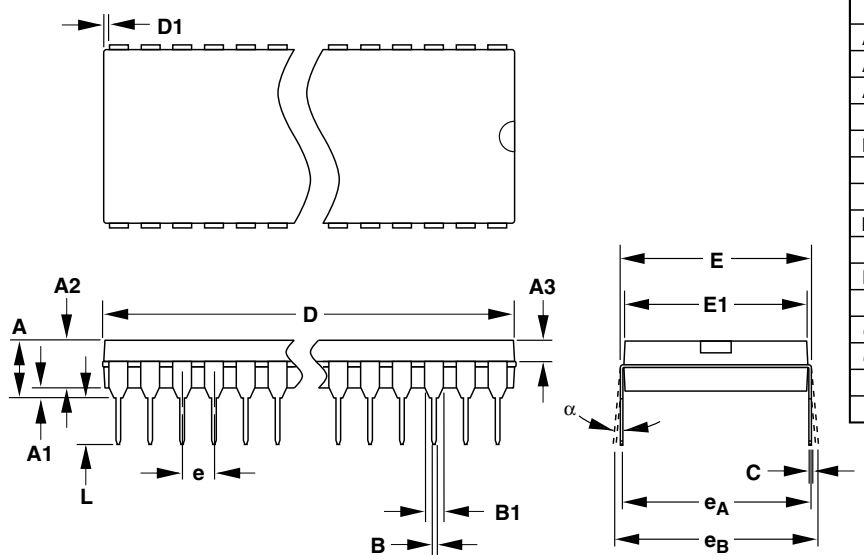
Figure 12. 16x4 Crosspoint Switch Using Serial "Daisy Chain" Connection

Pin Configurations (continued)



8x4 Video Crosspoint Switches with Buffers

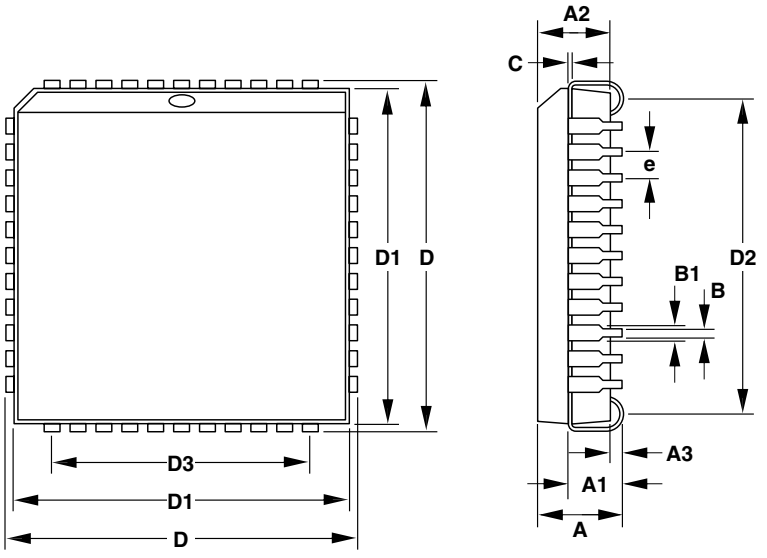
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	2.025	2.075	51.44	52.71
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81
α	0°	15°	0°	15°

21-348A

40-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.685	0.695	17.40	17.65
D1	0.650	0.655	16.51	16.64
D2	0.590	0.630	14.99	16.00
D3	0.500 REF		12.70 REF	
e	0.050 REF		1.27 REF	

21-350A

44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE