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19-0841; Rev 0; 6/07

1000 Base-T, ±15kV ESD Protection LAN Switch

MAX4927

General Description

The MAX4927 meets the needs of high-speed differential switching, including that of Gigabit Ethernet (10/100/1000) Base-T switching as well as LVDS and LVPECL switching. The MAX4927 provides enhanced ESD protection up to ±15kV and excellent high-frequency response, making the device especially useful for interfaces that must go to an outside connection.

The MAX4927 offers extremely low capacitance (C_{ON}), as well as low on-resistance (R_{ON}), for low-insertion loss and very wide bandwidth. In addition to the four pairs of DPDT switches, the MAX4927 provides LED switching for laptop computer/docking station use.

The MAX4927 is pin-to-pin equivalent to the PI3L500-A and STMUX1000L. The MAX4927 can replace either device in those applications, improving ESD protection and eliminating external ESD components. The MAX4927 is available in a space-saving 56-pin TQFN package and operates over the extended -40°C to +85°C temperature range.

Applications

Notebooks and Docking Stations

Servers and Routers with Ethernet Interfaces

Board-Level Redundancy Protection

SONET/SDH Signal Routing

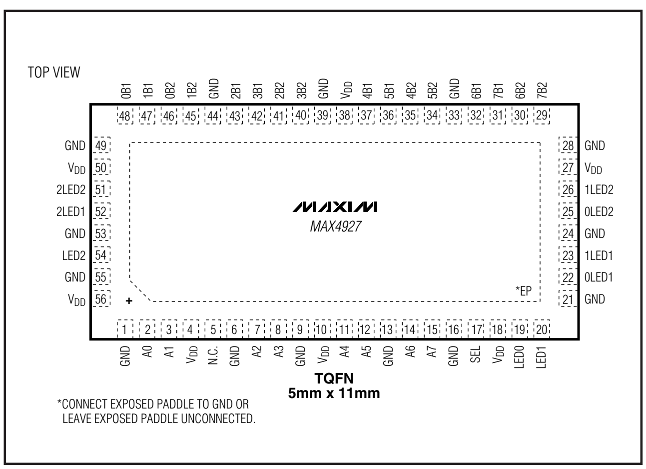
T3/E3 Redundancy Protection

LVDS and LVPECL Switching

Features

- **ESD Protection**
  - **±15kV–IEC 61000-4-2 Air-Gap Discharge**
  - **±8kV–IEC 61000-4-2 Contact Discharge**
  - **±15kV–Human Body Model**
- **Single +3.0V to +3.6V Power-Supply Voltage**
- **Low 4Ω (typ), 6.5Ω (max) On-Resistance (R_{ON})**
- **Ultra-Low 8pF (typ) On-Capacitance (C_{ON})**
- **-23dB Return Loss (100MHz)**
- **-3dB Bandwidth: 650MHz**
- **Optimized Pin Out for Easy Transformer and PHY Interface**
- **Built-In LED Switches for Switching Indicators to Docking Station**
- **Low 450µA (max) Quiescent Current**
- **Bidirectional 8 to 16 Multiplexer/Demultiplexer**
- **Standard Pin Out, Matching the PI3L500-A and STMUX1000L**
- **Space-Saving Lead-Free Package**
  - **56-Pin, 5mm x 11mm, TQFN Package**

Pin Configuration



Ordering Information

PART	PIN-PACKAGE	LED SWITCHES	PKG CODE
MAX4927ETN+	56 TQFN-EP*	3	T56511-1

+Denotes lead-free package.

***Note:** All devices are specified over the -40°C to +85°C operating temperature range.*

**EP = Exposed pad.*

Typical Operating Circuit and Functional Diagrams appear at end of data sheet.

1000 Base-T, ±15kV ESD Protection LAN Switch

ABSOLUTE MAXIMUM RATINGS

V_{DD} ....-0.3V to +4V
All Other Pins ....-0.3V to (V_{DD} + 0.3V)
Continuous Current (A_ to _B_) ....±120mA
Continuous Current (LED_ to _LED_) ....±40mA
Peak Current (A_ to _B_)
(pulsed at 1ms, 10% duty cycle) ....±240mA
Current into Any Other Pin ....±20mA

Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 40.9mW/°C above +70°C) 5278mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature.......... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V to +3.6V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
On-Resistance	R_{ON}	V_{DD} = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 0, 1.5V, 3V	T_A = +25°C		4	5.5	Ω
			T_{MIN} to T_{MAX}			6.5	
On-Resistance Match Between Switch Pairs (Note 2)	ΔR_{ON}	V_{DD} = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 0, 1.5V, 3V	T_A = +25°C		0.5	1.5	Ω
			T_{MIN} to T_{MAX}			2	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{DD} = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 1.5V, 3V			0.01		Ω
On-Resistance LED Switches	R_{ONLED}	V_{DD} = 3V, $I_{\_LED\_}$ = -40mA, $V_{LED\_}$ = 0, 1.5V, 3V				40	Ω
Off-Leakage Current	$I_{LA\_(OFF)}$	V_{DD} = 3.6V, $V_{A\_}$ = 0.3V, 3.3V; $V_{\_B1}$ or $V_{\_B2}$ = 3.3V, 0.3V		-1		+1	µA
On-Leakage Current	$I_{LA\_(ON)}$	V_{DD} = 3.6V, $V_{A\_}$ = 0.3V, 3.3V; $V_{\_B1}$ or $V_{\_B2}$ = 0.3V, 3.3V, or floating		-1		+1	µA
ESD PROTECTION							
ESD Protection		IEC 61000-4-2 Air-Gap Discharge			±15		kV
		IEC 61000-4-2 Contact Discharge			±8		
		Human Body Model (spec MIL-STD-883, Method 3015)			±15		
SWITCH AC PERFORMANCE							
Insertion Loss	I_{LOS}	R_S = R_L = 50Ω, unbalanced, f = 1MHz (Note 2)			0.6		dB
Return Loss	R_{LOS}	f = 100MHz			-23		dB
Crosstalk	V_{CT1}	Any switch to any switch; R_S = R_L = 50Ω, unbalanced, Figure 1	f = 25MHz		-50		dB
	V_{CT2}		f = 100MHz		-26		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V to +3.6V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH AC CHARACTERISTICS						
-3dB Bandwidth	BW	$R_S = R_L = 50\Omega$, unbalanced		650		MHz
Off-Capacitance	C_{OFF}	f = 1MHz, _B_, A_		3.5		pF
On-Capacitance	C_{ON}	f = 1MHz, _B_, A_		6.5		pF
Turn-On Time	t_{ON}	$V_{A\_}$ = 1V, $R_L = 100\Omega$, Figure 2			50	ns
Turn-Off Time	t_{OFF}	$V_{A\_}$ = 1V, $R_L = 100\Omega$, Figure 2			50	ns
Propagation Delay	t_{PLH}, t_{PHL}	$R_S = R_L = 50\Omega$, unbalanced, Figure 3		0.15		ns
Output Skew Between Ports	$t_{SK(o)}$	Skew between any two ports, Figure 4		0.01		ns
SWITCH LOGIC						
Input-Voltage Low	V_{IL}	V_{DD} = 3.0V			0.8	V
Input-Voltage High	V_{IH}	V_{DD} = 3.6V	2.0			V
Input-Logic Hysteresis	V_{HYST}	V_{DD} = 3.3V		100		mV
Input Leakage Current	I_{SEL}	V_{DD} = 3.6V, V_{SEL} = 0V or V_{DD}	-1		+1	µA
Operating-Supply Voltage Range	V_{DD}		3.0		3.6	V
Quiescent Supply Current	I_{DD}	V_{DD} = 3.6V, V_{SEL} = 0V or V_{DD}		280	450	µA

Note 1: Specifications at T_A = -40°C are guaranteed by design.
Note 2: Guaranteed by design.

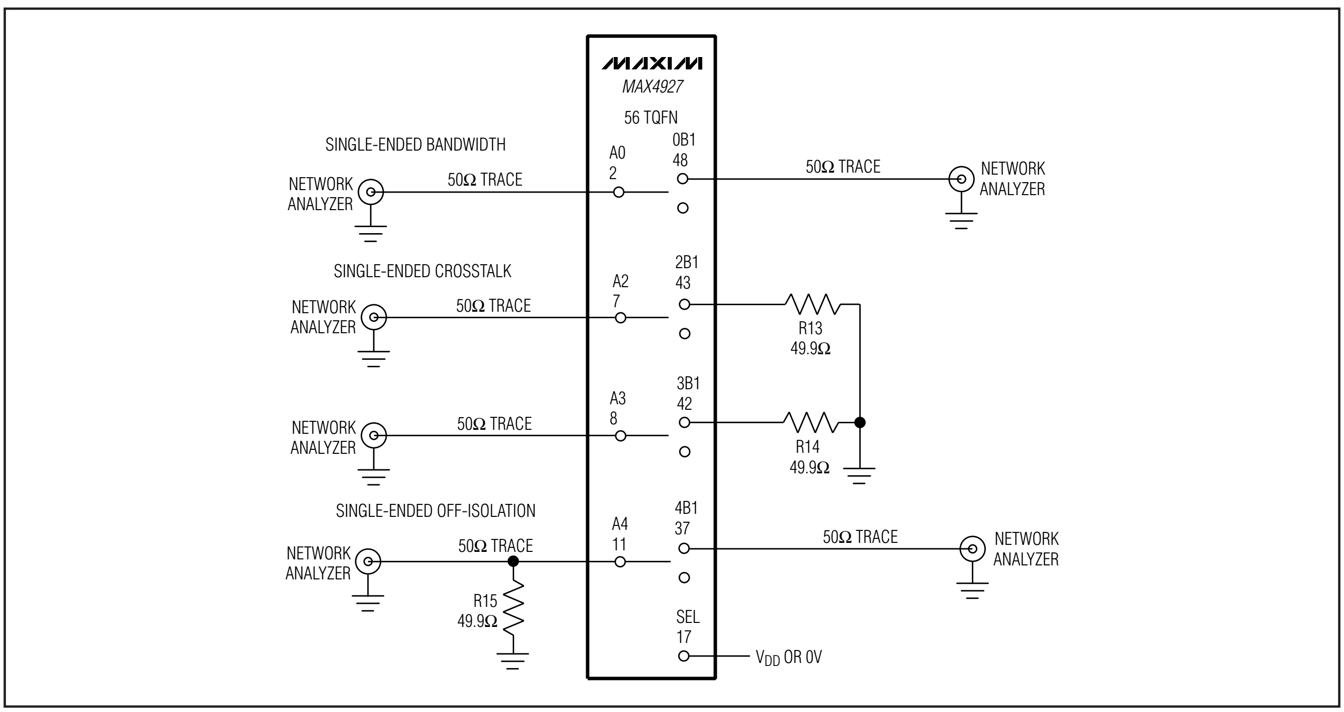


Figure 1. Single-Ended Bandwidth, Crosstalk, and Off-Isolation

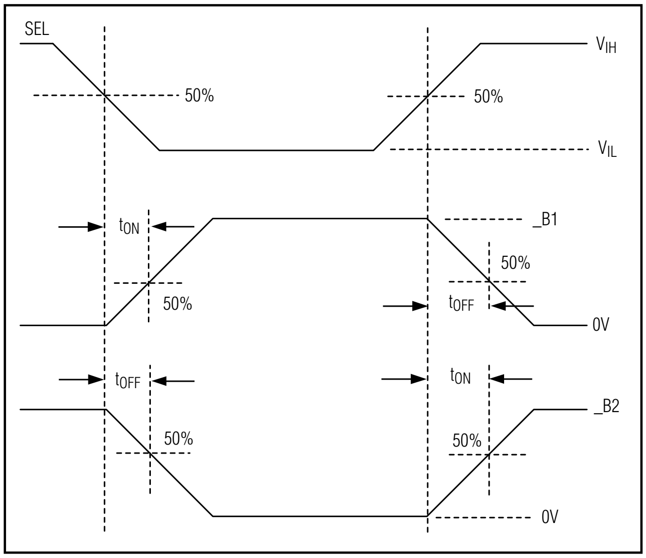


Figure 2. Turn-On and Turn-Off Times

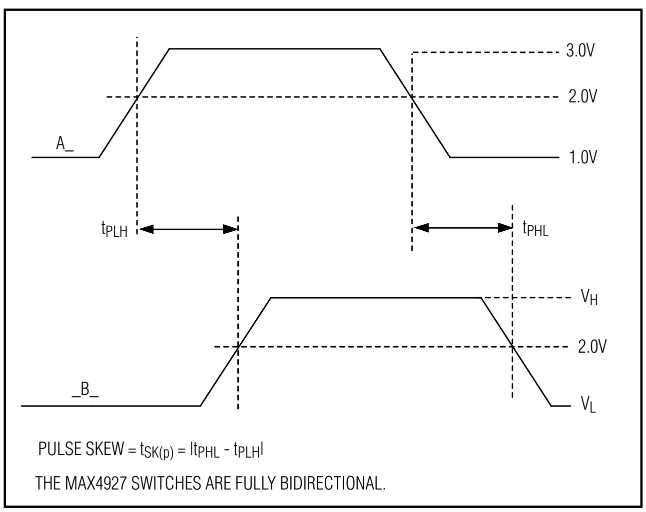


Figure 3. Propagation Delay Times

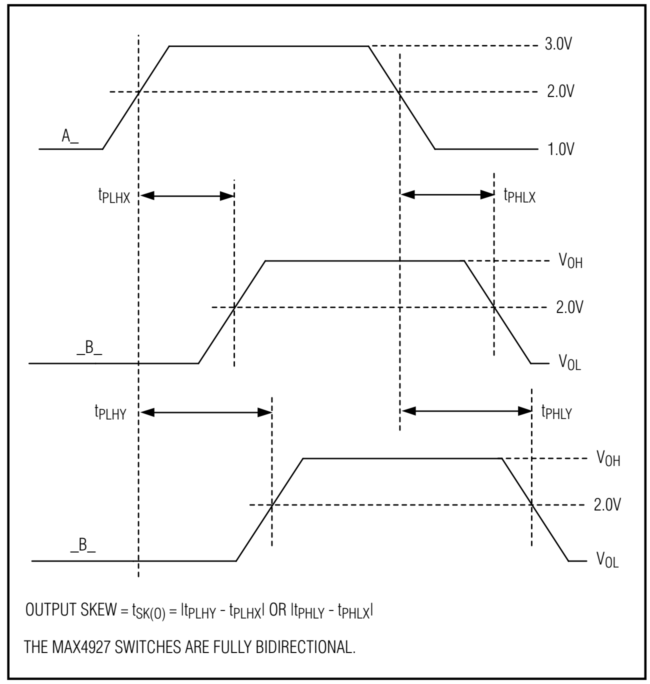
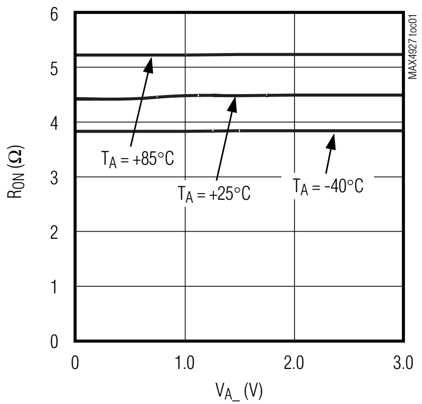


Figure 4. Output Skew

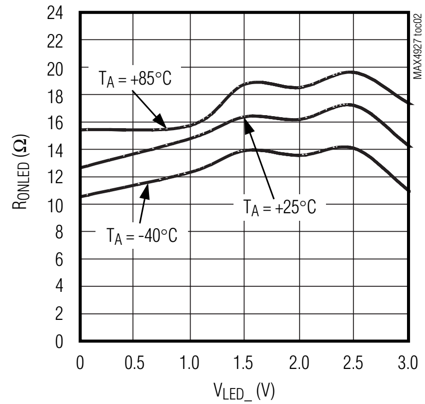
Typical Operating Characteristics

(V_{DD} = 3.3V, T_A = +25°C, unless otherwise noted.)

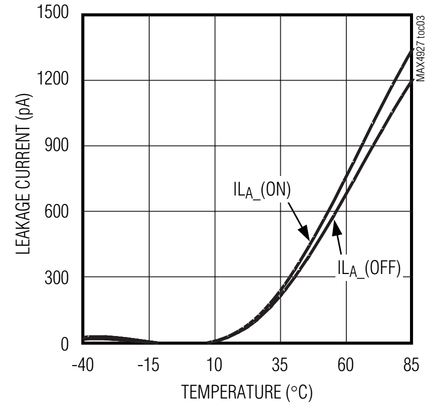
ON-RESISTANCE vs. $V_{A\_}$



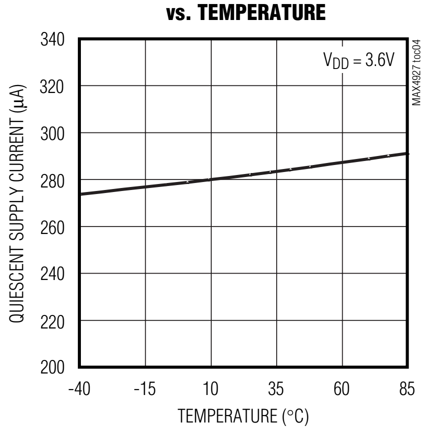
LED_ ON-RESISTANCE vs. $V_{LED\_}$



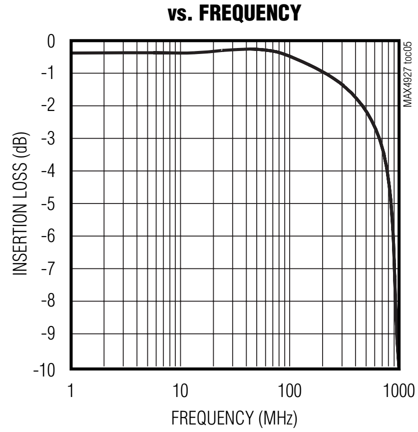
LEAKAGE CURRENT vs. TEMPERATURE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



SINGLE-ENDED INSERTION LOSS vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 6, 9, 13, 16, 21, 24, 28, 33, 39, 44, 49, 53, 55	GND	Ground
2	A0	Switch 0. Common terminal 0.
3	A1	Switch 1. Common terminal 1.
4, 10, 18, 27, 38, 50, 56	V_{DD}	Positive-Supply Voltage Input. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor (see the *Power-Supply Bypassing* section).
5	N.C.	No Connection. Not internally connected.
7	A2	Switch 2. Common terminal 2.
8	A3	Switch 3. Common terminal 3.
11	A4	Switch 4. Common terminal 4.
12	A5	Switch 5. Common terminal 5.
14	A6	Switch 6. Common terminal 6.
15	A7	Switch 7. Common terminal 7.
17	SEL	Select Input. SEL selects switch connection. See the truth table (Table 1).
19	LED0	LED0 Input
20	LED1	LED1 Input
22	0LED1	0LED1 Output. Drive SEL low (SEL = 0) to connect LED0 to 0LED1.
23	1LED1	1LED1 Output. Drive SEL low (SEL = 0) to connect LED1 to 1LED1.
25	0LED2	0LED2 Output. Drive SEL high (SEL = 1) to connect LED0 to 0LED2.
26	1LED2	1LED2 Output. Drive SEL high (SEL = 1) to connect LED1 to 1LED2.
29	7B2	Switch 7. Normally open terminal 7.
30	6B2	Switch 6. Normally open terminal 6.
31	7B1	Switch 7. Normally closed terminal 7.
32	6B1	Switch 6. Normally closed terminal 6.
34	5B2	Switch 5. Normally open terminal 5.
35	4B2	Switch 4. Normally open terminal 4.
36	5B1	Switch 5. Normally closed terminal 5.
37	4B1	Switch 4. Normally closed terminal 4.
40	3B2	Switch 3. Normally open terminal 3.
41	2B2	Switch 2. Normally open terminal 2.
42	3B1	Switch 3. Normally closed terminal 3.
43	2B1	Switch 2. Normally closed terminal 2.
45	1B2	Switch 1. Normally open terminal 1.
46	0B2	Switch 0. Normally open terminal 0.
47	1B1	Switch 1. Normally closed terminal 1.
48	0B1	Switch 0. Normally closed terminal 0.

Pin Description (continued)

PIN	NAME	FUNCTION
51	2LED2	2LED2 Output. Drive SEL high (SEL = 1) to connect LED2 to 2LED2.
52	2LED1	2LED1 Output. Drive SEL low (SEL = 0) to connect LED2 to 2LED1.
54	LED2	LED2 Input
EP	EP	Exposed Paddle. Connect EP to GND or leave EP unconnected.

Detailed Description

The MAX4927 is a high-speed analog switch targeted for 1000 Base-T applications. In a typical application, the MAX4927 switches the signals from two separate interface transformers and connects the signals to a single 1000 Base-T Ethernet PHY (see the *Typical Operating Circuit*). This configuration simplifies docking-station design by avoiding signal reflections associated with unterminated transmission lines in a T configuration. The MAX4927 is protected against ±15kV electrostatic discharge (ESD) events. The MAX4927 also includes LED switches that allow the LED output signals to be routed to a docking station along with the Ethernet signals. See the *Functional Diagrams.*

With its low resistance and capacitance, as well as high ESD protection, the MAX4927 can be used to switch most low-voltage differential signals, such as LVDS, SERDES, and LVPECL, as long as the signals do not exceed maximum ratings of the device.

The MAX4927 switch provides an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4927 features three built-in LED switches.

The MAX4927 incorporates a unique architecture design utilizing only n-channel switches within the main Ethernet switch, reducing I/O capacitance and channel resistance. An internal two-stage charge pump with a nominal 7.5V output provides the high voltage needed to drive the gates of the n-channel switches while maintaining a consistently low R_{ON} throughout the input signal range. An internal bandgap reference set to 1.23V and an internal oscillator running at 2.5MHz provide proper charge-pump operation. Unlike other charge-pump circuits, the MAX4927 includes internal flyback capacitors, reducing design time, board space, and cost.

Digital Control Inputs

The MAX4927 provides a single digital control input, SEL. SEL controls the high-frequency switches as well as the LED switches as shown in Table 1.

Table 1. Truth Table

SEL	CONNECTION
0	A_ to _B1, LED_ to _LED1
1	A_ to _B2, LED_ to _LED2

Analog Signal Levels

The on-resistance of the MAX4927 is very low and stable as the analog input signals are swept from ground to V_{DD} (see the *Typical Operating Characteristics*). The switches are bidirectional, allowing A_ and _B_ to be configured as either inputs or outputs.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. All the high-frequency switch inputs (A_, _B_), LED switch inputs (LED_, _LED_), and SEL have high ESD protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. After an ESD event, the MAX4927 keeps working without latchup or damage.

ESD protection can be tested in various ways. All signal and control inputs of the MAX4927 are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge Method specified in IEC 61000-4-2
- ±15kV using the Air-Gap Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

1000 Base-T, ±15kV ESD Protection LAN Switch

Human Body Model

Figure 5a shows the Human Body Model. Figure 5b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX4927 helps equipment design to meet IEC 61000-4-2 without the need for additional ESD-protected components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 5c shows the IEC 61000-4-2 model, and Figure 5d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance.

The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

The Air-Gap Discharge Method involves approaching the device with a charged probe. The Contact Discharge Method connects the probe to the device before the probe is energized.

Applications Information

Typical Operating Circuit

The *Typical Operating Circuit* shows the MAX4927 in a 1000 Base-T docking station application.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{DD} before applying analog signals, especially if the analog signal is not current limited.

Power-Supply Bypassing

Bypass at least one V_{DD} input to ground with a 0.1µF or larger ceramic capacitor as close to the device as possible. Use the smallest physical size possible for optimal performance (0603 body size is recommended).

It is also recommended to bypass more than one V_{DD} input. A good strategy is to bypass one V_{DD} input with a 0.1µF capacitor, and at least a second V_{DD} input with a 10nF capacitor (use 0603 or smaller physical size ceramic capacitor).

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance PCB traces as short as possible. Ensure that bypass capacitors are as close as possible to the device. Use large ground planes where possible.

Chip Information

PROCESS: BiCMOS

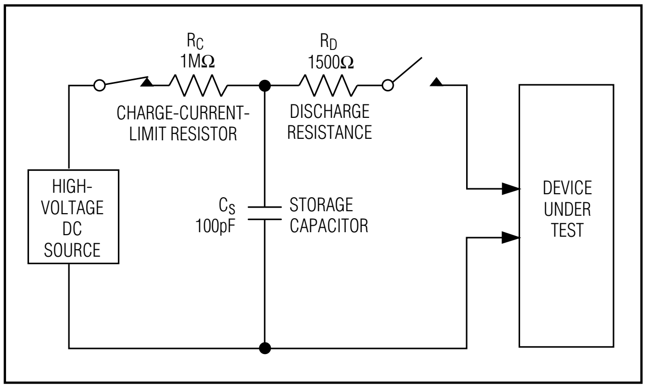


Figure 5a. Human Body ESD Test Model

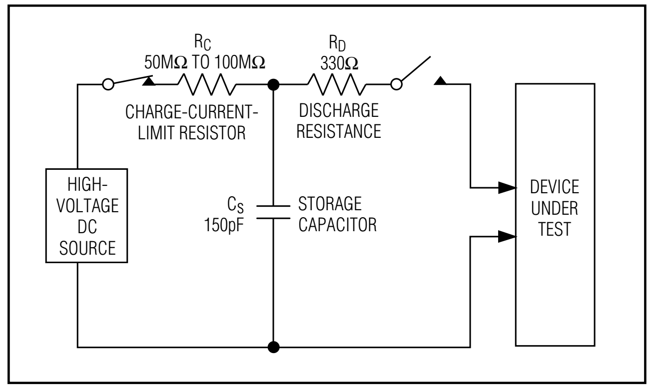


Figure 5c. IEC 61000-4-2 ESD Test Model

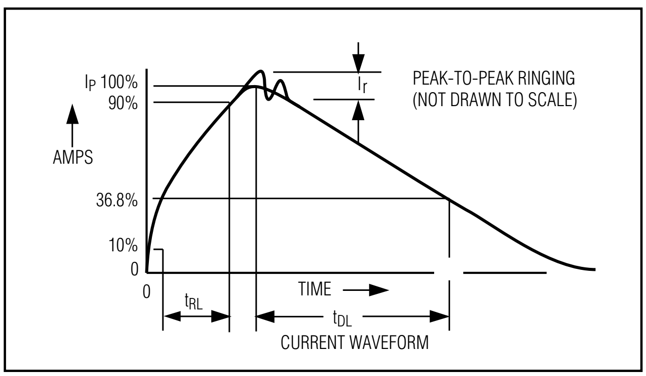


Figure 5b. Human Body Current Waveform

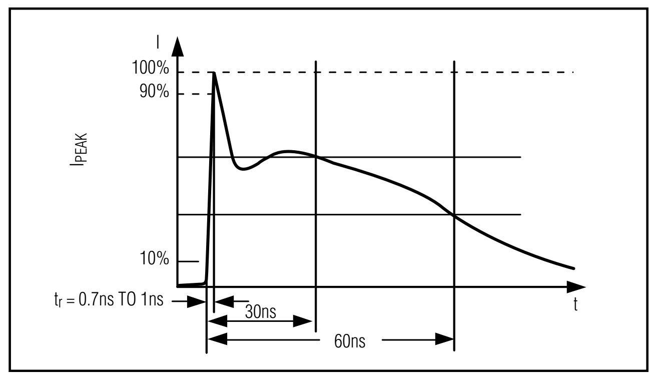
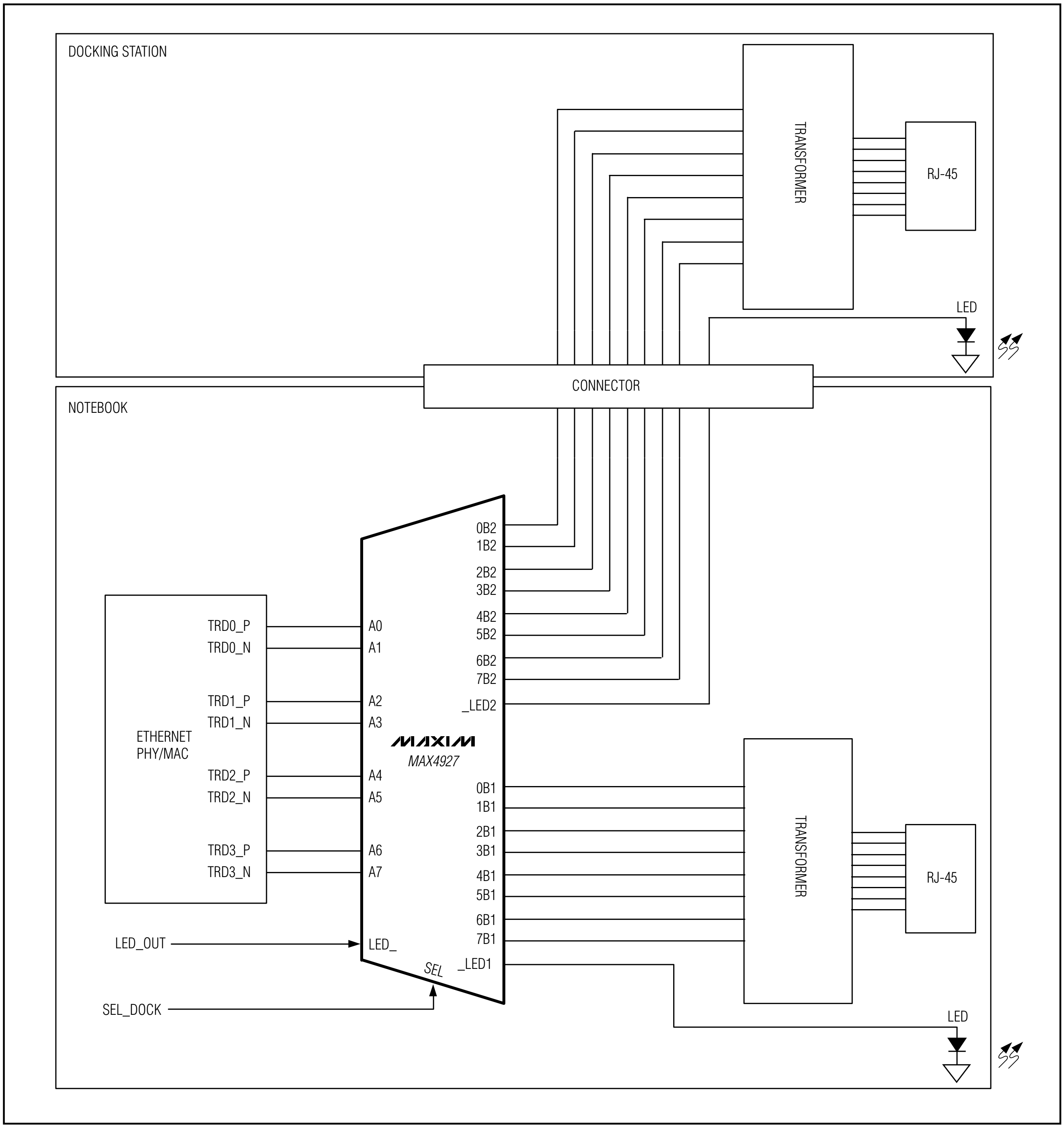
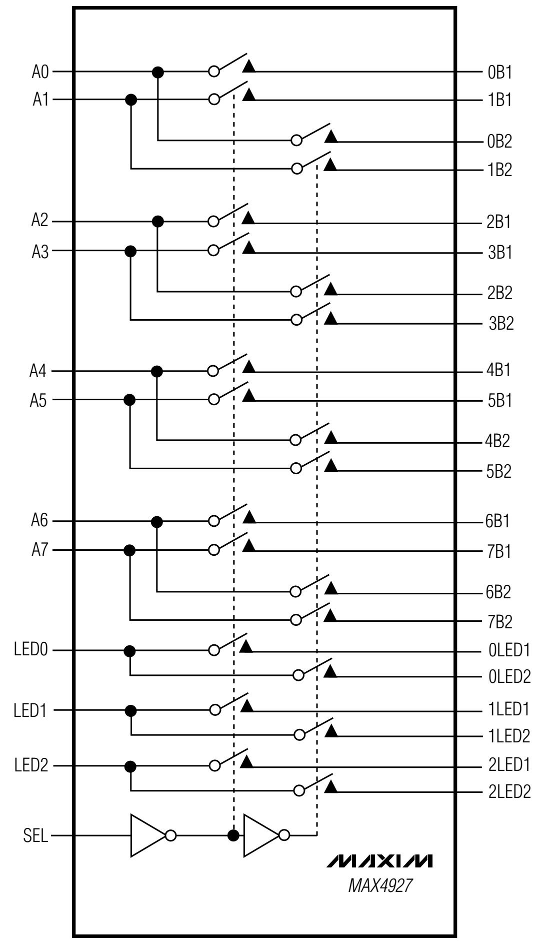


Figure 5d. IEC 61000-4-2 ESD Generator Current Waveform

Typical Operating Circuit

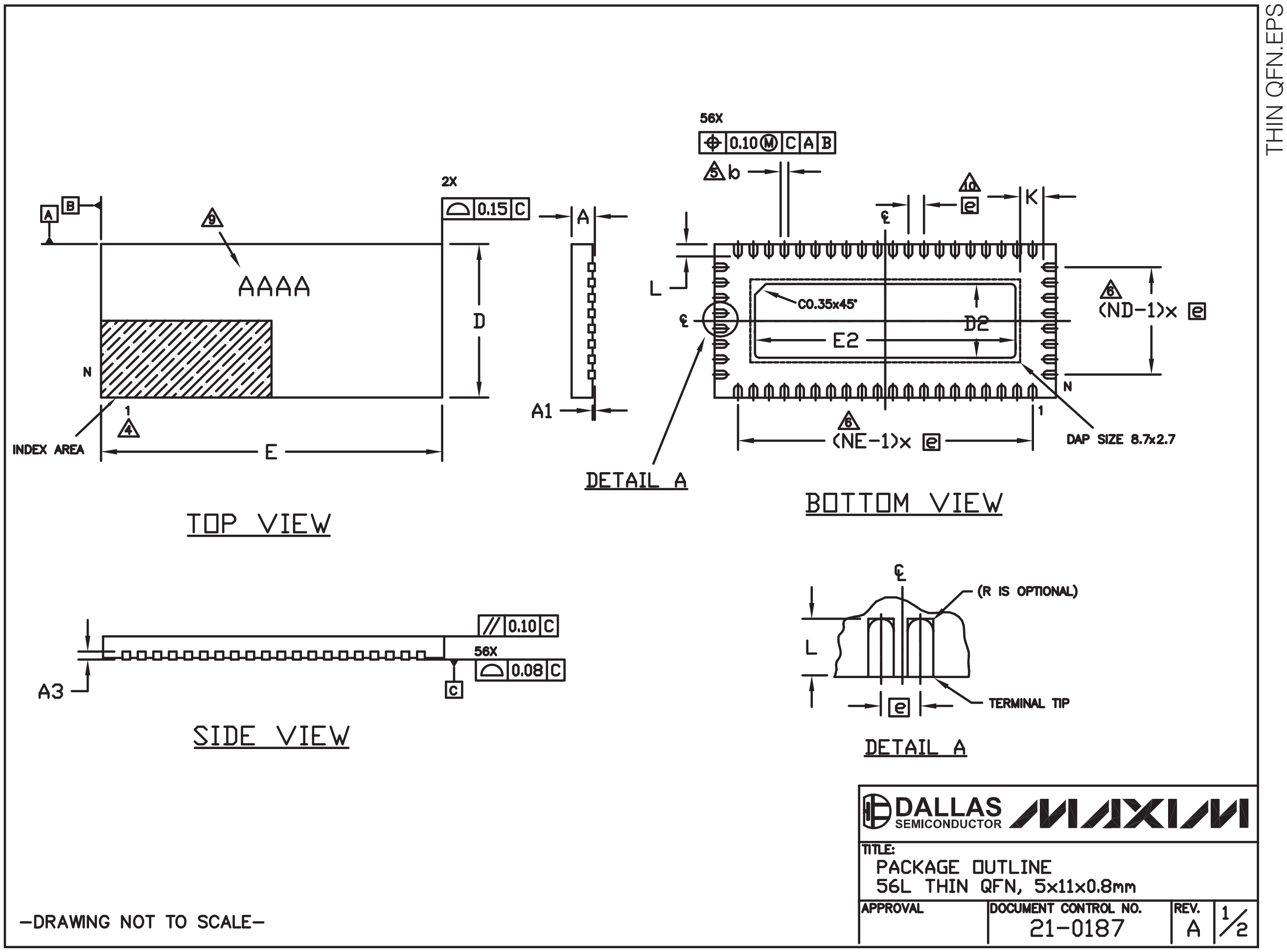


Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	-	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	4.90	5.00	5.10	
E	10.90	11.00	11.10	
e	0.50 BSC.			
k	0.25	-	-	
L	0.30	0.40	0.50	
N	56			
ND	8			
NE	20			

	EXPOSED PAD VARIATIONS					
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T56511-1	2.30	2.40	2.50	8.30	8.40	8.50

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
10. LEAD CENTERLINES TO BE AT DEFINED BY DIMESION e ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
56L THIN QFN, 5x11x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0187	A	2/2