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**MAXIM**

# PCIe, Single Lane, 2:1/1:2 Multiplexer and Redriver with Equalization

**MAX4969**

## General Description

The MAX4969 active 2:1 and 1:2 multiplexer equalizes and redrives PCIe® signals up to 5.0GT/s (Gigatransfers per second) and operates from a single +3.3V supply.

The MAX4969 features PCIe-required electrical idle and receiver detection on each channel, and improves signal integrity at the receiver through independent programmable input equalization and output deemphasis.

The MAX4969 is available in a small, 42-pin (3.5mm x 9.0mm) TQFN package optimal for simplified layout and space-saving requirements. The MAX4969 is specified over the 0°C to +70°C commercial operating temperature range.

## Applications

Blade Servers

Workstations

Communications Switches

Test Equipment

Storage Area Network

## Features

♦ **Single +3.3V Supply Operation**

♦ **PCIe Gen 1 (2.5GT/s) and Gen 2 (5.0GT/s) Return Loss ≥ 8dB (1.25GHz ≤ f ≤ 2.5GHz)**

♦ **Independent Input Equalization**

♦ **Independent Output Deemphasis**

♦ **Independent Output Level Selection Reduced Power and EMI**

♦ **On-Chip 50Ω Input/Output Terminations**

♦ **Inline Signal Traces for Simplified Layout**
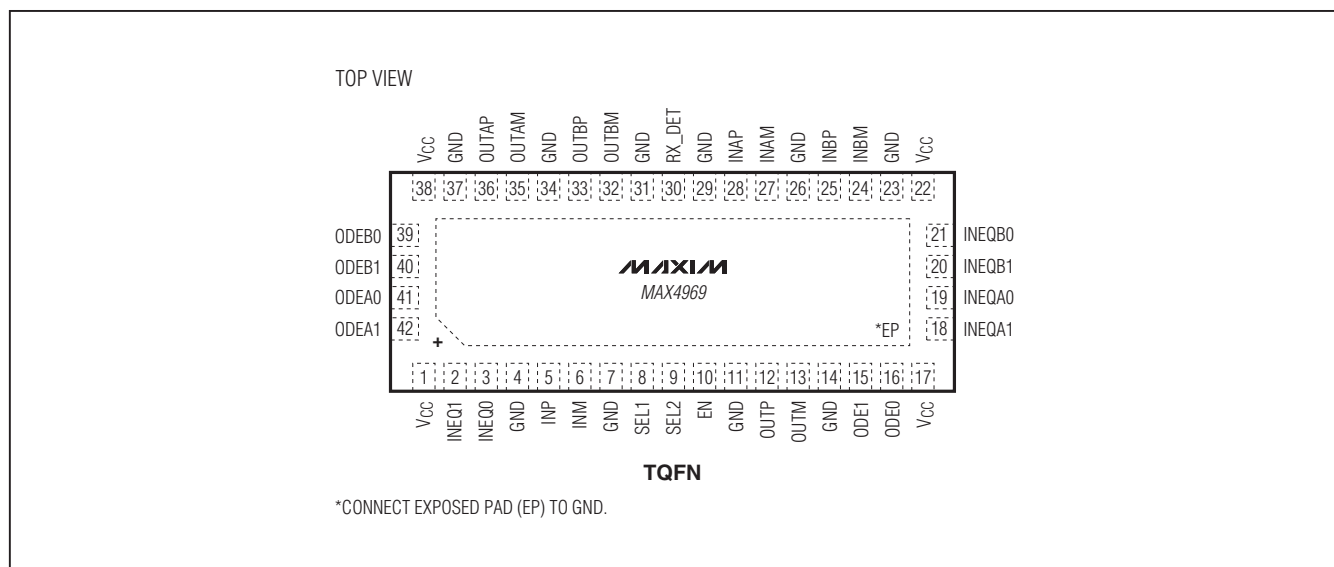
♦ **Space-Saving, 3.5mm x 9.0mm TQFN Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------|-----------|-------------|
| MAX4969CTO+ | 0°C to +70°C | 42 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*\*EP = Exposed pad.*

## Pin Configuration



TOP VIEW

Pins (top row, left to right): 38 VCC, 37 GND, 36 OUTAP, 35 OUTAM, 34 GND, 33 OUTBP, 32 OUTBM, 31 GND, 30 RX_DET, 29 GND, 28 INAP, 27 INAM, 26 GND, 25 INBP, 24 INBM, 23 GND, 22 VCC

Left side (top to bottom): 39 ODEB0, 40 ODEB1, 41 ODEA0, 42 ODEA1

Right side (top to bottom): 21 INEQB0, 20 INEQB1, 19 INEQA0, 18 INEQA1

*EP

Bottom row (left to right): 1 VCC, 2 INEQ1, 3 INEQ0, 4 GND, 5 INP, 6 INM, 7 GND, 8 SEL1, 9 SEL2, 10 EN, 11 GND, 12 OUTP, 13 OUTM, 14 GND, 15 ODE1, 16 ODE0, 17 VCC

MAX4969

**TQFN**

*\*CONNECT EXPOSED PAD (EP) TO GND.*

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*For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.*

**MAX4969**

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

$V_{CC}$....................................................................-0.3V to +4.0V
All Other Pins (Note 1) ............................ -0.3V to ($V_{CC}$ + 0.3V)
Continuous Current, IN_P, IN_M, OUT_P, OUT_M ........ ±30mA
Peak Current, IN_P, IN_M, OUT_P,
   OUT_M (for 10kHz, 1% duty cycle) ......................... ±100mA
Continuous Power Dissipation ($T_A$ = +70°C)
   42-Pin TQFN (derate 34.5mW/°C above +70°C) ......2758mW

Junction-to-Case Thermal Resistance
   $\theta_{JC}$ (Note 2) ............................................................... +2°C/W
Junction-to-Ambient Thermal Resistance
   $\theta_{JA}$ (Note 2) ........................................................... +29°C/W
Operating Temperature Range ........................... 0°C to +70°C
Junction Temperature Range.......................... -40°C to +150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ...............................+300°C

**Note 1:** All I/O pins are clamped by internal diodes.
**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 75nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = 0°C to +70°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | | |
| Power-Supply Range | $V_{CC}$ | | | 3.0 | | 3.6 | V |
| Supply Current | $I_{CC}$ | EN = $V_{CC}$ | INEQ_ = ODE_ = GND | | 120 | 150 | mA |
| | | | INEQ_ = ODE_ = $V_{CC}$ | | 160 | 200 | |
| | | EN = GND | | | 50 | | |
| Input Impedance, Differential | $Z_{RX-DIFF-DC}$ | DC | | 80 | 100 | 120 | Ω |
| Output Impedance, Differential | $Z_{TX-DIFF-DC}$ | DC | | 80 | 100 | 120 | Ω |
| Common-Mode Resistance to GND, Input Terminations Not Powered | $Z_{RX-HIGH-IMP-DC-POS}$ | $V_{IN\_P}$ = $V_{IN\_M}$ = 0 to 200mV | | 50 | | | kΩ |
| | $Z_{RX-HIGH-IMP-DC-NEG}$ | $V_{IN\_P}$ = $V_{IN\_M}$ = -150mV to 0V | | 1 | | | kΩ |
| Common-Mode Resistance to GND, Input Terminations Powered | $Z_{RX-DC}$ | DC | | 40 | 50 | 60 | Ω |
| Output Short-Circuit Current | $I_{TX-SHORT}$ | Single-ended (Note 4) | | | | 90 | mA |
| Common-Mode Delta, Between Active and Idle States | $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | | | -100 | | +100 | mV |
| DC Output Offset, During Active State | $V_{TX-CM-DC-LINE-DELTA}$ | Difference between DC average of $V_{OUT\_P}$ and $V_{OUT\_M}$ | | -25 | | +25 | mV |
| DC Output Offset, During Electrical Idle | $V_{TX-IDLE-DIFF-DC}$ | ABS($V_{OUT\_P}$ - $V_{OUT\_M}$) | | -10 | | +10 | mV |
| **AC PERFORMANCE** | | | | | | | |
| Input Return Loss, Differential | $RL_{RX-DIFF}$ | 0.05GHz < f ≤ 1.25GHz (Note 4) | | 10 | | | dB |
| | | 1.25GHz < f ≤ 2.5GHz (Note 4) | | 8 | | | dB |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 75nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = 0°C to +70°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Return Loss, Common Mode | $RL_{RX-CM}$ | 0.05GHz < f ≤ 2.5GHz (Note 4) | 6 | | | dB |
| Output Return Loss, Differential | $RL_{TX-DIFF}$ | 0.05GHz < f ≤ 1.25GHz (Note 4) | 10 | | | dB |
| | | 1.25GHz < f ≤ 2.5GHz (Note 4) | 8 | | | dB |
| Output Return Loss, Common Mode | $RL_{TX-CM}$ | 0.05GHz < f ≤ 2.5GHz (Note 4) | 6 | | | dB |
| Differential Input Signal Range, Redriver Operation | $V_{RX-DIFF-PP}$ | 0.05GHz < f ≤ 2.5GHz | 150 | | 1200 | mV$_{P-P}$ |
| Differential Output Voltage, Full Swing, No Deemphasis | $V_{TX-DIFF-PP}$ | 2 x ABS($V_{OUT\_P}$ - $V_{OUT\_M}$), ODE_1 = GND, ODE_0 = $V_{CC}$ (see Table 1), f = 500MHz | 800 | 1000 | 1200 | mV$_{P-P}$ |
| Differential Output Voltage, Low Swing, No Deemphasis | $V_{TX-DIFF-PP-LOW}$ | 2 x ABS($V_{OUT\_P}$ - $V_{OUT\_M}$), ODE_1 = ODE_0 = GND (see Table 1), f = 500MHz | 600 | 750 | 900 | mV$_{P-P}$ |
| Output Deemphasis Ratio, 0dB | $V_{TX-DE-RATIO-0dB}$ | f = 2.5GHz, ODE_1 = GND, ODE_0 = $V_{CC}$ or GND, Figure 1 (see Table 1) | | 0 | | dB |
| Output Deemphasis Ratio, 3.5dB | $V_{TX-DE-RATIO-3.5dB}$ | f = 2.5GHz, ODE_1 = $V_{CC}$, ODE_0 = GND, Figure 1 (see Table 1) | | 3.5 | | dB |
| Output Deemphasis Ratio, 6dB | $V_{TX-DE-RATIO-6dB}$ | f = 2.5GHz, ODE_1 = $V_{CC}$, ODE_0 = $V_{CC}$, Figure 1 (see Table 1) | | 6 | | dB |
| Input Equalization, 0dB | $V_{RX-EQ-0dB}$ | f = 2.5GHz, INEQ_1 = GND, INEQ_0 = GND or $V_{CC}$ (see Table 2) | | 0 | | dB |
| Input Equalization, 3.5dB | $V_{RX-EQ-3.5dB}$ | f = 2.5GHz, INEQ_1 = $V_{CC}$, INEQ_0 = GND (see Table 2) | | 3.5 | | dB |
| Input Equalization, 6dB | $V_{RX-EQ-6dB}$ | f = 2.5GHz, INEQ_1 = $V_{CC}$, INEQ_0 = $V_{CC}$ (see Table 2) | | 6 | | dB |
| Output Common-Mode Voltage | $V_{TX-CM-AC-PP}$ | MAX($V_{OUT\_P}$ + $V_{OUT\_M}$)/2 - MIN($V_{OUT\_P}$ + $V_{OUT\_M}$)/2 (Note 4) | | | 100 | mV$_{P-P}$ |
| Propagation Delay | $T_{PD}$ | (Note 4) | 160 | 280 | 400 | ps |
| Rise/Fall Time | $T_{TX-RISE-FALL}$ | (Notes 4, 5) | 30 | | | ps |
| Rise/Fall Time Mismatch | $T_{TX-RF-MISMATCH}$ | (Notes 4, 5) | | | 20 | ps |
| Output Skew Same Pair | $T_{SK}$ | (Note 4) | | 10 | 15 | ps |
| Deterministic Jitter | $T_{TX-DJ-DD}$ | K28.5 ≤ pattern, AC-coupled, $R_L$ = 50Ω, effects of deemphasis deembedded (Note 4), 5GT/s | | 20 | | ps$_{P-P}$ |
| Random Jitter | $T_{TX-RJ-DD}$ | D10.2 pattern, f > 1.5MHz | | 0.5 | 1.4 | ps$_{RMS}$ |
| Electrical Idle Entry Delay | $T_{TX-IDLE-SET-TO-IDLE}$ | From input to output | | 15 | | ns |
| Electrical Idle Exit Delay | $T_{TX-IDLE-TO-DIFF-DATA}$ | From input to output | | 8 | | ns |

**MAX4969**

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 75nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = 0°C to +70°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Electrical Idle Detect Threshold | $V_{TX-IDLE-THRESH}$ | | 65 | 100 | 120 | $mV_{P-P}$ |
| Output Voltage During Electrical Idle (AC) | $V_{TX-IDLE-DIFF-AC-P}$ | ABS($V_{OUT\_P}$ - $V_{OUT\_M}$) | | | 35 | $mV_{P-P}$ |
| Receiver Detect Pulse Amplitude | $V_{TX-RCV-DETECT}$ | Voltage change in positive direction (Note 4) | | | 600 | mV |
| Receiver Detect Pulse Width | | | | 100 | | ns |
| Receiver Detect Retry Period | | | | 200 | | ns |
| **CONTROL LOGIC** | | | | | | |
| Input Logic-Level Low | $V_{IL}$ | | | | 0.6 | V |
| Input Logic-Level High | $V_{IH}$ | | 1.4 | | | V |
| Input Logic Hysteresis | $V_{HYST}$ | | | 130 | | mV |
| Input Pulldown Resistor | $R_{DOWN}$ | | 37.5 | 60 | 150 | kΩ |

**Note 3:** All devices are 100% production tested at $T_A$ = +70°C. Specifications for all temperature limits are guaranteed by design.
**Note 4:** Guaranteed by design.
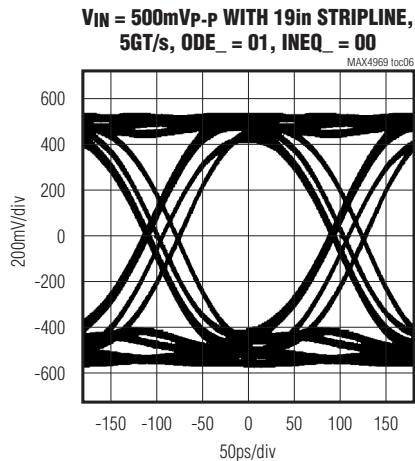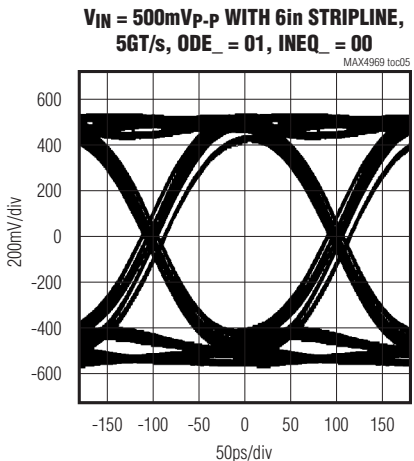**Note 5:** Rise and fall times are measured using 20% and 80% levels.
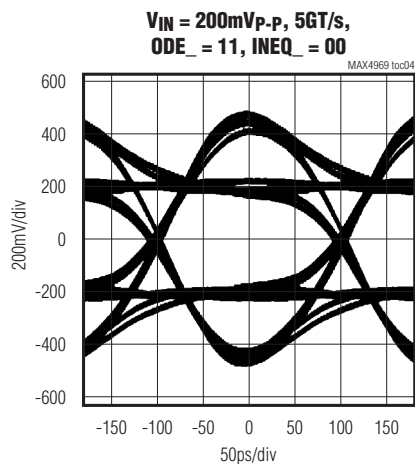
## Timing Diagram



$$DE(dB) = 20 \left[ \log \left( \frac{V_{HIGH\_P-P}}{V_{LOW\_P-P}} \right) \right]$$
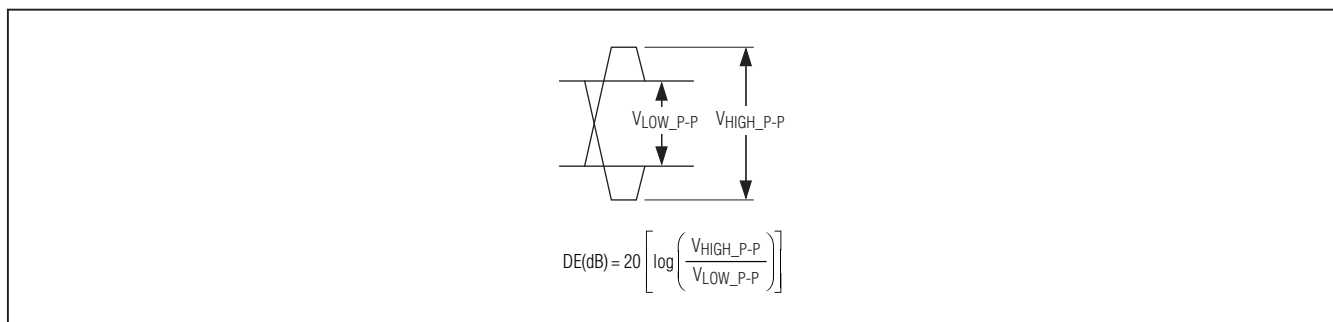
*Figure 1. Illustration of Output Deemphasis*

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**MAX4969**

## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)
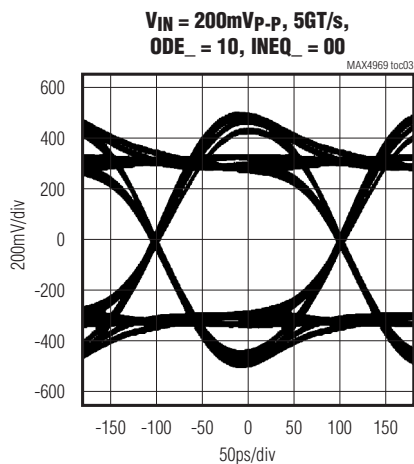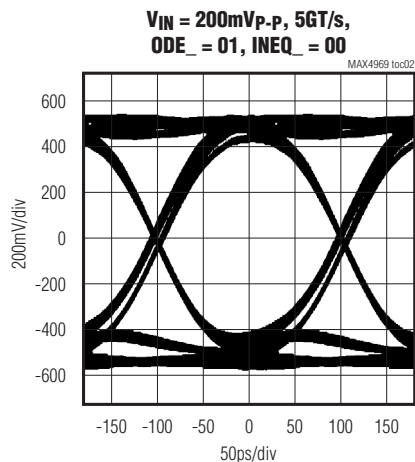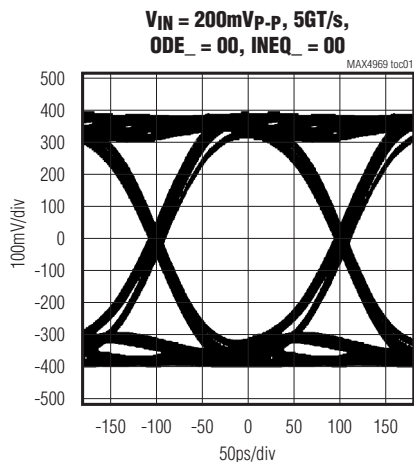


$V_{IN}$ = 200mV$_{P-P}$, 5GT/s, ODE_ = 00, INEQ_ = 00
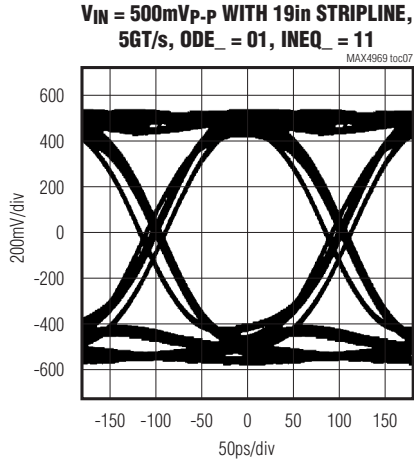
MAX4969 toc01



$V_{IN}$ = 200mV$_{P-P}$, 5GT/s, ODE_ = 01, INEQ_ = 00

MAX4969 toc02



$V_{IN}$ = 200mV$_{P-P}$, 5GT/s, ODE_ = 10, INEQ_ = 00

MAX4969 toc03



$V_{IN}$ = 200mV$_{P-P}$, 5GT/s, ODE_ = 11, INEQ_ = 00

MAX4969 toc04



$V_{IN}$ = 500mV$_{P-P}$ WITH 6in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 00

MAX4969 toc05



$V_{IN}$ = 500mV$_{P-P}$ WITH 19in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 00

MAX4969 toc06

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MAX4969

## Typical Operating Characteristics (continued)

(V_CC = +3.3V, T_A = +25°C, unless otherwise noted.)
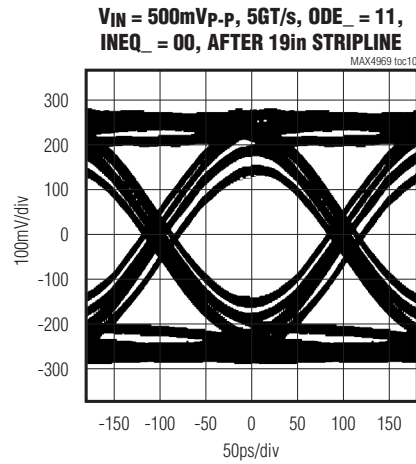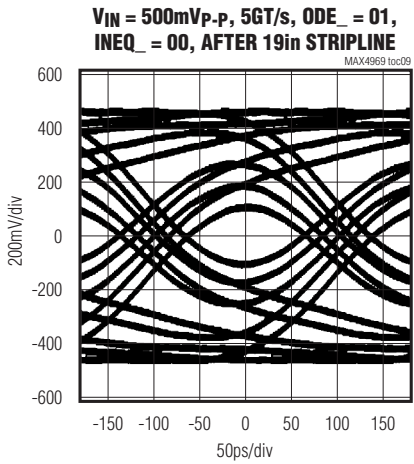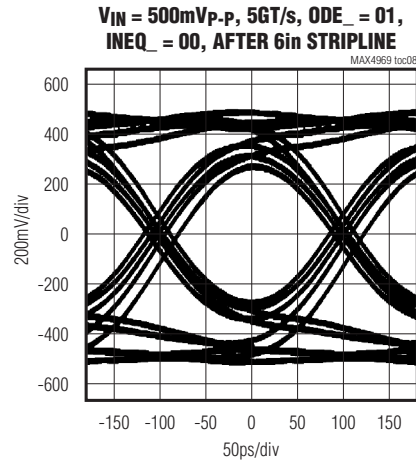
**V_IN = 500mV_P-P WITH 19in STRIPLINE, 5GT/s, ODE_ = 01, INEQ_ = 11**

MAX4969 toc07

**V_IN = 500mV_P-P, 5GT/s, ODE_ = 01, INEQ_ = 00, AFTER 6in STRIPLINE**

MAX4969 toc08

**V_IN = 500mV_P-P, 5GT/s, ODE_ = 01, INEQ_ = 00, AFTER 19in STRIPLINE**

MAX4969 toc09

**V_IN = 500mV_P-P, 5GT/s, ODE_ = 11, INEQ_ = 00, AFTER 19in STRIPLINE**

MAX4969 toc10

***MAXIM***
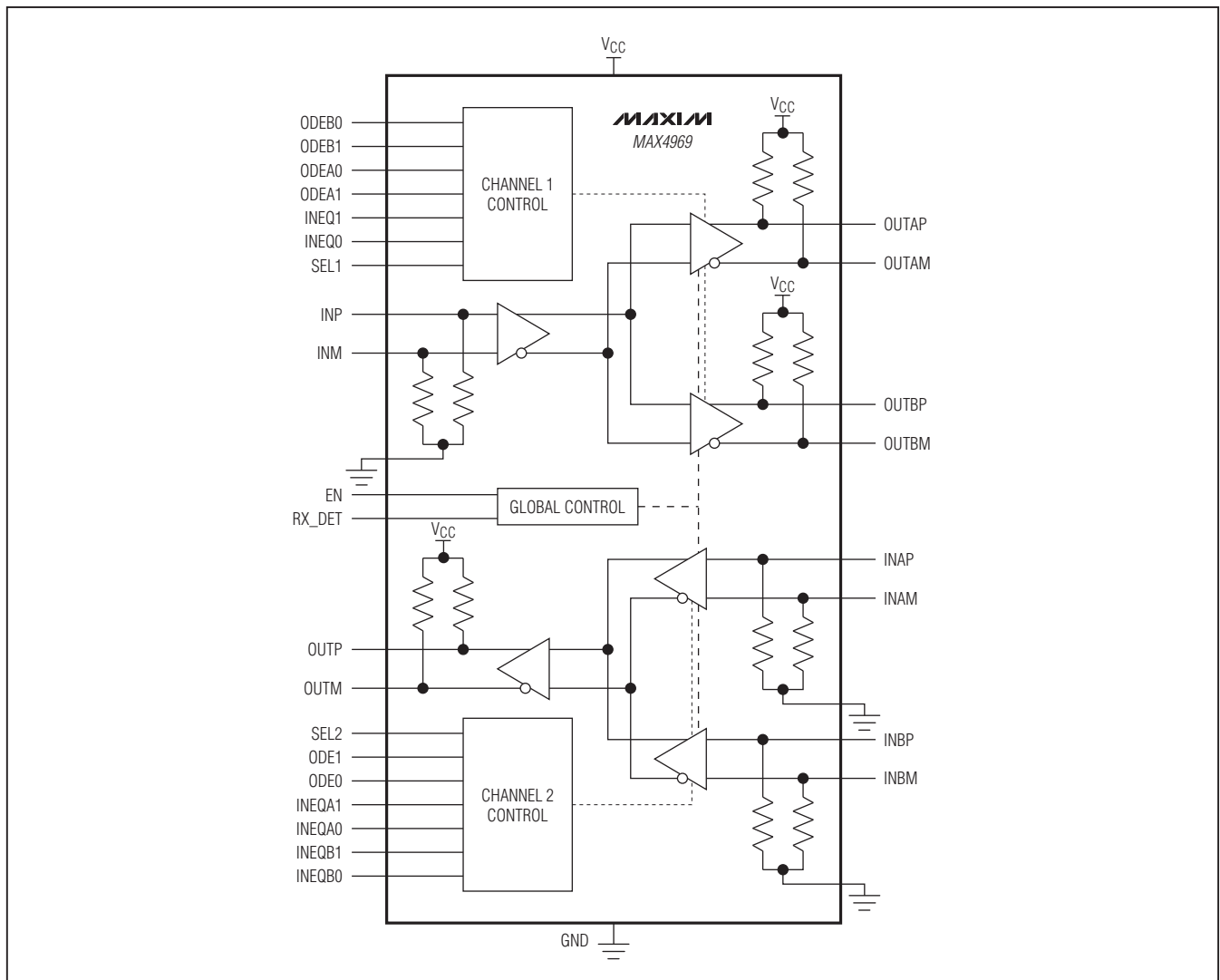
MAX4969

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1, 17, 22, 38 | V<sub>CC</sub> | Power-Supply Input. Bypass V$_{CC}$ to GND with 1µF and 0.01µF capacitors in parallel as close to the device as possible, recommended on each V$_{CC}$ pin. |
| 2 | INEQ1 | Channel 1 Input Equalization Control MSB. See Table 2. INEQ1 is internally pulled down by a 60kΩ (typ) resistor. |
| 3 | INEQ0 | Channel 1 Input Equalization Control LSB. See Table 2. INEQ0 is internally pulled down by a 60kΩ (typ) resistor. |
| 4, 7, 11, 14, 23, 26, 29, 31, 34, 37 | GND | Ground |
| 5 | INP | Channel 1 Noninverting Input |
| 6 | INM | Channel 1 Inverting Input |
| 8 | SEL1 | Channel 1 Active Output Selection Input. Drive SEL1 low to activate A outputs. Drive SEL high to activate B outputs. SEL1 is internally pulled down by a 60kΩ (typ) resistor. |
| 9 | SEL2 | Channel 2 Active Input Selection Input. Drive SEL2 low to activate A inputs. Drive SEL high to activate B inputs. SEL2 is internally pulled down by a 60kΩ (typ) resistor. |
| 10 | EN | Enable Input. Drive EN low for reduced power standby mode. Drive EN high for normal operation. EN is internally pulled down by a 60kΩ (typ) resistor. |
| 12 | OUTP | Channel 2 Noninverting Output |
| 13 | OUTM | Channel 2 Inverting Output |
| 15 | ODE1 | Channel 2 Output Deemphasis Control MSB. See Table 1. ODE1 is internally pulled down by a 60kΩ (typ) resistor. |
| 16 | ODE0 | Channel 2 Output Deemphasis Control LSB. See Table 1. ODE0 is internally pulled down by a 60kΩ (typ) resistor. |
| 18 | INEQA1 | Channel 2 Input A Equalization Control MSB. See Table 2. INEQA1 is internally pulled down by a 60kΩ (typ) resistor. |
| 19 | INEQA0 | Channel 2 Input A Equalization Control LSB. See Table 2. INEQA0 is internally pulled down by a 60kΩ (typ) resistor. |
| 20 | INEQB1 | Channel 2 Input B Equalization Control MSB. See Table 2. INEQB1 is internally pulled down by a 60kΩ (typ) resistor. |
| 21 | INEQB0 | Channel 2 Input B Equalization Control LSB. See Table 2. INEQB0 is internally pulled down by a 60kΩ (typ) resistor. |
| 24 | INBM | Channel 2 Inverting Input B |
| 25 | INBP | Channel 2 Noninverting Input B |
| 27 | INAM | Channel 2 Inverting Input A |
| 28 | INAP | Channel 2 Noninverting Input A |
| 30 | RX_DET | Receiver Detection Control Bit. Toggle RX_DET to initiate receiver detection. RX_DET is internally pulled down by a 60kΩ (typ) resistor. |
| 32 | OUTBM | Channel 1 Inverting Output B |
| 33 | OUTBP | Channel 1 Noninverting Output B |
| 35 | OUTAM | Channel 1 Inverting Output A |
| 36 | OUTAP | Channel 1 Noninverting Output A |
| 39 | ODEB0 | Channel 1 Output B Deemphasis Control LSB. See Table 1. ODEB0 is internally pulled down by a 60kΩ (typ) resistor. |

**MAXIM**

**MAX4969**

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 40 | ODEB1 | Channel 1 Output B Deemphasis Control MSB. See Table 1. ODEB1 is internally pulled down by a 60kΩ (typ) resistor. |
| 41 | ODEA0 | Channel 1 Output A Deemphasis Control LSB. See Table 1. ODEA0 is internally pulled down by a 60kΩ (typ) resistor. |
| 42 | ODEA1 | Channel 1 Output A Deemphasis Control MSB. See Table 1. ODEA1 is internally pulled down by a 60kΩ (typ) resistor. |
| — | EP | Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. EP is not intended as an electrical connection point. |

*Functional Diagram*

***MAXIM***

# PCIe, Single Lane, 2:1/1:2 Multiplexer and Redriver with Equalization

## Detailed Description

The MAX4969 is an active 2:1/1:2 multiplexer designed to equalize and redrive PCIe signals up to 5.0GT/s. The MAX4969 features PCIe-required electrical idle and receiver detection on each channel, and improves signal integrity at the receiver through independent programmable input equalization and output deemphasis.

### Enable Input (EN)

The MAX4969 features an active-high enable input (EN). EN has an internal pulldown resistor of 60kΩ (typ). When EN is driven low or left unconnected, the MAX4969 enters reduced power standby mode and the redrivers are disabled. Drive EN high for normal operation.

### Active Input/Output Select (SEL1, SEL2)

SEL1 selects the active output for channel 1 and SEL2 selects the active input for channel 2. Drive SEL1 or SEL2 low or leave unconnected to activate A inputs or outputs. Drive SEL1 or SEL2 high to activate B inputs or outputs. SEL1 and SEL2 have internal pulldown resistors of 60kΩ (typ).

## Table 1. Output Deemphasis

| ODE_1 | ODE_0 | OUTPUT DEEMPHASIS (dB) |
|-------|-------|------------------------|
| 0 | 0 | 0, low swing |
| 0 | 1 | 0, full swing |
| 1 | 0 | 3.5, full swing |
| 1 | 1 | 6, full swing |

## Table 2. Input Equalization

| INEQ_1 | INEQ_0 | INPUT EQUALIZATION (dB) |
|--------|--------|-------------------------|
| 0 | X | 0 |
| 1 | 0 | 3.5 |
| 1 | 1 | 6 |

*X = Don't Care*

### Programmable Output Deemphasis (ODE_0, ODE_1)

The MAX4969 features independent programmable output deemphasis capable of providing 0dB, 3.5dB, or 6dB deemphasis on any channel. When both ODE_0 and ODE_1 are driven low or left unconnected, the output is in low-swing mode (750mV typ) (see Table 1). ODE0, ODE1, ODEA0, ODEA1, ODEB0, and ODEB1 have internal pulldown resistors of 60kΩ (typ).

### Programmable Input Equalization (INEQ_0, INEQ_1)

The MAX4969 features independent programmable input equalization capable of providing 0dB, 3.5dB, or 6dB of high-frequency equalization on any channel (see Table 2.) INEQ0, INEQ1, INEQA0, INEQA1, INEQB0, and INEQB1 have internal pulldown resistors of 60kΩ (typ).

### Receiver Detection (RX_DET)

The MAX4969 features receiver detection on each channel. Receiver detection initializes on the rising edge of EN, or upon initial power-up if EN is high. Receiver detection can also be initiated on a rising or falling edge of the RX_DET, SEL1, or SEL2 inputs when EN is high. During this time, the part remains in reduced power standby mode and the outputs are squelched, despite the logic-high state of EN. Once started, receiver detection repeats indefinitely on each channel. Once a receiver is detected on one of the channels, up to $2^{16}$ more attempts are made on the other channel. Upon receiver detection, channel output and electrical idle detection are enabled (see Table 3). RX_DET has an internal pulldown resistor of 60kΩ (typ).

### Electrical Idle Detection

The MAX4969 features electrical idle detection to prevent unwanted noise from being redriven at the output. If the MAX4969 detects that the differential input has fallen below $V_{TX\text{-}IDLE\text{-}THRESH}$, the MAX4969 squelches the output. For differential input signals that are above $V_{TX\text{-}IDLE\text{-}THRESH}$, the MAX4969 turns on the output and redrives the signal.

## Table 3. Receiver Detection

| RX_DET/ SEL1/SEL2 | EN | DESCRIPTION |
|-------------------|----|-------------|
| X | 0 | Receiver detection inactive |
| 0 | 1 | Following a rising or falling edge; indefinite retry until receiver detected |
| Rising or falling edge | 1 | Initiate receiver detection |
| 1 | 1 | Following a rising or falling edge; indefinite retry until receiver detected |

*X = Don't Care*

# PCIe, Single Lane, 2:1/1:2 Multiplexer and Redriver with Equalization

## Typical Application Circuit
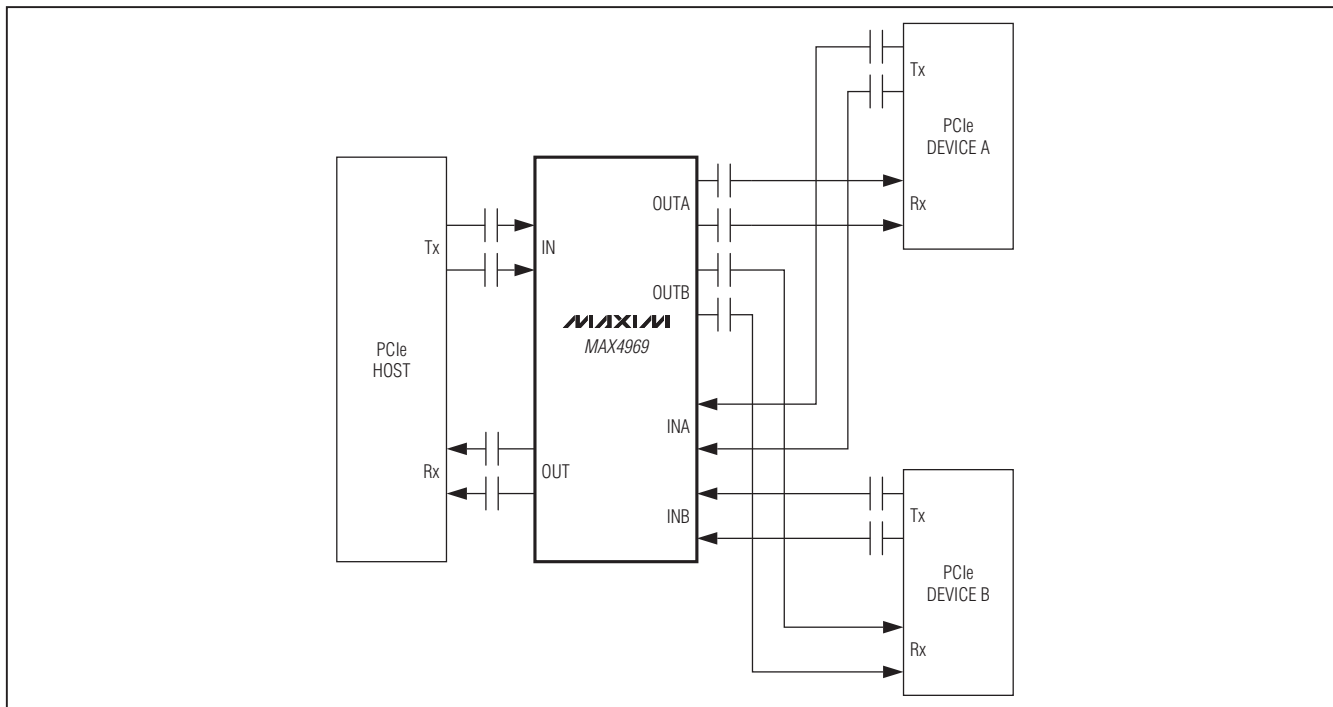


## Applications Information

### Layout

Circuit board layout and design can significantly affect the performance of the MAX4969. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. It is recommended to run receive and transmit on different layers to minimize crosstalk and to place 1µF and 0.01µF power-supply bypass capacitors in parallel as close to $V_{CC}$ as possible on each $V_{CC}$ pin. Always connect $V_{CC}$ to a power plane.

### Exposed Pad Package

The exposed-pad, 42-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX4969 must be soldered to the circuit board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

## Power-Supply Sequencing

**Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.**

Proper power-supply sequencing is recommended for all devices. Always apply GND then $V_{CC}$ before applying signals, especially if the signal is not current limited.

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 42 TQFN-EP | T423590+1 | **21-0181** |