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19-1587; Rev 0; 11/99

Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

General Description

The MAX5104 low-power, serial, voltage-output, dual 12-bit digital-to-analog converter (DAC) consumes only 500µA from a single +5V supply. This device features Rail-to-Rail® output swing and is available in a space-saving 16-pin QSOP package. To maximize the dynamic range, the DAC output amplifiers are configured with an internal gain of +2V/V.

The 3-wire serial interface is SPI™/QSPI™/MICROWIRE™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include programmable power-down (2µA), hardware power-down lockout (PDL), a separate reference voltage input for each DAC that accepts AC and DC signals, and an active-low clear input (CL) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality, and a serial-data output pin for daisy chaining.

Applications

Industrial Process Control

Remote Industrial Controls

Digital Offset and Gain Adjustment

Microprocessor-Controlled Systems

Motion Control

Automatic Test Equipment (ATE)

Features

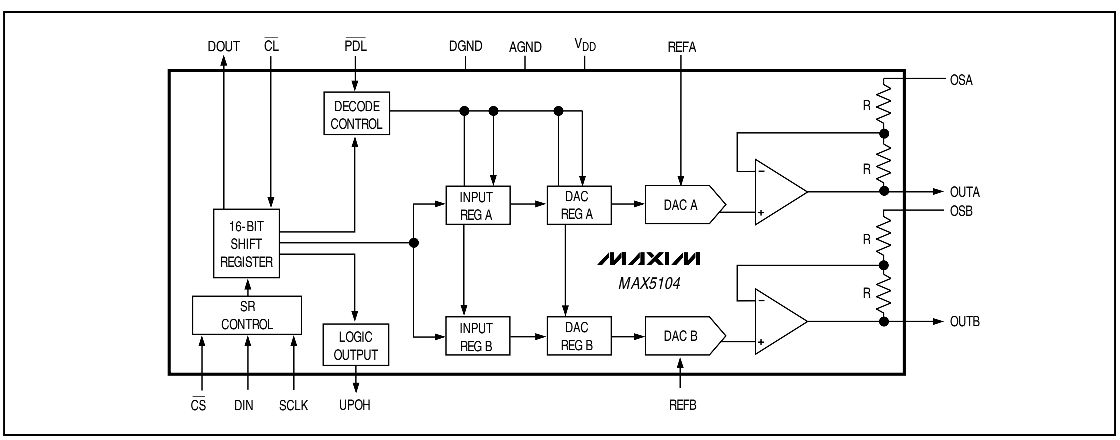
- ♦ **12-Bit Dual DAC with Internal Gain of +2V/V**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **12µs Settling Time**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Quiescent Current**
  - **500µA (normal operation)**
  - **2µA (power-down mode)**
- ♦ **SPI/QSPI/MICROWIRE Compatible**
- ♦ **Space-Saving 16-Pin QSOP Package**
- ♦ **Power-On Reset Clears Registers and DACs to Zero**
- ♦ **Adjustable Output Offset**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5104CEE	0°C to +70°C	16 QSOP	±4
MAX5104EEE	-40°C to +85°C	16 QSOP	±4

Pin Configuration appears at end of data sheet.

Functional Diagram



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SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ... -0.3V to +6V
V_{DD} to DGND ... -0.3V to +6V
AGND to DGND ... ±0.3V
OSA, OSB to AGND ... (V_{AGND} - 4V) to (V_{DD} + 0.3V)
REF_, OUT_ to AGND ... -0.3V to (V_{DD} + 0.3V)
Digital Inputs (SCLK, DIN, $\overline{CS}$, $\overline{CL}$, $\overline{PDL}$) to DGND ... (-0.3V to +6V)
Digital Outputs (DOUT, UPO) to DGND ... -0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin ... ±20mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.30mW/°C above +70°C) ... 667mW
Operating Temperature Ranges
MAX5104CEE ... 0°C to +70°C
MAX5104EEE ... -40C° to +85°C
Junction Temperature ... +150°C
Storage Temperature Range ... -65°C to +150°C
Lead Temperature (soldering, 10sec) ... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = +2.048V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C (OS_ connected to AGND for a gain of +2V/V).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			12			Bits
Integral Nonlinearity	INL	(Note 1)			±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error	V_{OS}	Code = 10			±10	mV
Offset Tempco	TCV_{OS}	Normalized to 2.048V		4		ppm/°C
Gain Error				-0.2	±8	LSB
Gain-Error Tempco		Normalized to 2.048V		4		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		20	600	µV/V
REFERENCE INPUT						
Reference Input Range	REF		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1554 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference 3dB Bandwidth		Input code = 1FFE hex, $V_{REF\_}$ = 0.67Vp-p at 2.5V_{DC}		300		kHz
Reference Feedthrough		Input code = 0000 hex, $V_{REF\_}$ = (V_{DD} - 1.4Vp-p), f = 1kHz		-82		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FFE hex, $V_{REF\_}$ = 1Vp-p at 1.25V_{DC}, f = 25kHz		75		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK	3			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK			0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 to V_{DD}		0.001	±1	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = +2.048V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C (OS_ connected to AGND for a gain of +2V/V).)

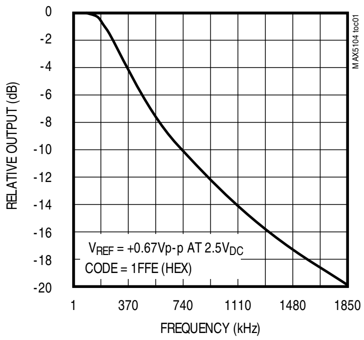
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (DOUT, UPO)						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.40	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 4V		15		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
OSA or OSB Input Resistance	$R_{OS\_}$		24	34		kΩ
Time Required to Exit Shutdown				25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, SCLK = 100kHz, V_{SCLK} = 5Vp-p		5		nVs
Digital Crosstalk				5		nVs
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current	I_{DD}	(Note 3)		0.5	0.65	mA
Power-Supply Current in Shutdown	$I_{DD(SHDN)}$	(Note 3)		2	10	µA
Reference Current in Shutdown				0	±1	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}	(Note 4)	100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		40			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Accuracy is specified from code 6 to code 4095.
Note 2: Accuracy is better than 1LSB for $V_{OUT\_}$ greater than 6mV and less than V_{DD} - 50mV. Guaranteed by PSRR test at the end points.
Note 3: Digital inputs are set to either V_{DD} or DGND, code = 0000 hex, R_L = ∞.
Note 4: SCLK minimum clock period includes the rise and fall times.

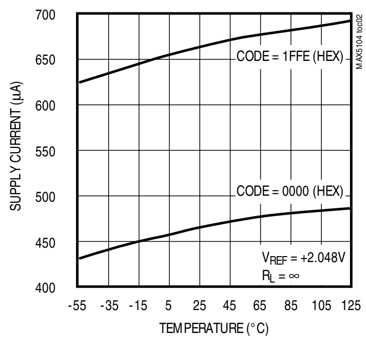
Typical Operating Characteristics

(V_{DD} = +5V, R_L = 10kΩ, C_L = 100pF, OS_ pins connected to AGND, T_A = +25°C, unless otherwise noted.)

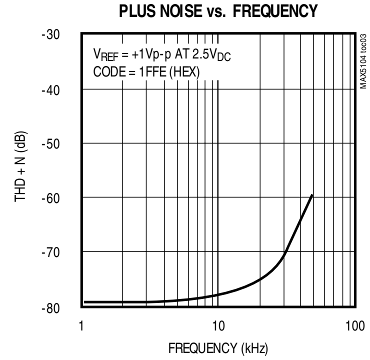
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



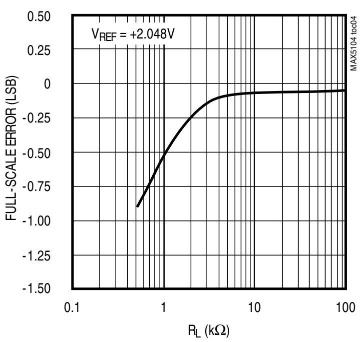
SUPPLY CURRENT vs. TEMPERATURE



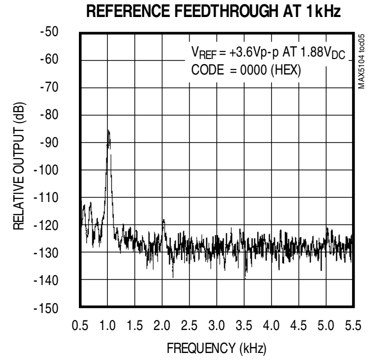
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



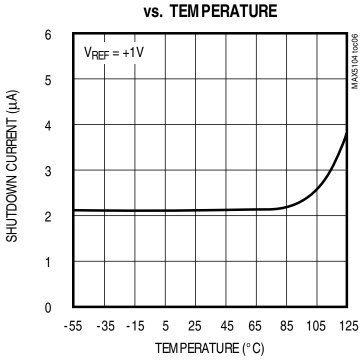
FULL-SCALE ERROR vs. RESISTIVE LOAD



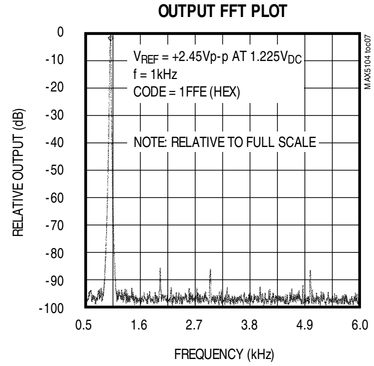
REFERENCE FEEDTHROUGH AT 1kHz



SHUTDOWN CURRENT vs. TEMPERATURE



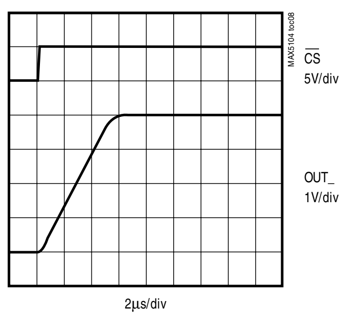
OUTPUT FFT PLOT



Typical Operating Characteristics (continued)

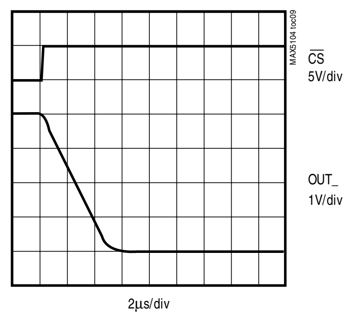
(V_{DD} = +5V, R_L = 10kΩ, C_L = 100pF, OS_ pins connected to AGND, T_A = +25°C, unless otherwise noted.)

DYNAMIC RESPONSE RISE TIME



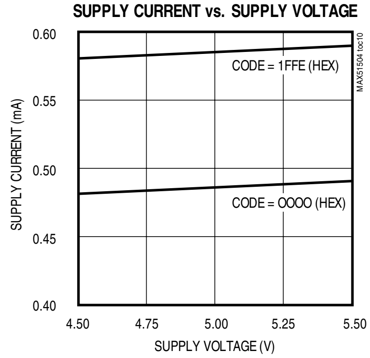
V_{REF} = +2.048V

DYNAMIC RESPONSE FALL TIME

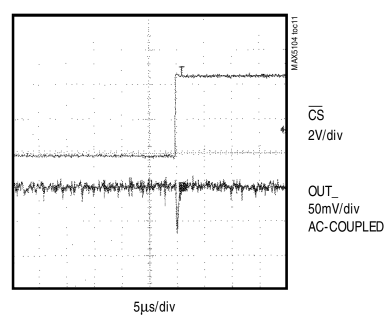


V_{REF} = +2.048V

SUPPLY CURRENT vs. SUPPLY VOLTAGE

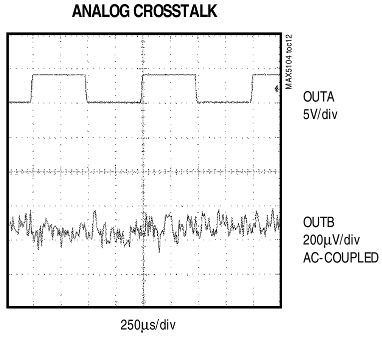


MAJOR-CARRY TRANSITION



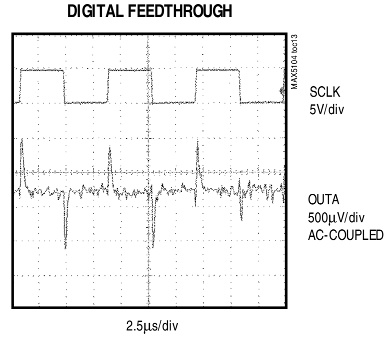
TRANSITION FROM 1000 (HEX) TO 0FFE (HEX)

ANALOG CROSSTALK



V_{REF} = +2.048V, GAIN = +2V/V, CODE = 1FFE HEX

DIGITAL FEEDTHROUGH



Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	OUTA	DAC A Output Voltage
3	OSA	DAC A Offset Adjustment
4	REFA	Reference for DAC A
5	$\overline{CL}$	Active-Low Clear Input. Resets all registers to zero. DAC outputs go to 0V.
6	$\overline{CS}$	Chip-Select Input
7	DIN	Serial-Data Input
8	SCLK	Serial-Clock Input
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output
12	$\overline{PDL}$	Power-Down Lockout. The device cannot be powered down when $\overline{PDL}$ is low.
13	REFB	Reference for DAC B
14	OSB	DAC B Offset Adjustment
15	OUTB	DAC B Output Voltage
16	V_{DD}	Positive Power Supply

Detailed Description

The MAX5104 dual, 12-bit, voltage-output DAC is easily configured with a 3-wire serial interface. The device includes a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, trimmed internal resistors produce an internal gain of +2V/V that maximizes output voltage swing. The amplifier's offset-adjust pin allows for a DC shift in the DAC's output.

Both DACs use an inverted R-2R ladder network that produces a weighted voltage proportional to the input voltage value. Each DAC has its own reference input to facilitate independent full-scale values. Figure 1 depicts a simplified circuit diagram of one of the two DACs.

Reference Inputs

The reference inputs accept both AC and DC values with a voltage range extending from 0 to (V_{DD} - 1.4V).

Determine the output voltage using the following equation (OS_ = AGND):

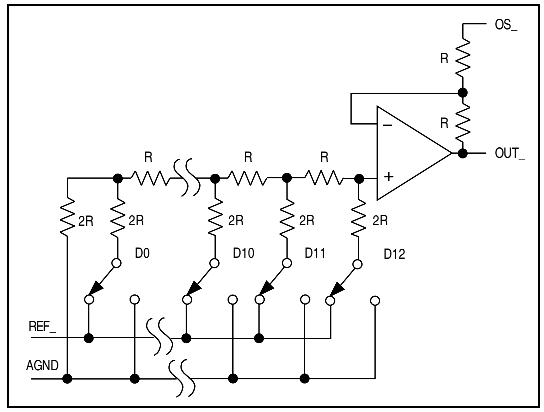


Figure 1. Simplified DAC Circuit Diagram

$$V_{OUT} = (V_{REF} \cdot NB / 4096) \cdot 2$$

where NB is the numeric value of the DAC's binary input code (0 to 4095) and V_{REF} is the reference voltage.

The reference input impedance ranges from 14kΩ (1554 hex) to several gigohms (with an input code of 0000 hex). The reference input capacitance is code dependent and typically ranges from 15pF with an input code of all zeros to 50pF with a full-scale input code.

Output Amplifier

The MAX5104's output amplifiers have internal resistors that provide for a gain of +2V/V when OS_ is connected to AGND. These resistors are trimmed to minimize gain error. The output amplifiers have a typical slew rate of 0.75V/µs and settle to 1/2LSB within 15µs, with a load of 10kΩ in parallel with 100pF. Loads less than 2kΩ degrade performance.

The OS_ pin can be used to produce an adjustable offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to the OS_ pin to produce an output range from 1V to (1V + $V_{REF} \cdot 2$). Note that the DAC's output range is still limited by the maximum output voltage specification.

Power-Down Mode

The MAX5104 features a software-programmable shutdown mode that reduces the typical supply current to 2µA. The two DACs can be powered down independently, or simultaneously using the appropriate programming command. Enter power-down mode by writing the appropriate input-control word (Table 1). In power-down mode, the reference inputs and amplifier outputs become high impedance, and the serial interface remains active. Data in the input registers is saved,

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A0	C1	C0	D11......................D0 (MSB) (LSB)	S0	
0	0	1	12-bit DAC data	0	Load input register A; DAC registers are unchanged.
1	0	1	12-bit DAC data	0	Load input register B; DAC registers are unchanged.
0	1	0	12-bit DAC data	0	Load input register A; all DAC registers are updated.
1	1	0	12-bit DAC data	0	Load input register B; all DAC registers are updated.
0	1	1	12-bit DAC data	0	Load all DAC registers from the shift register (start up both DACs with new data).
1	0	0	XXXXXXXXXXXX	0	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1	1	1	XXXXXXXXXXXX	0	Shut down both DACs (provided $\overline{PDL}$ = 1).
0	0	0	0 0 1 X XXXXXXXX	0	Update DAC register A from input register A (start up DAC A with data previously stored in input register A).
0	0	0	1 0 1 X XXXXXXXX	0	Update DAC register B from input register B (start up DAC B with data previously stored in input register B).
0	0	0	1 1 0 X XXXXXXXX	0	Power Down DAC A (provided $\overline{PDL}$ = 1).
0	0	0	1 1 1 X XXXXXXXX	0	Power Down DAC B (provided $\overline{PDL}$ = 1).
0	0	0	0 1 0 X XXXXXXXX	0	UPO goes low (default).
0	0	0	0 1 1 X XXXXXXXX	0	UPO goes high.
0	0	0	1 0 0 1 XXXXXXXX	0	Mode 1, DOUT clocked out on SCLK's rising edge.
0	0	0	1 0 0 0 XXXXXXXX	0	Mode 0, DOUT clocked out on SCLK's falling edge (default).
0	0	0	0 0 0 X XXXXXXXX	0	No operation (NOP).

X = Don't care

Note: *D11, D10, D9, and D8 become control bits when A0, C1, and C0 = 0. S0 is a sub-bit, always zero.*

allowing the MAX5104 to recall the output state prior to entering power-down when returning to normal mode. Exit power-down by recalling the previous condition or by updating the DAC with new information. When returning to normal operation (exiting power-down), wait 20µs for output stabilization.

Serial Interface

The MAX5104's 3-wire serial interface is compatible with both MICROWIRE (Figure 2) and SPI/QSPI (Figure 3) serial-interface standards. The 16-bit serial input word consists of 1 address bit, 2 control bits, 12 bits of data (MSB to LSB), and 1 sub-bit as shown in Figure 4. The address and control bits determine the MAX5104's response, as outlined in Table 1.

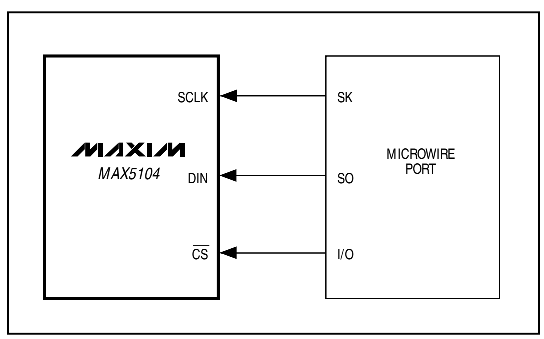


Figure 2. Connections for MICROWIRE

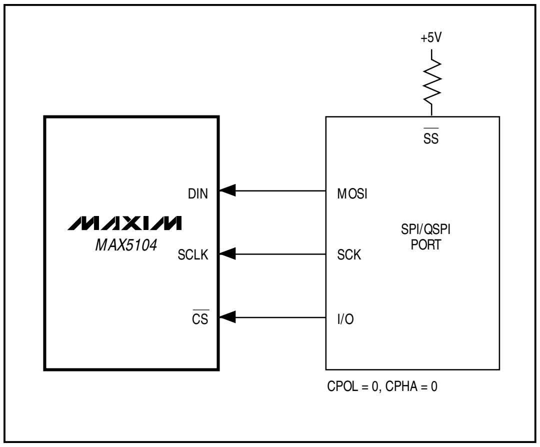


Figure 3. Connections for SPI/QSPI

MSB...LSB			
← 16 Bits of Serial Data →			
Address Bits	Control Bits	MSB...Data Bits...LSB	Sub Bit
A0	C1, C0	D11.......................D0	S0
← 1 Address/2 Control Bits →		← 12 Data Bits →	0

Figure 4. Serial-Data Format

The MAX5104's digital inputs are double buffered, which allows any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC registers concurrently. The address and control bits allow the DACs to act independently. Send the 16-bit data as one 16-bit word (QSPI) or two 8-bit packets (SPI, MICROWIRE), with $\overline{CS}$ low during this period. The address and control bits determine which register will be updated, and the state of the registers when exiting power-down. The 3-bit address/control determines the following:

- Registers to be updated
- Clock edge on which data is to be clocked out via the serial-data output (DOUT)
- State of the user-programmable logic output
- Configuration of the device after power-down

The general timing diagram of Figure 5 illustrates how data is acquired. Driving $\overline{CS}$ low enables the device to receive data; otherwise, the interface control circuitry is disabled. With $\overline{CS}$ low, data at DIN is clocked into the register on the rising edge of SCLK. As $\overline{CS}$ goes high, data is latched into the input and/or DAC registers, depending on the address and control bits. The maximum clock frequency guaranteed for proper operation is 10MHz. Figure 6 shows a more detailed timing diagram of the serial interface.

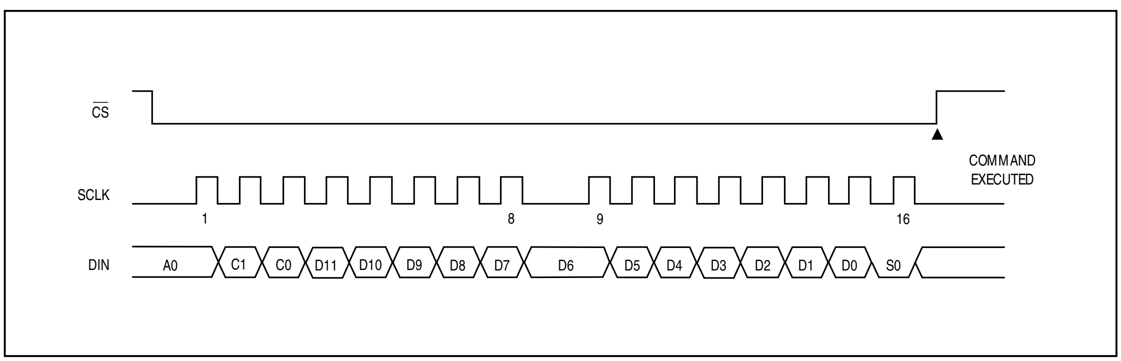


Figure 5. Serial-Interface Timing Diagram

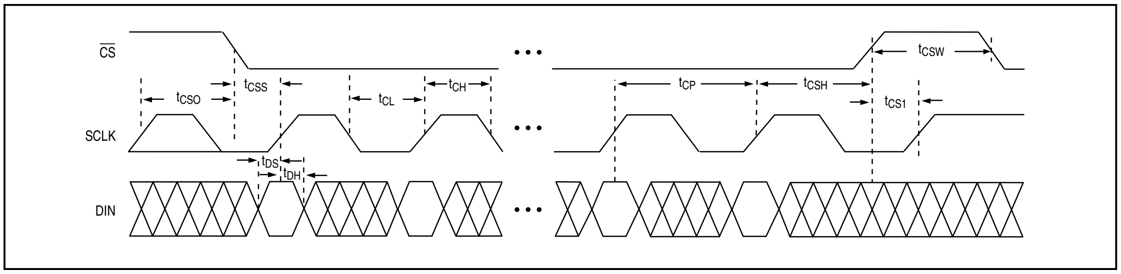


Figure 6. Detailed Serial-Interface Timing Diagram

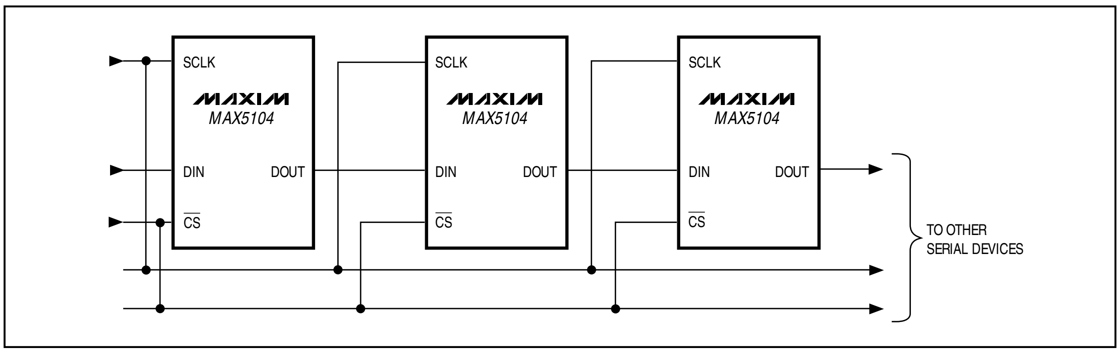


Figure 7. Daisy Chaining MAX5104s

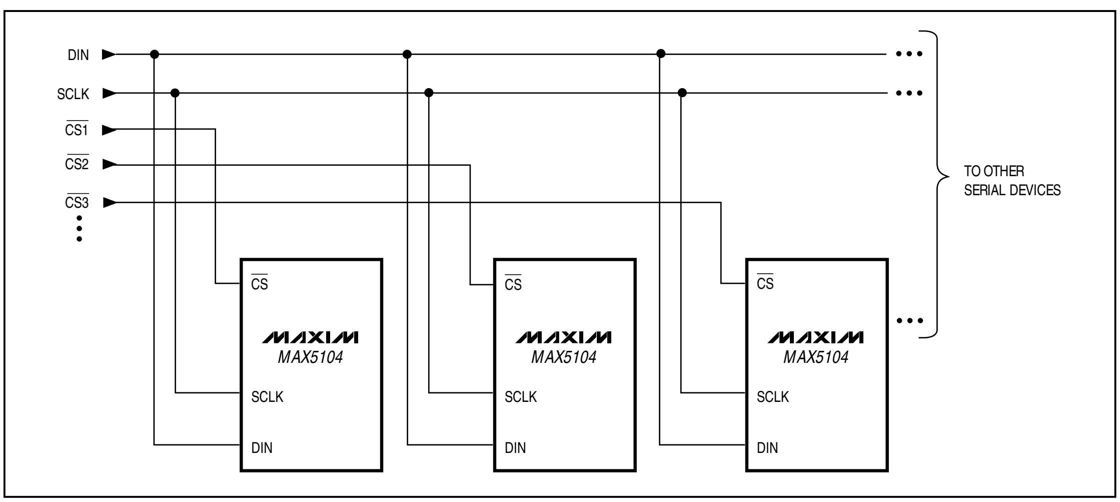


Figure 8. Multiple MAX5104s Sharing a Common DIN Line

Serial-Data Output

The serial-data output, DOUT, is the internal shift register's output. DOUT allows for daisy chaining of devices and data readback. The MAX5104 can be programmed to shift data out of DOUT on SCLK's falling edge (Mode 0) or on the rising edge (Mode 1). Mode 0 provides a lag of 16 clock cycles, which maintains compatibility with SPI/QSPI and MICROWIRE interfaces. In Mode 1, the output data lags 15.5 clock cycles. On power-up, the device defaults to Mode 0.

User-Programmable Logic Output

User-programmable logic output (UPO) allows an external device to be controlled through the serial interface (Table 1), thereby reducing the number of microcontroller I/O pins required. On power-up, UPO is low.

Power-Down Lockout Input

The power-down lockout ($\overline{PDL}$) pin disables software shutdown when low. When in power-down, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to power-down. $\overline{PDL}$ can also be used to asynchronously wake up the device.

Daisy-Chaining Devices

Any number of MAX5104s can be daisy-chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5104's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. See the digital output V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX5104s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

Applications Information

Unipolar Output

Figure 9 shows the MAX5104 configured for unipolar, rail-to-rail operation with a gain of +2V/V. The MAX5104 can produce a 0 to 4.096V output with a 2.048V reference (Figure 9). Table 2 lists the unipolar output codes. An offset to the output can be achieved by connecting a voltage to OS_, as shown in Figure 10. By applying $V_{OS\_}$ = -1V, the output values will range between 1V and (1V + V_{REF} · 2).

Bipolar Output

The MAX5104 can be configured for a bipolar output (Figure 11). The output voltage is given by the equation (OS_ = AGND):

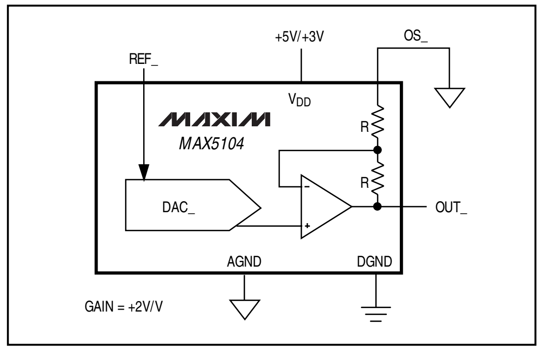


Figure 9. Unipolar Output Circuit (Rail-to-Rail)

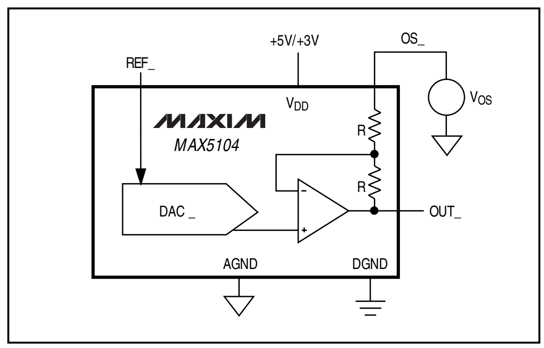


Figure 10. Setting OS_ for Output Offset

Table 2. Unipolar Code Table (Gain = +2)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 (0)	$+V_{REF}\left(\frac{4095}{4096}\right)\cdot 2$
1000 0000 0001 (0)	$+V_{REF}\left(\frac{2049}{4096}\right)\cdot 2$
1000 0000 0000 (0)	$+V_{REF}\left(\frac{2048}{4096}\right)\cdot 2 = V_{REF}$
0111 1111 1111 (0)	$+V_{REF}\left(\frac{2047}{4096}\right)\cdot 2$
0000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{4096}\right)\cdot 2$
0000 0000 0000 (0)	0V

Note: *( ) are for the sub-bit.*

$$V_{OUT} = V_{REF} [((2 \cdot NB) / 4096) - 1]$$

where NB represents the numeric value of the DAC's binary input code. Table 3 shows digital codes and the corresponding output voltage for Figure 11's circuit.

Using an AC Reference

In applications where the reference has an AC signal component, the MAX5104 has multiplying capabilities within the reference input voltage range specifications. Figure 12 shows a technique for applying a sinusoidal input to REF_, where the AC signal is offset before being applied to the reference input.

Harmonic Distortion and Noise

The total harmonic distortion plus noise (THD+N) is typically less than -78dB at full scale with a 1Vp-p input swing at 5kHz.

Digital Calibration and Threshold Selection

Figure 13 shows the MAX5104 in a digital calibration application. With a bright-light value applied to the photodiode (on), the DAC is digitally ramped until it trips the comparator. The microprocessor (µP) stores this "high" calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration.

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1 111 (0)	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0 001 (0)	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0 000 (0)	0V
0111 1111 1 111 (0)	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0 001 (0)	$+V_{REF}\left(\frac{2047}{4096}\right) \cdot 2$
0000 0000 0 000 (0)	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

Note: *( ) are for the sub-bit.*

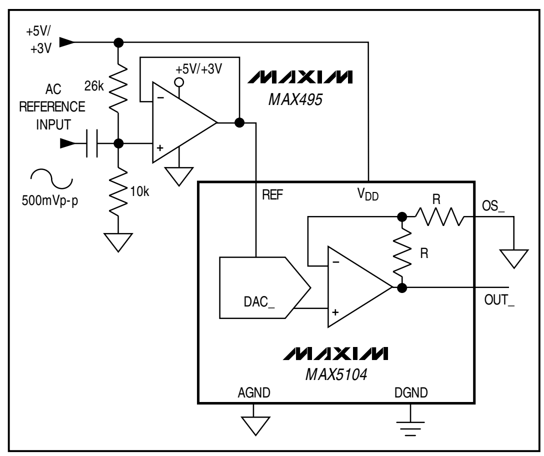


Figure 12. AC Reference Input Circuit

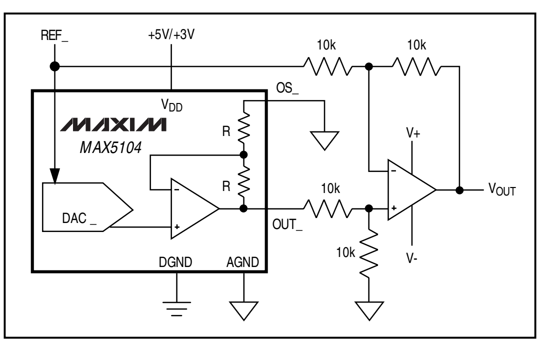


Figure 11. Bipolar Output Circuit

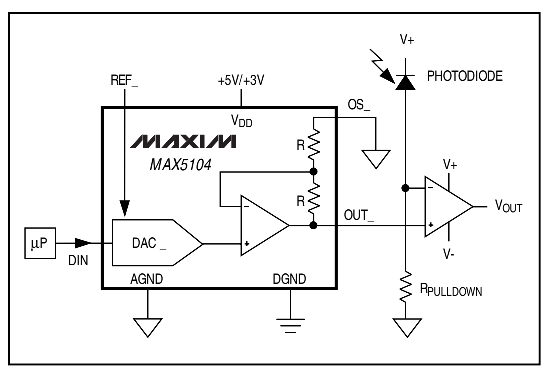


Figure 13. Digital Calibration

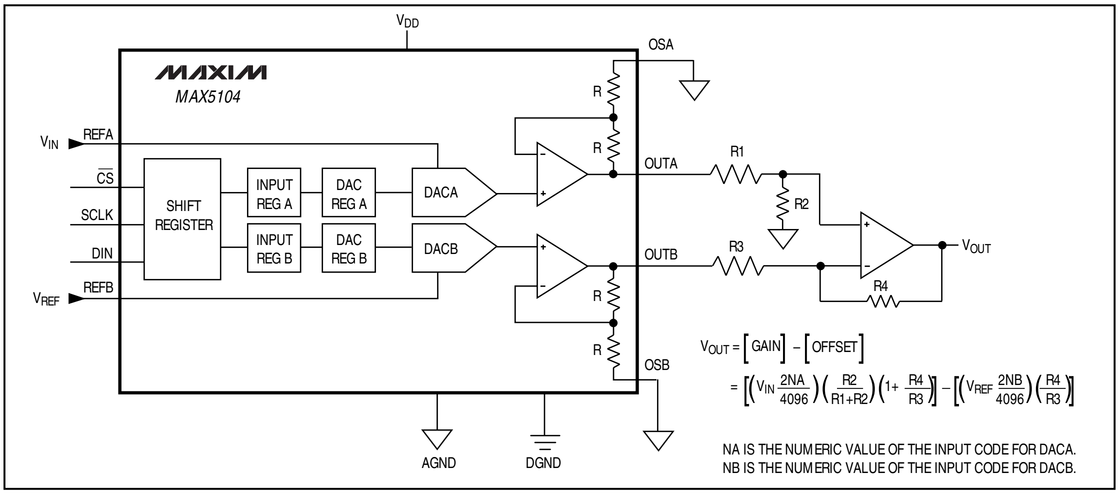


Figure 14. Digital Control of Gain and Offset

The µP then programs the DAC to set an output voltage at the midpoint of the two calibrated values. Applications include tachometers, motion sensing, automatic readers, and liquid-clarity analysis.

Digital Control of Gain and Offset

The two DACs can be used to control the offset and gain for curve-fitting nonlinear functions, such as transducer linearization or analog compression/expansion applications. The input signal is used as the reference for the gain-adjust DAC, whose output is summed with the output from the offset-adjust DAC. The relative weight of each DAC output is adjusted by R1, R2, R3, and R4 (Figure 14).

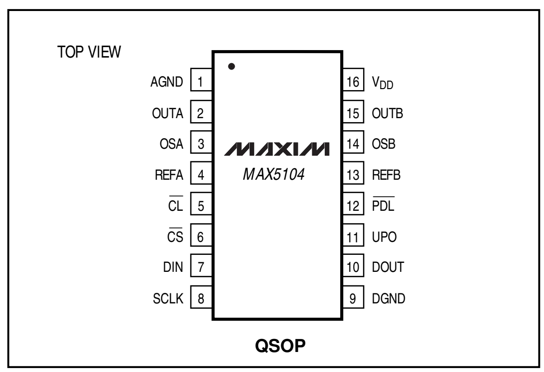
Power-Supply Considerations

On power-up, the input and DAC registers clear (set to zero code). For rated performance, $V_{REF\_}$ should be at least 1.4V below V_{DD}. Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize lead lengths to reduce lead inductance.

Grounding and Layout Considerations

Digital and AC transient signals on AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3053

SUBSTRATE CONNECTED TO AGND

Package Information

Package information is available on Maxim's website: www.maxim-ic.com.

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