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19-4516; Rev 1; 2/97

MAXIM

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

MAX514

General Description

The MAX514 contains four 12-bit R-2R multiplying digital-to-analog converters (DACs), each with a serial-in parallel-out shift register, a DAC register, and control logic. The MAX514's 3-wire serial interface design minimizes the number of package pins and internal level translators, so it uses less board space and dissipates less power (10mW max) than parallel-interface devices.

When used with microprocessors (µPs) with a serial port, the MAX514 minimizes digital-noise feedthrough from its logic input pins to its analog output. To further reduce noise, the µP serial port can be used as a dedicated analog bus and kept inactive while the MAX514 is in use. Serial interfacing also simplifies opto-coupler or transformer-isolated applications.

This device uses low-tempco thin-film resistors, laser trimmed to ±1LSB linearity, with gain accuracy better than ±1½LSB.

The MAX514 is specified with a +5V power supply. All logic inputs are TTL and CMOS compatible. It comes in space-saving 24-pin DIP and 28-pin SO packages.

Applications

Digital Offset/Gain Adjustment

Arbitrary Waveform Generators

Industrial Process Controls

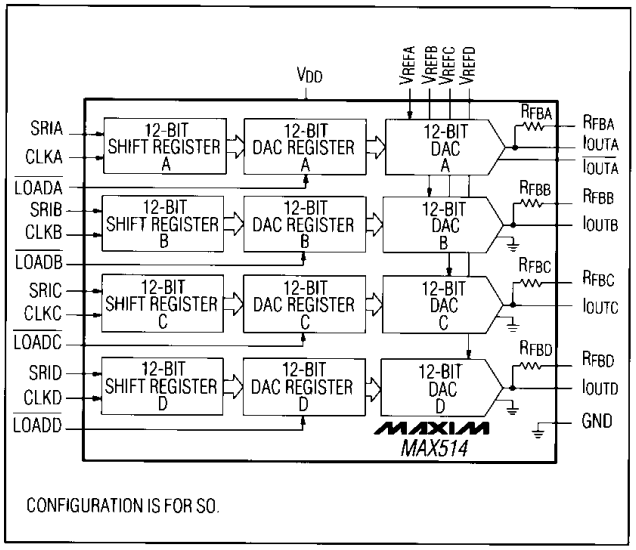
Automatic Test Equipment

Motion Control Systems

Programmable Amplifiers/Attenuators

µP-Controlled Systems

Functional Diagram



CONFIGURATION IS FOR SO.

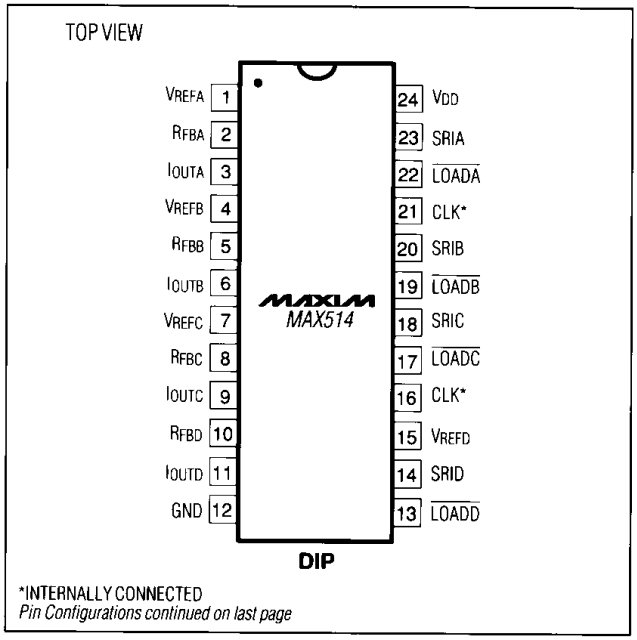
Features

- ♦ **Four 12-Bit Accurate DACs**
- ♦ **Fast 3-Wire Serial Interface**
- ♦ **Low Differential Nonlinearity: ±½LSB Max**
- ♦ **Low Integral Nonlinearity: ±1LSB Max**
- ♦ **Gain Accuracy to ±1½LSB Max**
- ♦ **Low Gain Tempco: 5ppm/°C Max**
- ♦ **Operates from a Single +5V Power Supply**
- ♦ **TTL/CMOS Compatible**
- ♦ **Available in 24-Pin DIP and 28-Pin SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	DNL (LSBs)
MAX514ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX514BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX514ACWI	0°C to +70°C	28 Wide SO	±1/2
MAX514BCWI	0°C to +70°C	28 Wide SO	±1
MAX514AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX514BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX514AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX514BEWI	-40°C to +85°C	28 Wide SO	±1

Pin Configurations



*INTERNALLY CONNECTED

Pin Configurations continued on last page

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
I_{OUTA} to GND ..... -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow Plastic DIP
(derate 8.7mW/°C above +70°C) 696mW
28-Pin Wide SO
(derate 12.5mW/°C above +70°C) ..... 1000mW/°C
Maximum Current into Any Pin 50mA
Operating Temperature Ranges:
MAX514_C__ ..... 0°C to +70°C
MAX514_E__ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, I_{OUT} = $\overline{I_{OUTA}}$ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL						±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		MAX514A			±1/2	LSB
				MAX514B			±1	
Full-Scale Error (Gain Error)	FSE	Using internal R_{FB}	T_A = +25°C	MAX514A			±1.5	LSB
				MAX514B			±2.5	
			T_A = T_{MIN} to T_{MAX}	ALL			±2.5	
Full-Scale Temperature Coefficient (Note 1)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V					±0.001	%/%
DYNAMIC PERFORMANCE (Note 1)								
Current Settling Time	t_S	T_A = +25°C, to 1/2LSB, I_{OUT} load is 100Ω | 13pF, DAC register alternately loaded with all 1s and all 0s				0.25	1	µs
Digital Feedthrough	Q	V_{REF} = 0V, I_{OUT} load is 100Ω | 13pF, DAC register alternately loaded with all 1s and all 0s				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	V_{REF} = ±10V_{p-p} at 10kHz, DAC register loaded with all 0s				0.4	1	mV_{p-p}
Total Harmonic Distortion	THD	V_{REF} = 6V_{RMS} at 1kHz, DAC register loaded with all 1s				-85		dB
Output Noise Voltage Density	e_n	T_A = +25°C, 10Hz to 100kHz, measured between R_{FB} and I_{OUT}				13	15	nV/√Hz
REFERENCE INPUT								
Reference Input Resistance	R_{REF}	V_{REF} pin to I_{OUT}			7	11	25	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C
ANALOG OUTPUTS								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s	T_A = +25°C			±0.5	±5	nA
			T_A = T_{MIN} to T_{MAX}				±25	
$\overline{I_{OUTA}}$ Leakage Current (DAC A, SO package only)	I_{LKG}	DAC register loaded with all 1s	T_A = +25°C			±0.5	±5	nA
			T_A = T_{MIN} to T_{MAX}				±25	
I_{OUT} Capacitance (Note 1)	C_{OUT1}	DAC register loaded with all 0s				55	80	pF
		DAC register loaded with all 1s				85	110	
$\overline{I_{OUTA}}$ Capacitance (DAC A, SO package only) (Note 1)	C_{OUT2}	DAC register loaded with all 0s				85	110	pF
		DAC register loaded with all 1s				55	80	

ELECTRICAL CHARACTERISTICS (continued)

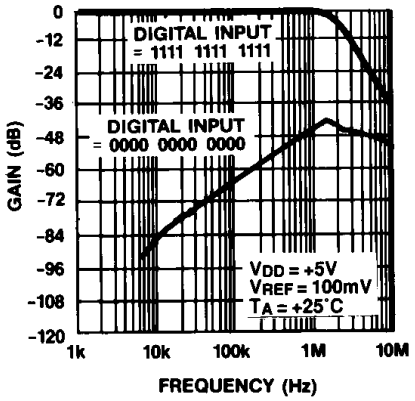
(V_{DD} = +5V, V_{REF} = +10V, I_{OUT} = $\overline{I_{OUTA}}$ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High Voltage	V_{IH}		2.4			V
Digital Input Low Voltage	V_{IL}				0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
CLK Input Leakage Current (DIP only, pins 16, 21)	I_{IN}	V_{IN} = 0V or V_{DD}			±4	µA
Digital Input Capacitance (Note 1)	C_{IN}	V_{IN} = 0V or V_{DD}			8	pF
CLK Input Capacitance (DIP only, pins 16, 21) (Note 1)	C_{IN}	V_{IN} = 0V or V_{DD}			32	pF
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		90			ns
CLK Pulse Width Low	t_{CL}		120			ns
SRI Data to CLK Setup	t_{DS}		40			ns
SRI Data to CLK Hold	t_{DH}		80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}		120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}		0			ns
$\overline{LOAD}$ High to CLK	t_{LC}		0			ns
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	For specified performance	4.75		5.25	V
Positive Supply Current	I_{DD}	All digital inputs at V_{IL} or V_{IH}			2000	µA
		All digital inputs at 0V or V_{DD}		20	400	

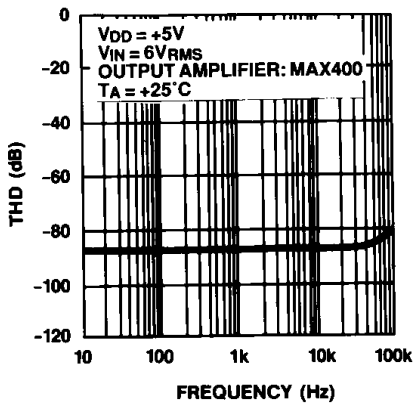
Note 1: Guaranteed by design, not subject to test.

Typical Operating Characteristics

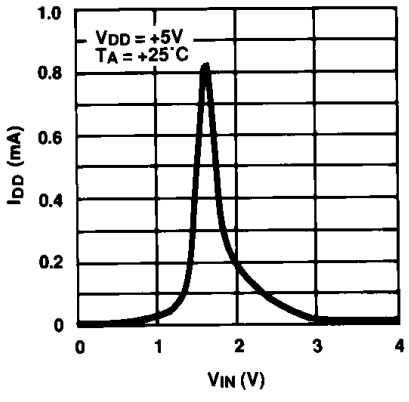
GAIN vs. FREQUENCY (OUTPUT AMPLIFIER: MAX400)



TOTAL HARMONIC DISTORTION vs. FREQUENCY (MULTIPLYING MODE)



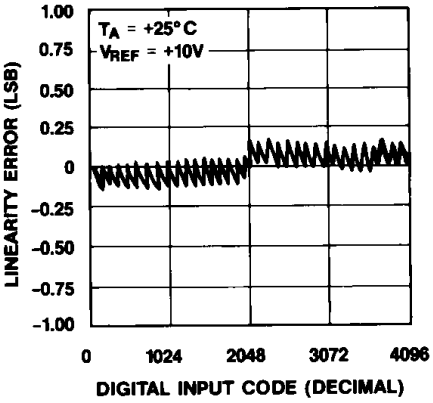
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



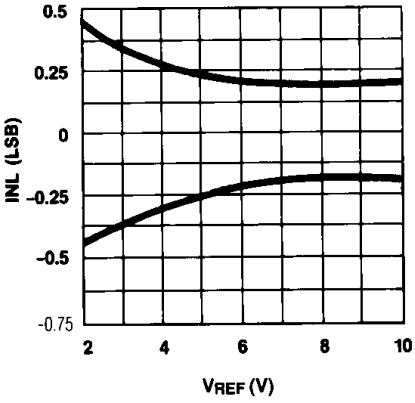
CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

Typical Operating Characteristics (continued)

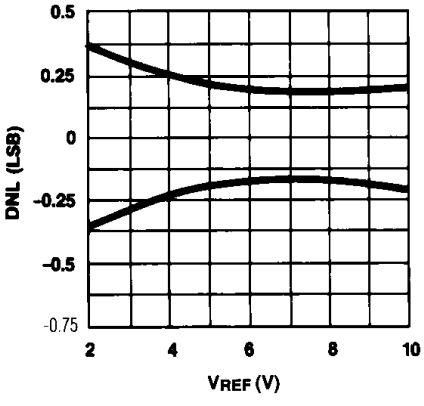
LINEARITY ERROR vs. DIGITAL CODE



INL ERROR vs. REFERENCE VOLTAGE



DNL ERROR vs. REFERENCE VOLTAGE



Pin Description

24-PIN DIP	28-PIN SO	NAME	FUNCTION
1	1	V_{REFA}	Reference Voltage Input for DACA
2	2	R_{FBA}	Internal Feedback Resistor for DACA
3	3	I_{OUTA}	DACA Output Current
–	4	$\overline{I_{OUTA}}$	DACA Inverted Current Output
4	5	V_{REFB}	Reference Voltage Input for DACB
5	6	R_{FBB}	Internal Feedback Resistor for DACB
6	7	I_{OUTB}	DACB Output Current
7	8	V_{REFC}	Reference Voltage Input for DACC
8	9	R_{FBC}	Internal Feedback Resistor for DACC
9	10	I_{OUTC}	DACC Output Current
15	11	V_{REFD}	Reference Voltage Input for DACD
10	12	R_{FBD}	Internal Feedback Resistor for DACD
11	13	I_{OUTD}	DACD Output Current
12	14	GND	Power-Supply Ground
13	15	$\overline{LOADD}$	Load DACD Input (active low). Driving this input low transfers the contents of shift register D to DAC register D and updates analog output D.
14	16	SRID	Serial Data Input for DACD
–	17	CLKD	Serial Clock Input for DACD
16, 21	–	CLK	Serial Clock Input for all four DACs. CLK pins are internally connected on DIP packaged parts.
17	18	$\overline{LOADC}$	Load DACC Input (active low). Driving this input low transfers the contents of shift register C to DAC register C and updates analog output C.
18	19	SRIC	Serial Data Input for DACC
–	20	CLKC	Serial Clock Input for DACC
19	21	$\overline{LOADB}$	Load DACB Input (active low). Driving this input low transfers the contents of shift register B to DAC register B and updates analog output B.
20	22	SRIB	Serial Data Input for DACB
–	23	CLKB	Serial Clock Input for DACB
–	24	N.C.	No Connect
22	25	$\overline{LOADA}$	Load DACA Input (active low). Driving this input low transfers the contents of shift register A to DAC register A and updates analog output A.
23	26	SRIA	Serial Data Input for DACA
–	27	CLKA	Serial Clock Input for DACA
24	28	V_{DD}	Positive Supply Voltage

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

Detailed Description

DAC Section

The MAX514 contains four current-output digital-to-analog converters (DACs). Each DAC consists of a laser-trimmed R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either I_{OUT} or GND ($\overline{I_{OUTA}}$ for DAC A, SO package only), depending upon the status of each input data bit.

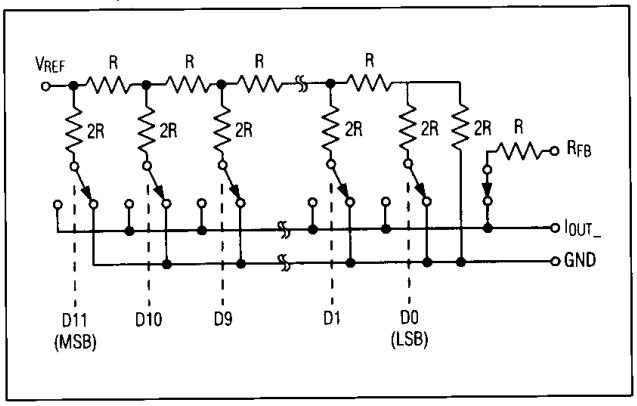


Figure 1. Simplified D/A Circuit for 1/4 of MAX514

Each of the current outputs (I_{OUT}) can be converted to a voltage by adding an external output amplifier as shown in Figure 3. V_{REF} inputs accept a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used for the reference input, a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

Each internal feedback resistor (R_{FB}) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent power-supply rejection and gain-temperature coefficient.

Digital Inputs and Interface Logic

Figure 2 shows the write-cycle timing diagram for the MAX514. The most significant bit (MSB) is always loaded first on the rising edge of the clock (CLK). Once all data is shifted into the MAX514, each DAC register is loaded by taking the corresponding $\overline{LOAD}$ signal low. The DAC registers are transparent when their $\overline{LOAD}$ input is low, and latched when their $\overline{LOAD}$ input is high. If $\overline{LOAD}$ is taken low before the least significant bit (LSB) is shifted into the shift register, the DAC output can produce a "glitch." If this is undesirable, avoid it by delaying the $\overline{LOAD}$ signal 30ns after the rising edge of the LSB CLK edge.

The digital interface of the dual-in-line package (DIP) and small outline (SO) devices differs slightly. Each DAC in the SO has its own CLK input, while DACs in the DIP share a common CLK input. The common CLK input of the DIPs is located on pins 16 and 21, which are internally connected. DACs can be individually loaded by separately controlling the four $\overline{LOAD}$ inputs. Data is shifted into each DAC through its SRI pin using the common CLK input. The output voltage of each DAC is updated after its $\overline{LOAD}$ input has been exercised, while the remaining DAC outputs are unchanged.

If simultaneous updating of all four DAC outputs is desired, the $\overline{LOAD}$ inputs on DIP devices should be bussed together and driven from a common source. Simultaneous updating of the four DAC outputs on SO devices can be accomplished by bussing the four CLK inputs together and the four $\overline{LOAD}$ inputs together.

The MAX514's input buffers act as level shifters, converting TTL levels into DAC switch-drive levels. Input buffers are compatible with both TTL and 5V CMOS logic, however the power supply current (I_{DD}) is dependent upon the input logic levels. Supply current is significantly

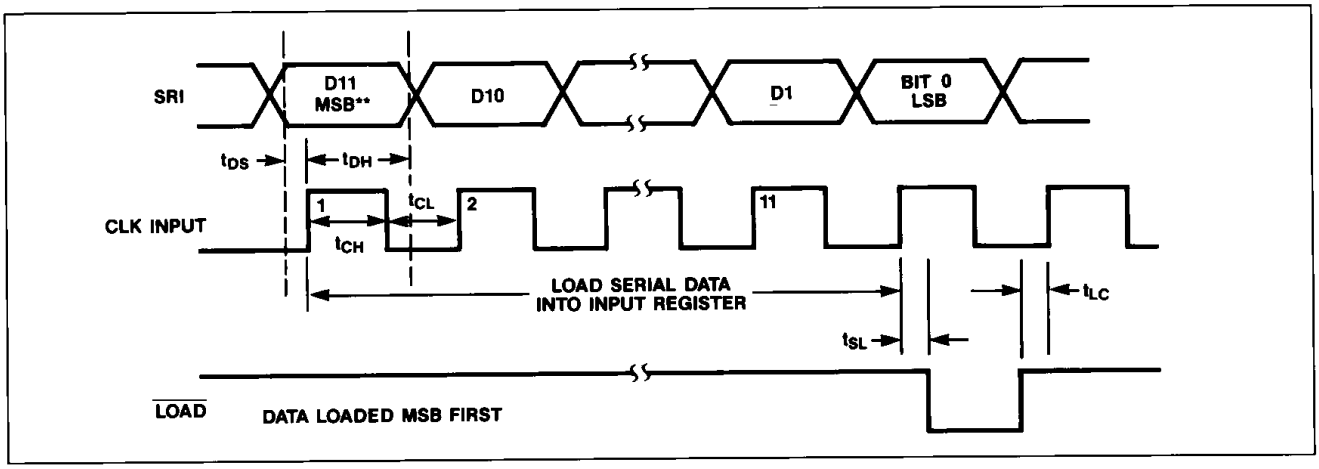


Figure 2. Write-Cycle Timing Diagram

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

reduced when logic inputs are driven as close to DGND as possible, and above 4V. This phenomenon is shown in the *Supply Current vs. Logic Input Voltage* graph in the *Typical Operating Characteristics*.

Circuit Configurations

Unipolar Operation

Figure 3 shows the basic application circuit for one-fourth of the MAX514. This circuit is used for unipolar operation or 2-quadrant multiplication. The unipolar output-code table is given in Table 1. Note that the polarity of the output voltage is the inverse of the reference voltage input (V_{REF}).

In many applications, gain adjustment will not be necessary: The gain accuracy of the part may be sufficient, or gain may be trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. When the DAC is trimmed and operated over a wide temperature range, use low tempco (<300ppm/°C) resistors for R1 and R2.

The capacitor, C1, provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the DAC outputs.

Bipolar Operation

Figure 4 shows the MAX514 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4, and R5) are required for each DAC output. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR

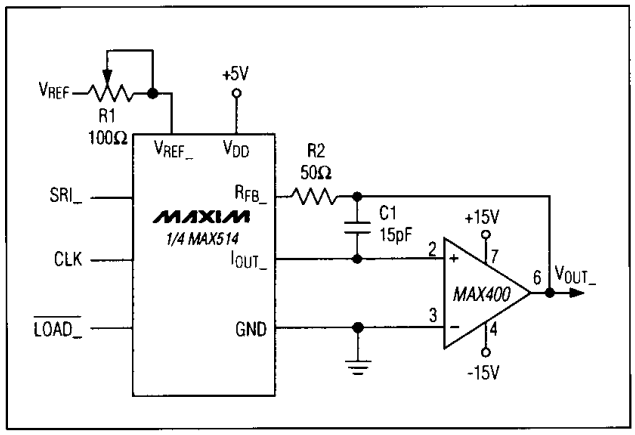


Figure 3. Unipolar Operation for 1/4 of MAX514

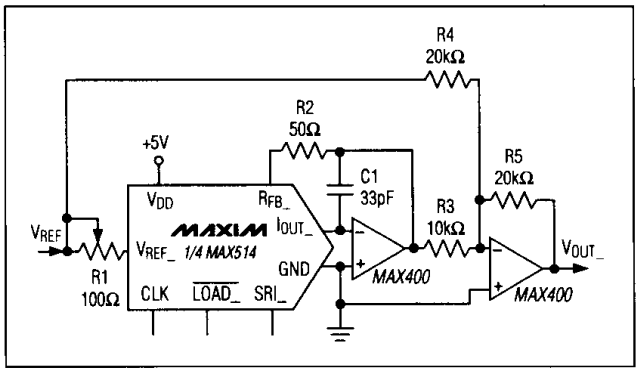


Figure 4. Bipolar Operation for 1/4 of MAX514

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

Table 2. Offset Binary Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 3. Twos Complement Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

instruction to make the MAX514 work with twos-complement coding. Table 3 shows the code relationships to output voltage for the twos-complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is used to adjust the ratio of R3 and R4 for 0V out. Full-scale error can be trimmed by loading the DAC with all 0s or all 1s, and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. Gain adjustment will not be necessary in many applications, in which case resistors R1 and R2 in Figure 4 can be omitted. If gain trimming is desired, low tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single-Supply Operation (Voltage Mode)

The MAX514 can be conveniently used in voltage mode with a single supply. I_{OUT} must not be allowed to go 0.3V lower than GND or 0.3V higher than V_{DD}. Otherwise, internal protection diodes may turn on, causing high current flow and possible damage to the device.

Figure 5 shows the MAX514 connected as a voltage-output DAC. I_{OUT} is connected to the reference voltage source and GND is grounded ($\overline{I_{OUTA}}$, on the SO package, should also be grounded). The DAC output now appears at the V_{REF} pin, which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when lower output impedance is required. The R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the circuit response time

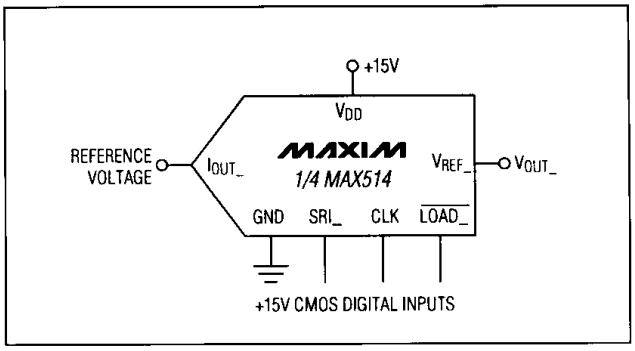


Figure 5. Single-Supply Operation for 1/4 of MAX514 Using Voltage Switching Mode

depends on the reference source's behavior with changing load conditions.

Since a negative reference is not required for a positive output when operating in voltage mode, the complete circuit can be powered from a single supply. Note that, when operating in voltage mode, the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral nonlinearity (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode.

Applications Information

Output Amplifier Offset

For best linearity, I_{OUT}, $\overline{I_{OUTA}}$, and GND should be terminated at exactly 0V. In most applications, I_{OUT} is connected to the summing junction of an inverting op amp. The amplifier's input offset voltage can degrade the DAC's linearity by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\,(1 + R_{FB} / R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically 4/3V_{OS} to 2V_{OS}, a change of 2/3V_{OS}. An amplifier with 3mV of offset, therefore, degrades linearity by 2mV — almost a full LSB when a 10V reference voltage is used. For best linearity, amplifiers with low offset voltage (such as the MAX400) should be used as output amplifiers for the MAX514. A good rule of thumb is that V_{OS} should be no more than 1/10LSB.

The output-amplifier input bias current (I_B) can also limit performance since I_B x R_{FB} generates an offset error. I_B should, therefore, be much less than the DAC output

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

current for 1LSB, which is typically 250nA with a 10V reference voltage. One-tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias-current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to GND.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic signal coupling from the V_{REF} inputs to I_{OUT}. This coupling is primarilly a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent upon the circuit-board layout and on-chip capacitive coupling. Guard traces between the digital input, V_{REF} inputs, and I_{OUT} pins minimize layout-induced feedthrough. Each DAC output follows the digital inputs when the corresponding $\overline{LOAD}$ pin is low. In this state, invalid outputs and voltage glitches can appear at the DAC outputs. Keeping the $\overline{LOAD}$ inputs high until all of the data is shifted into the DAC eliminates this problem.

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. The value of this capacitor depends on the type of op amp used, but it typically ranges from 10pF to 33pF. Too small a value causes output ringing, while excessive capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit-board trace and stray capacitance at I_{OUT} at low as possible.

The capacitance at each I_{OUT} pin (C_{OUT}) is code dependent and is typically 55pF with all switches connected to GND, and 85pF with all switches connected to I_{OUT}.

Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to a "single point" ground through a separate, low-resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code-dependent error if these terminals are connected to GND (or a "virtual ground") through a resistive path.

A 1µF bypass capacitor, in parallel with a 0.01µF ceramic capacitor, should be connected across the DAC V_{DD} and GND as close to the pins as possible.

The MAX514 has high-impedance digital inputs. To minimize noise pick-up and prevent static charge accumulation if the pins are left floating (such as when a circuit card is left unconnected), they should be tied to either V_{DD} or GND through high-value resistors (1MΩ).

Pin Configurations (continued)