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19-5651; Rev 0; 12/10

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs



## General Description

The MAX5214/MAX5216 are pin-compatible, 14-bit and 16-bit digital-to-analog converters (DACs). The MAX5214/MAX5216 are single-channel, low-power, buffered voltage-output DACs. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption. The MAX5214/MAX5216 accept a wide 2.7V to 5.25V supply voltage range. Power consumption is extremely low to accommodate most low-power and low-voltage applications. These devices feature a 3-wire SPI™-/QSPI™-/MICROWIRE™-/DSP-compatible serial interface to save board space and to reduce the complexity in isolated applications. The MAX5214/MAX5216 minimize the digital noise feedthrough from input to output with SCLK and DIN input buffers powered down after completion of each serial input frame. On power-up, the MAX5214/MAX5216 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers that need to be off on power-up. The DAC output is buffered resulting in a low supply current of 80µA (max) and a low offset error of ±0.25mV. A zero level applied to the $\overline{CLR}$ pin asynchronously clears the contents of the input and DAC registers and sets the DAC output to zero independent of the serial interface. The MAX5214/MAX5216 are available in an ultra-small (3mm x 3mm), 8-pin µMAX® package and are specified over the -40°C to +105°C extended industrial temperature range.

## Applications

2-Wire Sensors

Communication Systems

Automatic Tuning

Gain and Offset Adjustment

Power Amplifier Control

Process Control and Servo Loops

Portable Instrumentation

Programmable Voltage and Current Sources

Automatic Test Equipment

*SPI/QSPI are trademarks of Motorola, Inc.*

*MICROWIRE is a trademark of National Semiconductor Corp.*

*µMAX is a registered trademark of Maxim Integrated Products, Inc.*

## Features

- **Low-Power Consumption (80µA max)**
- **14-/16-Bit Resolution in a 3mm x 3mm, 8-Pin µMAX Package**
- **Relative Accuracy**
  - **±0.25 LSB INL (MAX5214, 14-Bit)**
  - **±1.0 LSB INL (MAX5216, 16-Bit)**
- **Guaranteed Monotonic Over All Operating Ranges**
- **Low Gain and Offset Error**
- **Wide 2.7V to 5.25V Supply Range**
- **Rail-to-Rail Buffered Output Operation**
- **Safe Power-On Reset (POR) to Zero DAC Output**
- **Fast 50MHz, 3-Wire, SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- **Asynchronous $\overline{CLR}$ Clears DAC Output to Code 0**
- **High Reference Input Resistance for Power Reduction**
- **Buffered Voltage Output Directly Drives 10kΩ Loads**

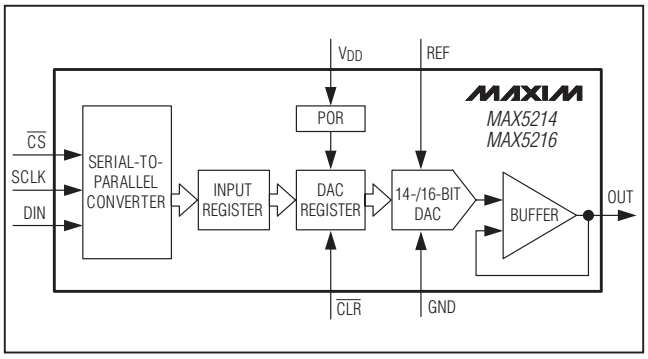
## Ordering Information

| PART | PIN-PACKAGE | RESOLUTION (BITS) |
|---|---|---|
| **MAX5214**GUA+ | 8 µMAX | 14 |
| **MAX5216**GUA+ | 8 µMAX | 16 |

***Note:*** *All devices are specified over the -40°C to +105°C operating temperature range.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Functional Diagram



# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND ..... -0.3V to +6V
REF, OUT, $\overline{CLR}$ to GND ..... -0.3V to the lower of ($V_{DD}$ + 0.3V) and +6V
SCLK, DIN, $\overline{CS}$ to GND ..... -0.3V to +6V
Continuous Power Dissipation ($T_A$ = +70°C)
μMAX (derate at 4.8mW/°C above +70°C) ..... 387mW
Maximum Current into Any Input or Output ..... ±50mA
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

μMAX
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..... 206°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) ..... 42°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5V, $V_{REF}$ = 5V, $C_L$ = 100pF, $R_L$ = 10kΩ, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC ACCURACY (Note 2)** | | | | | | |
| Resolution | N | MAX5214 | 14 | | | Bits |
| | | MAX5216 | 16 | | | |
| Integral Nonlinearity | INL | MAX5214 (14-bit) (Note 3) | -1 | ±0.25 | +1 | LSB |
| | | MAX5216 (16-bit) (Note 3) | -3 | ±1 | +3 | |
| Differential Nonlinearity | DNL | MAX5214 (14-bit) (Note 3) | -1 | ±0.1 | +1 | LSB |
| | | MAX5216 (16-bit) (Note 3) | -1 | ±0.1 | +1 | |
| Offset Error | OE | (Note 4) | -1.25 | ±0.25 | +1.25 | mV |
| Offset-Error Drift | | | | ±0.5 | | μV/°C |
| Gain Error | GE | (Note 4) | -0.06 | -0.04 | 0 | %FS |
| Gain Temperature Coefficient | | | | ±2 | | ppmFS/°C |
| **REFERENCE INPUT** | | | | | | |
| Reference-Input Voltage Range | $V_{REF}$ | | 2 | | $V_{DD}$ | V |
| Reference-Input Impedance | $R_{REF}$ | | 200 | 256 | | kΩ |
| **DAC OUTPUT** | | | | | | |
| Output Voltage Range | | No load (typical) | | | $V_{DD}$ | V |
| | | 10kΩ load | 0.2 | | $V_{DD}$ - 0.2 | |
| DC Output Impedance | | | | 0.1 | | Ω |
| Capacitive Load (Note 5) | $C_L$ | Series resistance = 0Ω | | | 0.1 | nF |
| | | Series resistance = 1kΩ | | | 15 | μF |
| Resistive Load (Note 5) | $R_L$ | | 5 | | | kΩ |
| Short-Circuit Current | | $V_{DD}$ = 5.25V | -10 | ±5 | +10 | mA |
| Power-Up Time | | From power-down mode | | 25 | | μs |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{REF}$ = 5V, $C_L$ = 100pF, $R_L$ = 10kΩ, $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CLR}$)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{DD}$ | V |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{DD}$ | | ±0.1 | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 10 | pF |
| Hysteresis Voltage | $V_{HYS}$ | | | 0.15 | | V |
| **DYNAMIC PERFORMANCE (Note 5)** | | | | | | |
| Voltage-Output Slew Rate | SR | Positive and negative | | 0.5 | | V/µs |
| Voltage-Output Settling Time | | 1/4 scale to 3/4 scale, to ≤ 0.5 LSB, 14-bit | | 14 | | µs |
| Reference -3dB Bandwidth | BW | Hex code = 2000 (MAX5214), Hex code = 8000 (MAX5216) | | 100 | | kHz |
| Digital Feedthrough | | Code = 0, all digital inputs from 0V to $V_{DD}$, SCLK < 50MHz | | 0.5 | | nV·s |
| DAC Glitch Impulse | | Major code transition | | 2 | | nV·s |
| Output Noise | | 10kHz | | 70 | | nV/√Hz |
| Integrated Output Noise | | 0.1Hz to 10Hz | | 1.5 | | $µV_{P-P}$ |
| **POWER REQUIREMENTS** | | | | | | |
| Supply Voltage | $V_{DD}$ | | 2.7 | | 5.25 | V |
| Supply Current | $I_{DD}$ | No load; all digital inputs at 0V or $V_{DD}$, supply current only; excludes reference input current, midscale | | 70 | 80 | µA |
| Power-Down Supply Current | | No load, all digital inputs at 0V or $V_{DD}$ | | 0.4 | 2 | µA |
| **TIMING CHARACTERISTICS (Notes 5 and 6) (Figures 1 and 2)** | | | | | | |
| Serial Clock Frequency | $f_{SCLK}$ | | 0 | | 50 | MHz |
| SCLK Pulse-Width High | $t_{CH}$ | | 8 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 8 | | | ns |
| $\overline{CS}$ Fall to SCLK Fall Setup Time | $t_{CSS0}$ | | 8 | | | ns |
| $\overline{CS}$ Fall to SCLK Fall Hold Time | $t_{CSH0}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Fall Hold Time | $t_{CSH1}$ | | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Fall | $t_{CSA}$ | | | | 12 | ns |
| SCLK Fall to $\overline{CS}$ Fall | $t_{CSF}$ | | 100 | | | ns |
| DIN to SCLK Fall Setup Time | $t_{DS}$ | | 5 | | | ns |
| DIN to SCLK Fall Hold Time | $t_{DH}$ | | 4.5 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSPW}$ | | 20 | | | ns |
| $\overline{CLR}$ Pulse-Width Low | $t_{CLPW}$ | | 20 | | | ns |
| $\overline{CLR}$ Rise to $\overline{CS}$ Fall | $t_{CSC}$ | | 20 | | | ns |

**Note 2:** Static accuracy tested without load.
**Note 3:** Linearity is tested within 20mV of GND and $V_{DD}$.
**Note 4:** Gain and offset is tested within 100mV of GND and $V_{DD}$.
**Note 5:** Guaranteed by design; not production tested.
**Note 6:** All timing specifications measured with $V_{IL}$ = $V_{GND}$, $V_{IH}$ = $V_{DD}$.

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

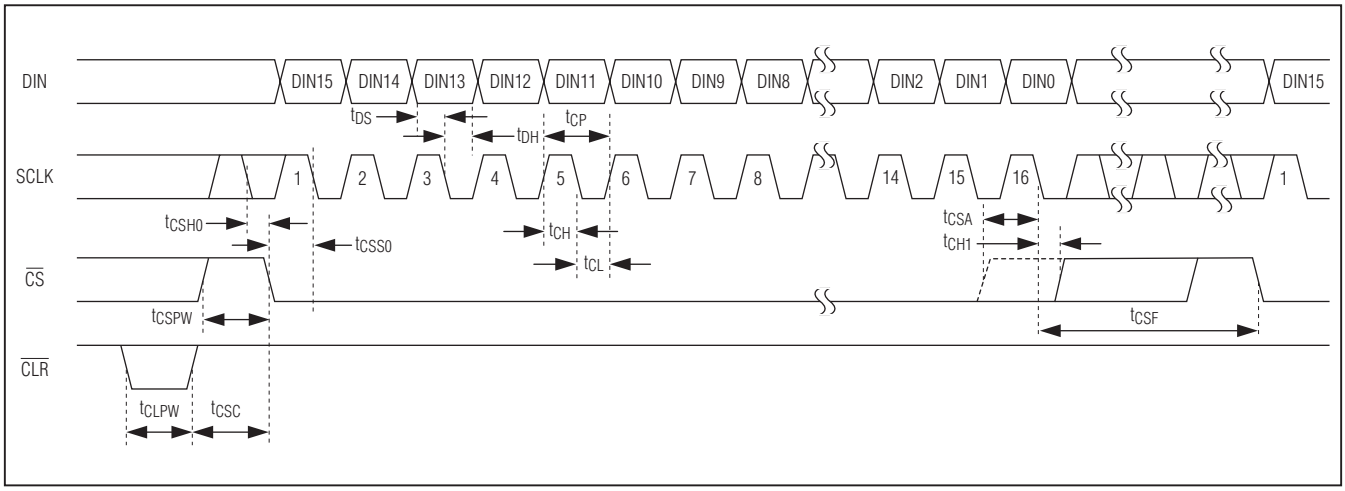



*Figure 1. 16-Bit Serial-Interface Timing Diagram (MAX5214)*

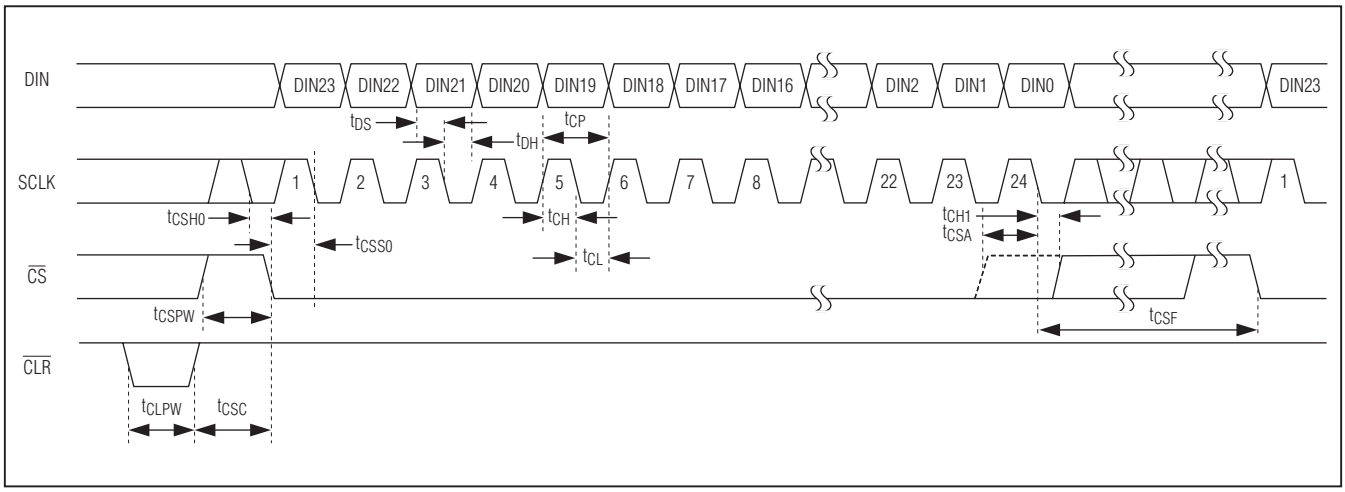
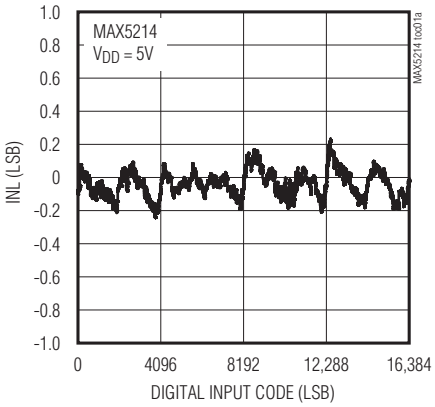



*Figure 2. 24-Bit Serial-Interface Timing Diagram (MAX5216)*

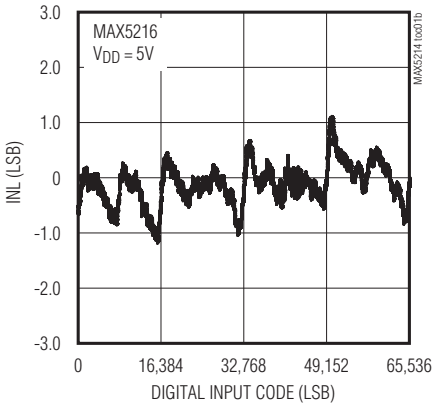
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

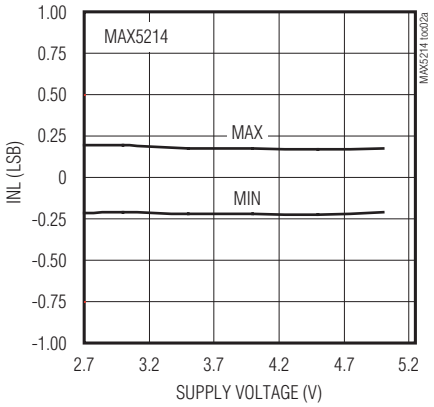
**INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE**



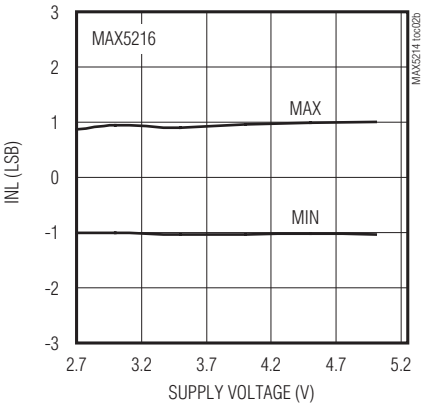

**INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE**



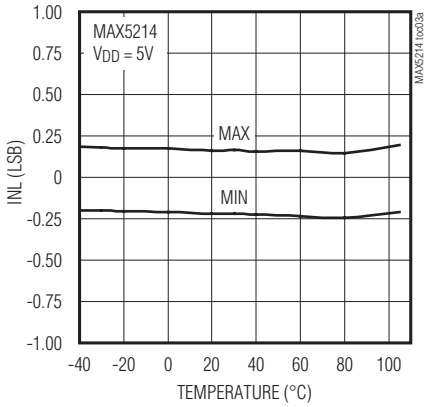

**INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE**



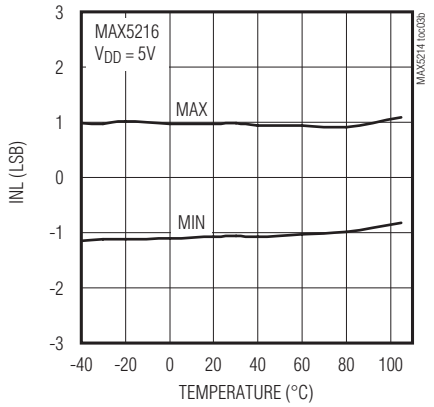

**INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE**



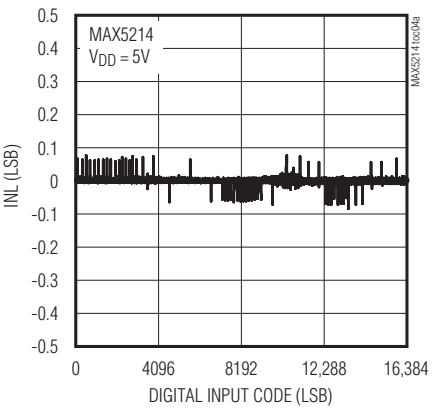

**INTEGRAL NONLINEARITY vs. TEMPERATURE**



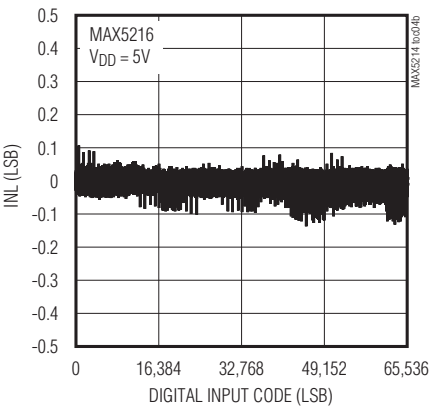

**INTEGRAL NONLINEARITY vs. TEMPERATURE**



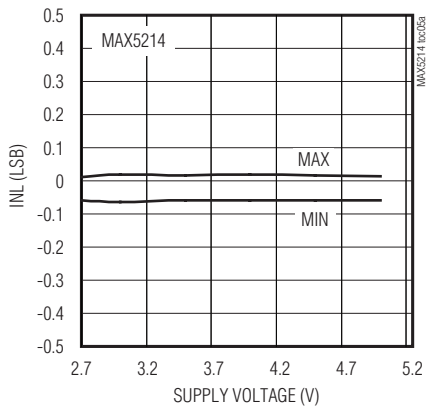

**DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE**




**DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE**




**DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE**

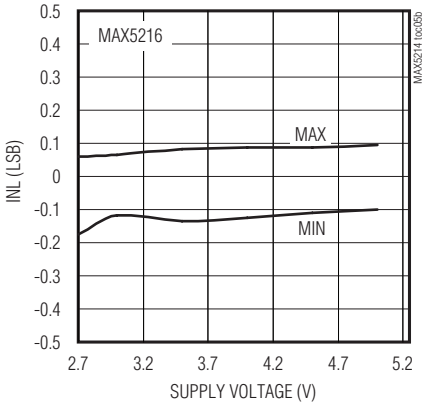


# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

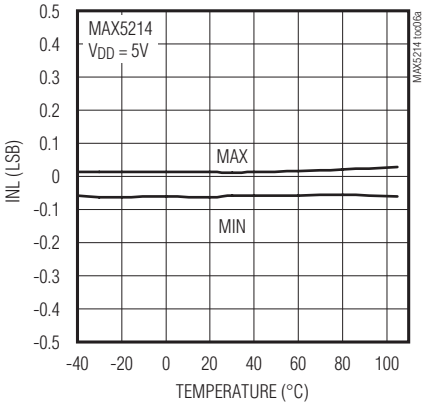
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

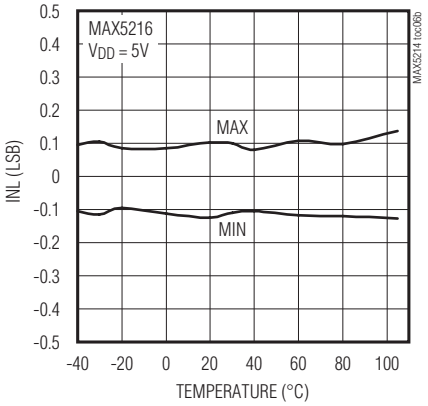
**DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE**



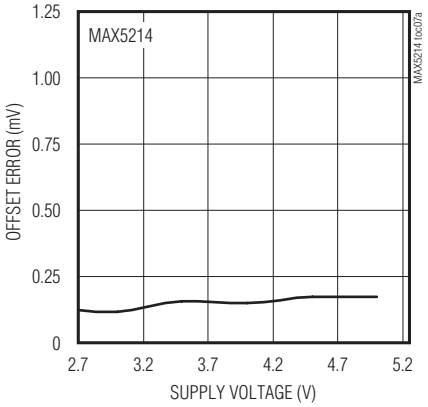

**DIFFERENTIAL NONLINEARITY vs. TEMPERATURE**



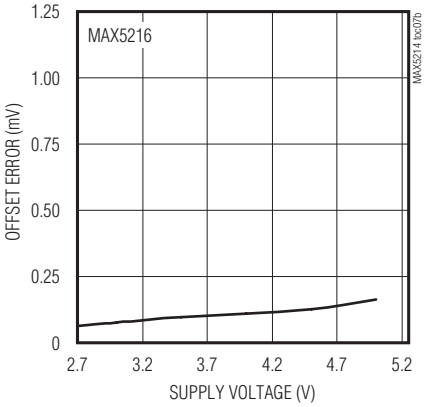

**DIFFERENTIAL NONLINEARITY vs. TEMPERATURE**



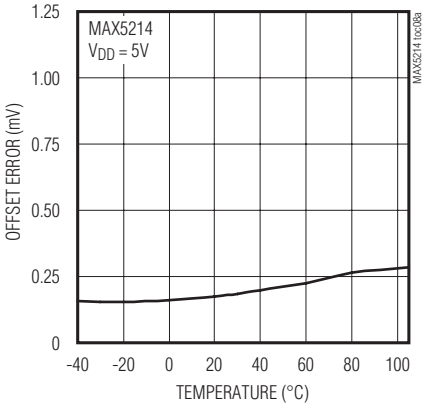

**OFFSET ERROR vs. SUPPLY VOLTAGE**



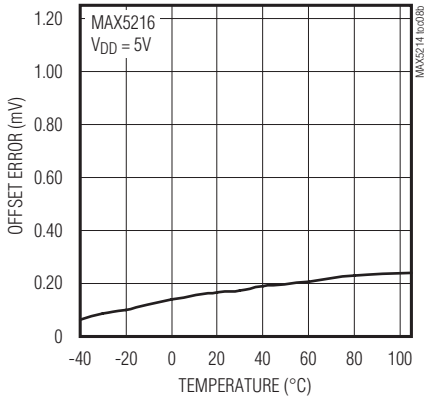

**OFFSET ERROR vs. SUPPLY VOLTAGE**



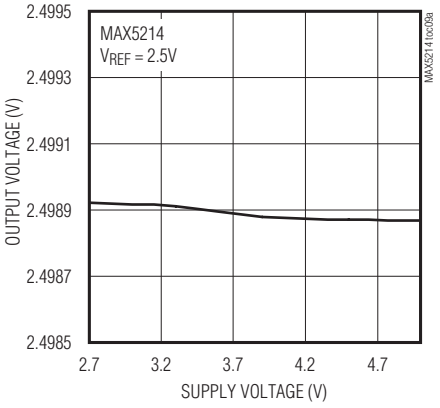

**OFFSET ERROR vs. TEMPERATURE**



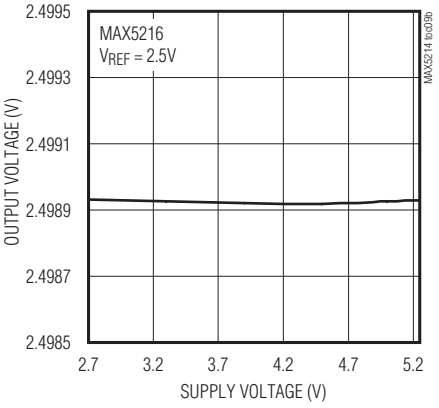

**OFFSET ERROR vs. TEMPERATURE**




**FULL-SCALE OUTPUT vs. SUPPLY VOLTAGE**



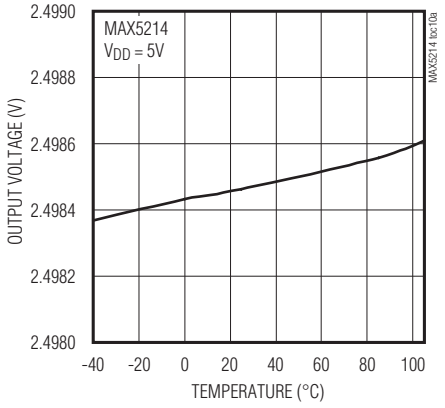

**FULL-SCALE OUTPUT vs. SUPPLY VOLTAGE**



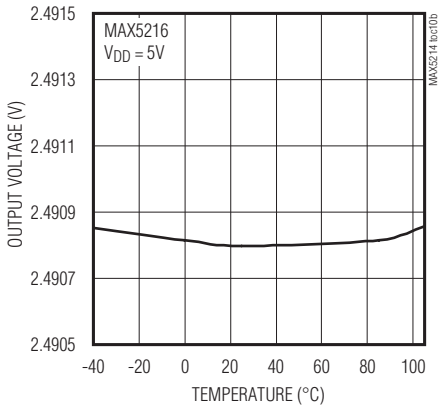
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

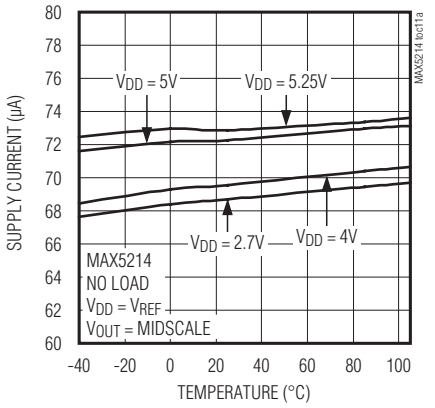
**FULL-SCALE OUTPUT vs. TEMPERATURE**



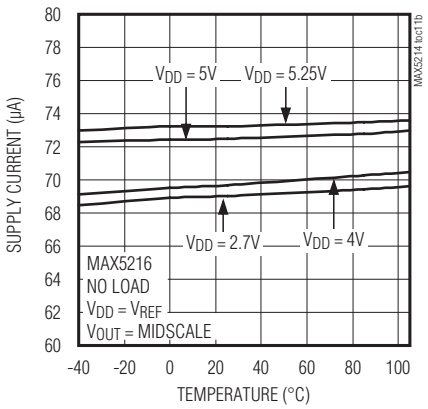

**FULL-SCALE OUTPUT vs. TEMPERATURE**



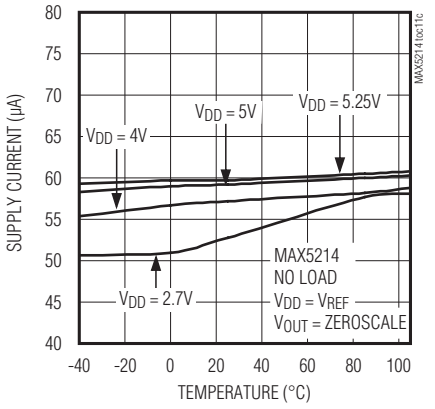

**SUPPLY CURRENT vs. TEMPERATURE**



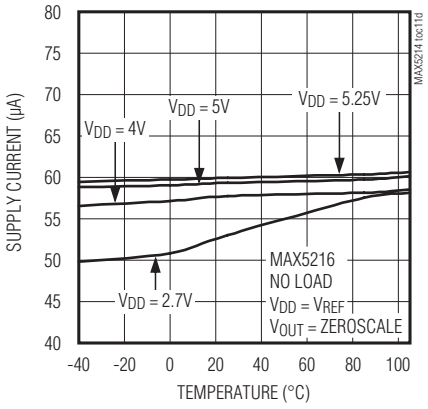

**SUPPLY CURRENT vs. TEMPERATURE**




**SUPPLY CURRENT vs. TEMPERATURE**




**SUPPLY CURRENT vs. TEMPERATURE**

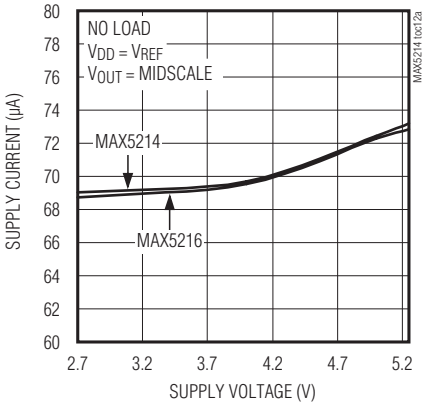


# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

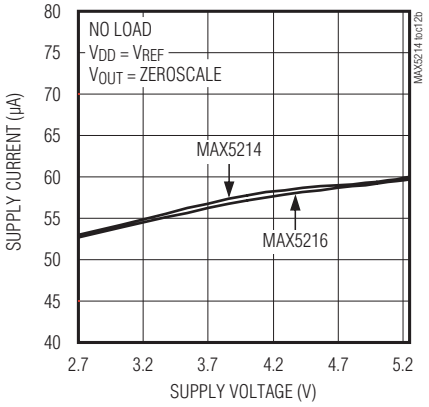
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

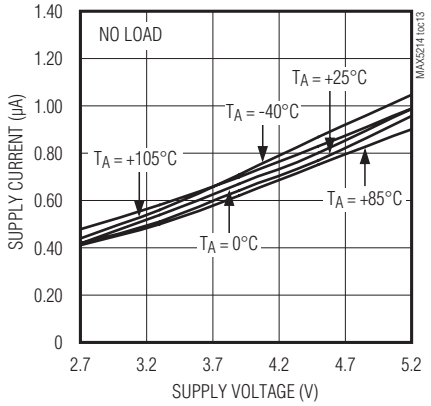
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



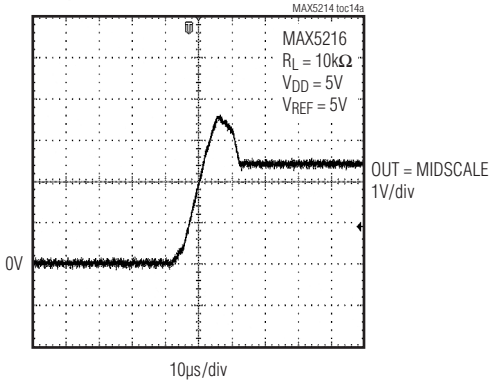

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



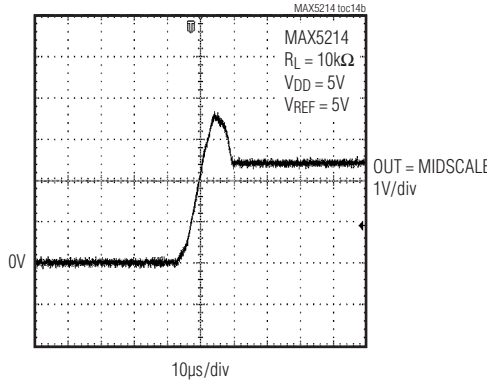

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (POWER-DOWN MODE)**



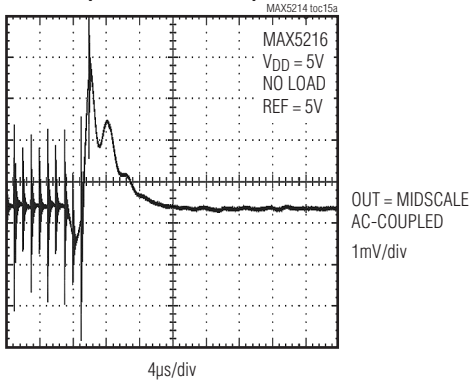

**VOUT vs. TIME (EXITING POWER-DOWN MODE)**




**VOUT vs. TIME (EXITING POWER-DOWN MODE)**



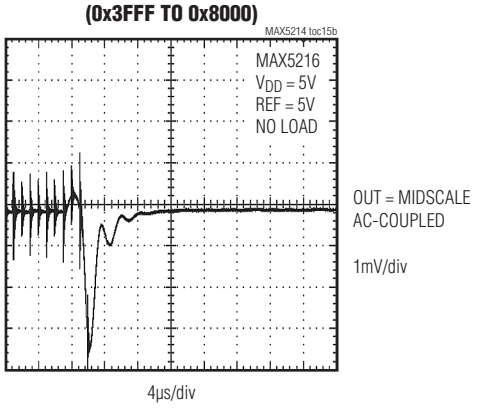

**MAJOR CODE TRANSITION (0x8000 TO 0x7FFF)**



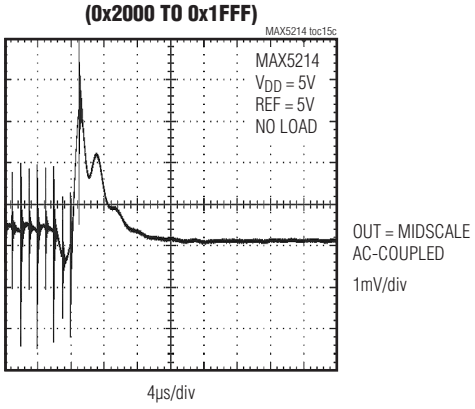
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

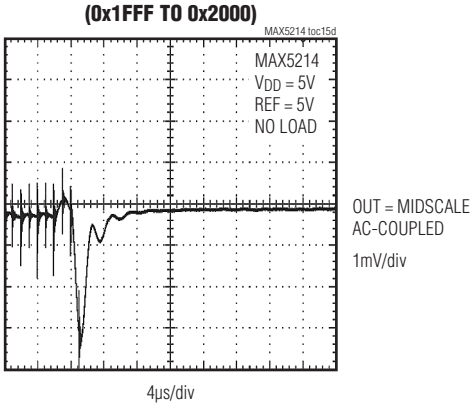
**MAJOR CODE TRANSITION (0x3FFF TO 0x8000)**



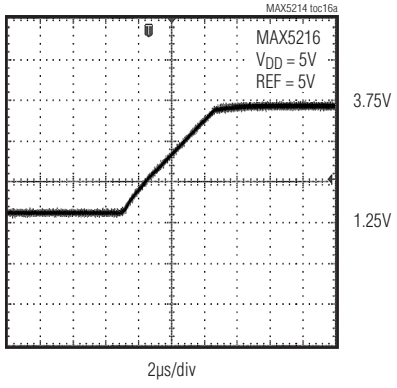

**MAJOR CODE TRANSITION (0x2000 TO 0x1FFF)**



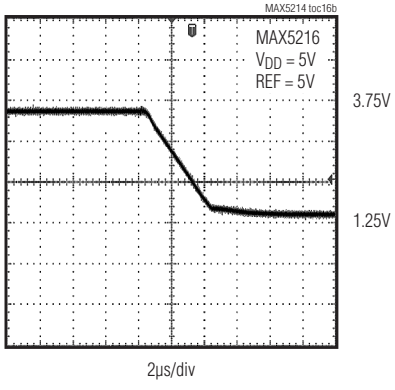

**MAJOR CODE TRANSITION (0x1FFF TO 0x2000)**



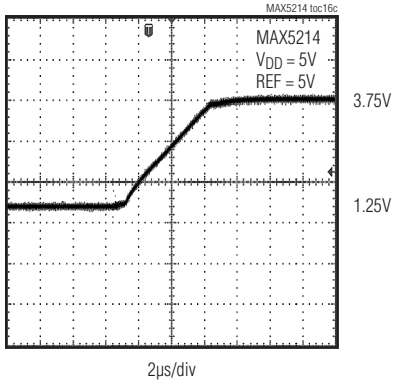

**SETTLING TIME HIGH**




**SETTLING TIME LOW**




**SETTLING TIME HIGH**

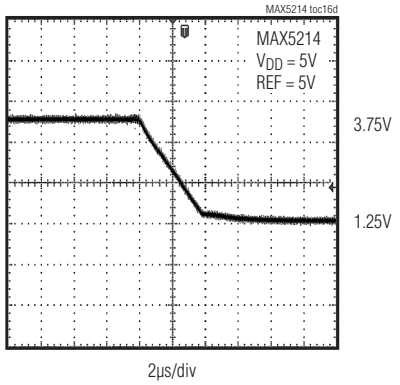


# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

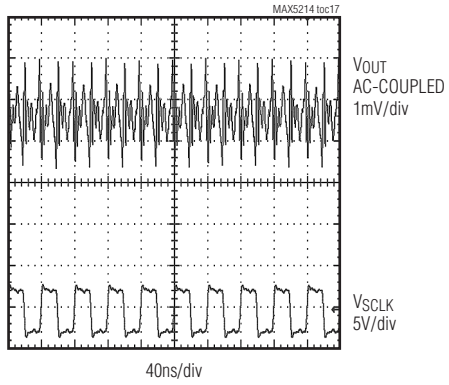
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

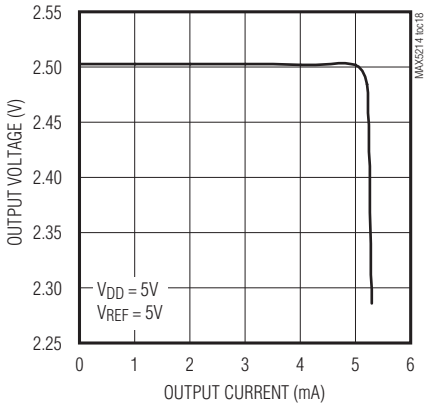
**SETTLING TIME LOW**



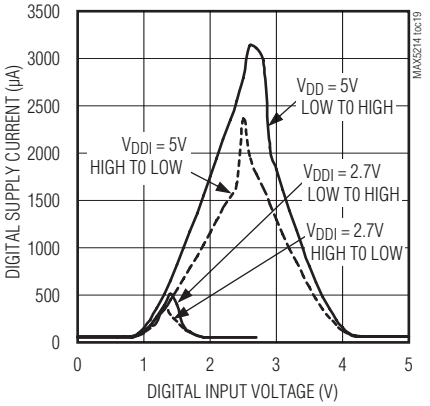

**DIGITAL FEEDTHROUGH**



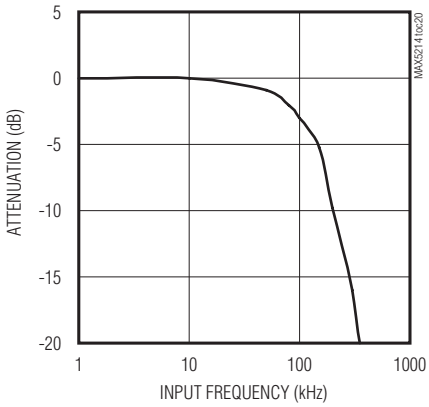

**OUTPUT VOLTAGE vs. OUTPUT CURRENT**




**SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE**

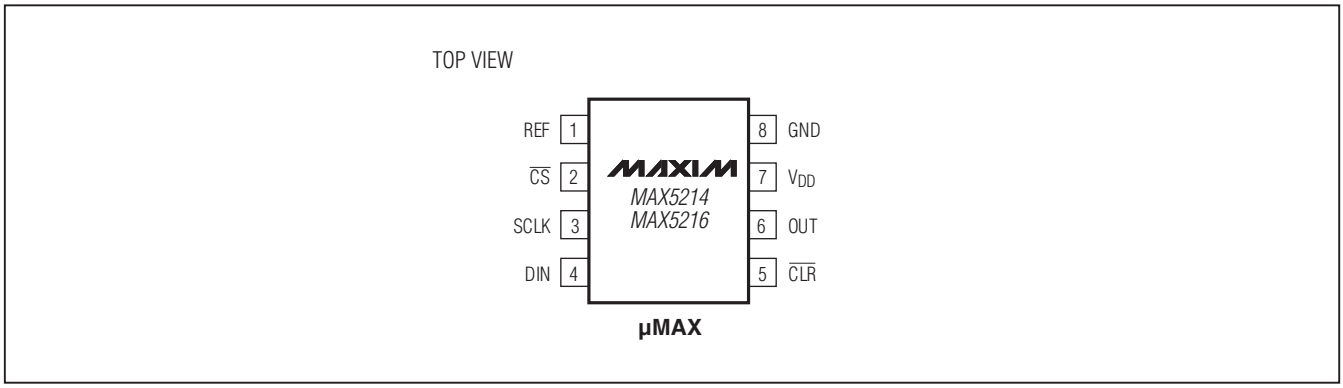



**REFERENCE INPUT BANDWIDTH vs. FREQUENCY**



# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

## Pin Configuration




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | REF | Reference Voltage Input. Bypass REF with a 0.1µF capacitor to GND. |
| 2 | $\overline{CS}$ | Active-Low Chip-Select Input |
| 3 | SCLK | Serial-Clock Input |
| 4 | DIN | Data In |
| 5 | $\overline{CLR}$ | Active-Low Asynchronous Digital-Clear Input. Drive $\overline{CLR}$ low to clear the contents of the input and DAC registers and set the DAC output to zero. |
| 6 | OUT | Buffered DAC Output |
| 7 | $V_{DD}$ | Supply Voltage. Bypass $V_{DD}$ with a 0.1µF capacitor to GND. |
| 8 | GND | Ground |

## Detailed Description

The MAX5214/MAX5216 are pin-compatible and software-compatible 14-bit and 16-bit DACs. The MAX5214/MAX5216 are single-channel, low-power, high-reference input resistance, and buffered voltage-output DACs. The MAX5214/MAX5216 minimize the digital noise feedthrough from their inputs to their outputs by powering down the SCLK and DIN input buffers after completion of each data frame. The data frames are 16-bit for the MAX5214 and 24-bit for the MAX5216. On power-up, the MAX5214/MAX5216 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The MAX5214/MAX5216 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, power-on-reset (POR) circuit, $\overline{CLR}$ to asynchronously clear the device independent of the serial interface, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

### Output Amplifier (OUT)

The MAX5214/MAX5216 include an internal buffer on the DAC output. The internal buffer provides improved load regulation and transition glitch suppression for the DAC output. The output buffer slews at 0.5V/µs and drives up to 10kΩ in parallel with 100pF. The analog supply voltage ($V_{DD}$) determines the maximum output voltage range of the device as $V_{DD}$ powers the output buffer.

### DAC Reference (REF)

The external reference input features a typical input impedance of 256kΩ and accepts an input voltage from +2V to $V_{DD}$. Connect an external voltage supply between REF and GND to apply an external reference.

Visit **www.maxim-ic.com/products/references** for a list of available voltage-reference devices.

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

### Serial Interface

The MAX5214/MAX5216 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, $\overline{CS}$, and DIN. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16-bit for the MAX5214 and 24-bit for the MAX5216. The first 2 bits are the control bits followed by 14 data bits (MSB first) for the MAX5214 and 22 data bits (MSB first) for the MAX5216 as shown in Tables 1 and 2. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, drive $\overline{CS}$ high and keep $\overline{CS}$ high for a minimum of 20ns before the next write sequence. The SCLK can be either high or low between $\overline{CS}$ write pulses. Figures 1 and 2 show the timing diagram for the complete 3-wire serial interface transmission. The MAX5216 DAC code is unipolar binary with $V_{OUT}$ = (code/65,535) x $V_{REF}$. The MAX5214 DAC code is unipolar binary with $V_{OUT}$ = (code/16,383) x $V_{REF}$. See Tables 1 and 2.

## Table 1. Operating Mode Truth Table (MAX5214)

| 16-BIT WORD | | | | | | | | | | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CONTROL BITS | | DATA BITS | | | | | | | | | | | | | | |
| MSB | | LSB | | | | | | | | | | | | | | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | No operation |
| 1 | 0 | 0 | X | A1 | A0 | X | X | X | X | X | X | X | X | X | X | Power-down (see Table 3) |
| 0 | 1 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Write through |
| 1 | 1 | Reserved, Do Not Use | | | | | | | | | | | | | | |

## Table 2. Operating Mode Truth Table (MAX5216)

| 24-BIT WORD | | | | | | | | | | | | | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CONTROL BITS | | DATA BITS | | | | | | | | | | | | | | | | | |
| MSB | | LSB | | | | | | | | | | | | | | | | | |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5–D0 | |
| 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | No operation |
| 1 | 0 | 0 | X | A1 | A0 | X | X | X | X | X | X | X | X | X | X | X | X | X | Power-down (see Table 3) |
| 0 | 1 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | X | Write through |
| 1 | 1 | Reserved, Do Not Use | | | | | | | | | | | | | | | | | |

### Writing to the Devices

1) Drive $\overline{CS}$ low, enabling the shift register.
2) Clock 16/24 bits of data into DIN (MSB first and LSB last), observing the specified setup and hold times.
3) After clocking in the last data bit, drive $\overline{CS}$ high. $\overline{CS}$ must remain high for 20ns before the next transmission is started.

Figure 1 shows a write operation for the transmission of 16 bits. If $\overline{CS}$ is driven high at any point prior to receiving 16 bits, the transmission is discarded.

Figure 2 shows a write operation for the transmission of 24 bits. If $\overline{CS}$ is driven high at any point prior to receiving 24 bits, the transmission is discarded.

### Clear ($\overline{CLR}$)

The MAX5214/MAX5216 feature an asynchronous active-low $\overline{CLR}$ logic input that sets the DAC output to zero. Driving $\overline{CLR}$ low clears the contents of both the input and DAC registers and also aborts the on-going SPI command. To allow a new SPI command, drive $\overline{CLR}$ high.

### Power-Down Mode

The MAX5214/MAX5216 feature a software-controlled power-down mode. In power-down, the output disconnects from the buffer and is grounded with one of the three selectable internal resistors. See Table 3 for the selectable internal resistor values in power-down mode. The selected mode takes effect on the 16th SCLK falling edge of the MAX5214 and 24th SCLK falling edge of the MAX5216. The serial interface remains active in power-down mode. In order to abort the power-down mode selection, pull $\overline{CS}$ high prior to the 16th (MAX5214) or 24th (MAX5216) SCLK falling edge. The contents of the DAC register remain valid while in power-down mode, allowing for the DAC to return to previous code by writing 0x8000 for the MAX5214 or 0x800000 for the MAX5216 (Table 3). A write to the write-through register causes the device to immediately exit power-down mode and transition to the requested code (see Tables 1 and 2).

## Table 3. Power-Down Modes

| A1 | A0 | DESCRIPTION | DAC OPERATION CONDITION |
|---|---|---|---|
| 0 | 0 | DAC powers up and returns to its previous code setting. | Normal operation |
| 0 | 1 | DAC powers down; OUT is high impedance. | Power-down |
| 1 | 0 | DAC powers down; OUT connects to ground through an internal 100kΩ resistor. | |
| 1 | 1 | DAC powers down; OUT connects to ground through an internal 1kΩ resistor. | |

## Table 4. MAX5216 Input Code vs. Output Voltage

| DAC LATCH CONTENTS MSB → LSB | ANALOG OUTPUT ($V_{OUT}$) |
|---|---|
| 1111 1111 1111 1111 | $V_{REF}$ x (65,535/65,535) |
| 1000 0000 0000 0000 | $V_{REF}$ x (32,768/65,535) = 1/2 $V_{REF}$ |
| 0000 0000 0000 0001 | $V_{REF}$ x (1/65,535) |
| 0000 0000 0000 0000 | 0V |

## Table 5. MAX5214 Input Code vs. Output Voltage

| DAC LATCH CONTENTS MSB → LSB | ANALOG OUTPUT ($V_{OUT}$) |
|---|---|
| 1111 1111 1111 11XX | $V_{REF}$ x (16,383/16,383) |
| 1000 0000 0000 00XX | $V_{REF}$ x (8,192/16,383) = 1/2 $V_{REF}$ |
| 0000 0000 0000 01XX | $V_{REF}$ x (1/16,383) |
| 0000 0000 0000 00XX | 0V |

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

## Applications Information

### Power-On Reset (POR)

When first power is applied to $V_{DD}$, the input registers are set to zero so the DAC output is set to code zero. To optimize DAC linearity, wait until the supplies have settled. The MAX5214/MAX5216 output voltage range is 0 to $V_{REF}$.

### Power Supplies and Bypassing Considerations

Bypass $V_{DD}$ with high-quality 0.1µF ceramic capacitors to a low-impedance ground as close as possible to the device.

Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

### Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to the star ground for the DAC system. Refer the remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5214/MAX5216 GND. Carefully lay out the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to improve noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5214/MAX5216 package.

## Definitions

### Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

### Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL is greater than -1 LSB, the DAC guarantees no missing codes and is monotonic.

### Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point.

Typically, the point at which the offset error is specified is at or near the zero-scale point of the transfer function.

### Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

### Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

### Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

### Digital-to-Analog Glitch Impulse

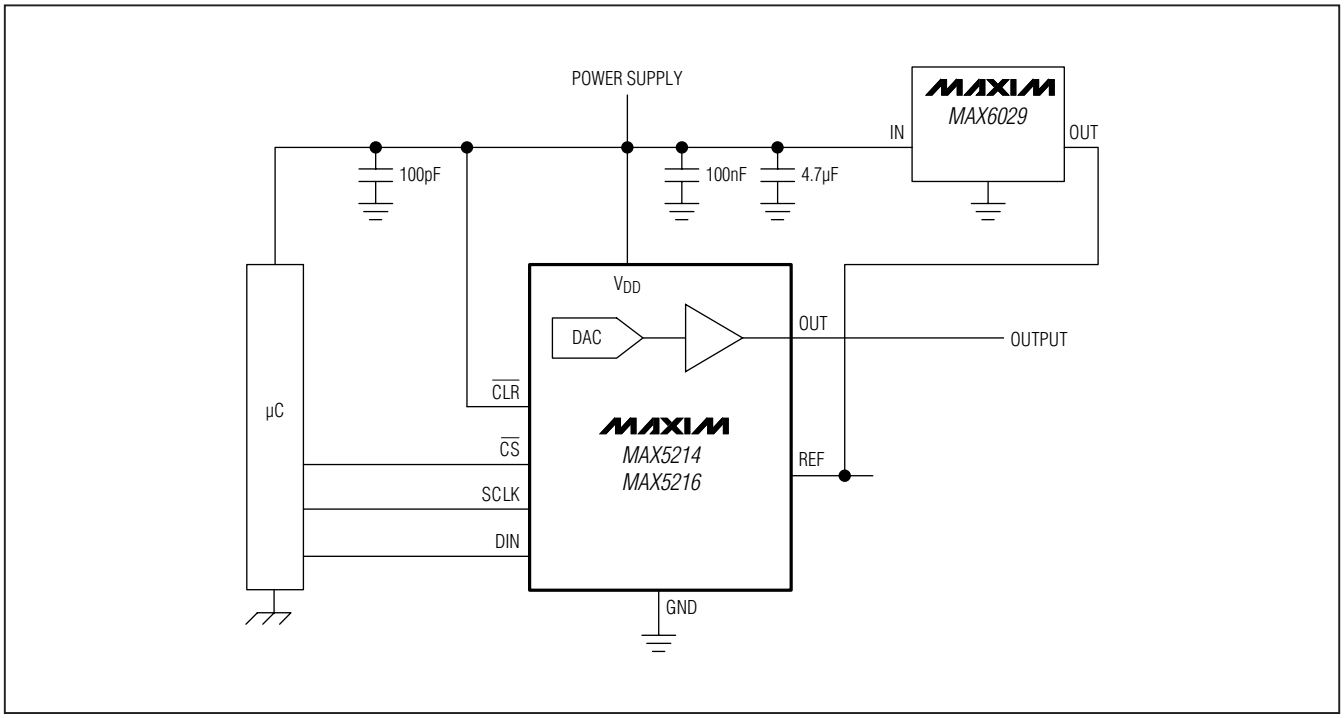
A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

### Digital-to-Analog Power-Up Glitch Impulse

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

## Typical Operating Circuit




## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 8 µMAX | U8+3 | 21-0036 | 90-0092 |

# 14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 12/10 | Initial release | — |