Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EVALUATION KIT AVAILABLE

MAX5318

18-Bit, High-Accuracy Voltage Output DAC with Digital Gain, Offset Control, and SPI Interface

General Description

The MAX5318 is a high-accuracy, 18-bit, serial SPI input, buffered voltage output digital-to-analog converter (DAC) in a 4.4mm x 7.8mm, 24-lead TSSOP package. The device features ±2 LSB INL (max) accuracy and a ±1 LSB DNL (max) accuracy over the full temperature range of -40°C to +105°C.

The DAC voltage output is buffered resulting in a fast settling time of 3µs and a low offset and gain drift of ±0.5ppm/°C of FSR (typ). The force-sense output (OUT) maintains accuracy while driving loads with long lead lengths. Additionally, a separate AVSS supply, allows the output amplifier to go to 0V (GND) while maintaining full linearity performance.

The MAX5318 includes user-programmable digital gain and offset correction to enable easy system calibration.

At power-up, the device resets its outputs to zero or mid-scale. The wide 2.7V to 5.5V supply voltage range and integrated low-drift, low-noise reference buffer amplifier make for ease of use.

The MAX5318 features a 50MHz 3-wire SPI interface. The MAX5318 is available in a 24-lead TSSOP package and operates over the -40°C to +105°C temperature range.

Applications

- Test and Measurement Equipment
- Automatic Test Equipment
- Gain and Offset Adjustment
- Data-Acquisition Systems
- Process Control and Servo Loops
- Programmable Voltage and Current Sources
- Automatic Tuning and Calibration
- Communication Systems
- Medical Imaging

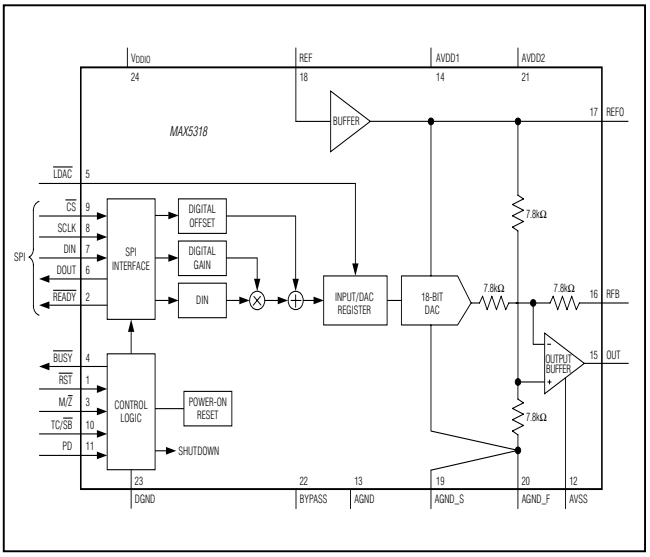
For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX5318.related.

Benefits and Features

- **Ideal for ATE and High-Precision Instruments**
  - ✧ **INL Accuracy Guaranteed with ±2 LSB (Max) Over Temperature**
- **Fast Settling Time (3µs) with 10kΩ || 100pF Load**
- **Safe Power-Up-Reset to Zero or Midscale DAC Output (Pin-Selectable)**
  - ✧ **Predetermined Output Device State in Power-Up and Reset in System Design**
- **Negative Supply (AVSS) Option Allows Full INL and DNL Performance to 0V**
- **SPI Interface Compatible with 1.8V to 5.5V Logic**
- **High Integration Reduces Development Time and PCB Area**
  - ✧ **Buffered Voltage Output Directly Drives 2kΩ Load Rail-to-Rail**
  - ✧ **Integrated Reference Buffer**
  - ✧ **No External Amplifiers Required**
- **Small 4.4mm x 7.8mm, 24-Pin TSSOP Package**

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6465; Rev 0; 9/12

ABSOLUTE MAXIMUM RATINGS

AGND to DGND .....-0.3V to +0.3V
AGND_F, AGND_S to AGND .....-0.3V to +0.3V
AGND_F, AGND_S to DGND .....-0.3V to +0.3V
AVDD to AGND .....-0.3V to +6V
AVDD to REF .....-0.3V to +6V
AVSS to AGND .....-2V to +0.3V
V_{DDIO} to DGND .....-0.3V to +6V
BYPASS to DGND ..... -0.3V to the lower of ($V_{AVDD\_}$ or V_{DDIO} + 0.3V) and +4.5V
OUT, REFO, RFB to AGND ..... -0.3V to the lower of (V_{AVDD} + 0.3V) and +6V
REF to AGND .....-0.3V to the lower of V_{AVDD} and +6V
SCLK, DIN, $\overline{CS}$, $\overline{BUSY}$, $\overline{LDAC}$, $\overline{READY}$, M/$\overline{Z}$, TC/$\overline{SB}$, $\overline{RST}$, PD, DOUT to DGND..... -0.3V to the lower of (V_{DDIO} + 0.3V) and +6V
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 13.9mW/°C above +70°C).....1111.1mW
Operating Temperature Range ..... -40°C to +105°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Case Thermal Resistance (θ_{JA}) .....13°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....72°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		18			Bits
Integral Nonlinearity (Note 3)	INL	DIN = 0x00000 to 0x3FFFF (binary mode), DIN = 0x20000 to 0x1FFFF (two's complement mode)	-2	±0.5	+2	LSB
		DIN = 0x01900 to 0x3FFFF (binary mode), DIN = 0x21900 to 0x1FFFF (two's complement mode), V_{AVSS} = 0V				
Differential Nonlinearity (Note 3)	DNL		-1	±0.275	+1	LSB
Zero Code Error	OE	DIN = 0, T_A = +25°C	-48	±4	+48	LSB
		DIN = 0, T_A = -40°C to +105°C		±14		
Zero Code Error Drift (Note 4)		DIN = 0	-1.6	±0.10	+1.6	ppm/°C
Gain Error	GE	T_A = +25°C	-16	±1	+16	LSB
		T_A = -40°C to +105°C		±27		
Gain Error Temperature Coefficient (Note 4)	TCGE		-2.5	±0.10	+2.5	ppm/°C of FSR
Output Voltage Range		No load	0		V_{AVDD} - 0.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Voltage Output	$V_{OUT-RESET}$	$\overline{RST}$ = pulse low	M/$\overline{Z}$ = DGND		75		µV
			M/$\overline{Z}$ = V_{DDIO}		2.048		V
		$\overline{RST}$ = pulse low, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		2.048		V
		$\overline{RST}$ = DGND	M/$\overline{Z}$ = DGND		-68		mV
			M/$\overline{Z}$ = V_{DDIO}		2.036		V
		$\overline{RST}$ = DGND, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		2.036		V
DC Output Impedance (Normal Mode)	R_{OUT}	Closed-loop connection (RFB connected to OUT)			4		mΩ
Output Resistance (Power-Down Mode)		PD = V_{DDIO}			2		kΩ
Output Current	I_{OUT}	Source/sink within 100mV of the supply rails			±4		mA
		Source/sink within 800mV of the supply rails			±25		
Load Capacitance to GND	C_L					200	pF
Load Resistance to GND	R_L	For specified performance		2			kΩ
Short-Circuit Current	I_{SC}	OUT shorted to AGND or AVDD			±60		mA
		REFO shorted to AGND or AVDD			±65		
		BYPASS shorted to AGND or AVDD			±48		
Short-Circuit Duration	T_{SC}	Short to AGND or AVDD			Indefinite		s
DC Power-Supply Rejection	DC PSRR	V_{OUT} at full scale, V_{AVDD} = 4.5V to 5.5V		-2.5	±0.20	+2.5	LSB/V
		V_{AVSS} = -1.5V to -0.5V		-2.5	±0.012	+2.5	
STATIC PERFORMANCE—VOLTAGE REFERENCE INPUT SECTION							
Reference High Input Range	V_{REF}			2.4		V_{AVDD} - 0.1	V
Reference Input Capacitance	C_{REF}				10		pF
Reference Input Resistance	R_{REF}				10		MΩ
Reference Input Current	I_B				±0.15		µA
STATIC PERFORMANCE—VOLTAGE REFERENCE OUTPUT SECTION							
Reference High Output Range				2.4		V_{AVDD} - 0.1	V
Reference High Output Load Regulation					500		ppm/mA
Reference Output Capacitor		R_{ESR} < 5Ω			0.1		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DDIO} = **4.5V to 5.5V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—V_{BYPASS} OUT SECTION						
Output Voltage	V_{BYPASS}		2.3	2.4	2.5	V
Load Capacitance to GND	C_L	Required for stability, R_{ESR} = 0.1Ω (typ)	1		8	µF
POWER-SUPPLY REQUIREMENTS						
Positive Analog Power-Supply Range	V_{AVDD}		4.5		5.5	V
Digital Interface Power-Supply Range	V_{DDIO}		1.8		V_{AVDD}	V
Negative Analog Power-Supply Range	V_{AVSS}		-1.5	-1.25	0	V
Positive Analog Power-Supply Current	I_{AVDD}	No load, external reference, output at zero scale		5.2	6.5	mA
Negative Analog Power-Supply Current	I_{AVSS}	No load, external reference, output at zero scale	-1.5	-1.0		mA
Interface Power-Supply Current	I_{VDDIO}	Digital inputs at V_{DDIO} or DGND		0.2	5.0	µA
Positive Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode		20	50	µA
Negative Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode	-5	-3		µA
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR	From 10% to 90% full scale, positive and negative transitions		4.9		V/µs
Voltage Output Settling Time	t_S	From falling edge of LDAC to within 0.003% FS, R_L = 10kΩ, DIN = 04000h (6.25% FS) to 3C000h (93.75% FS)		3		µs
Busy Time	t_{BUSY}	(Note 5)		1.9		µs
DAC Glitch Impulse		Major code transition (1FFFFh to 20000h), R_L = 10kΩ, C_L = 50pF		4		nVs
Digital Feed Through		CSB = V_{DDIO}, f_{SCLK} = 1kHz, all digital inputs from 0V to V_{DDIO}		1		nVs
Output Voltage-Noise Spectral Density		At f = 1kHz to 10kHz, without reference, code = 20000h		26		nV/√Hz
Output Voltage Noise		At f = 0.1Hz to 10Hz, without reference, code = 20000h		1.55		$µV_{P-P}$
Wake-Up Time		From power-down mode		75		µs
Power-Up Time		From power-off		2		ms

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, GAIN = 0x3FFFF, OFFSET = 0x00000, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			18			Bits
Integral Nonlinearity (Note 3)	INL	DIN = 0x00000 to 0x3FFFF (binary mode), DIN = 0x20000 to 0x1FFFF (two's complement mode)		-2.0	±0.75	+2.0	LSB
		DIN = 0x01900 to 0x3FFFF (binary mode), DIN = 0x21900 to 0x1FFFF (two's complement mode), V_{AVSS} = 0V					
Differential Nonlinearity (Note 3)	DNL			-1.0	±0.3	+1.0	LSB
Zero Code Error	OE	DIN = 0, T_A = +25°C		-50	±6	+50	LSB
		DIN = 0, T_A = -40°C to +105°C			±25		
Zero Code Error Drift (Note 4)		DIN = 0		-2.7	±1.4	+2.7	ppm/°C
Gain Error	GE	T_A = +25°C		-16	±1.5	+16	LSB
		T_A = -40°C to +105°C			±35		
Gain Error Temperature Coefficient (Note 4)	TCGE			-3.2		+3.2	ppm/°C of FSR
Output Voltage Range		No load		0		V_{AVDD} - 0.1	V
Reset Voltage Output	$V_{OUT-RESET}$	$\overline{RST}$ = pulse low	M/$\overline{Z}$ = DGND		75		µV
			M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = pulse low, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = DGND	M/$\overline{Z}$ = DGND		-40		mV
			M/$\overline{Z}$ = V_{DDIO}		1.25		V
		$\overline{RST}$ = DGND, V_{AVSS} = 0V	M/$\overline{Z}$ = DGND		10		mV
			M/$\overline{Z}$ = V_{DDIO}		1.24		V
DC Output Impedance	R_{OUT}	Closed-loop connection, RFB connected to OUT			4		mΩ
Output Current	I_{OUT}	Source/sink within 100mV of the supply rails			±4		mA
		Source/sink within 800mV of the supply rails			±25		
Load Capacitance to GND	C_L					200	pF
Load Resistance to GND	R_L	For specified performance		2			kΩ
Short-Circuit Current	I_{SC}	OUT shorted to AGND or AVDD			±60		mA
		REFO shorted to AGND or AVDD			±65		
		BYPASS shorted to AGND or AVDD			±48		
Short-Circuit Duration	t_{SC}	Short to AGND or AVDD			Indefinite		s

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, GAIN = 0x3FFFF, OFFSET = 0x00000, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Power-Supply Rejection	DCPSRR	V_{OUT} at full scale, V_{AVDD} = 2.7V to 3.3V	-2.5	±0.4	+2.5	LSB/V
		V_{AVSS} = -1.5V to -0.5V	-2.5	±0.04	+2.5	
STATIC PERFORMANCE—VOLTAGE REFERENCE INPUT SECTION						
Reference High Input Range	V_{REF}		2.4		V_{AVDD} - 0.1	V
Reference Input Capacitance	C_{REF}			10		pF
Reference Input Resistance	R_{REF}			10		MΩ
Reference Input Current	IB			±0.15		µA
STATIC PERFORMANCE—VOLTAGE REFERENCE OUTPUT SECTION						
Reference High Output Range			2.4		V_{AVDD} - 0.1	V
Reference High Output Load Regulation				500		ppm/mA
Reference Output Capacitor		R_{ESR} < 5Ω		0.1		nF
STATIC PERFORMANCE—V_{BYPASS} OUT SECTION						
Output Voltage	V_{BYPASS}		2.3	2.4	2.5	V
Load Capacitance to GND	C_L	Required for stability, R_{ESR} = 0.1Ω (typ)	1		8	µF
POWER-SUPPLY REQUIREMENTS						
Positive Analog Power-Supply Range	V_{AVDD}		2.7		3.3	V
Interface Power-Supply Range	V_{DDIO}		1.8		5.5	V
Negative Analog Power-Supply Range	V_{AVSS}		-1.5	-1.25	0	V
Positive Analog Power-Supply Current	I_{AVDD}	No load, external reference, output at zero scale		5.0	6.5	mA
Negative Analog Power-Supply Current	I_{AVSS}	No load, external reference, output at zero scale	-1.5	-0.8		mA
Interface Power-Supply Current	I_{VDDIO}	Digital inputs at V_{DDIO} or DGND		0.2	5.0	µA
Positive Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode		20	50	µA
Negative Analog Power-Supply Power-Down Current		PD = V_{DDIO}, power-down mode	-5	-2		µA
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR	From 10% to 90% full scale, positive and negative transitions		4.9		V/µs
Voltage Output Settling Time	t_S	From falling edge of LDAC to within 0.003% FS, R_L = 10kΩ, DIN = 04000h (6.25% FS) to 3C000h (93.75% FS)		3		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DDIO} = **2.7V to 3.3V**, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V, V_{REF} = 2.5V, TC/$\overline{SB}$ = PD = $\overline{LDAC}$ = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, GAIN = 0x3FFFF, OFFSET = 0x00000, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (GAIN = 0x3FFFF and OFFSET = 0x00000.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Busy Time	t_{BUSY}	(Note 5)		1.9		µs
DAC Glitch Impulse		Major code transition (1FFFFh to 20000h), R_L = 10kΩ, C_L = 50pF		2.5		nVs
Digital Feedthrough		CSB = V_{DDIO}, f_{SCLK} = 1kHz, all digital inputs from 0V to V_{DDIO}		1		nVs
Output Voltage-Noise Spectral Density		At f = 1kHz to 10kHz, without reference, code = 20000h		26		nV/√Hz
Output Voltage Noise		At f = 0.1Hz to 10Hz, without reference, code = 20000h		1.55		μV_{P-P}
Wake-Up Time		From power-down mode		75		µs
Power-Up Time		From power-off		2		ms

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 5V, V_{DDIO} = **2.7V to 5.5V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$ = DGND, C_{REFO} = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)(GAIN = 0x3FFFF and OFFSET = 0x00000.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$, M/$\overline{Z}$, $\overline{RST}$)						
Input High Voltage	V_{IH}		0.7 x V_{DDIO}			V
Input Low Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Hysteresis (Note 4)	V_{IHYST}		200	300		mV
Input Leakage Current	I_{IN}			±0.1	±1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUT CHARACTERISTICS (DOUT, $\overline{READY}$, $\overline{BUSY}$)						
Output Low Voltage	V_{OL}	I_{SOURCE} = 5.0mA			0.25	V
Output High Voltage	V_{OH}	I_{SINK} = 5.0mA, except for $\overline{BUSY}$	V_{DDIO} - 0.25			V
Output Three-State Leakage	I_{OZ}	DOUT only		±0.1	±1	µA
Output Three-State Capacitance	C_{OZ}	DOUT only		15		pF
Output Short-Circuit Current	I_{OSS}	V_{DDIO} = 5.25V		±150		mA

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 5V, V_{DDIO} = **2.7V to 5.5V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$ = DGND, C_{REFO} = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)(GAIN = 0x3FFFF and OFFSET = 0x00000.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Serial Clock Frequency	f_{SCLK}	Stand-alone, write mode				50	MHz
		Stand-alone, read mode and daisy-chained read and write modes (Note 5)				12.5	
SCLK Period	t_{CP}	Stand-alone, write mode		20			ns
		Stand-alone, read mode and daisy-chained read and write modes		80			
SCLK Pulse Width High	t_{CH}	40% duty cycle		8			ns
SCLK Pulse Width Low	t_{CL}	40% duty cycle		8			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSSO}	First SCLK falling edge	Stand-alone, write mode	8			ns
			Stand-alone, read mode and daisy-chained read and write modes	38			
$\overline{CS}$ Fall to SCLK Fall Hold Time	t_{CSH0}	Inactive falling edge preceding first falling edge		0			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}	24th falling edge		2			ns
DIN to SCLK Fall Setup Time	t_{DS}			5			ns
DIN to SCLK Fall Hold Time	t_{DH}			4.5			ns
SCLK Rise to DOUT Settle Time	t_{DOT}	C_L = 20pF (Note 6)				32	ns
SCLK Rise to DOUT Hold Time	t_{DOH}	C_L = 0pF (Note 6)		2			ns
SCLK Fall to DOUT Disable Time	t_{DOZ}	24th active edge deassertion		2		30	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	Asynchronous assertion		2		30	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSDOZ}	Stand-alone, aborted sequence				35	ns
		Daisy-chained, aborted sequence				70	
SCLK Fall to $\overline{READY}$ Fall	t_{CRF}	24th falling-edge assertion, C_L = 20pF				30	ns
SCLK Fall to $\overline{READY}$ Hold	t_{CRH}	24th falling-edge assertion, C_L = 0pF		2			ns
SCLK Fall to $\overline{BUSY}$ Fall	t_{CBF}	$\overline{BUSY}$ assertion			5		ns
$\overline{CS}$ Rise to $\overline{READY}$ Rise	t_{CSR}	C_L = 20pF				35	ns
$\overline{CS}$ Rise to SCLK Fall	t_{CSA}	24th falling edge, aborted sequence		20			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	Stand alone		20			ns
SCLK Fall to $\overline{CS}$ Fall	t_{CSF}	24th falling edge		100			ns
$\overline{LDAC}$ Pulse Width	t_{LDPW}			20			ns
$\overline{LDAC}$ Fall to SCLK Fall Hold	t_{LDH}	Last active falling edge		20			ns
$\overline{RST}$ Pulse Width	t_{RSTPW}			20			ns

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 5V, V_{DDIO} = **1.8V to 2.7V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$ = DGND, C_{REFO} = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)(GAIN = 0x3FFFF and OFFSET = 0x00000.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$, M/$\overline{Z}$, $\overline{RST}$)						
Input High Voltage	V_{IH}		0.8 x V_{DDIO}			V
Input Low Voltage	V_{IL}				0.2 x V_{DDIO}	V
Input Hysteresis (Note 4)	V_{IHYST}		200	300		mV
Input Leakage Current	I_{IN}	Input = 0V at V_{DDIO}		±0.1	±1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS CHARACTERISTICS (DOUT, $\overline{READY}$, $\overline{BUSY}$)						
Output Low Voltage	V_{OL}	I_{SOURCE} = 1.0mA			0.2	V
Output High Voltage	V_{OH}	I_{SINK} = 1.0mA, except for $\overline{BUSY}$	V_{DDIO} - 0.2			V
Output Three-State Leakage	I_{OZ}	DOUT only		±0.1	±1	µA
Output Three-State Capacitance	C_{OZ}	DOUT only		15		pF
Output Short-Circuit Current	I_{OSS}	V_{DDIO} = 2.7V		±150		mA
TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCLK}	Stand-alone write mode			50	MHz
		Stand-alone read mode and daisy-chained read and write modes (Note 6)			8	
SCLK Period	t_{CP}	Stand-alone write mode	20			ns
		Stand-alone read mode and daisy-chained read and write modes	125			
SCLK Pulse-Width High	t_{CH}	40% duty cycle	9			ns
SCLK Pulse-Width Low	t_{CL}	40% duty cycle	9			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSSO}	First SCLK falling edge, Stand-alone write mode	12			ns
		First SCLK falling edge, Stand-alone read mode and daisy-chained read and write modes	72			
$\overline{CS}$ Fall to SCLK Fall Hold Time	t_{CSH0}	Inactive falling edge preceding first falling edge	0			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}	24th falling edge	4			ns
DIN to SCLK Fall Setup Time	t_{DS}		8			ns
DIN to SCLK Fall Hold Time	t_{DH}		8			ns
SCLK Rise to DOUT Settle Time	t_{DOT}	C_L = 20pF (Note 7)			40	ns
SCLK Rise to DOUT Hold Time	t_{DOH}	C_L = 0pF (Note 7)	2			ns

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 5V, V_{DDIO} = **1.8V to 2.7V**, V_{AVSS} = -1.25V, V_{REF} = 4.096V, R_L = 10kΩ, TC/$\overline{SB}$ = M/$\overline{Z}$ = DGND, C_{REFO} = 100pF, C_{BYPASS} = 1µF, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)(GAIN = 0x3FFFF and OFFSET = 0x00000.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to DOUT Disable Time	t_{DOZ}	24th active edge deassertion	2		40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	Asynchronous assertion	2		50	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSDOZ}	Stand-alone, aborted sequence			70	ns
		Daisy-chained, aborted sequence			130	
SCLK Fall to $\overline{READY}$ Fall	t_{CRF}	24th falling edge assertion, C_L = 20pF			60	ns
SCLK Fall to $\overline{READY}$ Hold	t_{CRH}	24th falling edge assertion, C_L = 0pF	2			ns
SCLK Fall to $\overline{BUSY}$ Fall	t_{CBF}	$\overline{BUSY}$ assertion		5		ns
$\overline{CS}$ Rise to $\overline{READY}$ Rise	t_{CSR}	C_L = 20pF			60	ns
$\overline{CS}$ Rise to SCLK Fall	t_{CSA}	24th falling edge, aborted sequence	20			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	Stand alone	20			ns
SCLK Fall to $\overline{CS}$ Fall	t_{CSF}	24th falling edge	100			ns
$\overline{LDAC}$ Pulse Width	t_{LDPW}		20			ns
$\overline{LDAC}$ Fall to SCLK Fall Hold	t_{LDH}	Last active falling edge	20			ns
$\overline{RST}$ Pulse Width	t_{RSTPW}		20			ns

Note 2: All devices are 100% tested at T_A = +25°C and T_A = +105°C. Limits at T_A = -40°C are guaranteed by design.
Note 3: Linearity is tested from V_{REF} to AGND.
Note 4: Guaranteed by design.
Note 5: The total analog throughput time from DIN to V_{OUT} is the sum of t_S and t_{BUSY} (4.9µs, typ).
Note 6: Daisy-chain speed is relaxed to accommodate (t_{CRF} + t_{CSS0}).
Note 7: DOUT speed limits overall SPI speed..

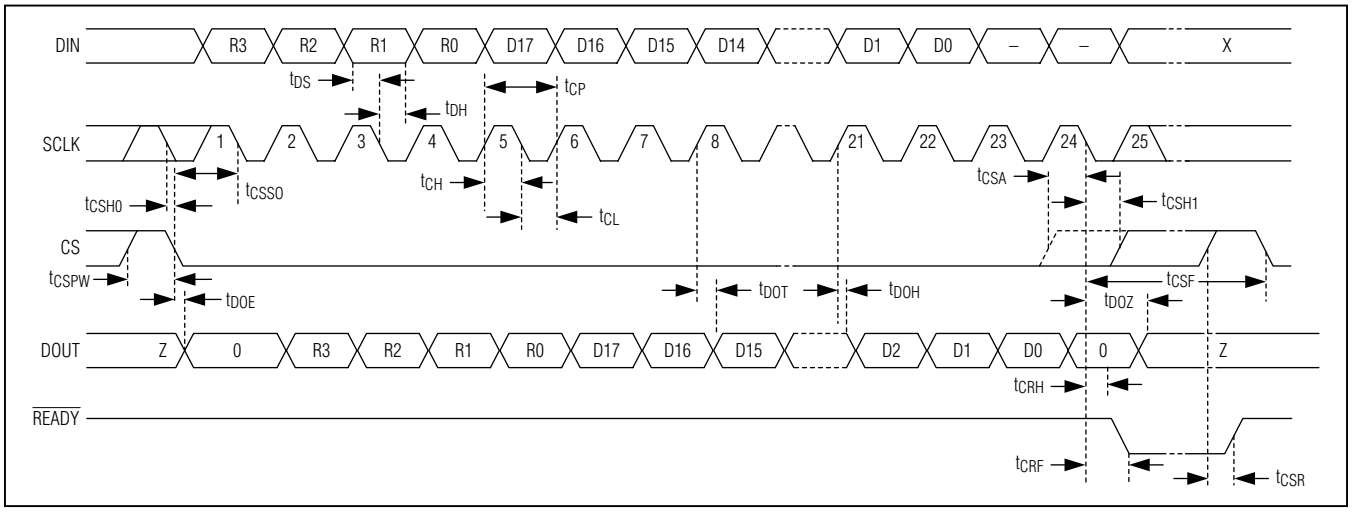
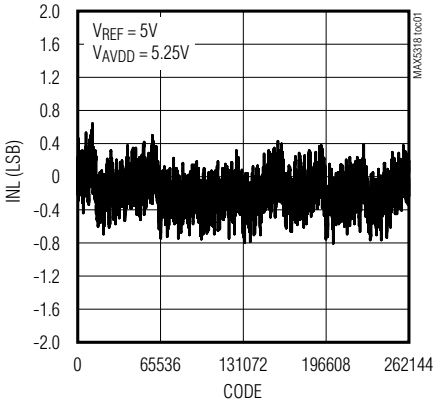


Figure 1. Serial Interface Timing Diagram, Stand-Alone Operation

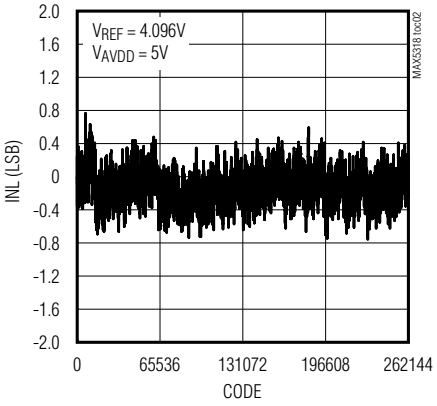
Typical Operating Characteristics

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

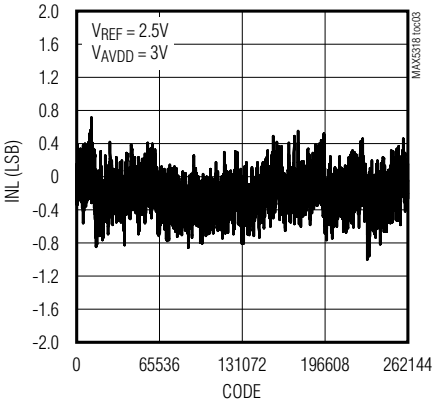
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



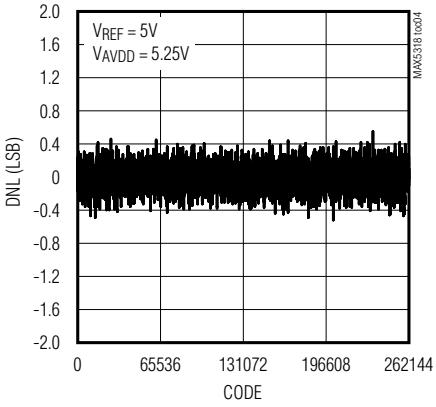
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



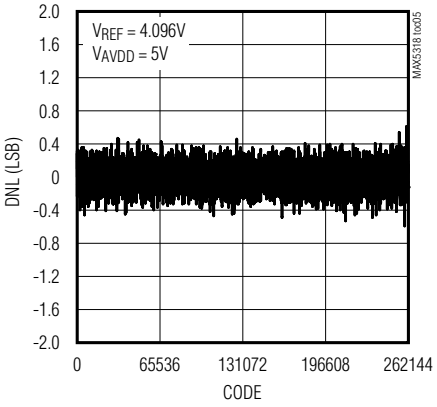
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



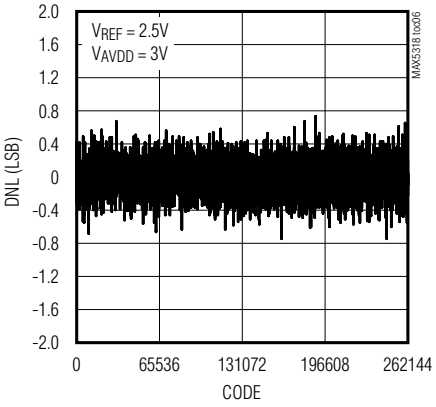
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



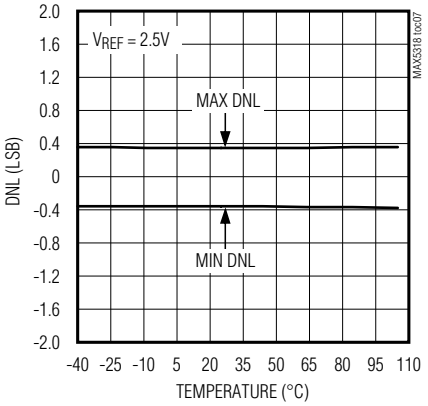
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



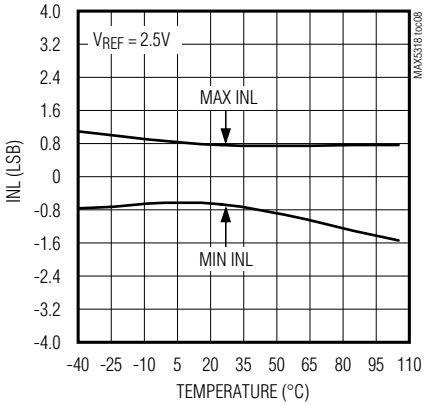
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

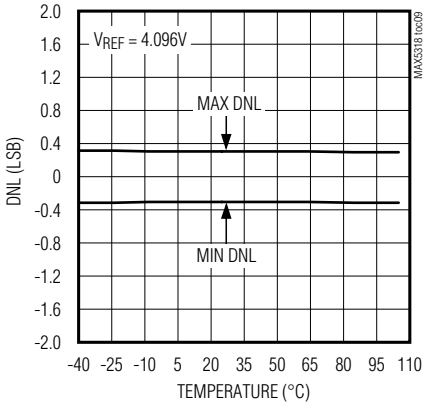
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



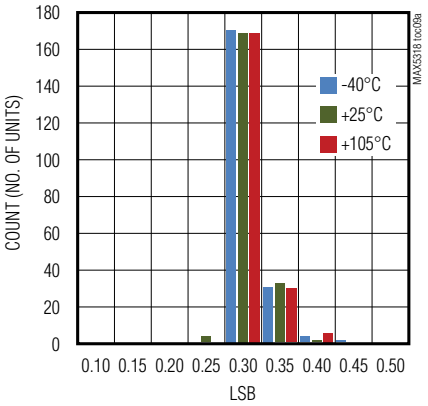
INTEGRAL NONLINEARITY vs. TEMPERATURE



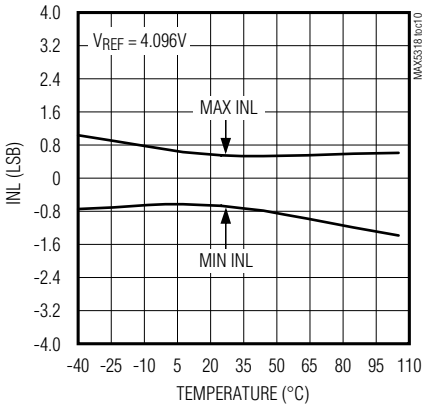
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



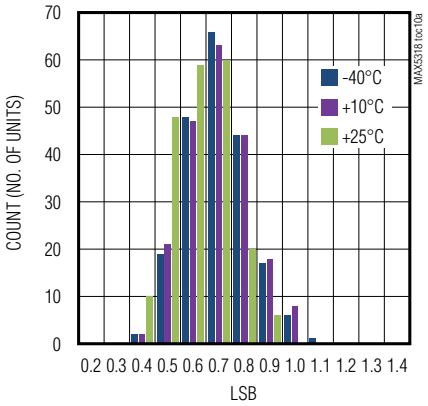
DNL DISTRIBUTION vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INL DISTRIBUTION vs. TEMPERATURE

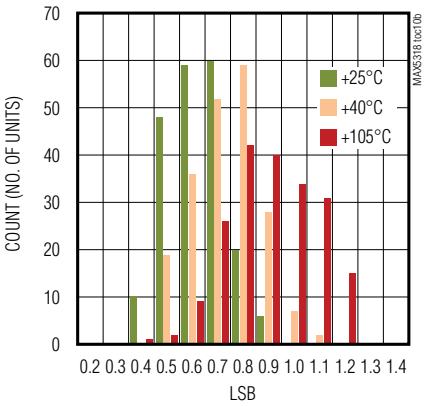


18-Bit, High-Accuracy Voltage Output DAC with Digital Gain, Offset Control, and SPI Interface

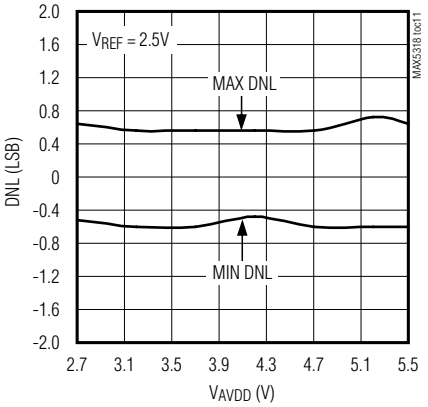
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

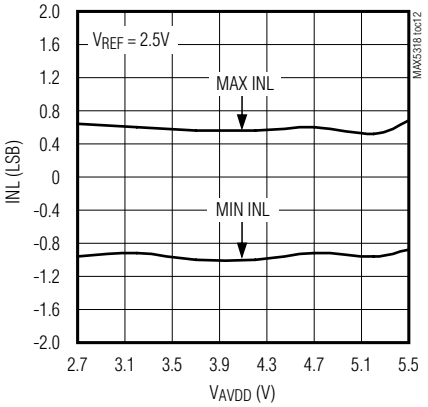
INL DISTRIBUTION vs. TEMPERATURE



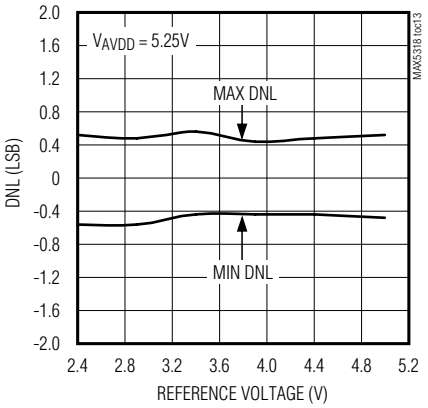
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



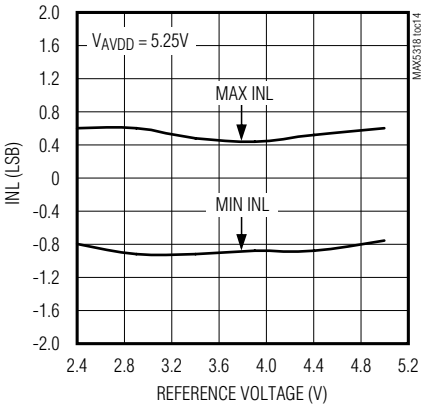
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



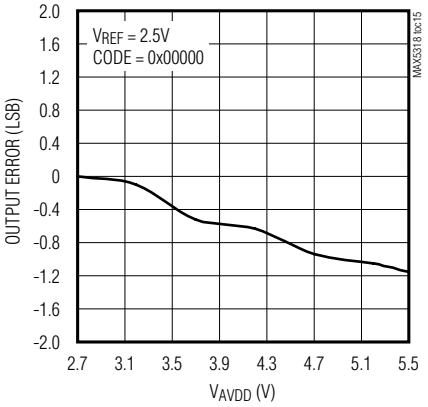
DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE



INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



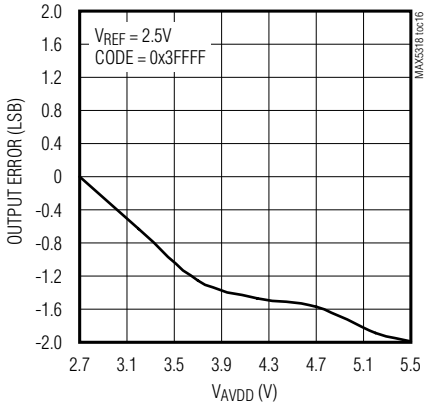
ZERO-SCALE OUTPUT ERROR vs. SUPPLY VOLTAGE



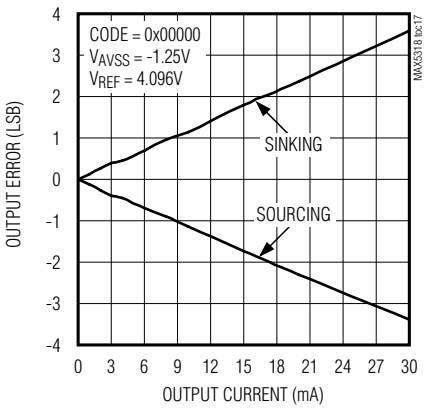
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

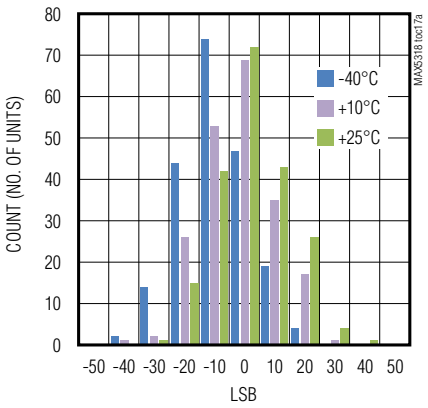
FULL-SCALE OUTPUT ERROR vs. SUPPLY VOLTAGE



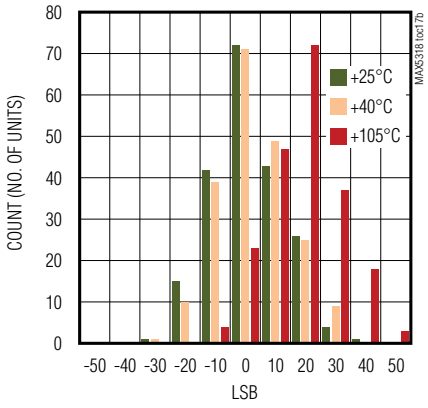
ZERO-SCALE OUTPUT ERROR vs. OUTPUT CURRENT



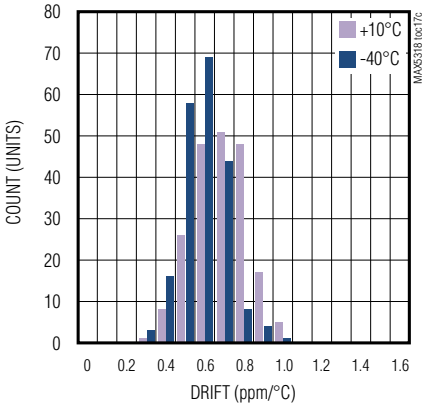
ZERO CODE ERROR DISTRIBUTION vs. TEMPERATURE



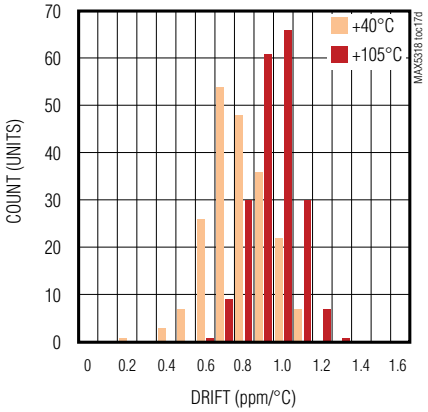
ZERO CODE ERROR DISTRIBUTION vs. TEMPERATURE



ZERO CODE ERROR DRIFT



ZERO CODE ERROR DRIFT

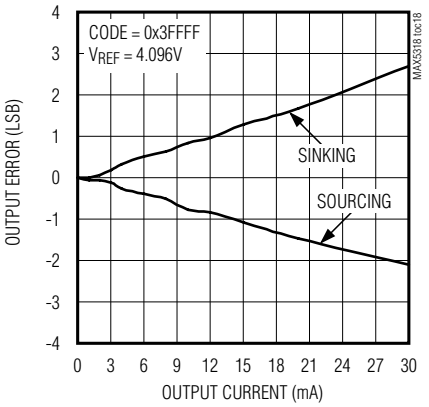


18-Bit, High-Accuracy Voltage Output DAC with Digital Gain, Offset Control, and SPI Interface

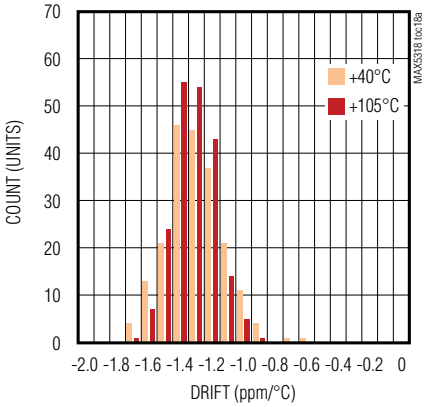
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

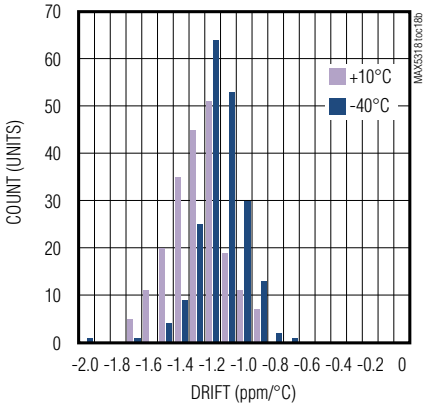
FULL-SCALE OUTPUT ERROR vs. OUTPUT CURRENT



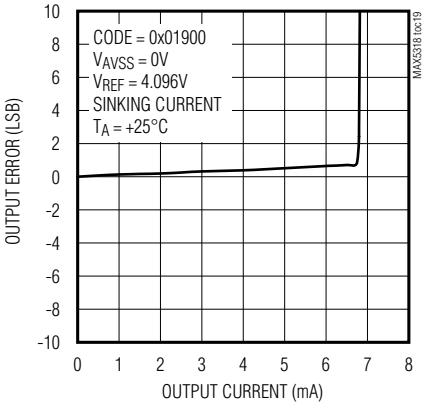
GAIN ERROR TEMPERATURE COEFFICIENT



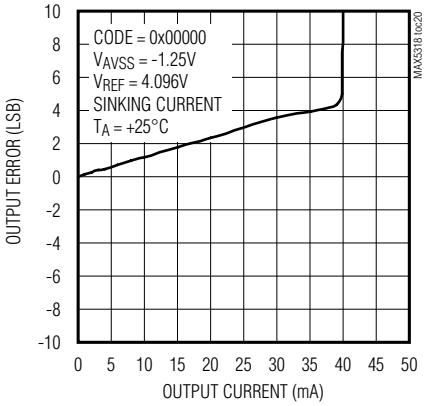
GAIN ERROR TEMPERATURE COEFFICIENT



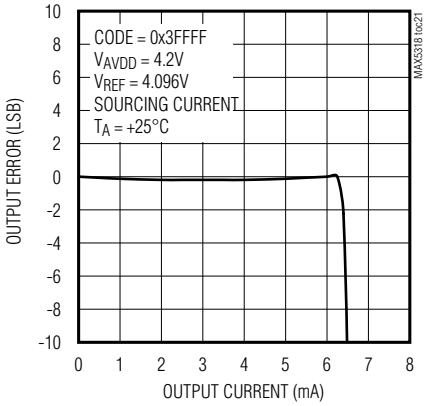
OUTPUT DRIVE CAPABILITY



OUTPUT DRIVE CAPABILITY



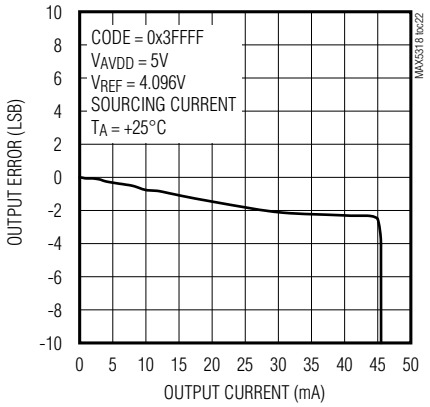
OUTPUT DRIVE CAPABILITY



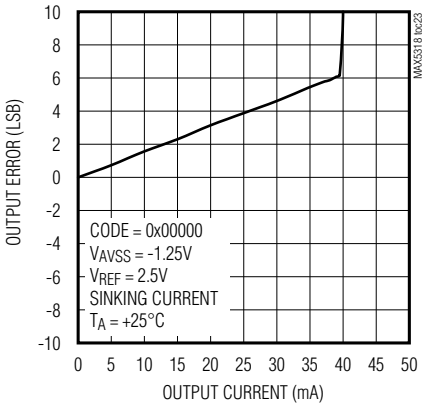
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

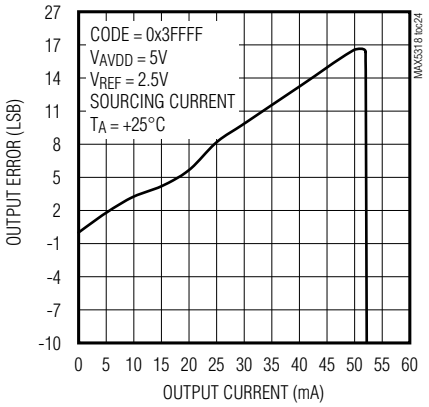
OUTPUT DRIVE CAPABILITY



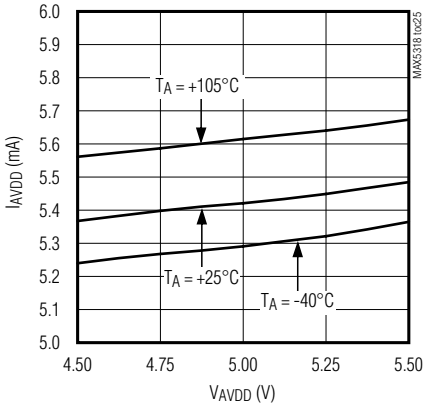
OUTPUT DRIVE CAPABILITY



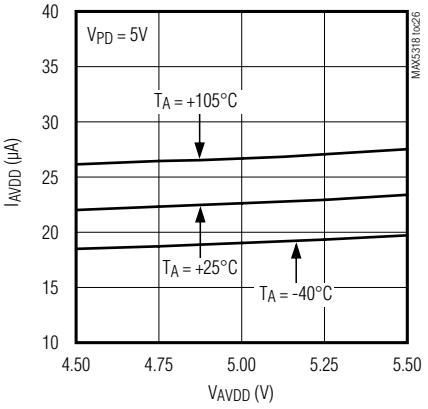
OUTPUT DRIVE CAPABILITY



SUPPLY CURRENT vs. SUPPLY VOLTAGE



POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE

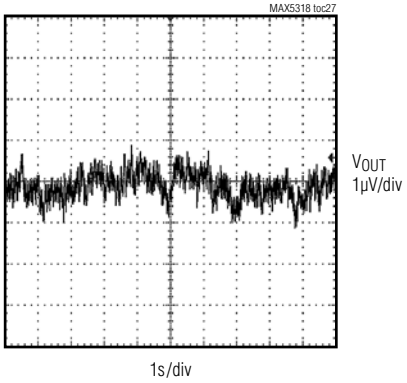


18-Bit, High-Accuracy Voltage Output DAC with Digital Gain, Offset Control, and SPI Interface

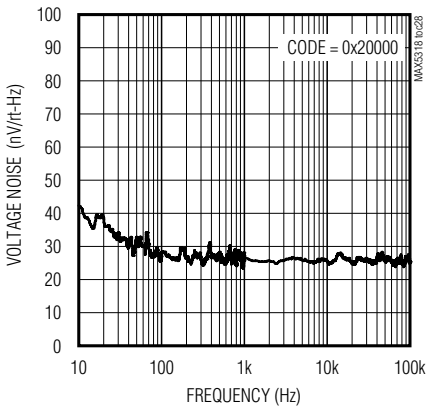
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

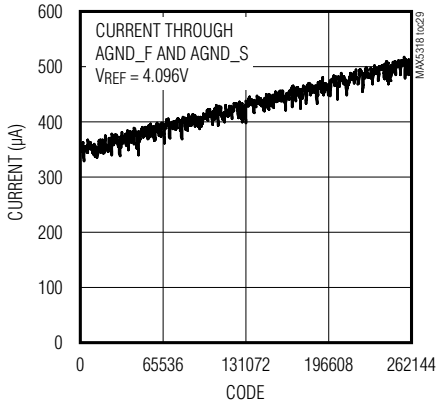
0.1Hz TO 10Hz OUTPUT NOISE



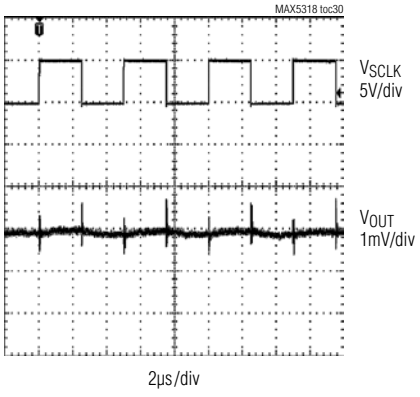
OUTPUT NOISE DENSITY



GROUND CURRENT vs. CODE



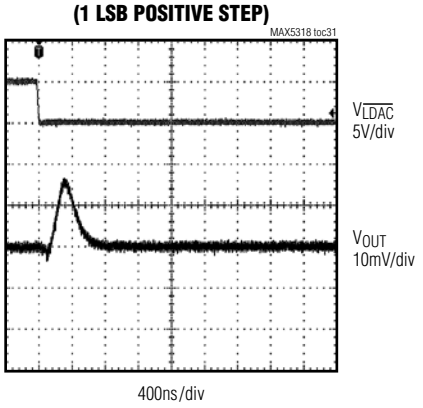
DIGITAL CLOCK FEEDTHROUGH



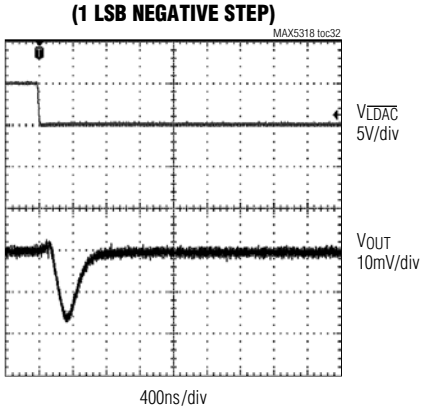
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

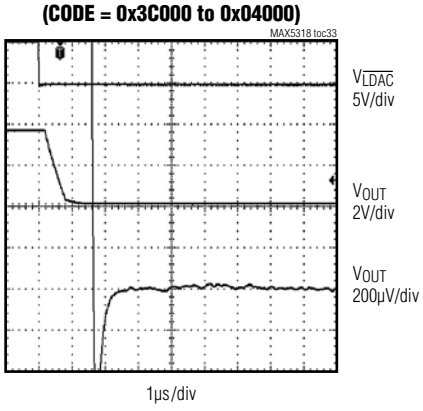
MAJOR CARRY GLITCH (1 LSB POSITIVE STEP)



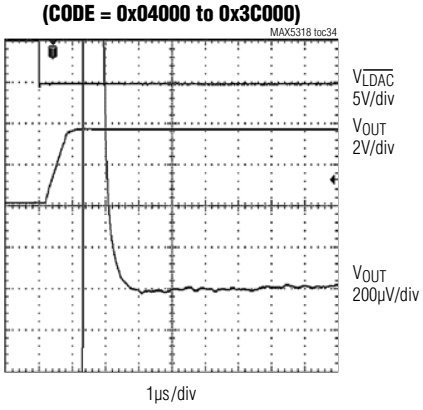
MAJOR CARRY GLITCH (1 LSB NEGATIVE STEP)



SETTLING TIME (CODE = 0x3C000 to 0x04000)



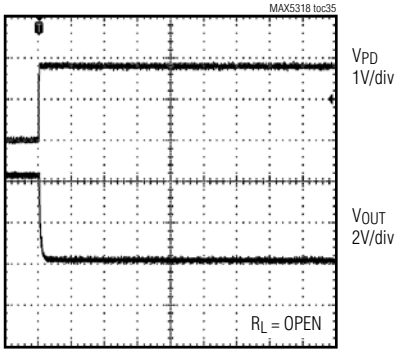
SETTLING TIME (CODE = 0x04000 to 0x3C000)



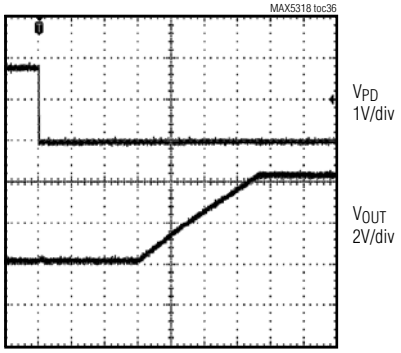
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DDIO} = 5V, V_{AVSS} = -1.25V, V_{AGND} = V_{DGND} = V_{AGND_F} = V_{AGND_S} = 0V; V_{REF} = 4.096V, TC/$\overline{SB}$ = PD = M/$\overline{Z}$ = DGND, $\overline{RST}$ = V_{DDIO}, C_{REFO} = 100pF, C_L = 100pF, R_L = 10kΩ, C_{BYPASS} = 1µF, T_A = +25°C, unless otherwise noted.)

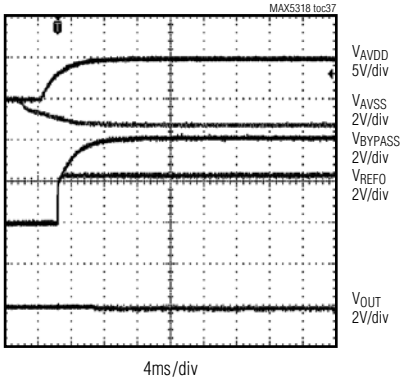
ENTERING POWER-DOWN RESPONSE



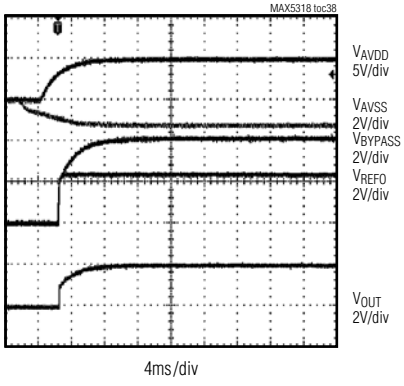
EXITING POWER-DOWN RESPONSE



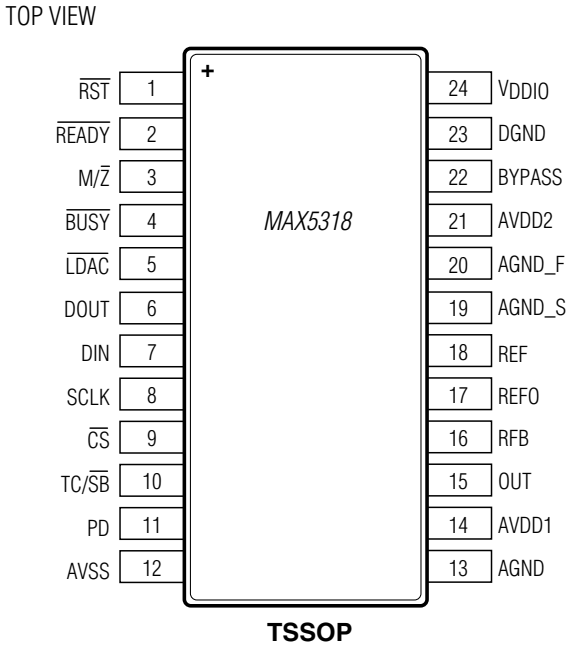
SLOW POWER-UP RESPONSE (RSTSEL = LOW)



SLOW POWER-UP RESPONSE (RSTSEL = HIGH)



Pin Configuration



TSSOP

Pin Description

PIN	NAME	FUNCTION
1	$\overline{RST}$	Active-Low Reset Input. Drive $\overline{RST}$ low to DGND to put the device into a reset state. A reset state sets all SPI input registers to their default power-on reset states as defined by the state of inputs M/$\overline{Z}$ and TC/$\overline{SB}$. Set $\overline{RST}$ high to VDDIO, the DAC output remains at the state defined by M/$\overline{Z}$ until $\overline{LDAC}$ is taken low.
2	$\overline{READY}$	SPI Active-Low Ready Output. $\overline{READY}$ asserts low when the device successfully completes processing an SPI data frame. $\overline{READY}$ asserts high at the next rising edge of $\overline{CS}$. In daisy-chain applications, the $\overline{READY}$ output typically drives the $\overline{CS}$ input of the next device in the chain or a GPIO of a microcontroller.
3	M/$\overline{Z}$	Reset Select Input. M/$\overline{Z}$ selects the default state of the analog output (OUT) after power-on or a hardware or software reset. Connect M/$\overline{Z}$ to V_{DDIO} to set the default output voltage to midscale or to DGND to set the default output voltage to zero scale.
4	$\overline{BUSY}$	Digital Input/Open-Drain Output. Connect a 2kΩ pullup resistor from $\overline{BUSY}$ to V_{DDIO}. $\overline{BUSY}$ goes low during the internal calculations of the DAC register data. During this time, the user can continue writing new data to the DIN, OFFSET, and GAIN registers, but no further updates to the DAC register and DAC output can take place. If $\overline{LDAC}$ is asserted low while $\overline{BUSY}$ is low, this event is stored. $\overline{BUSY}$ is bidirectional, and can be asserted low externally to delay $\overline{LDAC}$ action. $\overline{BUSY}$ also goes low during power-on reset, when $\overline{RST}$ is low, or when software reset is activated.

Pin Description (continued)

PIN	NAME	FUNCTION
5	$\overline{LDAC}$	Active-Low Load DAC Logic Input. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is inactive (high), the contents of the input registers are transferred to the DAC register and the DAC output is updated. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is asserted low, the $\overline{LDAC}$ event is stored and the DAC register update is delayed until $\overline{BUSY}$ deasserts. Any event on $\overline{LDAC}$ during power-on reset or when $\overline{RST}$ is low is ignored.
6	DOUT	SPI Bus Serial Data Output. See the *Serial Interface* section for details.
7	DIN	SPI Bus Serial Data Input. See the *Serial Interface* section for details.
8	SCLK	SPI Bus Serial Clock Input. See the *Serial Interface* section for details.
9	$\overline{CS}$	SPI Bus Active-Low Chip-Select Input. See the *Serial Interface* section for details.
10	TC/$\overline{SB}$	DIN Format Select Input. Connect TC/$\overline{SB}$ to DGND to set the data input format to straight binary or to V_{DDIO} to set it to two's complement.
11	PD	Active-High Power-Down Input. Connect PD to DGND for normal operation. Connect PD to V_{DDIO} to place the device in power-down. In power-down, OUT (analog voltage output) is connected to AGND through a 2kΩ resistor, but the contents of the input registers and the DAC latch do not change. The SPI interface remains active in power-down.
12	AVSS	Negative Analog Power-Supply Input. Connect to AGND or a negative supply voltage. When connected to the negative supply voltage, bypass AVSS with a 0.1µF capacitor to AGND.
13	AGND	Analog Ground. Connect to the analog ground plane.
14	AVDD1	Positive Analog Power-Supply Input. Bypass each AVDD_ locally with a 0.1µF and 10µF capacitor to AGND (analog ground plane). Connect AVDD1 and AVDD2 together.
15	OUT	Buffered Analog Voltage Output. Connect OUT to RFB externally to close the output buffer feedback loop. The buffered output is capable of directly driving a 10kΩ load. The state of M/$\overline{Z}$ sets the power-on reset state of OUT (zero or midscale). In power-down, OUT is connected to AGND through a 2kΩ pulldown resistor.
16	RFB	Feedback Resistor Input. RFB is connected through the internal feedback resistor to the inverting input of the analog output buffer. Externally connect RFB to OUT to close the output buffer feedback loop.
17	REFO	Voltage Reference Buffered Output. Bypass with a 100pF capacitor to AGND.
18	REF	High-Impedance 10MΩ Voltage Reference Input
19	AGND_S	DAC Analog Ground Sense
20	AGND_F	DAC Analog Ground Force. Connect to the analog ground plane.
21	AVDD2	Positive Analog Power-Supply Input. AVDD2 supplies power to the internal digital linear regulator. Bypass AVDD2 locally to AGND with 0.1µF and 10µF capacitors. Connect AVDD2 and AVDD1 together.
22	BYPASS	Internal Bypass Connection. Connect BYPASS to DGND with 0.01µF and 1µF capacitors.
23	DGND	Digital Ground
24	V_{DDIO}	Digital Interface Power-Supply Input. Connect to a 1.8V to 5.5V logic-level supply. Bypass V_{DDIO} with a 0.1µF capacitor to DGND. The supply voltage at V_{DDIO} sets the logic-level for the digital interface.

Detailed Description

The MAX5318 is a high-accuracy, 18-bit, serial SPI input, buffered voltage output digital-to-analog converter (DAC) in a 4.4mm x 7.8mm, 24-lead TSSOP package. The device features ±2 LSB INL (max) accuracy and a ±1 LSB DNL (max) accuracy over the full temperature range of -40°C to +105°C.

The DAC voltage output is buffered resulting in a fast settling time of 3µs and a low offset and gain drift of ±0.5ppm/°C of FSR (typ). The force-sense output (OUT) maintains accuracy while driving loads with long lead lengths. Additionally, a separate AVSS supply allows the output amplifier to go to 0V (GND) while maintaining full linearity performance.

The MAX5318 includes user-programmable digital gain and offset correction capability to enable easy system calibration.

At power-up, the device resets its outputs to zero or mid-scale, providing additional safety for applications, which drive valves or other transducers that need to be off on power-up. This is selected by the state of the M/$\overline{Z}$ input on power-up.

The wide 2.7V to 5.5V supply voltage range and integrated low-drift, low-noise reference buffer amplifier makes for ease of use. Since the reference buffer input has a high input resistance, an external buffer is not required. The device accepts an external reference between 2.4V and V_{AVDD} - 0.1V for maximum flexibility and rail-to-rail operation.

The MAX5318 features a 50MHz, 3-wire SPI, QSPI, MICROWIRE, and DSP-compatible serial interface. The separate digital interface supply voltage input (V_{DDIO}) is compatible with a wide range of digital logic levels from 1.8V to 5.5V, eliminating the need for separate voltage translators.

DAC Reference Buffer

The external reference input has a high input (REF) impedance of 10MΩll10pF and accepts an input voltage from +2.4V to V_{AVDD} - 0.1V. Connect an external reference supply between REF and AGND. Bypass the reference buffer output REFO to AGND with a 100pF capacitor. Connect the anode of an external Schottky diode to REF and the cathode to AVDD1 to prevent internal ESD diode conduction in the event that the reference voltage comes up before AVDD at power up. Follow the recommendations described in the *Power-Supply Sequencing* section.

Visit **www.maximintegrated.com/products/references** for a list of available external voltage-reference devices.

Output Amplifier (OUT)

The MAX5318 includes an internal buffer for the DAC output. The internal buffer provides improved load regulation for the DAC output. The output buffer slews at 5V/µs and drives up to 2kΩ in parallel with 200pF. The buffer has a rail-to-rail output capable of swinging to within 100mV of AVDD_ and AVSS.

The positive analog supply voltage (AVDD_) determines the maximum output voltage of the device as AVDD_ powers the output buffer.

The output is diode clamped to ground, preventing negative voltage excursions beyond approximately -0.6V.

Negative Supply Voltage (AVSS)

The negative supply voltage (AVSS) determines the minimum output voltage. If AVSS is connected to ground, the output voltage can be set to as low as 100mV without degrading linearity. For operation down to 0V, connect AVSS to a negative supply voltage between -0.1V and -1.5V. The MAX1735 is recommended for generating -1.25V from a -5V supply.

Force/Sense

The MAX5318 uses force/sense techniques to ensure that the load is regulated to the desired output voltage despite line drops due to long lead lengths. Since AGND_F and AGND_S have code dependent ground currents, a ground impedance less than 13mΩ ensures that the INL will not degrade by more than 0.1 LSB. Form a star ground connection (Figure 2a) near the device with AGND_F, AGND_S, and AGND tied together. Always refer remote DAC loads to this system ground for best performance. Figure 2b shows how to configure the device and an external op amp for proper force/sense operation. The amplifier provides as much drive as needed to force the sensed voltage (measured between RFB and AGND_S) to equal the desired voltage.

18-Bit Ideal Transfer Function

The MAX5318 features 18-bit gain and 18-bit offset adjustment as shown in Figure 3.

The incoming DIN code is multiplied and offset compensated by the generic equation shown in Equation 1. The resulting value is then applied to the DAC.

Equation 1) Generic gain and offset adjustment

$$DAC = DIN \times GAIN + OFFSET$$

The GAIN code is always an 18-bit straight binary word. The OFFSET code is always two's complement. It is therefore simply added to the output of the multiplier.

To guarantee that a gain of exactly 1 is possible, the actual gain coefficient applied to DIN is as defined in Equation 2.

Equation 2) Calculation of gain

$$G = \frac{(GAIN) + 1}{2^{18}}$$

When DIN is straight binary, the ideal transfer function is given by:

Equation 3) Straight binary ideal transfer function

$$V_{OUT} = G \times V_{DIN} + V_{OFFSET}$$

When DIN is two's complement, the ideal transfer function is given by:

Equation 4) Two's complement ideal transfer function

$$V_{OUT} = \frac{V_{REF}}{2} + G \times V_{DIN} + V_{OFFSET}$$

V_{DIN} and V_{OFFSET} are the voltages to which the DIN and OFFSET codes are converted and V_{OUT} is the voltage at the DAC output buffer. See the *Conversion Formulas for DIN, GAIN, and OFFSET* section for equations needed to convert the DIN and OFFSET codes into V_{DIN} and V_{OFFSET}.

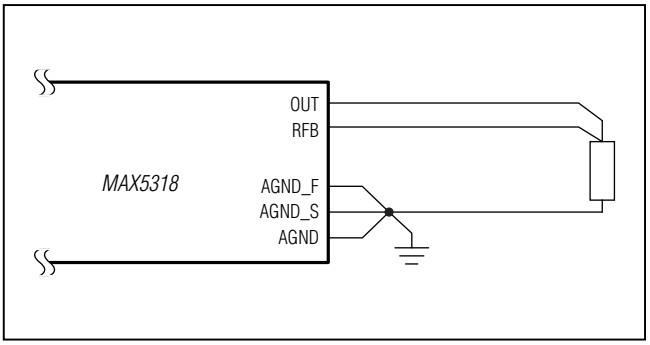


Figure 2a. Star Ground Connection

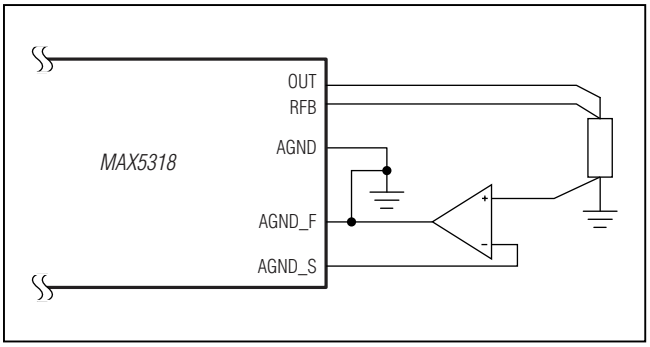


Figure 2b. Force/Sense Connection

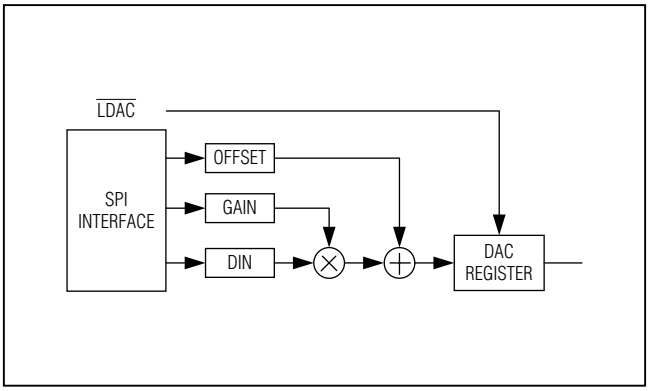


Figure 3. Gain and Offset Adjustment

The data DIN can be either straight binary or two's complement. In straight binary, zero code results in a zero-scale output. In two's complement, zero code results in a midscale output.

To better understand how GAIN and OFFSET affect the output voltage, see Figure 4 and Figure 5. Consider the generation of a ramp. For now assume OFFSET is set to 0x00000. In straight binary mode, with GAIN set to 0x3FFFF (G = 1), DIN starts from 0x00000 and increases to 0x3FFFF. The output voltage will start at 0V and increase to (V_{REF} - 1 LSB). If GAIN is reduced, the ramp will still start at 0V but the maximum level reached is reduced.

With DIN set to two's complement mode, to generate the same ramp, DIN would start at 0x20000 and increase until it wraps around to 0x00000. At this point the DAC output would be midscale. DIN then increases to 0x1FFFF where the output would be full-scale -1 LSB. As GAIN is reduced, the start of the ramp becomes larger and the end of the ramp becomes smaller. The ramp is therefore centered at midscale.

In both cases, a nonzero value for OFFSET results in the output moving up or down.

Should the output of the gain and offset adjust block overflow full-scale or underflow zero-scale, the data is clipped so the DAC output will be clipped rather than overflow or underflow.

The effect of gain and offset adjustment is shown in Figure 4 for straight binary mode and Figure 5 for two's complement mode.

If any of the DIN, GAIN, or OFFSET registers is changed, the device takes 1.9µs (t_{BUSY}) to compute the new values to present to the DAC. While the device is computing the new DAC value, the $\overline{BUSY}$ output is set low. See the section on the $\overline{BUSY}$ output and $\overline{LDAC}$ input for details.

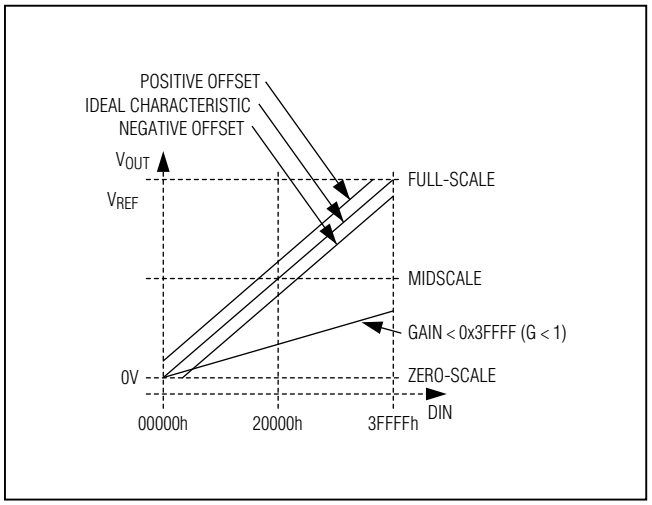


Figure 4. Gain and Offset Adjustment in Straight Binary Mode

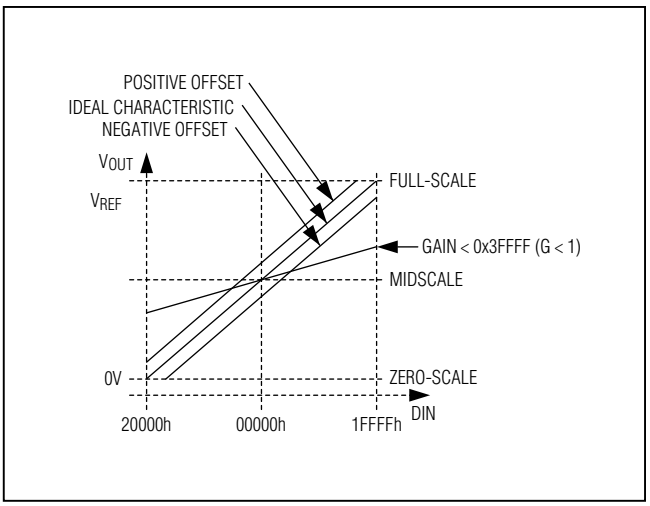


Figure 5. Gain and Offset Adjustment in Two's Complement Mode

Conversion Formulas for DIN, GAIN, and OFFSET

Tables 1a and 1b show how to convert the DIN code to V_{DIN} in straight binary and two's complement modes.

Table 2 shows how to convert the GAIN code to the gain factor G, which is multiplied with V_{DIN}. Table 3 shows how to convert the OFFSET code to V_{OFFSET}, which is summed with the product G•V_{DIN}.

Input, Gain, and Offset Ranges

The ranges of DIN, GAIN, and OFFSET are summarized in Table 4 to Table 6. Also shown are the range values for the 18-bit MAX5318 with a 4.096V reference. Note that V_{REF} is the reference voltage applied to REF and 1 LSB is equal to $V_{REF}/2^{18}$.

Table 1a. Converting DIN to V_{DIN} (Straight Binary Mode)

DIN	EQUATION FOR V_{DIN}	RANGE
0x00000 to 0x3FFFF	$V_{DIN} = V_{REF} \times \frac{DIN}{2^{18}}$	0V to (V_{REF} - 1 LSB)

Table 1b. Converting DIN to V_{DIN} (Two's Complement Mode)

DIN	EQUATION FOR V_{DIN} AND V_{OFFSET}	RANGE
0x20000 to 0x3FFFF	$V_{DIN} = V_{REF} \times \left(\frac{DIN - 0x20000}{2^{18}}\right) - \frac{V_{REF}}{2}$	$V_{REF}/2$ to -1 LSB
0x00000 to 0x1FFFF	$V_{DIN} = V_{REF} \times \frac{CODE}{2^{18}}$	0V to ($V_{REF}/2$ - 1 LSB)

Table 2. Converting GAIN to G

GAIN	EQUATION	RANGE
0x00000 to 0x3FFFF	$G = \frac{GAIN + 1}{2^{18}}$	$1/2^{18}$ to 1

Table 3. Converting OFFSET to V_{OFFSET}

OFFSET	EQUATION	RANGE
0x20000 to 0x3FFFF	$V_{OFFSET} = V_{REF} \times \left(\frac{OFFSET - 0x20000}{2^{18}}\right) - \frac{V_{REF}}{2}$	-VREF/2 to -1 LSB
0x00000 to 0x1FFFF	$V_{OFFSET} = V_{REF} \times \frac{OFFSET}{2^{18}}$	0V to (VREF/2 - 1 LSB)