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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-3067; Rev 1; 2/06

EVALUATION KIT AVAILABLE

32-Tap, Nonvolatile, Linear-Taper Digital Potentiometers in SOT23

General Description

The MAX5471/MAX5472/MAX5474/MAX5475 linear-taper digital potentiometers function as mechanical potentiometers, but replace the mechanics with a simple 3-wire up/down digital interface. These digital potentiometers feature nonvolatile memory (EEPROM) to return the wiper to its previously stored position upon power-up.

The MAX5471/MAX5472 are 2-terminal, variable resistors in 6-pin SOT23 packages. The MAX5474/MAX5475 are 3-terminal potentiometers in 8-pin SOT23 packages.

The MAX5471/MAX5474 have an end-to-end resistance of 50kΩ, and the MAX5472/MAX5475 have an end-to-end resistance of 100kΩ. All of these devices have 32 wiper positions, a low ratiometric temperature coefficient (5ppm/°C), and all operate from a single +2.7V to +5.25V supply. Each device is guaranteed over the extended -40°C to +85°C temperature range.

Applications

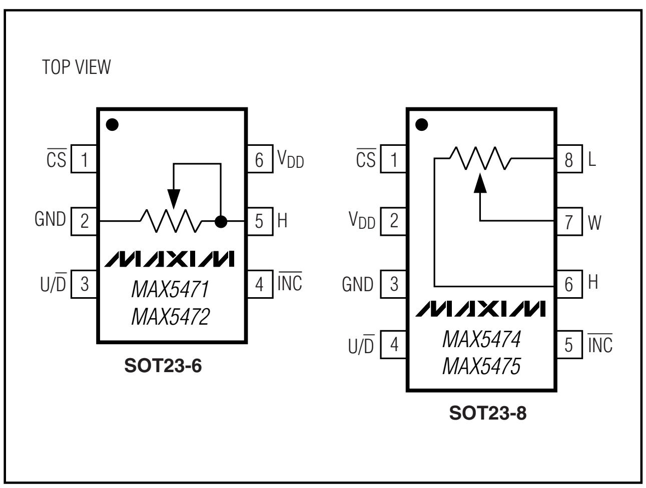
Mechanical Potentiometer Replacement

Liquid-Crystal-Display (LCD) Screen Adjustment

Audio Volume Control

Programmable Filters

Pin Configurations



Features

- ♦ **Wiper Position Stored in Nonvolatile Memory and Recalled Upon Power-Up**
- ♦ **Tiny SOT23 Package**
- ♦ **35ppm/°C End-to-End Resistance Temperature Coefficient**
- ♦ **5ppm/°C Ratiometric Temperature Coefficient**
- ♦ **32 Tap Positions**
- ♦ **Voltage-Divider or Variable-Resistor Potentiometer Configuration**
- ♦ **50kΩ and 100kΩ End-to-End Resistance Values**
- ♦ **1µA (max) Static Supply Current**
- ♦ **2.7V to 5.25V Single-Supply Operation**
- ♦ **200,000 Wiper Store Cycles**
- ♦ **50-Year Wiper Data Retention**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5471EZT-T	-40°C to +85°C	6 Thin SOT23-6	Z6-1
MAX5472EZT-T	-40°C to +85°C	6 Thin SOT23-6	Z6-1
MAX5474EKA-T	-40°C to +85°C	8 SOT23-8	K8S-3
MAX5475EKA-T	-40°C to +85°C	8 SOT23-8	K8S-3

Selector Guide

PART	END-TO-END RESISTANCE (kΩ)	TOP MARK
MAX5471EZT	50	ABQN
MAX5472EZT	100	ABQM
MAX5474EKA	50	AEIZ
MAX5475EKA	100	AEIY

32-Tap, Nonvolatile, Linear-Taper Digital Potentiometers in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6.0V
All Other
Pins to GND ....-0.3V to the lower of (V_{DD} + 0.3V) or +6.0V
Maximum Continuous Current into H, L, and W
MAX5471/MAX5474 ....±1.3mA
MAX5472/MAX5475 ....±0.6mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW/°C above +70°C)............727mW
8-Pin SOT23 (derate 8.9mW/°C above +70°C)............714mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Resolution	N		32			Tap
End-to-End Resistance		MAX5471/MAX5474	37.5	50	62.5	kΩ
		MAX5472/MAX5475	75	100	125	
End-to-End Resistance Temperature Coefficient	TC_R			35		ppm/°C
Ratiometric Resistance Temperature Coefficient				5		ppm/°C
Integral Nonlinearity	INL	Variable-resistor mode (Note 2)		±0.5	±1.0	LSB
		Voltage-divider mode (MAX5474/MAX5475) (Note 3)		±0.1	±0.5	
Differential Nonlinearity	DNL	Variable-resistor mode (Note 2)		±0.5	±1.0	LSB
		Voltage-divider mode (MAX5474/MAX5475) (Note 3)		±0.1	±0.5	
Full-Scale Error		MAX5474/MAX5475			-0.5	LSB
Zero-Scale Error		MAX5474/MAX5475			+0.5	LSB
Wiper Resistance	R_W	MAX5474/MAX5475 (Note 4)		600	1200	Ω
DIGITAL INPUTS ($\overline{CS}$, U/$\overline{D}$, $\overline{INC}$) (Note 5)						
Input High Voltage	V_{IH}	V_{DD} < 3.6V	0.7 x V_{DD}			V
		V_{DD} ≥ 3.6V	2.4			
Input Low Voltage	V_{IL}	V_{DD} < 3.6V			0.3 x V_{DD}	V
		V_{DD} ≥ 3.6V			0.8	
Input Current	I_{IN}			±0.1	±1	µA
DYNAMIC CHARACTERISTICS						
Wiper -3dB Bandwidth (Note 6)		MAX5471/MAX5474		400		kHz
		MAX5472/MAX5475		200		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 1, Note 7)						
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}		50			ns
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}		0			ns
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}		100			ns
$\overline{INC}$ Low Period	t_{IL}		50			ns
$\overline{INC}$ High Period	t_{IH}		50			ns
$\overline{INC}$ Cycle Time	t_{CYC}		100			ns
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}		100			ns
$\overline{INC}$ Active to $\overline{CS}$ Inactive	t_{IK}		100			ns
$\overline{CS}$ Deselect Time (Store)	t_{CPH}		100			ns
Wiper Settling Time	t_{IW}	(Note 8)		1		µs
Power-Up to Wiper Stable	t_{PU}			1		µs
Wiper Store Cycle	t_{WSC}		12			ms
NONVOLATILE MEMORY RELIABILITY						
Data Retention		T_A = +85°C		50		Year
Endurance		T_A = +25°C		200,000		Store
		T_A = +85°C		50,000		
POWER SUPPLY						
Supply Voltage	V_{DD}		2.70		5.25	V
Supply Current	I_{DD}	Write to memory			400	µA
Static Supply Current	I_{SD}	T_A = +25°C (Note 9)		0.35	1	µA

Note 1: All devices are production tested at T_A = +25°C and are guaranteed by design and characterization for -40°C < T_A < +85°C.

Note 2: The DNL and INL are measured with the potentiometer configured as a variable resistor. For the 3-terminal potentiometers (MAX5474/MAX5475), H is unconnected and L = GND. At V_{DD} = 5.25V, W is driven with a source current of 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration. At V_{DD} = 2.7V, the wiper terminal is driven with a source current of 40µA for the 50kΩ configuration, and 20µA for the 100kΩ configuration.

Note 3: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{DD} and L = GND (MAX5474/MAX5475 only). The wiper terminal is unloaded.

Note 4: The wiper resistance is the worst value measured by injecting the currents given in Note 2 into W with L = GND. $R_W = (V_W - V_H) / I_W$.

Note 5: The device draws higher supply current when digital inputs are driven with voltages between 0.3V x V_{DD} and 0.7 x V_{DD}. Drive the digital inputs as close as possible to V_{DD} or GND. (See the *Typical Operating Characteristics* for the Supply Current vs. Digital Input Voltage graph.)

Note 6: Wiper at midscale with a 10pF load.

Note 7: Digital timing is guaranteed by design and characterization, and is not production tested.

Note 8: Wiper settling time is the worst-case 0% to 50% rise time measured between consecutive wiper positions. H = V_{DD}, L = GND, and the wiper terminal is unloaded and measured with a 10pF oscilloscope probe (see the *Typical Operating Characteristics* for the Tap-to-Tap Switching Transient).

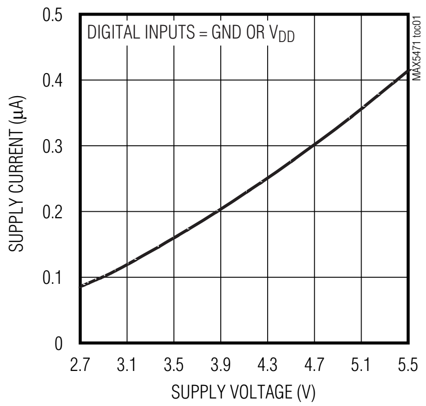
Note 9: Digital inputs $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ are connected to GND or V_{DD}. See the *Typical Operating Characteristics* for the Static Supply Current vs. Temperature graph.

32-Tap, Nonvolatile, Linear-Taper Digital Potentiometers in SOT23

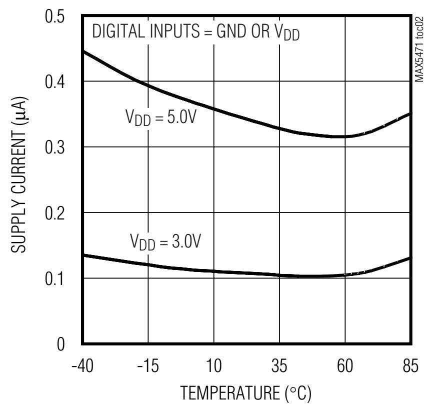
Typical Operating Characteristics

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)

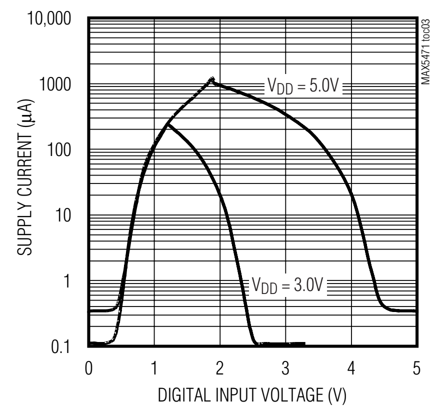
SUPPLY CURRENT vs. SUPPLY VOLTAGE



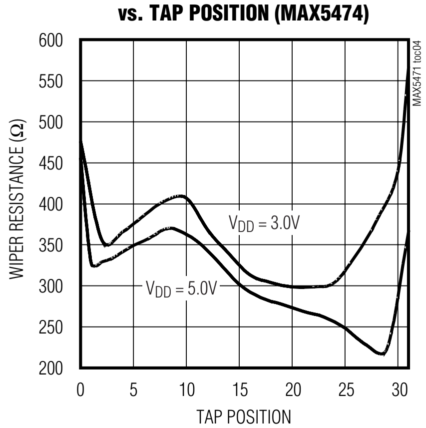
STATIC SUPPLY CURRENT vs. TEMPERATURE



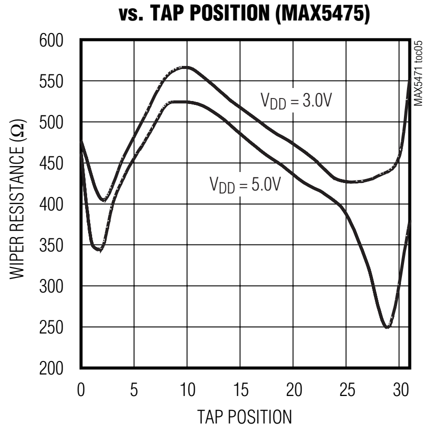
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



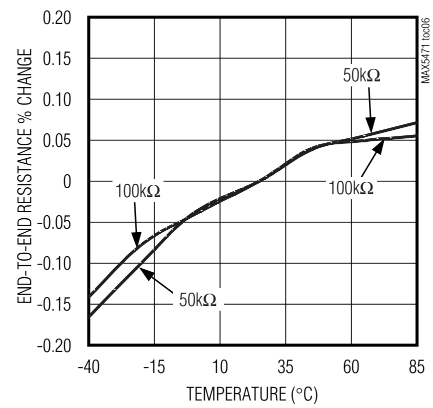
WIPER RESISTANCE vs. TAP POSITION (MAX5474)



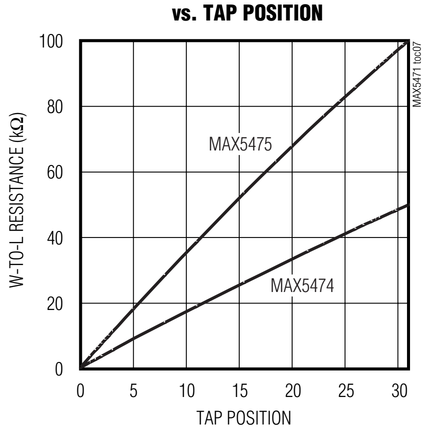
WIPER RESISTANCE vs. TAP POSITION (MAX5475)



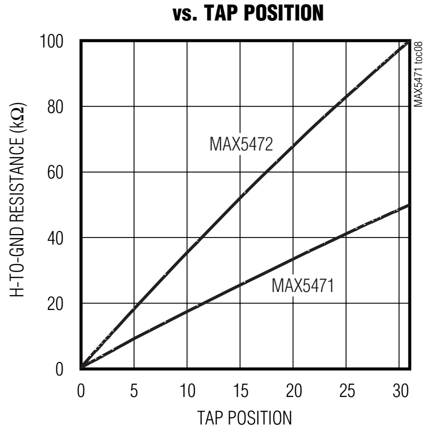
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



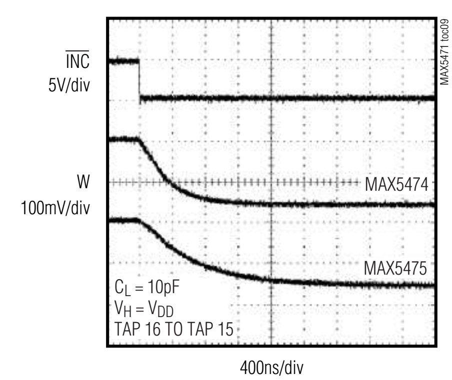
W-TO-L RESISTANCE vs. TAP POSITION



H-TO-GND RESISTANCE vs. TAP POSITION



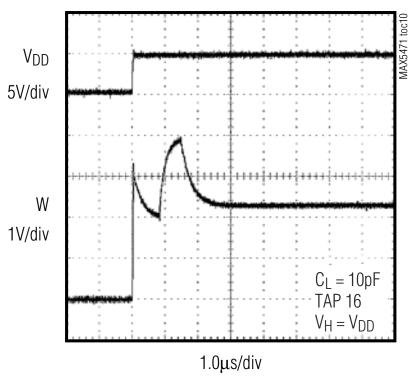
TAP-TO-TAP SWITCHING TRANSIENT



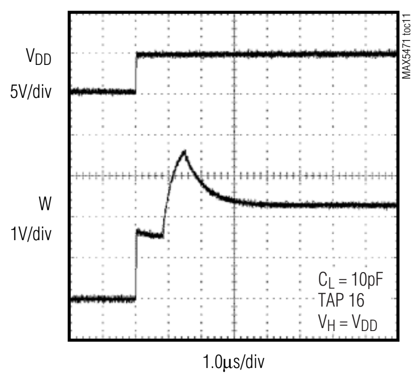
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)

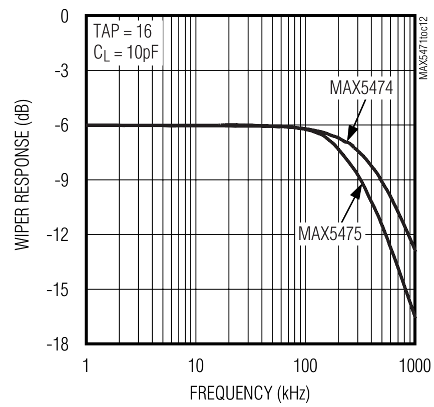
WIPER TRANSIENT AT POWER-ON (MAX5474)



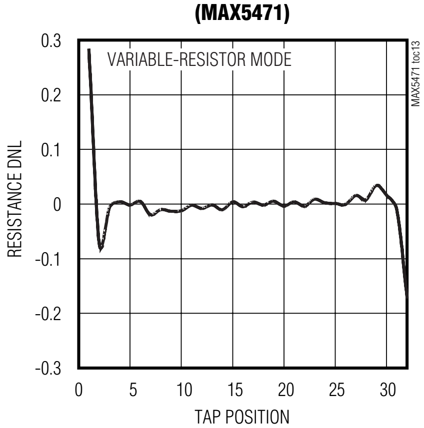
WIPER TRANSIENT AT POWER-ON (MAX5475)



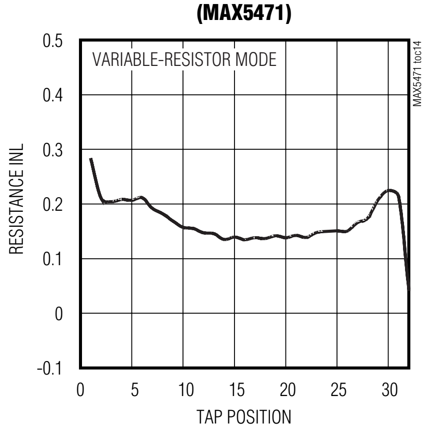
WIPER RESPONSE vs. FREQUENCY



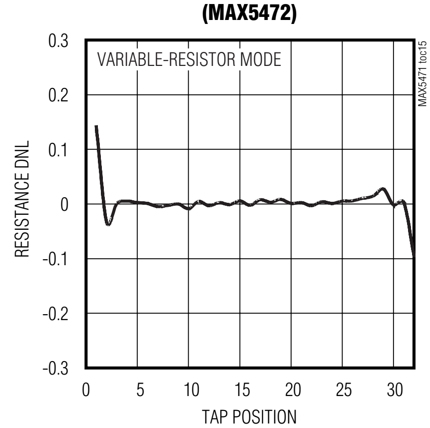
RESISTANCE DNL vs. TAP POSITION (MAX5471)



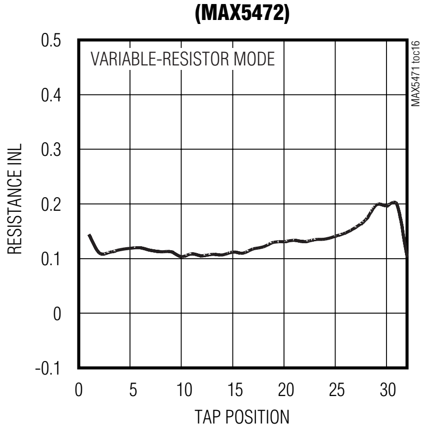
RESISTANCE INL vs. TAP POSITION (MAX5471)



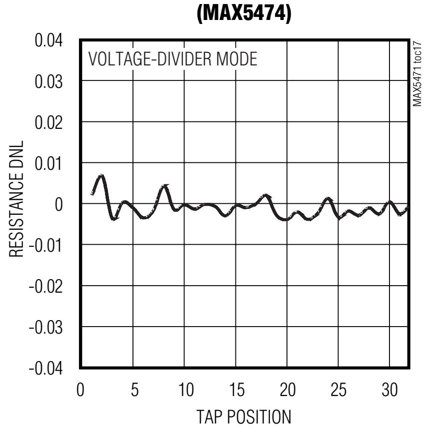
RESISTANCE DNL vs. TAP POSITION (MAX5472)



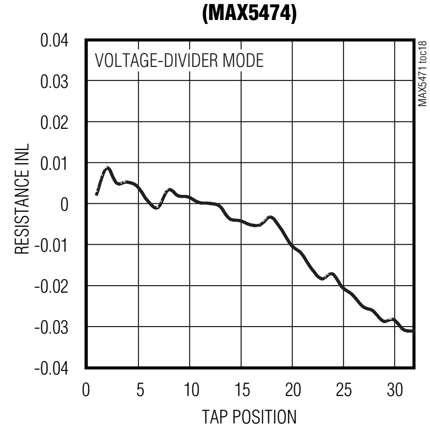
RESISTANCE INL vs. TAP POSITION (MAX5472)



RESISTANCE DNL vs. TAP POSITION (MAX5474)

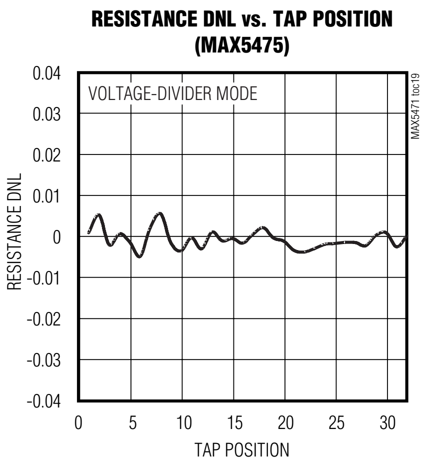


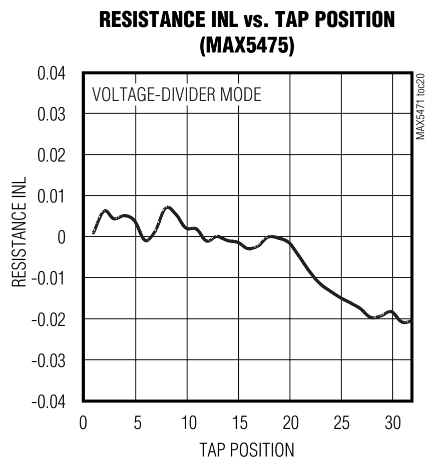
RESISTANCE INL vs. TAP POSITION (MAX5474)



Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN		NAME	FUNCTION
MAX5471/ MAX5472	MAX5474/ MAX5475		
1	1	$\overline{CS}$	Chip-Select Input. Drive low to change wiper position (W) through $\overline{INC}$ and U/$\overline{D}$. A low-to-high transition with $\overline{INC}$ high stores the wiper position in nonvolatile memory.
2	3	GND	Ground
3	4	U/$\overline{D}$	Up/Down Control Input. With U/$\overline{D}$ low, a high-to-low $\overline{INC}$ transition decrements the wiper position. With U/$\overline{D}$ high, a high-to-low $\overline{INC}$ transition increments the wiper position.
4	5	$\overline{INC}$	Wiper Increment Control Input. With $\overline{CS}$ low, the wiper position moves in the direction determined by the state of U/$\overline{D}$ on a high-to-low transition.
5	6	H	High Terminal of Resistor. The voltage at H can be greater than or less than the voltage at L. Current can flow into or out of H.
6	2	V_{DD}	Power Supply
—	7	W	Wiper Terminal of Resistor
—	8	L	Low Terminal of Resistor. The voltage at L can be greater than or less than the voltage at H. Current can flow into or out of L.

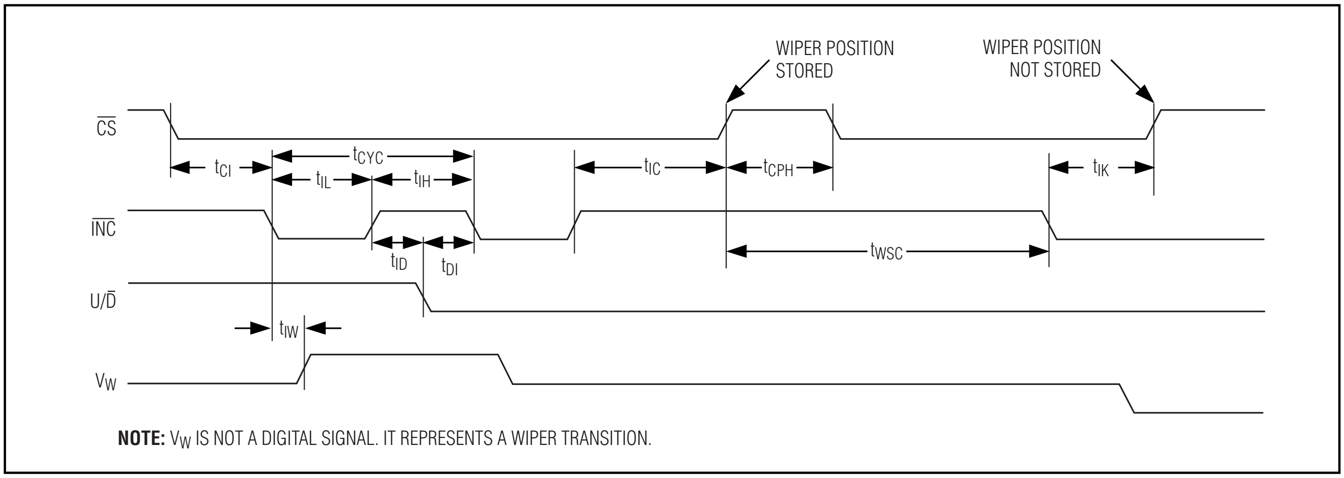


Figure 1. Digital Interface and Timing Diagram

Detailed Description

The MAX5471/MAX5472/MAX5474/MAX5475 contain a resistor array with 31 resistive elements (Figures 2 and 3). The MAX5471/MAX5474 have a total end-to-end resistance of 50kΩ, and the MAX5472/MAX5475 have an end-to-end resistance of 100kΩ. The MAX5471/MAX5472 wiper is connected to the high terminal, and the low terminal is internally connected to ground, making the device a variable resistor. The MAX5474/MAX5475 allow access to the high, low, and wiper terminals for a standard voltage-divider configuration.

The wiper is moved among the 32 tap points through a simple 3-wire interface. Nonvolatile memory allows the wiper position to be stored and recalled to the same point upon power-up.

Digital Interface

Logic inputs $\overline{\text{CS}}$, U/$\overline{\text{D}}$, and $\overline{\text{INC}}$ control the wiper position and store it in nonvolatile memory (see the *Truth Table*). The chip-select ($\overline{\text{CS}}$) input enables the serial interface when low and disables the interface when high. The position of the wiper is stored when $\overline{\text{CS}}$ transitions from low to high and $\overline{\text{INC}}$ is high (see the *Storing Wiper Position* section).

With the serial interface active ($\overline{\text{CS}}$ low), a high-to-low (falling edge) transition on $\overline{\text{INC}}$ moves the wiper position by one resistive element in the direction determined by the state of U/$\overline{\text{D}}$. If U/$\overline{\text{D}}$ is high, the wiper increments and it increases the resistance between W and L (it decreases the resistance between H and W). If U/$\overline{\text{D}}$ is low, the wiper decrements and it decreases the resistance between W and L (it increases the resistance between H and W). The direction of the wiper (state of U/$\overline{\text{D}}$) can be changed at any time as long as the setup and hold times are met.

Since the MAX5471/MAX5472 have the wiper internally connected to H, an increment command increases the resistance between H and GND, and a decrement command decreases the resistance between H and GND.

The wiper performs a make-before-break transition, ensuring that there is never an open circuit during a transition from one resistor tap to another. When the wiper is at either end of the resistor array (max/min), additional transitions in the direction of the endpoint do not change the counter value (the wiper does not wrap around).

Storing Wiper Position

The position of the wiper is stored in nonvolatile memory whenever $\overline{\text{CS}}$ transitions low-to-high (rising edge) while $\overline{\text{INC}}$ is high. Upon power-up, the wiper returns to this stored position. By keeping $\overline{\text{INC}}$ low while taking $\overline{\text{CS}}$ high, the serial interface can be disabled and the potentiometer placed in standby without storing the latest wiper position. The factory-default wiper position is midscale.

These devices can also be operated like a one-time programmable (OTP) device. Once the desired wiper position is trimmed and stored in nonvolatile memory, disable the serial interface by connecting $\overline{\text{CS}}$ to V_{DD}, and $\overline{\text{INC}}$ to GND. The disabled interface places the device in standby and disallows any changes to the wiper position. In OTP mode, these devices become a fixed 3-terminal potentiometer or a 1-terminal resistor to GND with less than 1µA of supply current.

Truth Table

$\overline{CS}$	U/$\overline{D}$	$\overline{INC}$	W
L	L	↓	Decrement
L	H	↓	Increment
L	X	↑	No change
H	X	X	No change
↓	X	X	No change
↑	X	L	Position not stored
↑	X	H	Position stored

↓ = High-to-low transition.
↑ = Low-to-high transition.
X = Don't care.

Standby Mode

The MAX5471/MAX5472/MAX5474/MAX5475 are always in standby mode, except during the transition of a logic input or while the wiper position is being stored. When in standby mode, the static supply current is reduced to less than 1µA and the resistive terminals (H, W, and L) are unaffected.

Applications Information

The MAX5471/MAX5472/MAX5474/MAX5475 are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 4 and 5 show an application where the voltage-divider or variable resistor is used to make an adjustable, positive LCD-bias voltage. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 4) or to a fixed resistor and a variable resistor (Figure 5).

Programmable Filter

Figure 6 shows the configuration of a 1st-order programmable filter. The gain of the filter is adjusted by R2, and the cutoff frequency is adjusted by R3. Use the following equations to calculate the gain (G) and the 3dB cutoff frequency (f_C):

$$G = 1 + \frac{R1}{R2}$$

$$f_C = \frac{1}{2\pi \times R3 \times C}$$

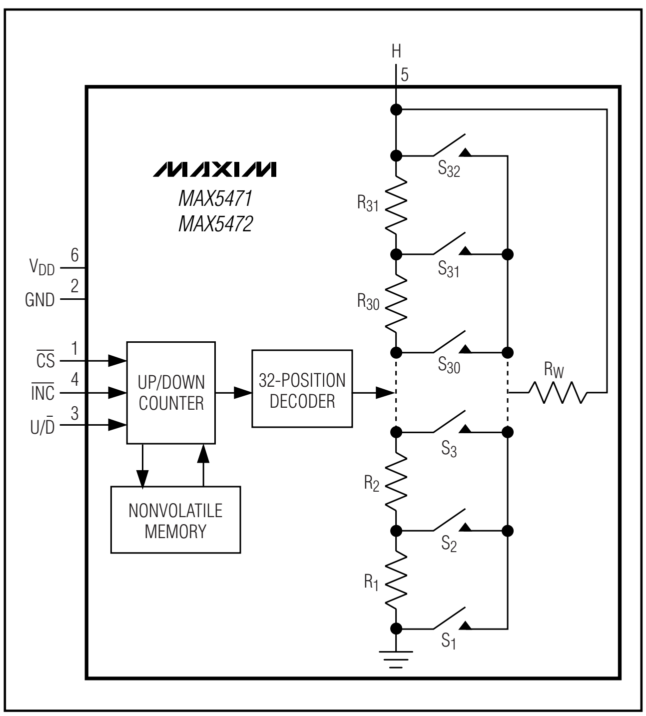


Figure 2. MAX5471/MAX5472 Functional Diagram

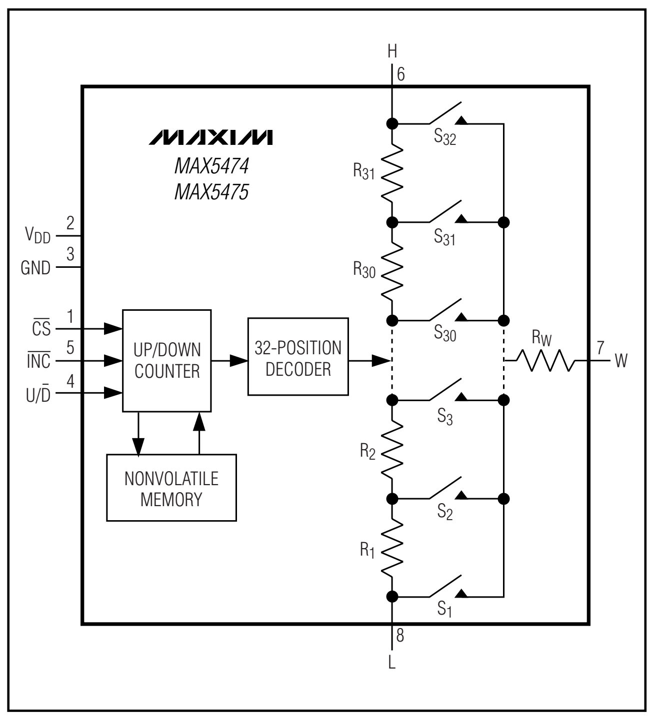


Figure 3. MAX5474/MAX5475 Functional Diagram

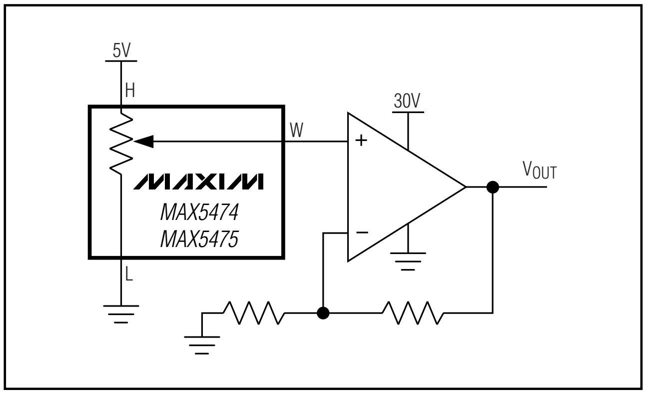


Figure 4. Positive LCD Bias Control Using a Voltage-Divider

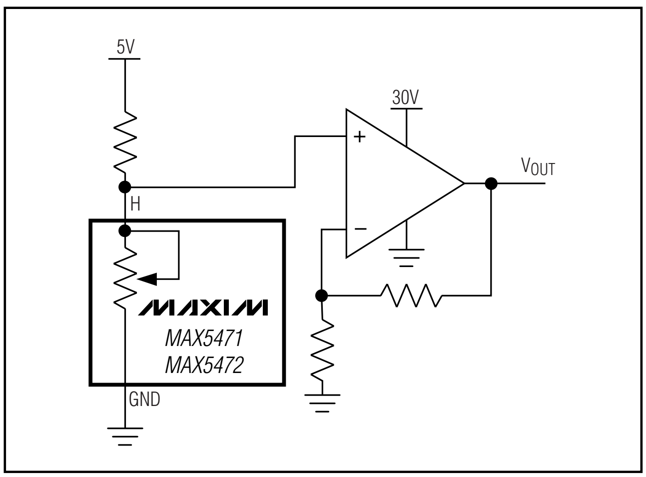


Figure 5. Positive LCD Bias Control Using a Variable Resistor

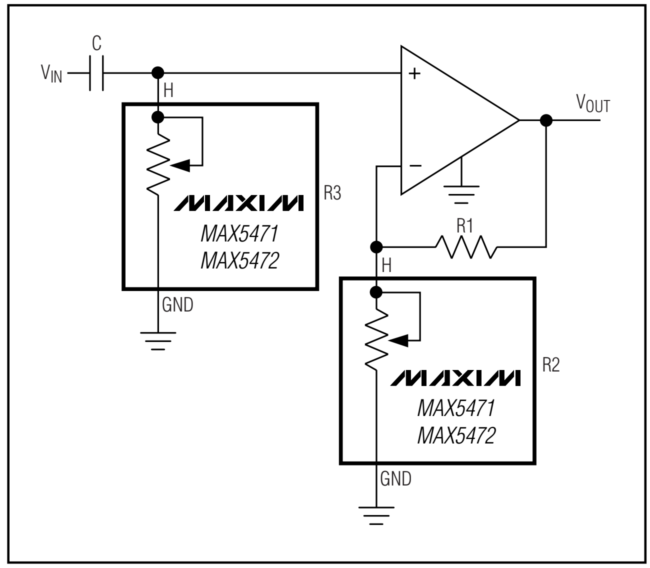


Figure 6. Programmable Filter

Chip Information

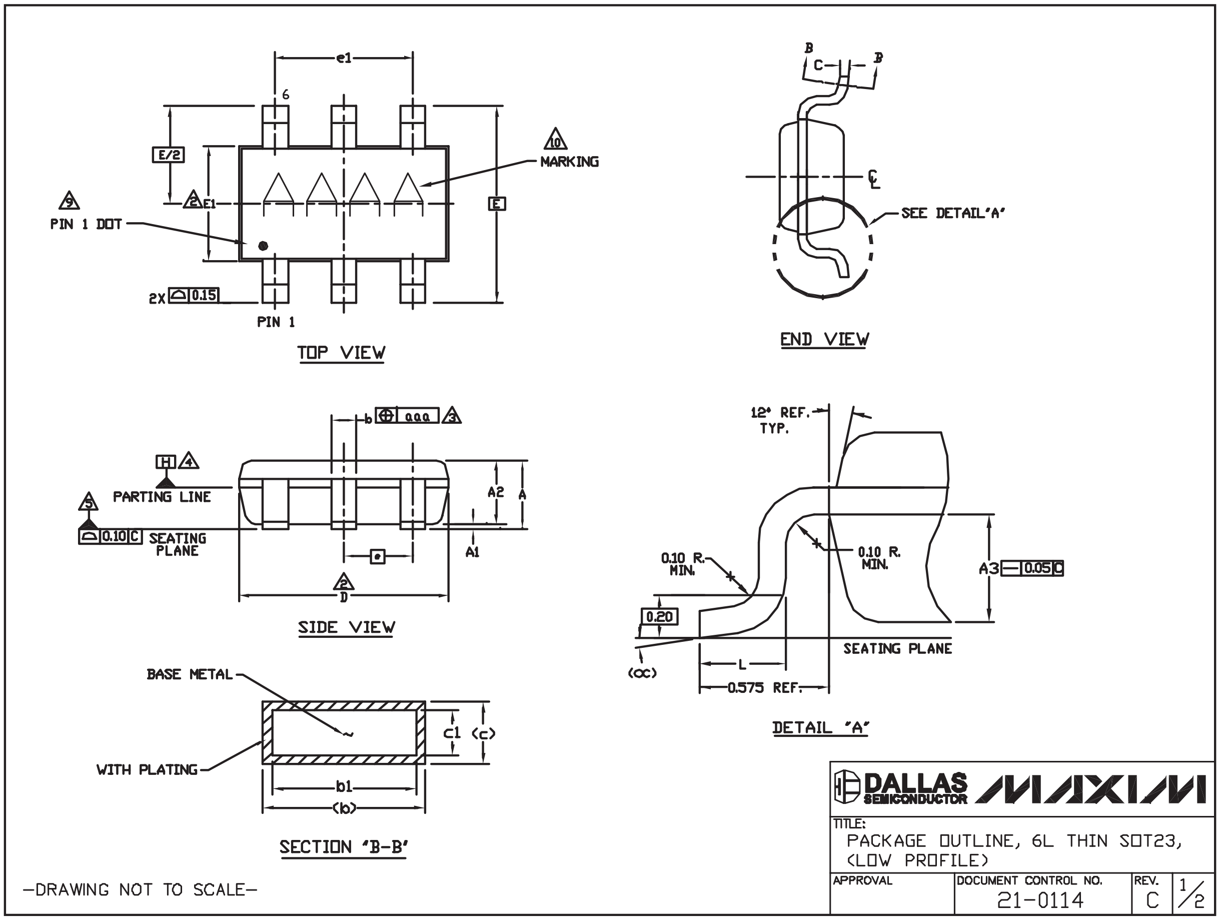
TRANSISTOR COUNT: 5031

PROCESS: BiCMOS

32-Tap, Nonvolatile, Linear-Taper Digital Potentiometers in SOT23

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



6L THIN SOT23.EPS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3	0.50 BSC		
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E	2.75 BSC		
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1	1.90 BSC		
e	0.95 BSC		
α	0°	4°	8°
aaa	0.20		
Pkg. codes: Z6-1; Z6-2			

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L THIN SOT23, (LOW PROFILE)

APPROVAL | DOCUMENT CONTROL NO. 21-0114 | REV. C | 2/2

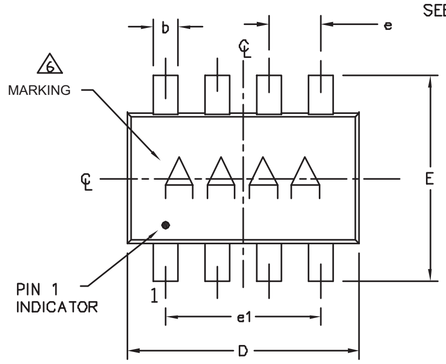
-DRAWING NOT TO SCALE-

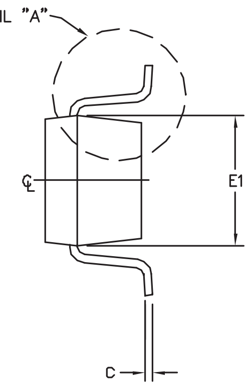
32-Tap, Nonvolatile, Linear-Taper Digital Potentiometers in SOT23

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

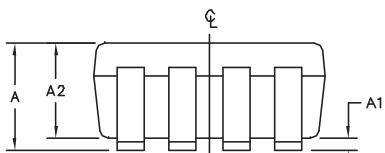
SOT23, 8L.EPS

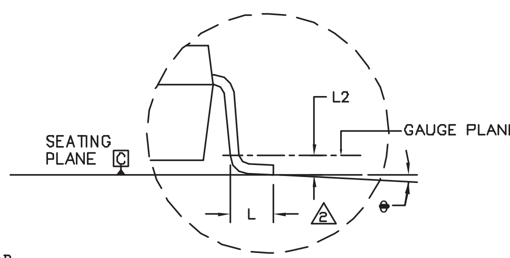




SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6; K8SN-1; K8CN-1





DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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