Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-3164; Rev 4; 7/08

EVALUATION KIT AVAILABLE

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

General Description

The MAX5580–MAX5585 quad, 12-/10-/8-bit, voltage-output, digital-to-analog converters (DACs) offer buffered outputs and a 3µs maximum settling time at the 12-bit level. The DACs operate from a +2.7V to +5.25V analog supply and a separate +1.8V to +5.25V digital supply. The 20MHz, 3-wire, serial interface is compatible with SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) protocol applications. Multiple devices can share a common serial interface in direct-access or daisy-chained configuration. The MAX5580–MAX5585 provide two multifunctional, user-programmable, digital I/O ports. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale. Software-selectable FAST and SLOW settling modes decrease settling time in FAST mode, or reduce supply current in SLOW mode.

The MAX5580/MAX5581 are 12-bit DACs, the MAX5582/MAX5583 are 10-bit DACs, and the MAX5584/MAX5585 are 8-bit DACs. The MAX5580/MAX5582/MAX5584 provide unity-gain-configured output buffers, while the MAX5581/MAX5583/MAX5585 provide force-sense-configured output buffers. The MAX5580–MAX5585 operate over the extended -40°C to +85°C temperature range and are available in a space-saving, 6.5mm x 4.4mm, 20-pin, TSSOP package.

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **3µs (max) 12-Bit Settling Time to 0.5 LSB**
- **Quad, 12-/10-/8-Bit Serial DACs in TSSOP Package**
- **±1 LSB (max) INL and DNL at 12-Bit Resolution**
- **Two User-Programmable Digital I/O Ports**
- **Single +2.7V to +5.25V Analog Supply**
- **+1.8V to AV_{DD} Digital Supply**
- **20MHz, 3-Wire, SPI-/QSPI-/MICROWIRE-/DSP-Compatible Serial Interface**
- **Glitch-Free Outputs Power Up to Zero Scale, Midscale, or Full Scale Controlled by PU Pin**
- **Unity-Gain or Force-Sense-Configured Output Buffers**

Applications

Portable Instrumentation
Automatic Test Equipment (ATE)
Digital Offset and Gain Adjustment
Automatic Tuning
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Controls
Motion Control
Microprocessor (µP)-Controlled Systems
Power Amplifier Control
Fast Parallel-DAC to Serial-DAC Upgrades

Pin Configuration appears at end of data sheet.

Ordering Information/Selector Guide

PART	RESOLUTION (BITS)	INL (LSB max)	OUTPUT BUFFER CONFIGURATION	PIN-PACKAGE
MAX5580AEUP+	12	±1	Unity gain	20 TSSOP-EP*
MAX5580BEUP+	12	±4	Unity gain	20 TSSOP-EP*
MAX5581AEUP+	12	±1	Force sense	20 TSSOP-EP*
MAX5581BEUP+	12	±4	Force sense	20 TSSOP-EP*
MAX5582EUP+	10	±1	Unity gain	20 TSSOP-EP*
MAX5583EUP+	10	±1	Force sense	20 TSSOP-EP*
MAX5584EUP+	8	±0.5	Unity gain	20 TSSOP-EP*
MAX5585EUP+	8	±0.5	Force sense	20 TSSOP-EP*

+Denotes a lead-free/RoHS-compliant package.

**EP = Exposed paddle.*

***Note:** All devices are specified over the -40°C to +85°C operating temperature range.*

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to DV_{DD} ..... ±6V
AGND to DGND ..... ±0.3V
AV_{DD} to AGND, DGND ..... -0.3V to +6V
DV_{DD} to AGND, DGND ..... -0.3V to +6V
FB_, OUT_,
REF to AGND ..... -0.3V to the lower of (AV_{DD} + 0.3V) or +6V
SCLK, DIN, $\overline{CS}$, PU,
$\overline{DSP}$ to DGND ..... -0.3V to the lower of (DV_{DD} + 0.3V) or +6V
UPIO1, UPIO2
to DGND ..... -0.3V to the lower of (DV_{DD} + 0.3V) or +6V
Maximum Current into Any Pin ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 21.7mW/°C above +70°C) 1739mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, V_{AGND} = 0, V_{DGND} = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution	N	MAX5580/MAX5581		12			Bits
		MAX5582/MAX5583		10			
		MAX5584/MAX5585		8			
Integral Nonlinearity	INL	V_{REF} = 2.5V at AV_{DD} = 2.7V and V_{REF} = 4.096V at AV_{DD} = 5.25V (Note 2)	MAX5580A/MAX5581A (12 bit)			±1	LSB
			MAX5580B/MAX5581B (12 bit)		±2	±4	
			MAX5582/MAX5583 (10 bit)		±0.5	±1	
			MAX5584/MAX5585 (8 bit)		±0.125	±0.5	
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 2)				±1	LSB
Offset Error	V_{OS}	MAX5580A/MAX5581A (12 bit), decimal code = 250				±5	mV
		MAX5580B/MAX5581B (12 bit), decimal code = 40			±5	±25	
		MAX5582/MAX5583 (10 bit), decimal code = 20			±5	±25	
		MAX5584/MAX5585 (8 bit), decimal code = 5			±5	±25	
Offset-Error Drift					5		ppm of FS/°C
Gain Error	GE	Full-scale output	MAX5580A, V_{REF} = 4.096V		±1	±5	LSB
			MAX5580A, V_{REF} = 2.5V		±1.5	±7	
			MAX5581A, V_{REF} = 4.096V		±0.5	±4	
			MAX5581A, V_{REF} = 2.5V		±1	±5	
			MAX5580B/MAX5581B (12 bit)		±20	±40	
			MAX5582/MAX5583 (10 bit)		±5	±10	
			MAX5584/MAX5585 (8 bit)		±2	±3	
Gain-Error Drift					1		ppm of FS/°C

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, V_{AGND} = 0, V_{DGND} = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	Full-scale output, AV_{DD} = 2.7V to 5.25V			200		µV/V
REFERENCE INPUT							
Reference-Input Range	V_{REF}			0.25		AV_{DD}	V
Reference-Input Resistance	R_{REF}	Normal operation (no code dependence)		145	200		kΩ
Reference Leakage Current		Shutdown mode			0.5	1	µA
DAC OUTPUT CHARACTERISTICS							
Output-Voltage Noise		SLOW mode, full scale	Unity gain		85		$µV_{RMS}$
			Force sense		67		
		FAST mode, full scale	Unity gain		140		
			Force sense		110		
Output-Voltage Range (Note 3)		Unity-gain output		0		AV_{DD}	V
		Force-sense output		0		AV_{DD} / 2	
DC Output Impedance					38		Ω
Short-Circuit Current		AV_{DD} = 5V, OUT_ to AGND, full scale, FAST mode			57		mA
		AV_{DD} = 3V, OUT_ to AGND, full scale, FAST mode			45		
Power-Up Time		From DV_{DD}, applied until interface is functional			30	60	µs
Wake-Up Time		Coming out of shutdown, outputs settled			40		µs
Output OUT_ and FB_ Open-Circuit Leakage Current		Programmed in shutdown mode, force-sense outputs only			0.01		µA
DIGITAL OUTPUTS (UPIO_)							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		DV_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
DIGITAL INPUTS (SCLK, $\overline{CS}$, DIN, $\overline{DSP}$, UPIO_)							
Input High Voltage	V_{IH}	DV_{DD} ≥ 2.7V		2.4			V
		DV_{DD} < 2.7V		0.7 x DV_{DD}			
Input Low Voltage	V_{IL}	DV_{DD} > 3.6V				0.8	V
		2.7V ≤ DV_{DD} ≤ 3.6V				0.6	
		DV_{DD} < 2.7V				0.2	
Input Leakage Current	I_{IN}				±0.1	±1	µA
Input Capacitance	C_{IN}				10		pF

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, V_{AGND} = 0, V_{DGND} = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PU INPUT							
Input High Voltage	V_{IH-PU}			DV_{DD} - 200mV			V
Input Low Voltage	V_{IL-PU}					200	mV
Input Leakage Current	I_{IN-PU}	PU still considered floating when connected to a tri-state bus				±200	nA
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	FAST mode			3.6		V/µs
		SLOW mode			1.6		
Voltage-Output Settling Time (Note 4), Figure 5	t_S	FAST mode	MAX5580/MAX5581 from code 322 to code 4095 to 0.5 LSB		2	3	µs
			MAX5582/MAX5583 from code 10 to code 1023 to 0.5 LSB		1.5	3	
			MAX5584/MAX5585 from code 3 to code 255 to 0.5 LSB		1	2	
		SLOW mode	MAX5580/MAX5581 from code 322 to code 4095 to 0.5 LSB		3	6	
			MAX5582/MAX5583 from code 10 to code 1023 0.5 LSB		2.5	6	
			MAX5584/MAX5585 from code 3 to code 255 to 0.5 LSB		2	4	
FB_ Input Voltage				0		V_{REF} / 2	V
FB_ Input Current						0.1	µA
Reference -3dB Bandwidth (Note 5)		Unity gain			200		kHz
		Force sense			150		
Digital Feedthrough		$\overline{CS}$ = DV_{DD}, code = zero scale, any digital input from 0 to DV_{DD} and DV_{DD} to 0, f = 100kHz			0.1		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition			2		nV-s
DAC-to-DAC Crosstalk		(Note 6)			15		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, V_{AGND} = 0, V_{DGND} = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Analog Supply Voltage Range	AV_{DD}			2.70		5.25	V
Digital Supply Voltage Range	DV_{DD}			1.8		AV_{DD}	V
Operating Supply Current	I_{AVDD} + I_{DVDD}	SLOW mode, all digital inputs at DGND or DV_{DD}, no load, V_{REF} = 4.096V	Unity gain		0.9	1.6	mA
			Force sense		1.6	2.4	
		FAST mode, all digital inputs at DGND or DV_{DD}, no load, V_{REF} = 4.096V	Unity gain		1.6	4	
			Force sense		2.3	4	
Shutdown Supply Current	$I_{AVDD(SHDN)}$ + $I_{DVDD(SHDN)}$	No clocks, all digital inputs at DGND or DV_{DD}, all DACs in shutdown mode			0.5	1	µA

Note 1: For the force-sense versions, FB_ is connected to its respective OUT_, and V_{OUT} (max) = V_{REF} / 2, unless otherwise noted.

Note 2: Linearity guaranteed from decimal code 250 to code 4095 for the MAX5580A/MAX5581A (12 bit, A grade), code 40 to code 4095 for the MAX5580B/MAX5581B (12 bit, B grade), code 20 to code 1023 for the MAX5582/MAX5583 (10 bit), and code 5 to code 255 for the MAX5584/MAX5585 (8 bit).

Note 3: Represents the functional range. The linearity is guaranteed at V_{REF} = 2.5V (for AV_{DD} from 2.7V to 5.25V), and V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V). See the *Typical Operating Characteristics* section for linearity at other voltages.

Note 4: Guaranteed by design.

Note 5: The reference -3dB bandwidth is measured with a $0.1V_{P-P}$ sine wave on V_{REF} and with full-scale input code.

Note 6: DC crosstalk is measured as follows: outputs of DACA–DACD are set to full scale and the output of DACD is measured. While keeping DACD unchanged, the outputs of DACA–DACC are transitioned to zero scale and the ΔV_{OUT} of DACD is measured.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

TIMING CHARACTERISTICS—DSP Mode Disabled (3V, 3.3V, 5V Logic) (Figure 1)

(DV_{DD} = 2.7V to 5.25V, AGND = DGND = 0, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	2.7V < DV_{DD} < 5.25V			20	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	20			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	20			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		10			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Rise to $\overline{CS}$ Fall Setup Time	t_{CS0}		10			ns
DIN to SCLK Rise Setup Time	t_{DS}		12			ns
DIN to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 mode			30	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 or DOUTRB mode			30	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		45			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t_{ZEN}	C_L = 20pF, from 8th rising edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	20			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	100			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	20			ns
GPO Output Settling Time	t_{GP}	Figure 6			100	ns
GPO Output High-Impedance Time	t_{GPZ}				100	ns

TIMING CHARACTERISTICS—DSP Mode Disabled (1.8V Logic) (Figure 1)

(DV_{DD} = 1.8V to 2.7V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	1.8V < DV_{DD} < 2.7V			10	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		20			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Rise to $\overline{CS}$ Fall Setup TIme	t_{CS0}		10			ns
DIN to SCLK Rise Setup Time	t_{DS}		20			ns
DIN to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 or DOUTRB mode			60	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		90			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t_{ZEN}	C_L = 20pF, from 8th rising edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	40			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	200			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	40			ns
GPO Output Settling Time	t_{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t_{GPZ}				200	ns

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

TIMING CHARACTERISTICS—DSP Mode Enabled (3V, 3.3V, 5V Logic) (Figure 2)

(DV_{DD} = 2.7V to 5.25V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	2.7V < DV_{DD} < 5.25V			20	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	20			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	20			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		10			ns
$\overline{DSP}$ Fall to SCLK Fall Setup Time	t_{DSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Fall to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
SCLK Fall to $\overline{DSP}$ Fall Delay	t_{DS0}		10			ns
DIN to SCLK Fall Setup Time	t_{DS}		12			ns
DIN to SCLK Fall Hold Time	t_{DH}		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			30	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 mode			30	ns
$\overline{CS}$ Rise to SCLK Fall Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		45			ns
$\overline{DSP}$ Pulse-Width High	t_{DSW}		20			ns
$\overline{DSP}$ Pulse-Width Low	t_{DSPWL}	(Note 8)	20			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	t_{ZEN}	C_L = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	20			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	100			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	20			ns
GPO Output Settling Time	t_{GP}	Figure 6			100	ns
GPO Output High-Impedance Time	t_{GPZ}				100	ns

TIMING CHARACTERISTICS—DSP Mode Enabled (1.8V Logic) (Figure 2)

(DV_{DD} = 1.8V to 2.7V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	1.8V < DV_{DD} < 2.7V			10	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	40			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		20			ns
$\overline{DSP}$ Fall to SCLK Fall Setup Time	t_{DSS}		20			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Fall to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
SCLK Fall to $\overline{DSP}$ Fall Delay	t_{DS0}		15			ns
DIN to SCLK Fall Setup Time	t_{DS}		20			ns
DIN to SCLK Fall Hold Time	t_{DH}		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 mode			60	ns
$\overline{CS}$ Rise to SCLK Fall Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		90			ns
$\overline{DSP}$ Pulse-Width High	t_{DSW}		40			ns
$\overline{DSP}$ Pulse-Width Low	t_{DSPWL}	(Note 8)	40			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	t_{ZEN}	C_L = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	40			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	200			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	40			ns
GPO Output Settling Time	t_{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t_{GPZ}				200	ns

Note 7: In some daisy-chain modes, data is required to be clocked in on one clock edge and the shifted data clocked out on the following edge. In the case of a 0.5 clock-period delay, it is necessary to increase the minimum high/low clock times to 25ns (2.7V) or 50ns (1.8V).

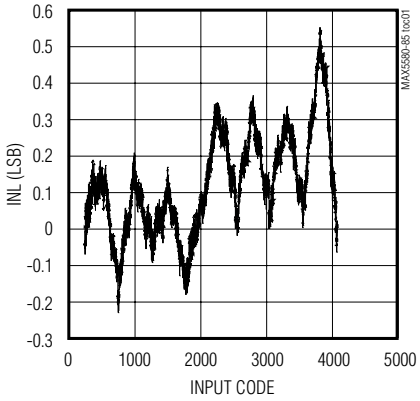
Note 8: The falling edge of $\overline{DSP}$ starts a DSP-type bus cycle, provided that $\overline{CS}$ is also active low to select the device. $\overline{DSP}$ active low and $\overline{CS}$ active low must overlap by a minimum of 10ns (2.7V) or 20ns (1.8V). $\overline{CS}$ can be permanently low in this mode of operation.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

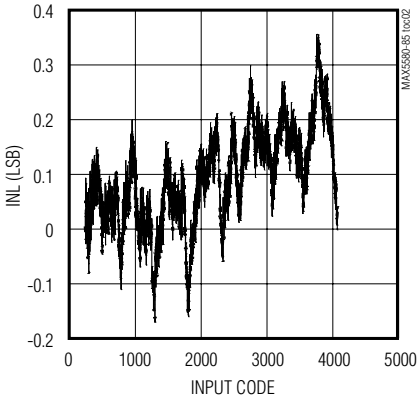
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

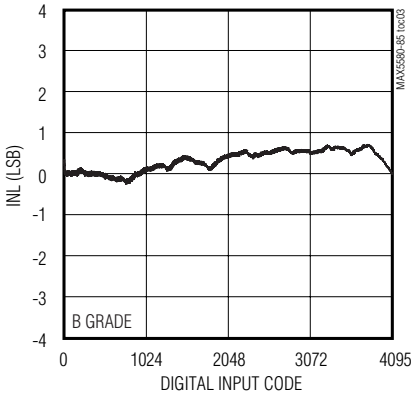
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5580A)



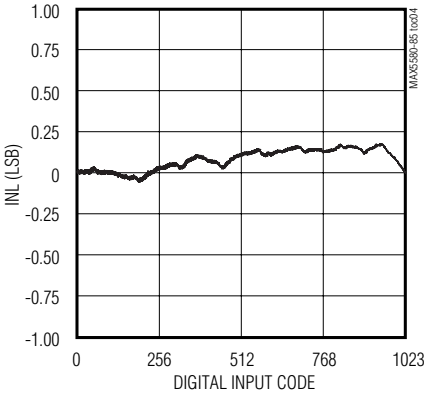
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5581A)



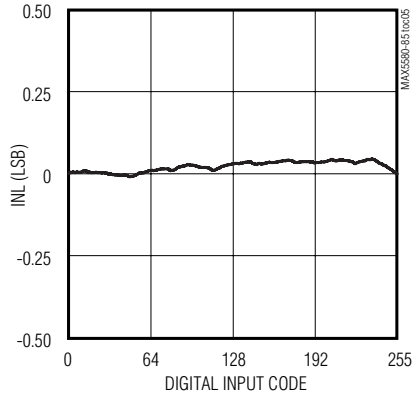
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (12 BIT)



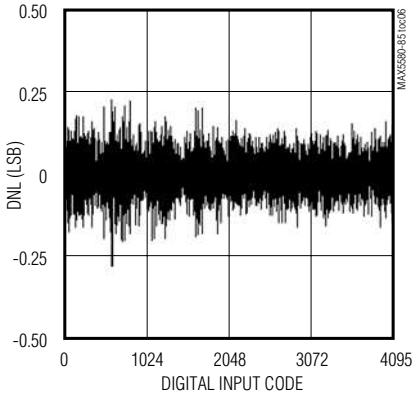
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (10 BIT)



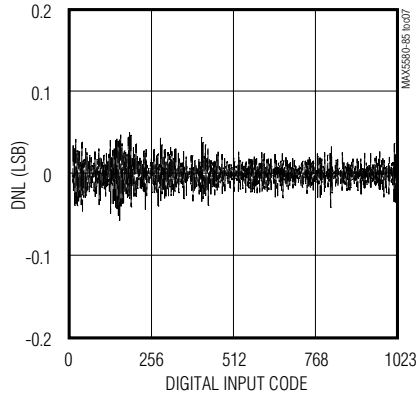
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (8 BIT)



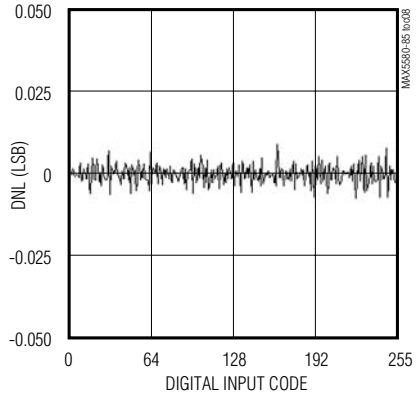
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (12 BIT)



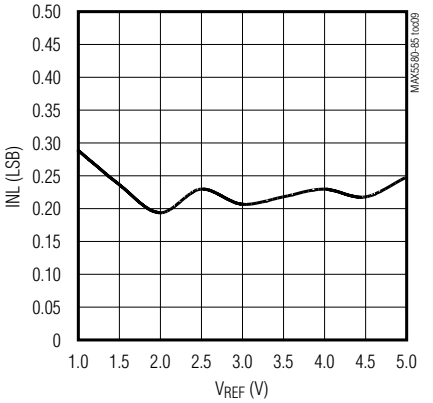
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (10 BIT)



DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (8 BIT)



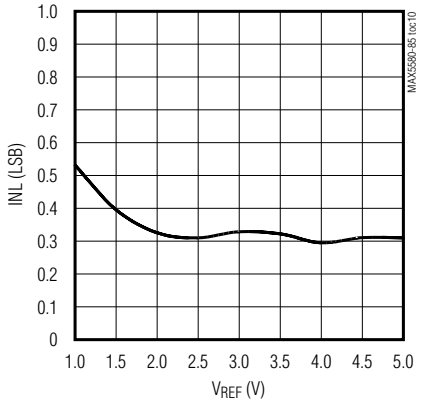
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (MAX5580A)



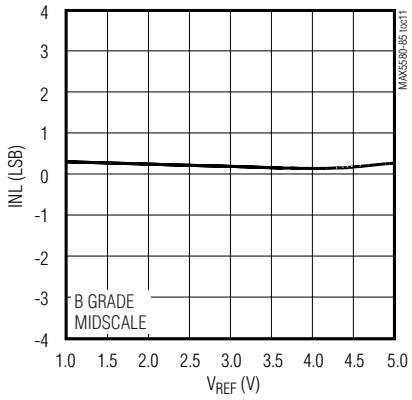
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

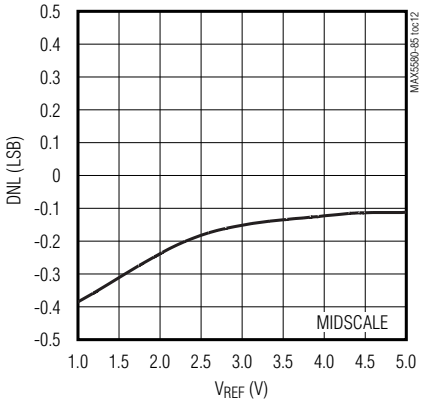
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (MAX5581A)



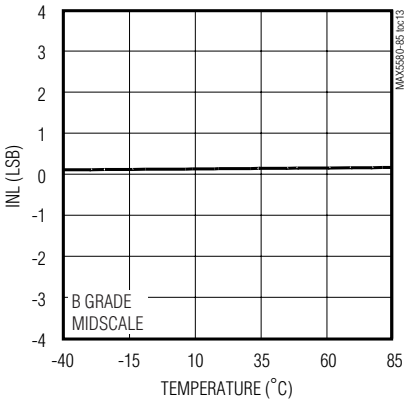
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (12 BIT)



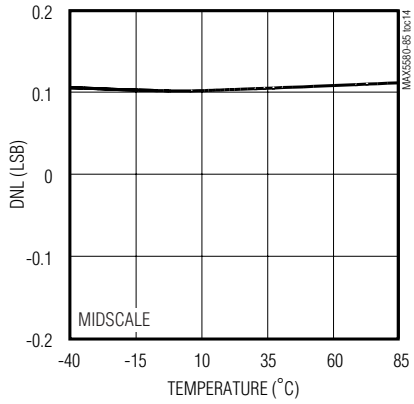
DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE (12 BIT)



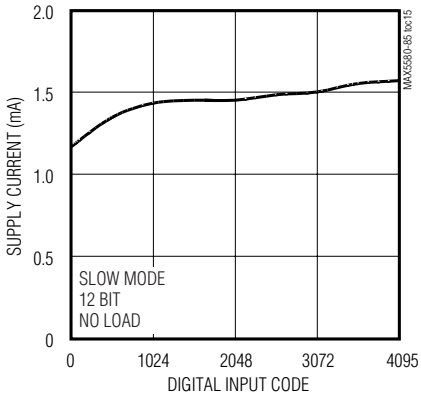
INTEGRAL NONLINEARITY vs. TEMPERATURE (12 BIT)



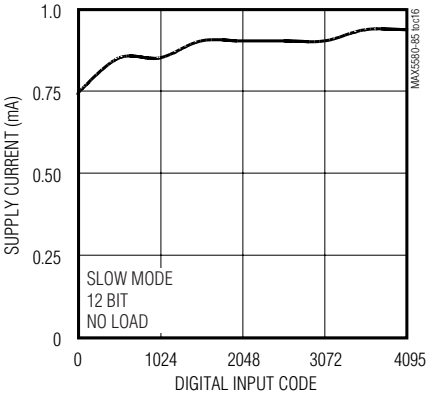
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE (12 BIT)



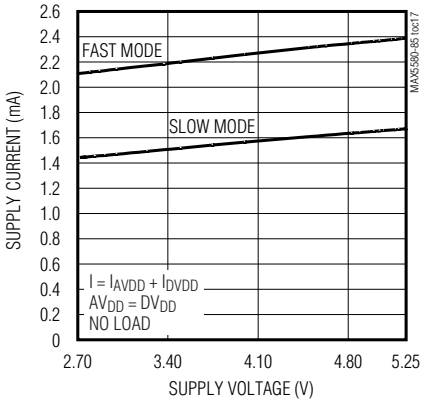
SUPPLY CURRENT vs. DIGITAL INPUT CODE (FORCE SENSE)



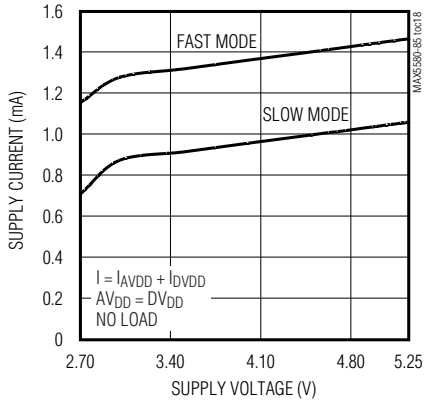
SUPPLY CURRENT vs. DIGITAL INPUT CODE (UNITY GAIN)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (FORCE SENSE)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (UNITY GAIN)

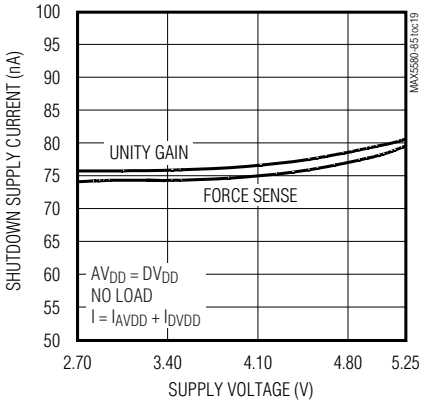


Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

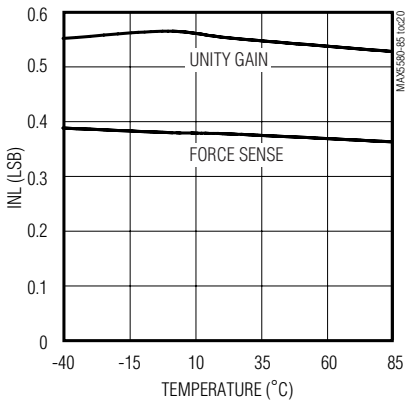
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

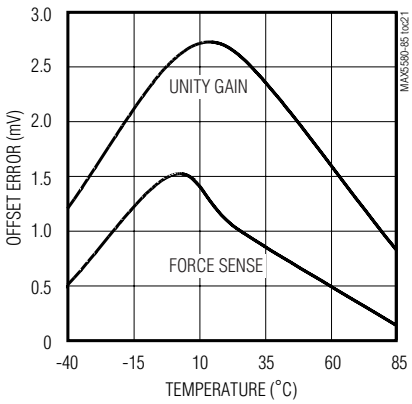
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



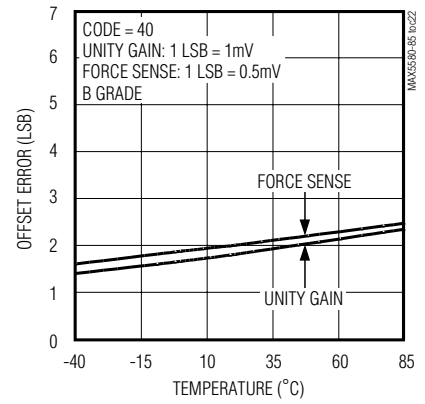
INTEGRAL NONLINEARITY vs. TEMPERATURE (A GRADE)



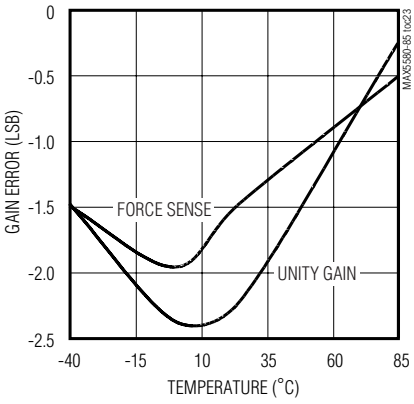
OFFSET ERROR vs. TEMPERATURE (A GRADE)



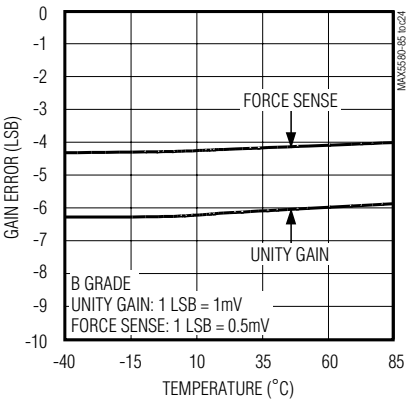
OFFSET ERROR vs. TEMPERATURE



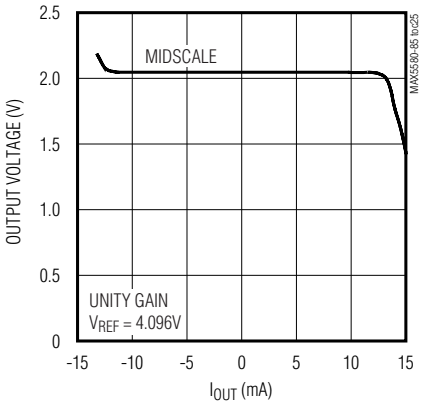
GAIN ERROR vs. TEMPERATURE (A GRADE)



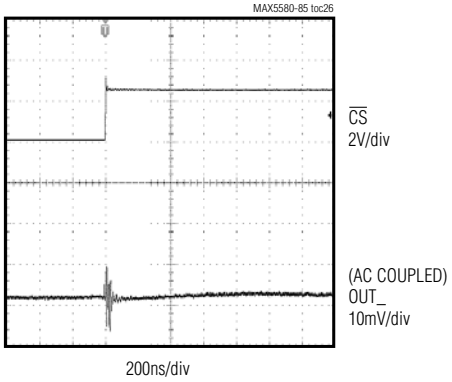
GAIN ERROR vs. TEMPERATURE



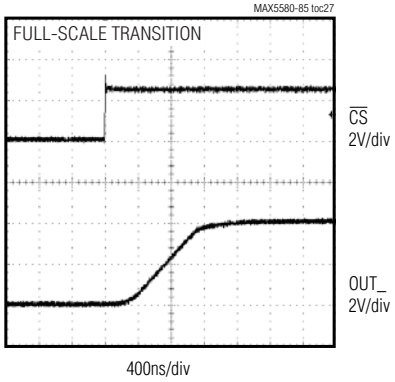
OUTPUT VOLTAGE vs. OUTPUT SOURCE/SINK CURRENT



MAJOR-CARRY TRANSITION GLITCH



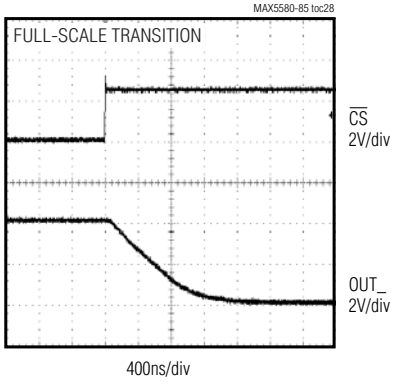
SETTLING TIME POSITIVE



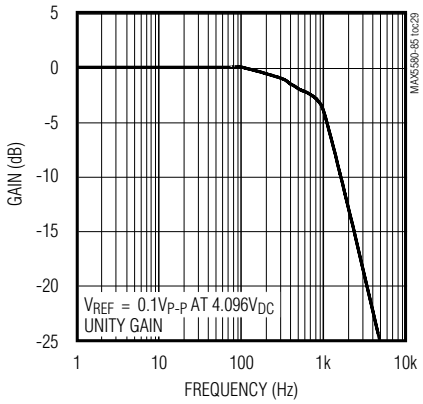
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

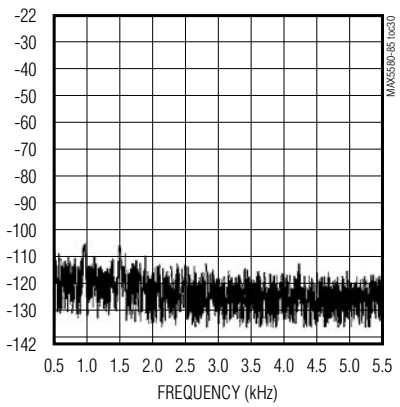
SETTLING TIME NEGATIVE



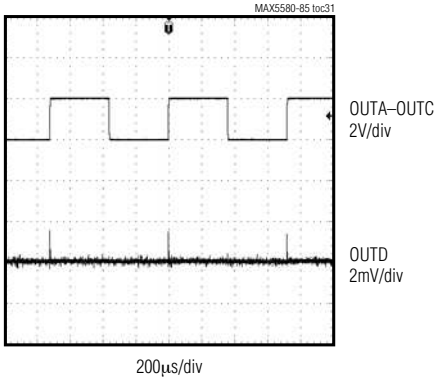
REFERENCE INPUT BANDWIDTH



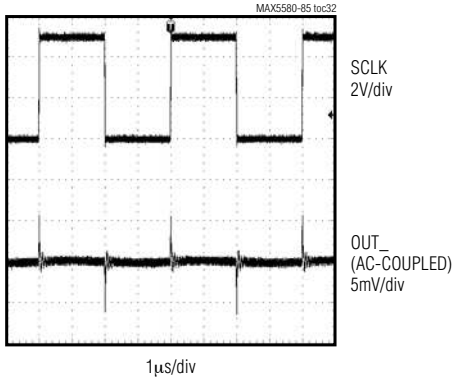
REFERENCE FEEDTHROUGH AT 1kHz



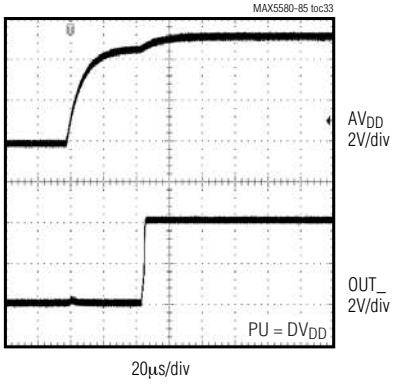
DAC-TO-DAC CROSSTALK



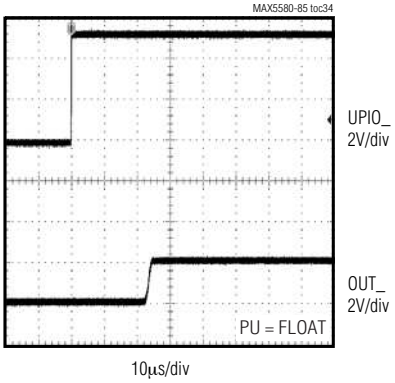
DIGITAL FEEDTHROUGH



POWER-UP GLITCH



EXITING SHUTDOWN TO MIDSCALE

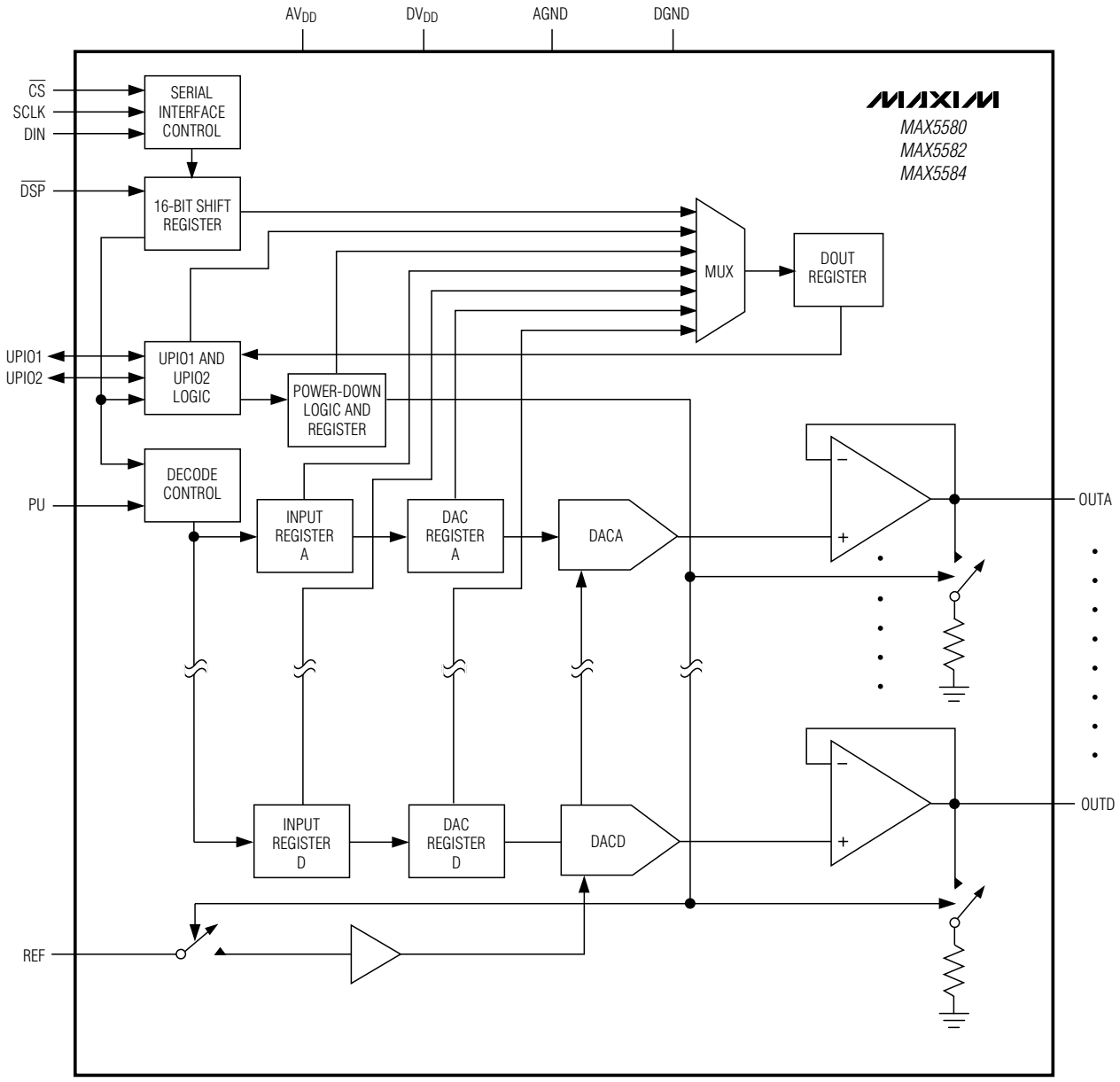


Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Pin Description

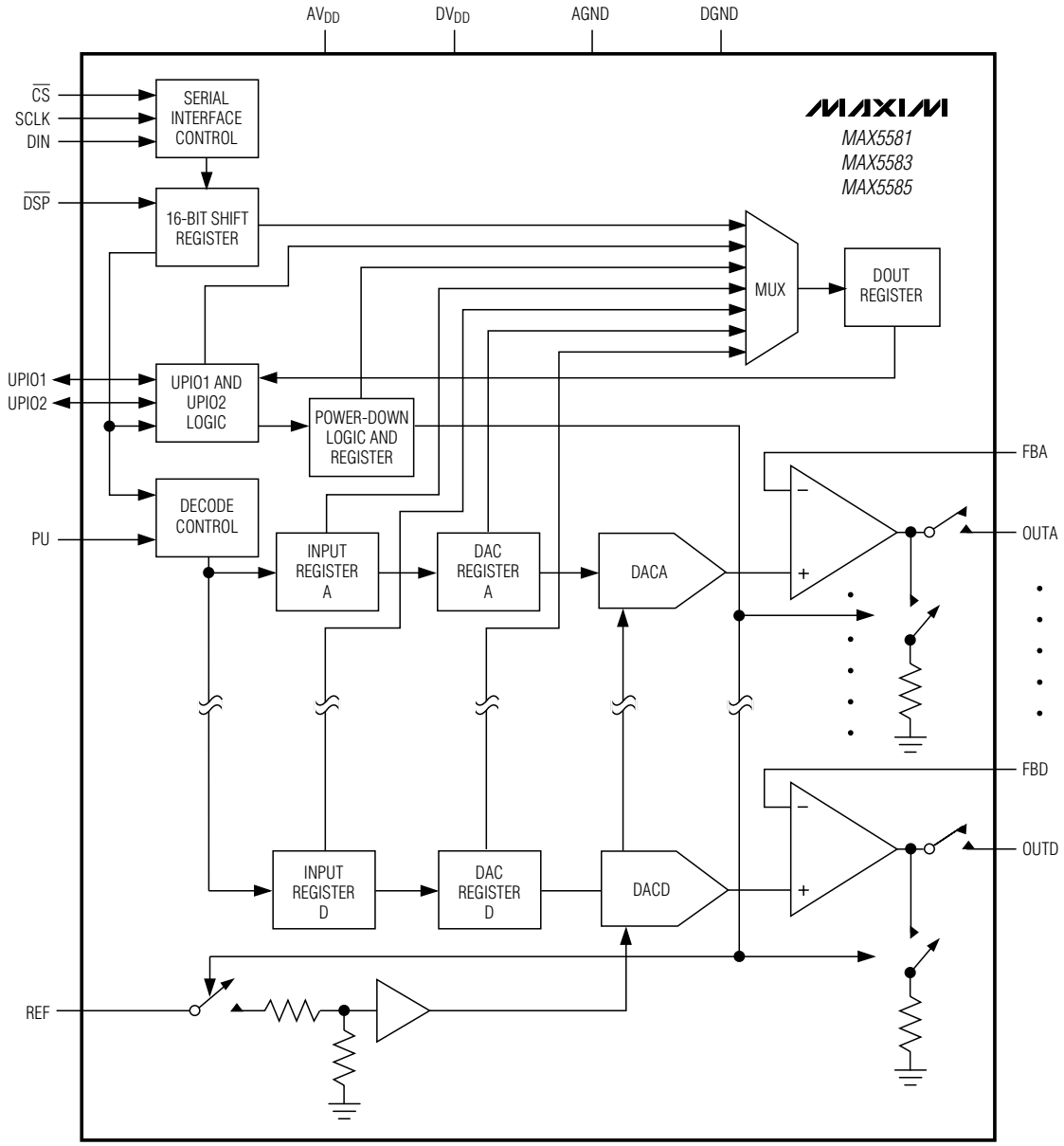
PIN		NAME	FUNCTION
MAX5580 MAX5582 MAX5584	MAX5581 MAX5583 MAX5585		
1	1	AGND	Analog Ground
2	2	AV_{DD}	Analog Supply
3, 5, 17, 19	—	N.C.	No Connection. Not internally connected.
—	3	FBB	Feedback for DACB
4	4	OUTB	DACB Output
—	5	FBA	Feedback for DACA
6	6	OUTA	DACA Output
7	7	PU	Power-Up State Select Input. Connect PU to DV_{DD} to set OUT_ to full scale upon power-up. Connect PU to DGND to set OUT_ to zero scale upon power-up. Float PU to set OUT_ to midscale upon power-up.
8	8	$\overline{CS}$	Active-Low Chip-Select Input
9	9	SCLK	Serial Clock Input
10	10	DIN	Serial Data Input
11	11	UPIO1	User-Programmable Input/Output 1
12	12	UPIO2	User-Programmable Input/Output 2
13	13	DV_{DD}	Digital Supply
14	14	DGND	Digital Ground
15	15	$\overline{DSP}$	Clock Enable. Connect $\overline{DSP}$ to DV_{DD} to clock in data on the rising edge of SCLK. Connect $\overline{DSP}$ to DGND to clock in data on the falling edge of SCLK.
16	16	OUTD	DACD Output
—	17	FBD	Feedback for DACD
18	18	OUTC	DACC Output
—	19	FBC	Feedback for DACC
20	20	REF	Reference Input
—	—	EP	Exposed Pad. Connect to AGND.

Functional Diagrams



Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Functional Diagrams (continued)



Detailed Description

The MAX5580–MAX5585 quad, 12-/10-/8-bit, voltage-output DACs offer buffered outputs and a 3µs maximum settling time at the 12-bit level. The DACs operate from a single 2.7V to 5.25V analog supply and a separate 1.8V to AV_{DD} digital supply. The MAX5580–MAX5585 include an input register and DAC register for each channel and a 16-bit data-in/data-out shift register. The 3-wire serial interface is compatible with SPI, QSPI, MICROWIRE, and DSP applications. The MAX5580–MAX5585 provide two user-programmable digital I/O ports, which are programmed through the serial interface. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale.

Reference Input

The reference input, REF, accepts both AC and DC values with a voltage range extending from analog ground (AGND) to AV_{DD}. The voltage at REF sets the full-scale output of the DACs. Determine the output voltage using the following equations:

Unity-gain versions:

$$V_{OUT\_} = (V_{REF} \times CODE) / 2^N$$

Force-sense versions (FB_ connected to OUT_):

$$V_{OUT} = 0.5 \times (V_{REF} \times CODE) / 2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX5580/MAX5581, N = 12 and CODE ranges from 0 to 4095. For the MAX5582/MAX5583, N = 10 and CODE ranges from 0 to 1023. For the MAX5584/MAX5585, N = 8 and CODE ranges from 0 to 255. Use the minature MAX6126 low-dropout, ultra-low-noise reference for optimum performance.

Output Buffers

The DACA–DACD output-buffer amplifiers of the MAX5580–MAX5585 are unity-gain stable with rail-to-rail output voltage swings and a typical slew rate of 3.6V/µs (FAST mode). The MAX5580/MAX5582/MAX5584 provide unity-gain outputs, while the MAX5581/MAX5583/MAX5585 provide force-sense outputs. For the MAX5581/MAX5583/MAX5585, access to the output amplifier's inverting input provides flexibility in output gain setting and signal conditioning (see the *Applications Information* section).

The MAX5580–MAX5585 offer FAST and SLOW settling-time modes. In the SLOW mode, the settling time is 6µs (max), and the supply current is 1.6mA (max). In the FAST mode, the settling time is 3µs (max), and the supply current is 4mA (max). See the *Digital Interface* section for settling-time mode programming details.

Use the serial interface to set the shutdown output impedance of the amplifiers to 1kΩ or 100kΩ for the MAX5580/MAX5582/MAX5584 and 1kΩ or high impedance for the MAX5581/MAX5583/MAX5585. The DAC outputs can drive a 10kΩ (typ) load and are stable with up to 500pF (typ) of capacitive load.

Power-On Reset

At power-up, all DAC outputs power up to full scale, midscale, or zero scale, depending on the configuration of the PU input. Connect PU to DV_{DD} to set OUT_ to full scale upon power-up. Connect PU to digital ground (DGND) at power-up to set OUT_ to zero scale. Leave PU floating to set OUT_ to midscale.

Digital Interface

The MAX5580–MAX5585 use a 3-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP protocol applications (Figures 1 and 2). Connect $\overline{DSP}$ to DV_{DD} before power-up to clock data in on the rising edge of SCLK. Connect $\overline{DSP}$ to DGND before power-up to clock data in on the falling edge of SCLK. After power-up, the device enters DSP frame-sync mode on the first rising edge of $\overline{DSP}$. Refer to the *MAX5580–MAX5585 Programmer's Handbook* for details.

The MAX5580–MAX5585 include a 16-bit input shift register. The data is loaded into the input shift register through the serial interface. The 16 bits can be sent in two serial 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until all 16 bits are transferred). The data is loaded MSB first. For the MAX5580/MAX5581, the 16 bits consist of 4 control bits (C3–C0) and 12 data bits (D11–D0) (see Table 1). For the 10-bit MAX5582/MAX5583 devices, D11–D2 are the data bits and D1 and D0 are sub-bits. For the 8-bit MAX5584/MAX5585 devices, D11–D4 are the data bits and D3–D0 are sub-bits. Set all sub-bits to zero for optimum performance.

Each DAC channel includes two registers: an input register and the DAC register. At power-up, the DAC output is set according to the state of PU. The DACs are double-buffered, which allows any of the following for each channel:

- Loading the input register without updating the DAC register
- Loading and updating the DAC register without updating the input register
- Updating the DAC register from the input register
- Updating the input and DAC registers simultaneously

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Table 1. Serial Write Data Format

MSB				16 BITS OF SERIAL DATA											LSB
CONTROL BITS				DATA BITS											
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

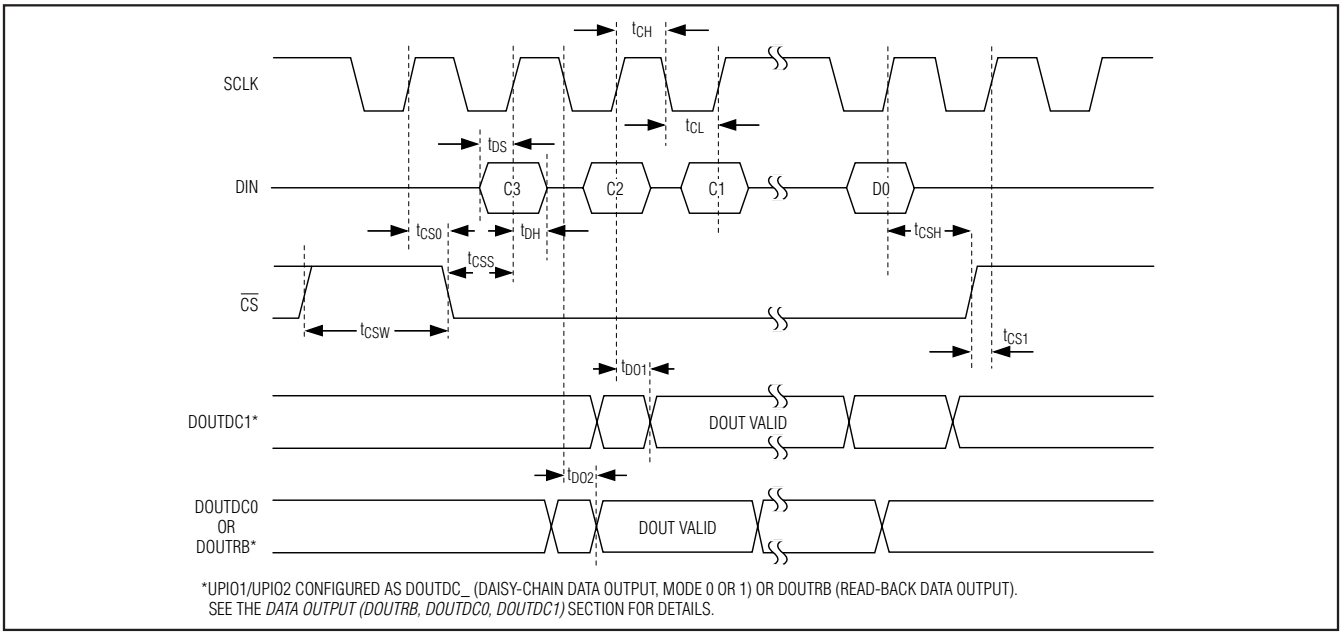


Figure 1. Serial-Interface Timing Diagram (DSP Mode Disabled)

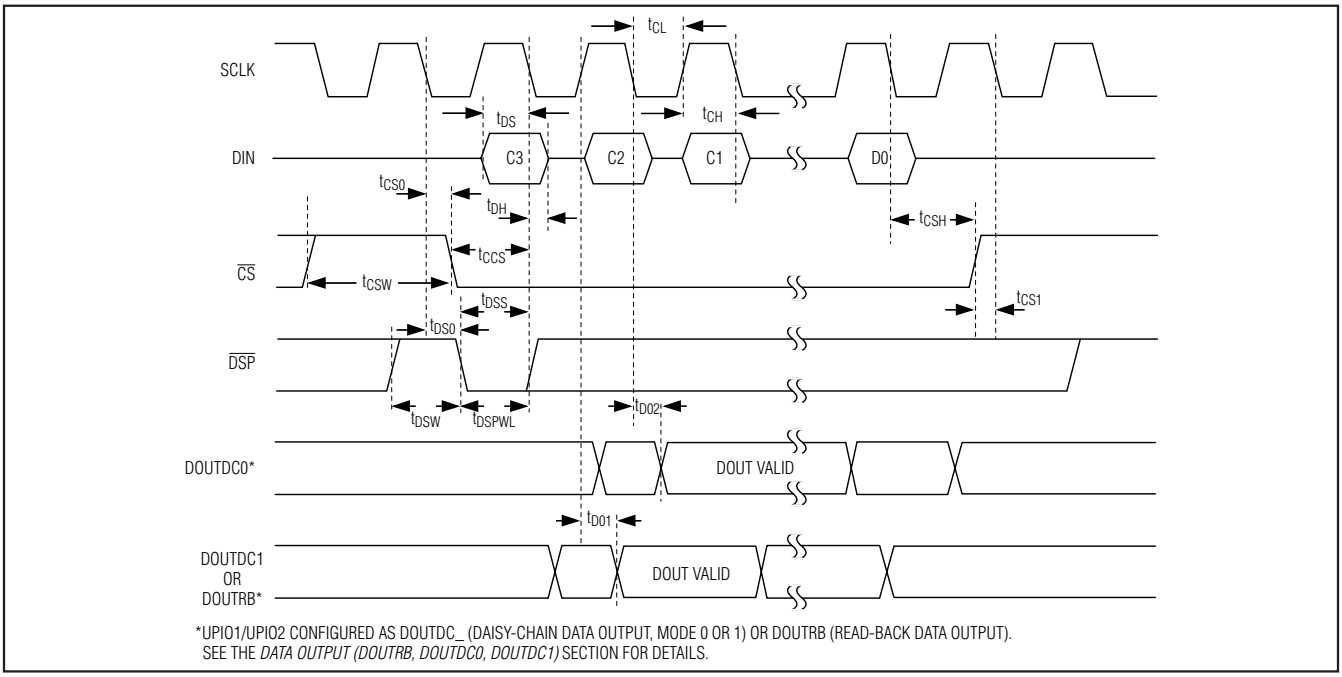


Figure 2. Serial-Interface Timing Diagram (DSP Mode Enabled)

Serial-Interface Programming Commands

Tables 2a, 2b, and 2c provide all the serial-interface programming commands for the MAX5580–MAX5585. Table 2a shows the basic DAC programming commands, Table 2b gives the advanced-feature programming commands, and Table 2c provides the 24-bit read commands. Figures 3 and 4 provide serial-interface diagrams for write operations.

Loading Input and DAC Registers

The MAX5580–MAX5585 contain a 16-bit shift register that is followed by a 12-bit input register and a 12-bit DAC register for each channel (see the *Functional Diagrams*). Tables 3, 4, and 5 highlight a few of the commands that handle the loading of the input and DAC registers. See Table 2a for all DAC programming commands.

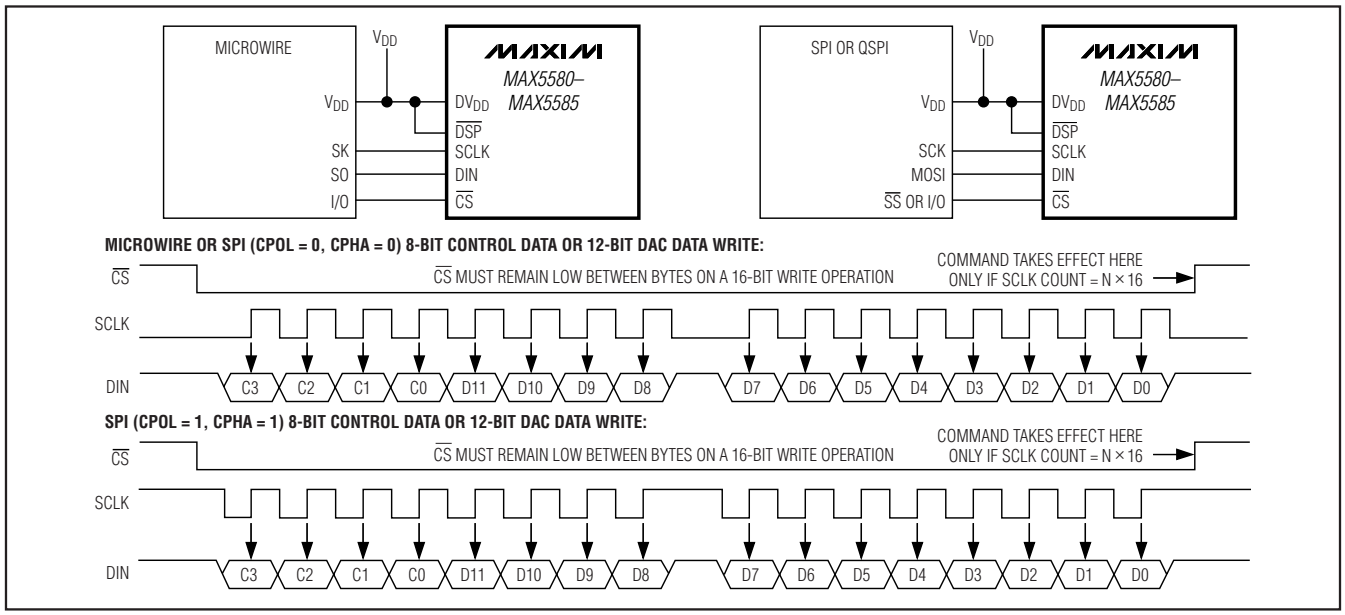


Figure 3. MICROWIRE and SPI Single DAC Writes (CPOL = 0, CPHA = 0 or CPOL = 1, CPHA = 1)

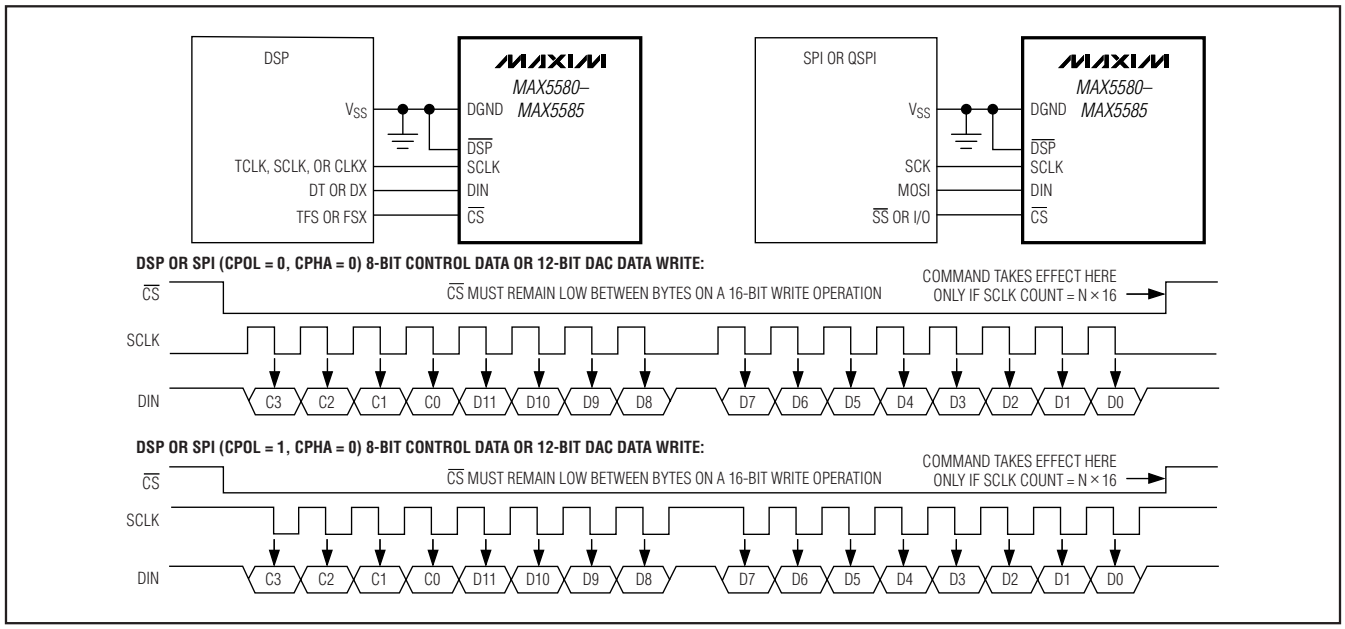


Figure 4. DSP and SPI Single DAC Writes (CPOL = 0, CPHA = 1 or CPOL = 1, CPHA = 0)

Table 2a. DAC Programming Commands

DATA	CONTROL BITS				DATA BITS												FUNCTION
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
INPUT REGISTERS (A–D)																	
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA input register from shift register; DACA output register is unchanged; DACA output is unchanged.*
DIN	0	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA output register from shift register; input register is unchanged; DACA output is updated.*
DIN	0	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA input register and output register from shift register; DACA output is updated.*
DIN	0	0	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB input register from shift register; DACB output register is unchanged; DACB output is unchanged.*
DIN	0	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB output register from shift register; input register is unchanged. DACB output is updated.*
DIN	0	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB input register and output register from shift register; DACB output is updated.*
DIN	0	1	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC input register from shift register; DACC output register is unchanged; DACC output is unchanged.*
DIN	0	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC output register from shift register; input register is unchanged; DACC output is updated.*
DIN	1	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC input register and output register from shift register; DACC output is updated.*
DIN	1	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD input register from shift register; DACD output register is unchanged; DACD output is unchanged.*
DIN	1	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD output register from shift register; input register is unchanged; DACD output is updated.*

Table 2a. DAC Programming Commands (continued)

DATA	CONTROL BITS				DATA BITS												FUNCTION
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
INPUT REGISTERS (A–D)																	
DIN	1	0	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD input register and output register from shift register; DACD output is updated.*
DIN	1	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load all DAC input registers from the shift register; all DAC output registers are unchanged; all DAC outputs are unchanged.*
DIN	1	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load all DAC input and output registers from shift register; DAC outputs are updated.*

**For the MAX5582/MAX5583 (10-bit version), D11–D2 are the significant bits and D1 and D0 are sub-bits. For the MAX5584/MAX5585 (8-bit version), D11–D4 are the significant bits and D3–D0 are sub-bits. Set all sub-bits to zero during the write commands.*

Table 2b. Advanced-Feature Programming Commands

DATA	CONTROL BITS				DATA BITS												Function
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
SELECT BITS																	
DIN	1	1	1	0	0	0	X	X	X	X	X	X	MD	MC	MB	MA	Load DAC_ output register from input register when M_ is one; DAC_ output register is unchanged if M_ is zero.
SHUTDOWN-MODE BITS																	
DIN	1	1	1	0	0	1	0	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0	Write DAC_ shutdown-mode bits; see Table 8.
DIN	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	Read DAC_ shutdown-mode bits.
DOUTR	X	X	X	X	X	X	X	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0	
UPIO CONFIGURATION BITS																	
DIN	1	1	1	0	1	0	0	X	UPSL2	UPSL1	UP3	UP2	UP1	UP0	X	X	Write UPIO configuration bits; see Table 18.
DIN	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	Read UPIO configuration bits.
DOUTR	X	X	X	X	X	X	X	X	UP3-2	UP2-2	UP1-2	UP0-2	UP3-1	UP2-1	UP1-1	UP0-1	
SETTLING-TIME-MODE BITS																	
DIN	1	1	1	0	1	1	0	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA	Write DAC_ settling-time-mode bits; see Table 11.

Table 2b. Advanced-Feature Programming Commands (continued)

DATA	CONTROL BITS				DATA BITS												Function
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DIN	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	Read DAC_ settling-time-mode bits.
DOUTR	X	X	X	X	X	X	X	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA	
DAC CPOL/CPHA BITS																	
DIN	1	1	1	1	0	0	0	0	X	X	X	X	X	X	CPOL	CPHA	Write CPOL, CPHA control bits.
DIN	1	1	1	1	0	0	0	1	X	X	X	X	X	X	X	X	Read CPOL, CPHA control bits.
DOUTR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPOL	CPHA	
UPIO_ AS GPI (GENERAL-PURPOSE INPUT)																	
DIN	1	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	Read UPIO_ inputs (valid only when UPIO1 or UPIO2 is configured as a general-purpose input); see Table 21.
DOUTRB	X	X	X	X	X	X	X	X	X	X	RTP2	LF2	LR2	RTP1	LF1	LR1	
OTHER COMMANDS																	
DIN	1	1	1	1	1	1	0	0	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	0	1	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	16-bit no-op command. all DACs are unaffected.

X = Don't care.

Table 2c. 24-Bit Read Commands

DATA	CONTROL BITS				DATA BITS																												FUNCTION
	C3	C2	C1	C0	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
READ INPUT AND DAC REGISTERS A—D																																	
DIN	1	1	1	1	0	1	0	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register A and DAC register A (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	D12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	0	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register B and DAC register B (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	D12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	1	0	0	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register C and DAC register C (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	E12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	1	0	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register D and DAC register D (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	E12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	

X = Don't care.

***D23–D12 represent the 12-bit data from the appropriate DAC output register. D11–D0 represent the 12-bit data from the corresponding input register. For the MAX5582/MAX5583, bits D13, D12, D1, and D0 are don't-care bits. For the MAX5584/MAX5585, bits D15–D12 and D3–D0 are don't-care bits.*

†During readback, all ones (0xFF) must be clocked into DIN for all 24 bits. No command can be issued before all 24 bits have been clocked out. CS must be kept low while all 24 bits are clocked out.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

DAC Programming Examples:
To load input register A from the shift register, leaving DAC register A unchanged (DAC output unchanged), use the command in Table 3.

The MAX5580–MAX5585 can load all the input registers (A–D) simultaneously from the shift register, leaving the DAC registers unchanged (DAC output unchanged), by using the command in Table 4.

To load all the input registers (A–D) and all the DAC registers (A–D) simultaneously, use the command in Table 5.

For the 10-bit and 8-bit versions, set sub-bits = 0 for best performance.

Advanced-Feature Programming Commands

Select Bits (M_)

The select bits allow synchronous updating of any combination of channels. The select bits command the loading of the DAC register from the input register of each channel. Set the select bit M_ = 1 to load the DAC register "_" with data from the input register "_", where "_" is replaced with A, B, C, or D, depending on the selected channel. Setting the select bit M_ = 0 results in no action for that channel (Table 6).

Select Bits Programming Example:
To load DAC register B from input register B while keeping other channels (A, C, D) unchanged, set MB = 1 and M_ = 0 (Table 7).

Table 3. Load Input Register A from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 4. Load Input Registers (A–D) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 5. Load Input Registers (A–D) and DAC Registers (A–D) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 6. Select Bits (M_)

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	0	X	X	X	X	X	X	MD	MC	MB	MA

X = Don't care.

Table 7. Select Bits Programming Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	0	X	X	X	X	X	X	0	0	1	0

X = Don't care.

Shutdown-Mode Bits (PD_0, PD_1)

Use the shutdown-mode bits and control bits to shut down each DAC independently. The shutdown-mode bits determine the output state of the selected channels. The shutdown-control bits put the selected channels into shutdown mode. To select the shutdown mode for DACA–DACD, set PD_0 and PD_1 according to Table 8 (where "_" is replaced with one of the selected channels (A–D)). The three possible states for unity-gain versions are 1) normal operation, 2) shutdown with 1kΩ output impedance, and 3) shutdown with 100kΩ output impedance. The three possible states for force-sense versions are 1) normal operation, 2) shutdown with 1kΩ output impedance, and 3) shutdown with the output in a high-impedance state. Table 9 shows the commands for writing to the shutdown-mode bits. Table 10 shows an example of writing the shutdown-control bits. This command shuts down DACA with 1kΩ to ground and shuts down DACB–DACD with 100kΩ to ground.

Always write the shutdown-mode-bits command first and then write the shutdown-control-bits command to properly shut down the selected channels. The shutdown-control-bits command can be written at any time after the shutdown-mode-bits command. It does not have to immediately follow the shutdown-mode-bits command.

Settling-Time-Mode Bits (SPD_)

The settling-time-mode bits select the settling time (FAST mode or SLOW mode) of the MAX5580–MAX5585. Set SPD_ = 1 to select FAST mode or set SPD_ = 0 to select SLOW mode, where "_" is replaced by A, B, C, or D, depending on the selected channel (Table 11). FAST mode provides a 3µs maximum settling time, and SLOW mode provides a 6µs maximum settling time.

Table 8. Shutdown-Mode Bits

PD_1	PD_0	DESCRIPTION
0	0	Shutdown with 1kΩ termination to ground on DAC_ output.
0	1	Shutdown with 100kΩ termination to ground on DAC_ output for unity-gain versions. Shutdown with high-impedance output for force-sense versions.
1	0	Ignored.
1	1	DAC_ is powered up in its normal operating mode.

Table 9. Shutdown-Mode Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	1	0	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0

X = Don't care.

Table 10. Shutdown-Mode-Bits Write Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	1	0	X	0	1	0	1	0	1	0	0

X = Don't care.

Table 11. Settling-Time-Mode Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	1	0	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA

X = Don't care.