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19-4593; Rev 3; 3/12

High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

General Description

The MAX5965A/MAX5965B are quad, monolithic, -48V power controllers designed for use in IEEE® 802.3af-compliant/IEEE 802.3at-compatible power-sourcing equipment (PSE). These devices provide powered device (PD) discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5965A/MAX5965B are pin compatible with the MAX5952/MAX5945/LTC4258/LTC4259A PSE controllers and provide additional features.

The MAX5965A/MAX5965B feature a high-power mode that provides up to 45W per port. The MAX5965A/MAX5965B provide new Class 5 and 2-event classification (Class 6) for detection and classification of high-power PDs. The MAX5965A/MAX5965B provide instantaneous readout of each port current through the I²C interface. The MAX5965A/MAX5965B also provide high-capacitance detection for legacy PDs.

These devices feature an I²C-compatible, 3-wire serial interface, and are fully software configurable and programmable. The class-overcurrent detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5965A/MAX5965B's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5965A/MAX5965B provide four operating modes to suit different system requirements. Auto mode allows the devices to operate automatically without any software supervision. Semi-automatic mode automatically detects and classifies a device connected to a port after initial software activation, but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5965A/MAX5965B provide input undervoltage lockout (UVLO), input undervoltage detection, a load-stability safety check during detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good status, and fault status. The MAX5965A/MAX5965B's programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5965A/MAX5965B are available in a 36-pin SSOP package and are rated for both extended (-40°C to +85°C) and upper commercial (0°C to +85°C) temperature ranges.

Applications

Power-Sourcing Equipment (PSE)
Switches/Routers
Midspan Power Injectors

Features

- **IEEE 802.3af Compliant/IEEE 802.3at Compatible**
- **Instantaneous Readout of Port Current Through I²C Interface**
- **High-Power Mode Enables Up to 45W Per Port**
- **High-Capacitance Detection for Legacy Devices**
- **Pin Compatible with MAX5952/MAX5945/LTC4258/LTC4259A**
- **Four Independent Power-Switch Controllers**
- **PD Detection and Classification (Including 2-Event Classification)**
- **Selectable Load-Stability Safety Check During Detection**
- **Supports Both DC and AC Load Removal Detections**
- **I²C-Compatible, 3-Wire Serial Interface**
- **Current Foldback and Duty-Cycle-Controlled Current Limit**
- **Open-Drain $\overline{INT}$ Signal**
- **Direct Fast Shutdown Control Capability**
- **Special Class 5 Classification**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5965AEAX+	-40°C to +85°C	36 SSOP
MAX5965AUAX+*	0°C to +85°C	36 SSOP
MAX5965BEAX+	-40°C to +85°C	36 SSOP
MAX5965BUAX+*	0°C to +85°C	36 SSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Selector Guide

PART	PIN-PACKAGE	AC DISCONNECT FEATURE
MAX5965AEAX+	36 SSOP	No
MAX5965AUAX+	36 SSOP	No
MAX5965BEAX+	36 SSOP	Yes
MAX5965BUAX+	36 SSOP	Yes

Pin Configuration appears at end of data sheet.

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High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)
AGND, DGND, DET_, V_{DD}, $\overline{RESET}$, A3–A0, $\overline{SHD\_}$, OSC, SCL, SDAIN, AUTO .....-0.3V to +80V
OUT_.....-12V to (AGND + 0.3V)
GATE_ (internally clamped) (Note 1) .....-0.3V to +11.4V
SENSE_ .....-0.3V to +24V
V_{DD}, $\overline{RESET}$, MIDSPAN, A3–A0, $\overline{SHD\_}$, OSC, SCL, SDAIN and AUTO to DGND .....-0.3V to +7V
$\overline{INT}$ and SDAOUT to DGND.....-0.3V to +12V
Maximum Current into $\overline{INT}$, SDAOUT, DET_.....80mA

Maximum Power Dissipation (T_A = +70°C)
36-Pin SSOP (derate 17.4mW/°C above +70°C) 1388.9mW
Operating Temperature Ranges:
MAX5965A/MAX5965B_EAX.....-40°C to +85°C
MAX5965A/MAX5965B_UAX.....0°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: GATE_ is internally clamped to 11.4V above V_{EE}. Driving GATE_ higher than 11.4V above V_{EE} may damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}	32		60	V
	V_{DGND}		0		60	
	V_{DD}	V_{DD} to V_{DGND}, V_{DGND} = V_{AGND}	2.4		3.6	
		V_{DD} to V_{DGND}, V_{DGND} = V_{EE}	3.0		3.6	
Supply Currents	I_{EE}	$V_{OUT\_}$ = V_{EE}, $V_{SENSE\_}$ = V_{EE}, DET_ = AGND, all logic inputs open, SCL = SDAIN = V_{DD}. $\overline{INT}$ and SDAOUT unconnected. Measured at AGND in power mode after GATE_ pullup		4.8	6.8	mA
	I_{DIG}	All logic inputs high, measured at V_{DD}		0.2	0.4	
GATE DRIVER AND CLAMPING						
GATE_ Pullup Current	I_{PU}	Power mode, gate drive on, $V_{GATE\_}$ = V_{EE} (Note 3)	-40	-50	-65	µA
Weak GATE_ Pulldown Current	I_{PDW}	$\overline{SHD\_}$ = DGND, $V_{GATE\_}$ = V_{EE} + 10V		42		µA
Maximum Pulldown Current	I_{PDS}	$V_{SENSE\_}$ = 600mV, $V_{GATE\_}$ = V_{EE} + 2V		100		mA
External Gate Drive	V_{GS}	$V_{GATE\_}$ - V_{EE}, power mode, gate drive on, I_{PU} = 1µA	9	10	11.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
Current-Limit Clamp Voltage	V_{SU_LIM}	Maximum $V_{SENSE\_}$ allowed during current limit, $V_{OUT\_}$ = 0V (ICUT = 000) (Note 4)	IVEE = 00	202	212	220	mV
			IVEE = 01	192	202	212	
			IVEE = 10	186	190	200	
			IVEE = 11	170	180	190	
Overcurrent Threshold After Startup	V_{FLT_LIM}	Overcurrent $V_{SENSE\_}$ threshold allowed for $t \le t_{FAULT}$ after startup; $V_{OUT\_}$ = 0V (IVEE = 00)	ICUT = 000 (Class 0/3)	177	186	196	mV
			ICUT = 110 (Class 1)	47	55	64	
			ICUT = 111 (Class 2)	86	94	101	
			ICUT = 001	265	280	295	
			ICUT = 010	310	327	345	
			ICUT = 011	355	374	395	
			ICUT = 100	398	419	440	
			ICUT = 101	443	466	488	
Foldback Initial OUT_ Voltage	V_{FLBK_ST}	$V_{OUT\_}$ - V_{EE}, above which the current-limit trip voltage starts folding back, IVEE = 00	ICUT = 000, ICUT = 110, ICUT = 111		32		V
			ICUT = 001…101		13		
Foldback Final OUT_ Voltage	V_{FLBK_END}	IVEE = 00, ICUT = 000, $V_{OUT\_}$ - V_{EE} above which the current-limit trip voltage reaches V_{TH_FB}			50		V
Minimum Foldback Current-Limit Threshold	V_{TH_FB}	$V_{OUT\_}$ = AGND = 60V, IVEE = 00, ICUT = 000			64		mV
SENSE_ Input Bias Current		$V_{SENSE\_}$ = V_{EE}		-5		+5	µA

High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY MONITORS						
V_{EE} Undervoltage Lockout	V_{EEUVLO}	V_{AGND} - V_{EE}, V_{AGND} - V_{EE} increasing		28.5		V
V_{EE} Undervoltage Lockout Hysteresis	$V_{EEUVLOH}$	Ports shut down if V_{AGND} - V_{EE} < V_{UVLO} - $V_{EEUVLOH}$		3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	V_{EE_OV} event bit sets and ports shut down if V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} increasing		62.5		V
V_{EE} Overvoltage Lockout Hysteresis	V_{OVH}			1		V
V_{EE} Undervoltage	V_{EE_UV}	V_{EE_UV} event bit is set if V_{AGND} - V_{EE} < V_{EE_UV}, V_{EE} increasing		40		V
V_{DD} Overvoltage	V_{DD_OV}	V_{DD_OV} event bit is set if V_{DD} - V_{DGND} > V_{DD_OV}; V_{DD} increasing		3.82		V
V_{DD} Undervoltage	V_{DD_UV}	V_{DD_UV} is set if V_{DD} - V_{DGND} < V_{DD_UV}, V_{DD} decreasing		2.7		V
V_{DD} Undervoltage Lockout	V_{DDUVLO}	Device operates when V_{DD} - V_{DGND} > V_{DDUVLO}, V_{DD} increasing		2		V
V_{DD} Undervoltage Lockout Hysteresis	V_{DDHYS}			120		mV
Thermal Shutdown Threshold	T_{SHD}	Ports shut down and device resets if its junction temperature exceeds this limit, temperature increasing (Note 5)		+150		°C
Thermal Shutdown Hysteresis	T_{SHDH}	Thermal hysteresis, temperature decreasing (Note 5)		20		°C
OUTPUT MONITOR						
OUT_ Input Current	I_{BOUT}	$V_{OUT\_}$ = V_{AGND}, all modes			2	µA
Idle Pullup Current at OUT_	I_{DIS}	OUT_ discharge current, detection and classification off, port shutdown, $V_{OUT\_}$ = AGND - 2.8V	200		265	µA
PGOOD High Threshold	PG_{TH}	$V_{OUT\_}$ - V_{EE}, $V_{OUT\_}$ decreasing	1.5	2.0	2.5	V
PGOOD Hysteresis	PG_{HYS}			220		mV
PGOOD Low-to-High Glitch Filter	t_{PGOOD}	Minimum time PGOOD has to be high to set bit in register 10h		3		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOAD DISCONNECT						
DC Load Disconnect Threshold	V_{DCTH}	Minimum $V_{SENSE\_}$ allowed before disconnect (DC disconnect active), $V_{OUT\_}$ = 0V	2.5	3.75	5.0	mV
AC Load Disconnect Threshold	I_{ACTH}	Current into DET_, for I < I_{ACTH} the port powers off, ACD_EN_ bit = H; V_{OSC} = 2.2V, MAX5965B (Note 6)	285	320	360	µA
Oscillator Buffer Gain	A_{OSC}	$V_{DET\_}/V_{OSC}$, ACD_EN_ bit = H, MAX5965B	2.9	3.0	3.1	V/V
OSC Fail Threshold	V_{OSC_FAIL}	Port does not power on if V_{OSC} < V_{OSC_FAIL} and ACD_EN_ bit is high, MAX5965B (Note 7)	1.8		2.2	V
OSC Input Impedance	Z_{OSC}	OSC input impedance when all the ACD_EN_ are active, MAX5965B	100			kΩ
Load Disconnect Timer	t_{DISC}	Time from $V_{SENSE\_}$ < V_{DCTH} to gate shutdown (Note 8)	300		400	ms
DETECTION						
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - $V_{DET\_}$ during the first detection phase	3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - $V_{DET\_}$ during the second detection phase	9.0	9.3	9.6	V
Current-Limit Protection	I_{DLIM}	$V_{DET\_}$ = V_{AGND}, during detection, measure current through DET_	1.5	1.8	2.2	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - $V_{OUT\_}$ < V_{DCP} after the first detection phase a short circuit to AGND is detected		1		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition		12.5		µA
Resistor Detection Window	R_{DOK}	(Note 9)	19.0		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values			15.2	kΩ
		Detection rejects higher values	32			

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS (Referred to DGND)							
Digital Input Low	V_{IL}					0.9	V
Digital Input High	V_{IH}			2.4			V
Internal Input Pullup/Pulldown Resistor	R_{DIN}	Pullup (pulldown) resistor to V_{DD} (DGND) to set default level		25	50	75	kΩ
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 15mA				0.4	V
Digital Input Leakage	I_{DL}	Input connected to the pull voltage				2	µA
Open-Drain Leakage	I_{OL}	Open-drain high impedance, $V_{OUT\_}$ = 3.3V				2	µA
TIMING							
Startup Time	t_{START}	Time during which a current limit set by V_{SU_LIM} is allowed, starts when the GATE_ is turned on (Note 9)		50	60	70	ms
Fault Time	t_{FAULT}	Maximum allowed time for an overcurrent condition set by V_{FLT_LIM} after startup (Note 9)		50	60	70	ms
Port Turn-Off Time	t_{OFF}	Minimum delay between any port turning off, does not apply in case of a reset			0.5		ms
Detection Reset Time		Time allowed for the port voltage to reset before detection starts			80	90	ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed				330	ms
Midspan Mode Detection Delay	t_{DMID}			2.0		2.4	s
Classification Time	t_{CLASS}	Time allowed for classification			19	23	ms
V_{EEUVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EEUVLO} thresholds before the device operates		2		4	ms
Restart Timer	$t_{RESTART}$	Time a port has to wait before turning on after an overcurrent fault during normal operation, RSTR_EN bits = high	RSTR bits = 00		16 x t_{FAULT}		ms
			RSTR bits = 01		32 x t_{FAULT}		
			RSTR bits = 10		64 x t_{FAULT}		
			RSTR bits = 11		0		
Watchdog Clock Period	t_{WD}	Rate of decrement of the watchdog timer			164		ms
ADC PERFORMANCE							
Resolution					9		Bits
Range					0.51		V
LSB Step Size					1		mV
Integral Nonlinearity (Relative)	INL				0.2	1.5	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity	DNL			0.2	1.5	LSB
Gain Error					3	%
ADC Absolute Accuracy		$V_{SENSE\_}$ = 300mV	295	300	305	LSB
TIMING CHARACTERISTICS (For 2-Wire Fast Mode)						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.2			µs
Hold Time for a START Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.2			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		100		300	ns
Data in Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R		20 + $0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F		20 + $0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}				50	ns

Note 2: Limits to T_A = -40°C are guaranteed by design.

Note 3: Default values. The charge/discharge currents are programmable through the serial interface (see the *Register Map and Description* section).

Note 4: Default values. The current-limit thresholds are programmed through the I²C-compatible serial interface (see the *Register Map and Description* section).

Note 5: Functional test is performed over thermal shutdown entering test mode.

Note 6: This is the default value. Threshold can be programmed through serial interface R23h[2:0].

Note 7: AC disconnect works only if (V_{DD} - V_{DGND}) ≥ 3V and DGND is connected to AGND.

Note 8: t_{DISC} can also be programmed through the serial interface (R16h) (see the *Register Map and Description* section).

Note 9: R_D = (V_{OUT2} - V_{OUT1})/(I_{DET2} - I_{DET1}). V_{OUT1}, V_{OUT2}, I_{DET2}, and I_{DET1} represent the voltage at OUT_ and the current at DET_ during phase 1 and 2 of the detection.

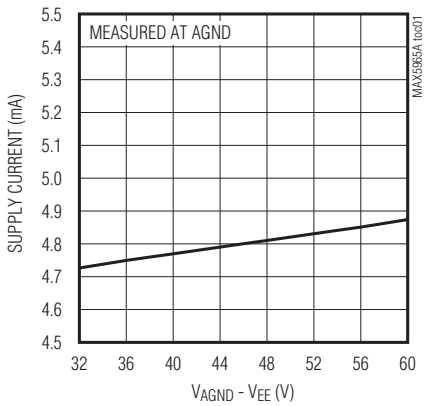
Note 10: Default values. The startup and fault times can also be programmed through the I²C serial interface (see the *Register Map and Description* section).

High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

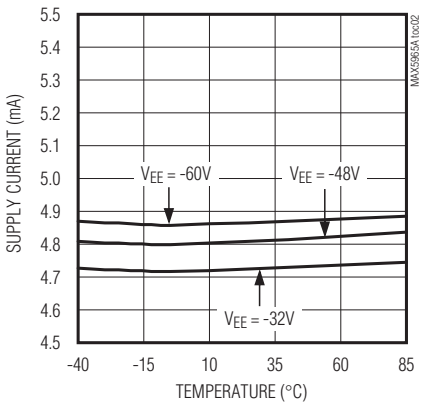
Typical Operating Characteristics

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, $R_{SENSE\_}$ = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

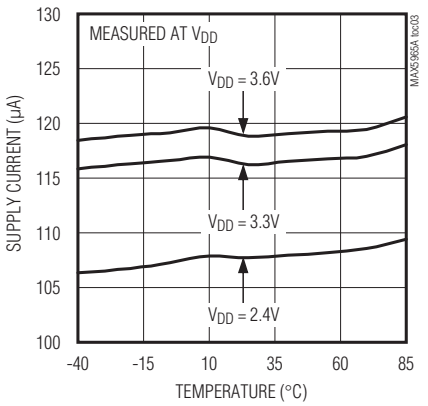
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



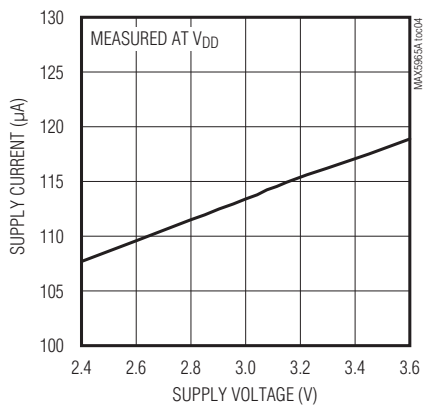
ANALOG SUPPLY CURRENT vs. TEMPERATURE



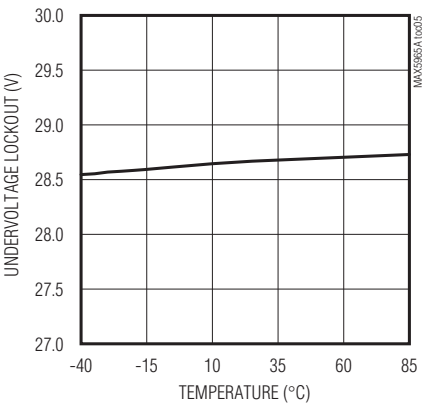
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



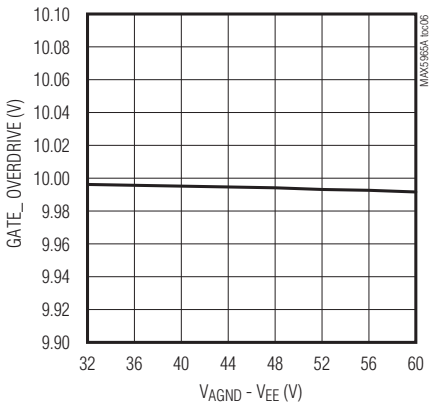
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



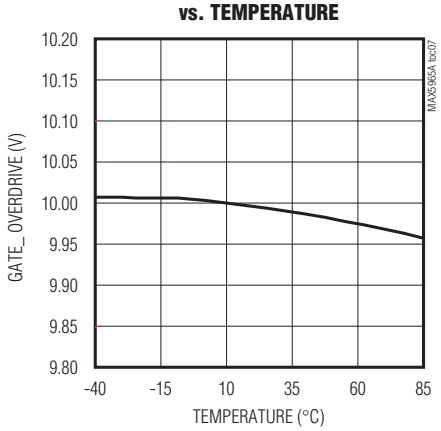
VEE UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



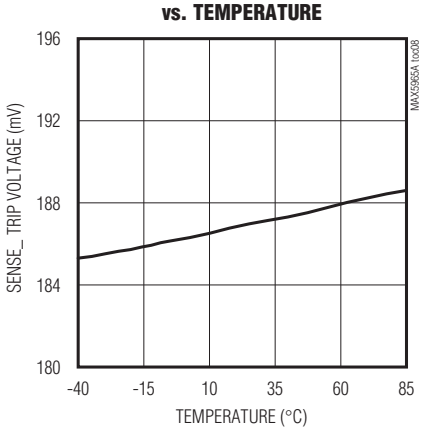
GATE_ OVERDRIVE vs. INPUT VOLTAGE



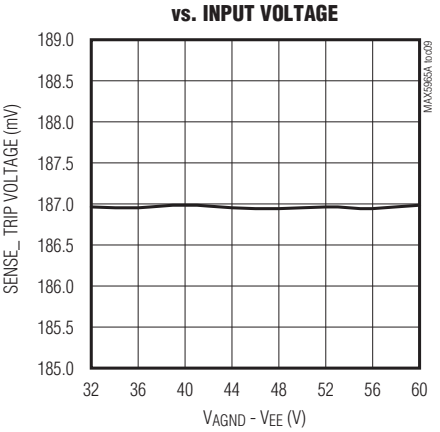
GATE_ OVERDRIVE vs. TEMPERATURE



SENSE_ TRIP VOLTAGE vs. TEMPERATURE



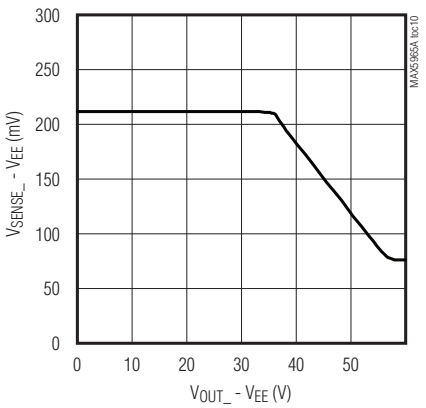
SENSE_ TRIP VOLTAGE vs. INPUT VOLTAGE



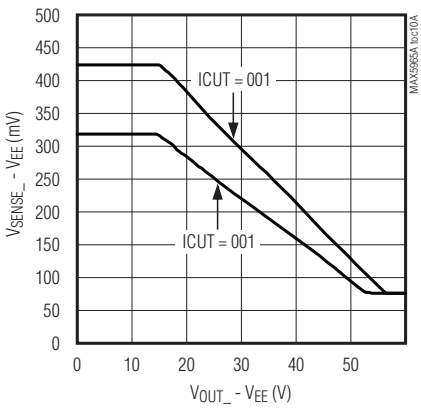
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, $R_{SENSE\_}$ = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

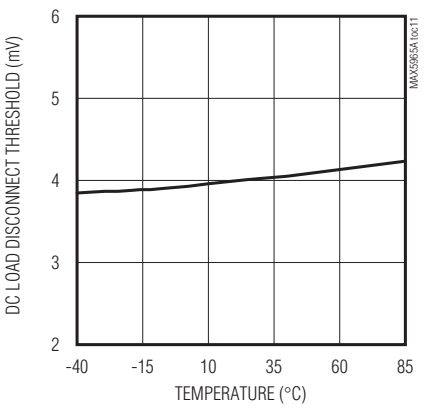
FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



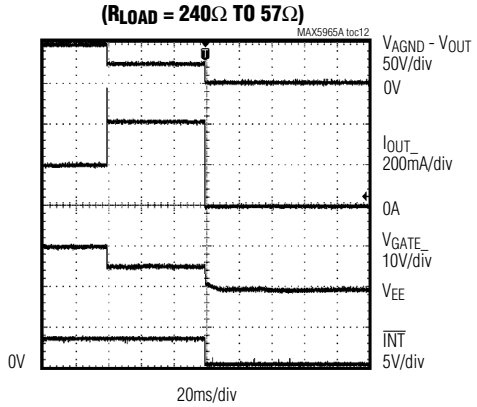
FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



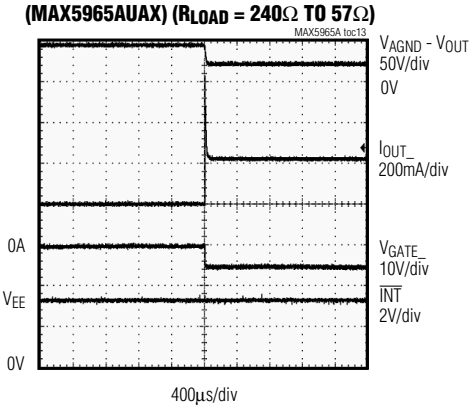
DC LOAD DISCONNECT THRESHOLD vs. TEMPERATURE



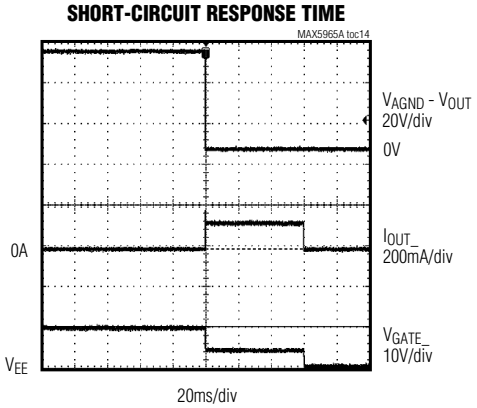
OVERCURRENT TIMEOUT (R_{LOAD} = 240Ω TO 57Ω)



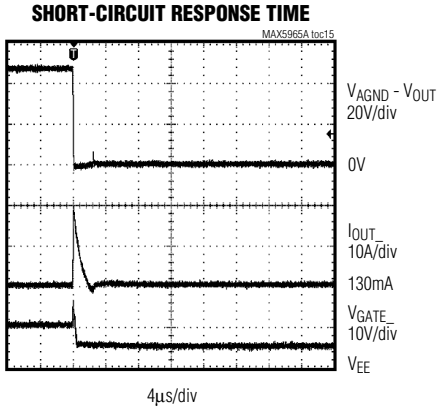
OVERCURRENT RESPONSE WAVEFORM (MAX5965AUAX) (R_{LOAD} = 240Ω TO 57Ω)



SHORT-CIRCUIT RESPONSE TIME



SHORT-CIRCUIT RESPONSE TIME

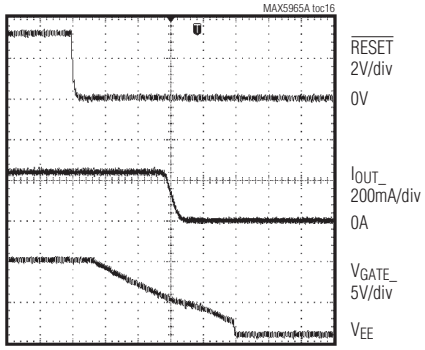


High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

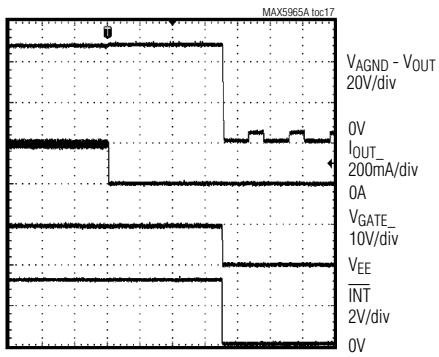
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, $R_{SENSE\_}$ = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

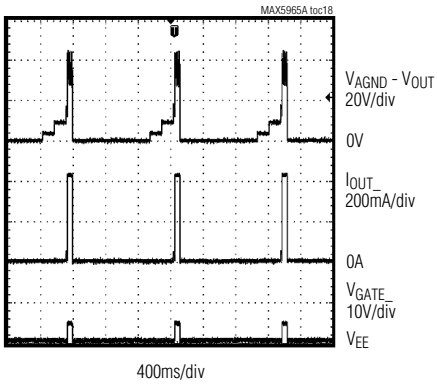
$\overline{RESET}$ TO OUT TURN-OFF DELAY



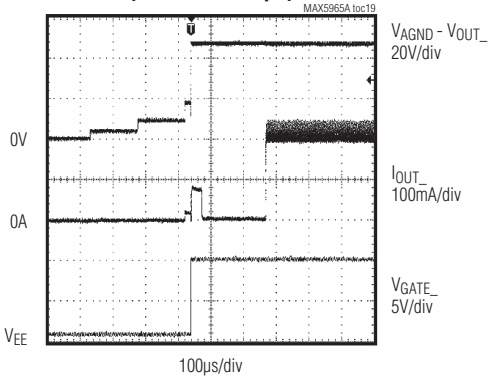
ZERO-CURRENT DETECTION WAVEFORM



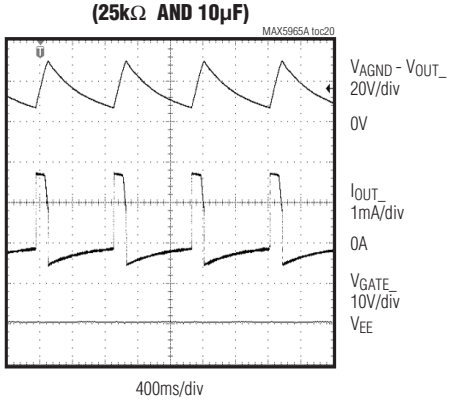
OVERCURRENT RESTART DELAY



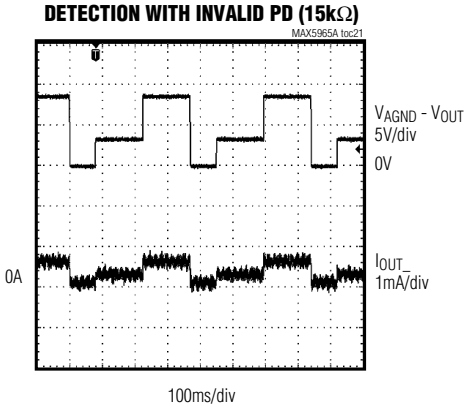
STARTUP WITH VALID PD (25kΩ AND 0.1µF)



DETECTION WITH INVALID PD (25kΩ AND 10µF)



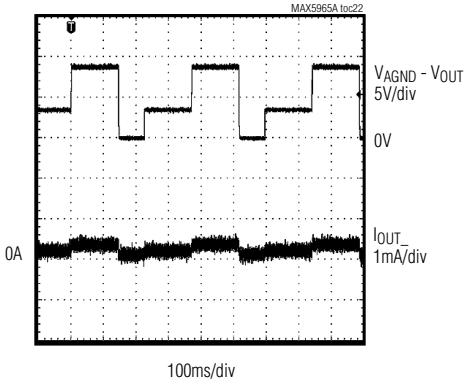
DETECTION WITH INVALID PD (15kΩ)



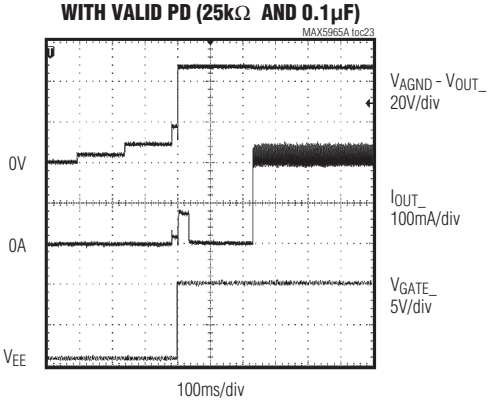
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, $R_{SENSE\_}$ = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

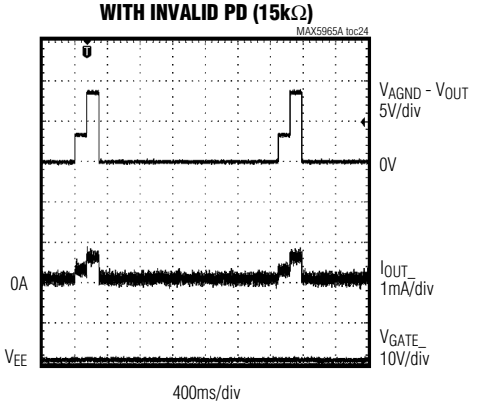
DETECTION WITH INVALID PD (33kΩ)



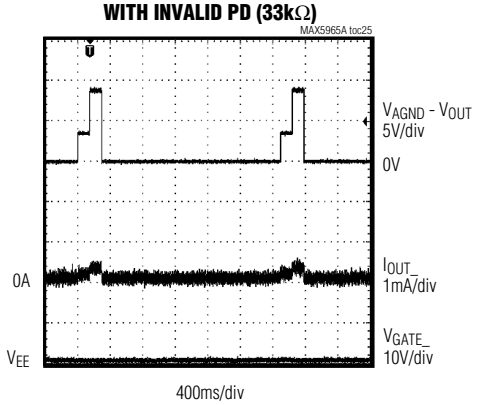
STARTUP IN MIDSPAN MODE WITH VALID PD (25kΩ AND 0.1µF)



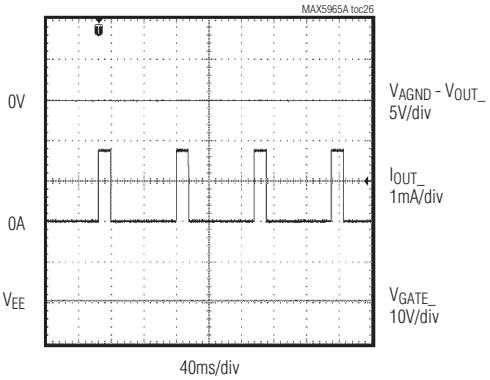
DETECTION WITH MIDSPAN MODE WITH INVALID PD (15kΩ)



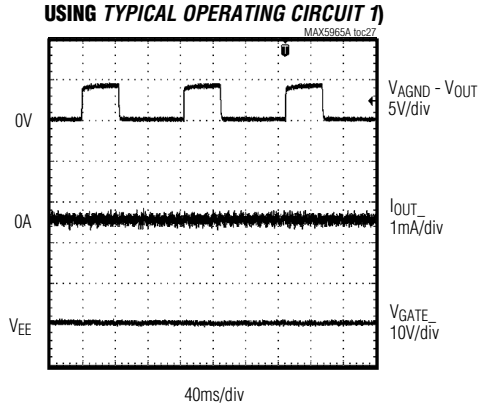
DETECTION WITH MIDSPAN MODE WITH INVALID PD (33kΩ)



OUTPUT SHORTED



DETECTION WITH INVALID PD (OPEN CIRCUIT, USING *TYPICAL OPERATING CIRCUIT 1*)

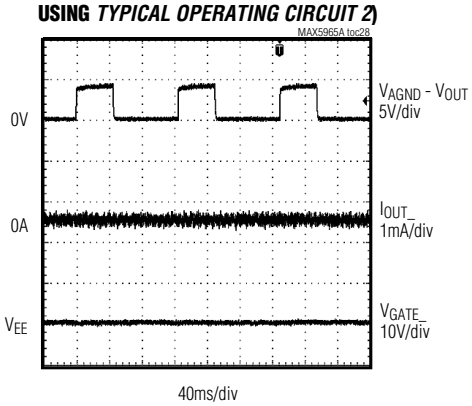


High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

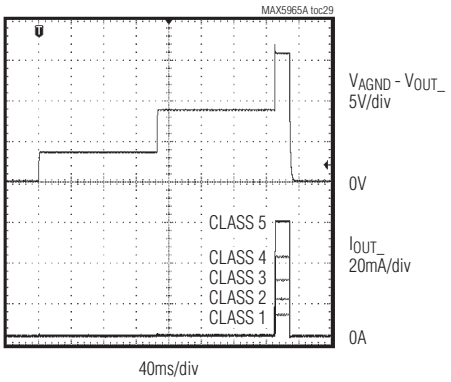
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, $R_{SENSE\_}$ = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

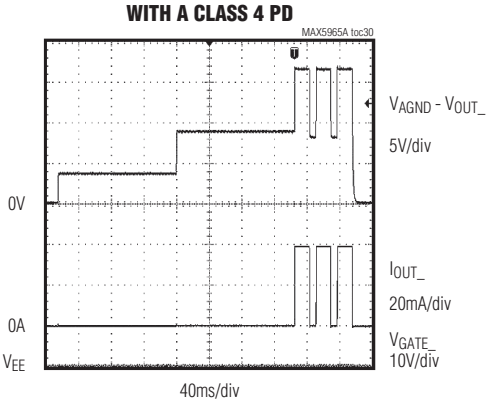
DETECTION WITH INVALID PD (OPEN CIRCUIT, USING *TYPICAL OPERATING CIRCUIT 2*)



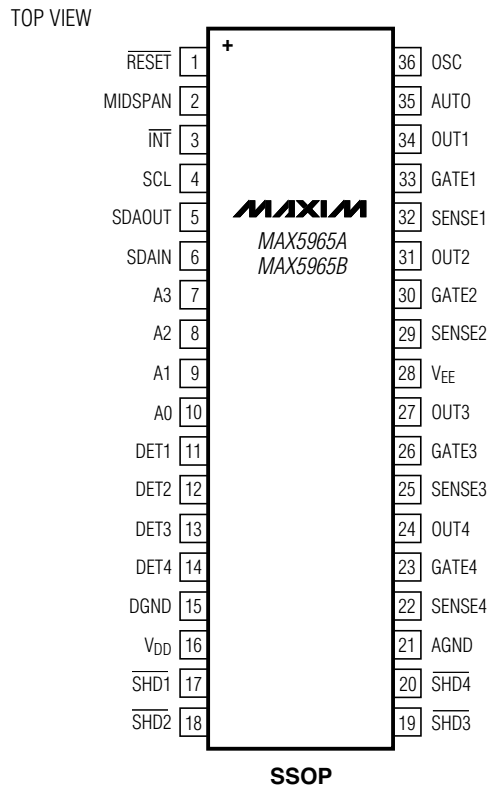
STARTUP WITH DIFFERENT PD CLASSES



2-EVENT CLASSIFICATION WITH A CLASS 4 PD



Pin Configuration



Pin Description

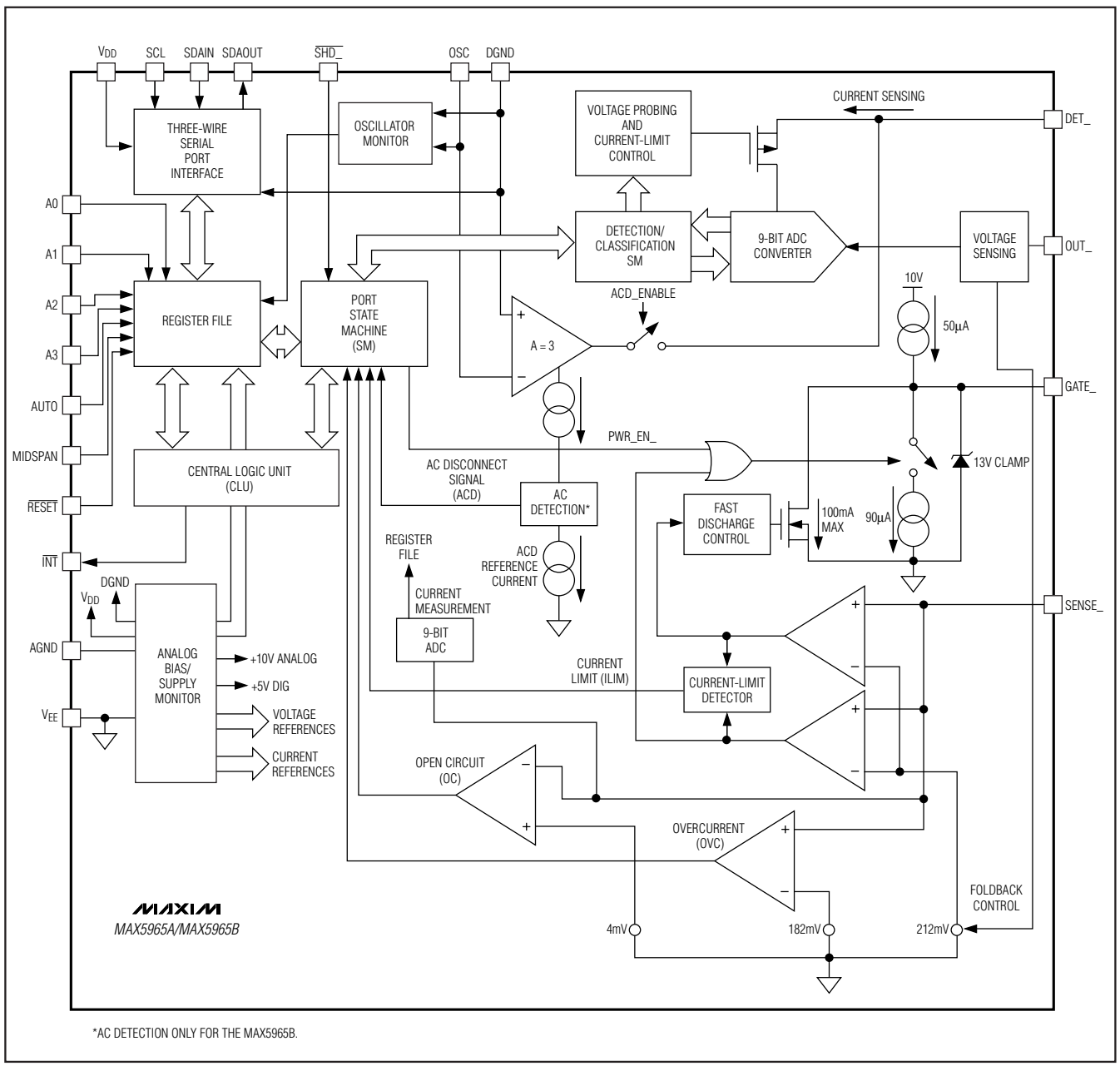
PIN	NAME	FUNCTION
1	$\overline{\text{RESET}}$	Hardware Reset. Pull $\overline{\text{RESET}}$ low for at least 300µs to reset the device. All internal registers reset to their default value. The address (A0–A3), and AUTO and MIDSPAN input-logic levels latch on during low-to-high transition of $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ is internally pulled up to V_{DD} with a 50kΩ resistor.
2	MIDSPAN	Midspan Mode Input. An internal 50kΩ pulldown resistor to DGND sets the default mode to endpoint PSE operation (power-over-signal pairs). Pull MIDSPAN to V_{DIG} to set midspan operation. The MIDSPAN value latches after the device is powered up or reset (see the *PD Detection* section).
3	$\overline{\text{INT}}$	Open-Drain Interrupt Output. $\overline{\text{INT}}$ goes low whenever a fault condition exists. Reset the fault condition using software or by pulling $\overline{\text{RESET}}$ low (see the *Interrupt* section for more information about interrupt management).
4	SCL	Serial Interface Clock Line Input
5	SDAOUT	Serial Output Data Line. Connect the data line optocoupler input to SDAOUT (see the *Typical Operating Circuits*). Connect SDAOUT to SDAIN if using a 2-wire, I^2C-compatible system.

High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

Pin Description (continued)

PIN	NAME	FUNCTION
6	SDAIN	Serial Interface Input Data Line. Connect the data line optocoupler output to SDAIN (see the *Typical Operating Circuits*). Connect SDAIN to SDAOUT if using a 2-wire, I^2C-compatible system.
7–10	A3–A0	Address Bits. A3–A0 form the lower part of the device's address. Address inputs default high with an internal 50kΩ pullup resistor to V_{DD}. The address values latch when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or after a reset. The 3 MSBs of the address are set to 010.
11–14	DET1–DET4	Detection/Classification Voltage Outputs. Use DET1 to set the detection and classification probe voltages on port 1. Use DET1 for the AC voltage sensing of port 1 when using the AC disconnect scheme (see the *Typical Operating Circuits*).
15	DGND	Digital Ground. Connect to digital ground.
16	V_{DD}	Positive Digital Supply. Connect to a digital power supply (reference to DGND).
17– 20	$\overline{SHD1}$–$\overline{SHD4}$	Port Shutdown Inputs. Pull $\overline{SHD\_}$ low to turn off the external FET on port_. Internally pulled up to V_{DD} with a 50kΩ resistor.
21	AGND	Analog Ground. Connect to the high-side analog supply.
22, 25, 29, 32	SENSE4, SENSE3, SENSE2, SENSE1	MOSFET Source Current-Sense Negative Inputs. Connect to the source of the power MOSFET and connect a current-sense resistor between SENSE_ and V_{EE} (see the *Typical Operating Circuits*).
23, 26, 30, 33	GATE4, GATE3, GATE2, GATE1	Port_ MOSFET Gate Drivers. Connect GATE_ to the gate of the external MOSFET (see the *Typical Operating Circuits*).
24, 27, 31, 34	OUT4, OUT3, OUT2, OUT1	MOSFET Drain-Output Voltage Senses. Connect OUT_ to the power MOSFET drain through a resistor (100Ω to 100kΩ). The low leakage at OUT_ limits the drop across the resistor to less than 100mV (see the *Typical Operating Circuits*).
28	V_{EE}	Low-Side Analog Supply Input. Connect the low-side analog supply to V_{EE} (-48V). Bypass with a 1µF capacitor between AGND and V_{EE}.
35	AUTO	Auto or Shutdown Mode Input. Force AUTO high to enter auto mode after a reset or power-up. Drive low to put the MAX5965A/MAX5965B into shutdown mode. In shutdown mode, software controls the operational modes of the MAX5965A/MAX5965B. A 50kΩ internal pulldown resistor defaults to AUTO low. AUTO latches when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or when the device resets. Software commands can take the MAX5965A/MAX5965B out of AUTO while AUTO is high.
36	OSC	Oscillator Input. AC-disconnect detection function uses OSC. Connect a 100Hz ±10%, $2V_{P-P}$ ±5%, +1.3V offset sine wave to OSC. If the oscillator positive peak falls below the OSC_FAIL threshold of 2V, the ports that have the AC function enabled shut down and are not allowed to power-up. When not using the AC-disconnect detection function, leave OSC unconnected.

Functional Diagram



High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

Detailed Description

The MAX5965A/MAX5965B are quad -48V power controllers designed for use in IEEE 802.3af-compliant/IEEE 802.3at-compatible PSE. The devices provide PD discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5965A/MAX5965B are pin compatible with the MAX5952/MAX5945/LTC4258/LTC4259A PSE controllers and provides additional features.

The MAX5965A/MAX5965B feature a high-power mode, which provides up to 45W per port. The devices allow the user to program the current-limit and overcurrent thresholds up to 2.5 times the default thresholds. The MAX5965A/MAX5965B can also be programmed to decrease the current-limit and overcurrent threshold by 15% for high operating voltage conditions to keep the output power constant.

The MAX5965A/MAX5965B provide new Class 5 and 2-event classification (Class 6) for detection and classification of high-power PDs. The MAX5965A/MAX5965B provide instantaneous readout of each port current through the I^2C interface. The MAX5965A/MAX5965B also provide high-capacitance detection for legacy PDs.

The MAX5965A/MAX5965B are fully software configurable and programmable through an I^2C-compatible, 3-wire serial interface with 49 registers. The class-overcurrent detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5965A/MAX5965B's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5965A/MAX5965B provide four operating modes to suit different system requirements. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode automatically detects and classifies a device connected to a port after initial software activation but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5965A/MAX5965B provide input undervoltage lockout, input undervoltage detection, a load-stability safety check during detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good, and fault status. The MAX5965A/MAX5965B's programmability includes start-up timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5965A/MAX5965B communicate with the system microcontroller through an I^2C-compatible interface. The MAX5965A/MAX5965B feature separate input and output data lines (SDAIN and SDAOUT) for use with optocoupler isolation. As slave devices, the MAX5965A/MAX5965B include four address inputs allowing 16 unique addresses. A separate $\overline{INT}$ output and four independent shutdown inputs ($\overline{SHD\_}$) provide fast response from a fault to port shutdown between the MAX5965A/MAX5965B and the microcontroller. A $\overline{RESET}$ input allows hardware reset of the device.

Reset

Reset is a condition the MAX5965A/MAX5965B enter after any of the following conditions:

1) After power-up (V_{EE} and V_{DD} rise above their UVLO thresholds).
2) Hardware reset. The $\overline{RESET}$ input is driven low and back high again any time after power-up.
3) Software reset. Writing a 1 into R1Ah[4] any time after power-up.
4) Thermal shutdown.

During a reset, the MAX5965A/MAX5965B reset their register map to the reset state as shown in Table 37 and latch in the state of AUTO (pin 35) and MIDSPAN (pin 2). During normal operation, change at the AUTO and MIDSPAN input is ignored. While the condition that caused the reset persists (i.e. high temperature, $\overline{RESET}$ input low, or UVLO conditions) the MAX5965A/MAX5965B do not acknowledge any addressing from the serial interface.

Port Reset (R1Ah[3:0])

Set high anytime during normal operation to turn off power and clear the events and status registers of the corresponding port. Port reset only resets the events and status registers.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the port waits between 2s and 2.4s before attempting to detect again. Midspan mode is activated by setting R11h[1] high. The status of the MIDSPAN pin is written to R11h[1] during power-up or after a reset. MIDSPAN is internally pulled low by a 50kΩ resistor.

Operation Modes

The MAX5965A/MAX5965B contain four independent, but identical state machines to provide reliable and real-time control of the four network ports. Each state machine has four operating modes: auto mode, semi-auto mode, manual, and shutdown. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode, upon request, continuously detects and classifies a device connected to a port but does not power up that port until instructed by software. Manual mode allows total software control of the device and is useful in system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

Switching between auto, semi, or manual mode does not interfere with the operation of the port. When the port is set into shutdown mode, all the port operations are immediately stopped and the port remains idle until shutdown is exited.

Automatic (Auto) Mode

Enter automatic (auto) mode by forcing the AUTO input high prior to a reset, or by setting R12h[P_M1,P_M0] to [1,1] during normal operation (see Tables 16a and 16b). In auto mode, the MAX5965A/MAX5965B performs detection, classification, and power up the port automatically once a valid PD is detected at the port. If a valid PD is not connected at the port, the MAX5965A/MAX5965B repeat the detection routine continuously until a valid PD is connected.

Going into auto mode, the DET_EN_ and CLASS_EN_ bits are set to high and stay high unless changed by software. Using software to set DET_EN_ and/or CLASS_EN_ low causes the MAX5965A/MAX5965B to skip detection and/or classification. As a protection, disabling the detection routine in auto mode does not allow the corresponding port to power up, unless the DET_BY (R23h[4]) is set to 1.

The AUTO status is latched into the register only during a reset. Any changes to the AUTO input after reset are ignored.

Semi-Automatic (Semi-Auto) Mode

Enter semi-auto mode by setting R12h[P_M1,P_M0] to [1,0] during normal operation (see Tables 16a and 16b). In semi-auto mode, the MAX5965A/MAX5965B, upon request, perform detection and/or classification repeatedly but do not power up the port(s), regardless of the status of the port connection.

Setting R19h[PWR_ON_] (Table 22) high immediately terminates detection/classification routines and turns on power to the port(s).

R14h[DET_EN_, CLASS_EN_] default to low in semi-auto mode. Use software to set R14h[DET_EN_, CLASS_EN_] to high to start the detection and/or classification routines. R14h[DET_EN_, CLASS_EN_] are reset every time the software commands a power off of the port (either through reset or PWR_OFF_). In any other case, the status of the bits is left unchanged (including when the state machine turns off the power because a load disconnect or a fault condition is encountered).

Manual Mode

Enter manual mode by setting R12h[P_M1,P_M0] to [0,1] during normal operation (see Tables 16a and 16b). Manual mode allows the software to dictate any sequence of operation. Write a 1 to both R14h[DET_EN_] and R14h[CLASS_EN_] to start detection and classification operations, respectively, and in that priority order. After execution, the command is cleared from the register(s). PWR_ON_ has highest priority. Setting PWR_ON_ high at any time causes the device to immediately enter the powered mode. Setting DET_EN_ and CLASS_EN_ high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ or CLASS_EN_ commands.

When switching to manual mode from another mode, DET_EN_, CLASS_EN_ default to low. These bits become pushbutton rather than configuration bits (i.e., writing ones to these bits while in manual mode commands the device to execute one cycle of detection and/or classification. The bits are reset back to zero at the end of the execution).

Shutdown Mode

Enter shutdown mode by forcing the AUTO input low prior to a reset, or by setting R12h[P_M1,P_M0] to [0,0] during normal operation (see Tables 16a and 16b). Putting the MAX5965A/MAX5965B into shutdown mode immediately turns off power and halts all operations to the corresponding port. The event and status bits of the affected port(s) are also cleared. In shutdown mode, the DET_EN_, CLASS_EN_, and PWR_ON_ commands are ignored.

In shutdown mode, the serial interface operates normally.

PD Detection

When PD detection is activated, the MAX5965A/MAX5965B probe the output for a valid PD. After each detection cycle, the device sets the DET_END_ bit R04h/05h[3:0] high and reports the detection results in the status registers R0Ch[2:0], R0Dh[2:0], R0Eh[2:0], and R0Fh[2:0]. The DET_END_ bit is reset to low when read through R05h or after a port reset.

High-Power, Quad, Monolithic, PSE Controllers for Power over Ethernet

A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af/at standard. Table 1 shows the IEEE 802.3af/at specification for a PSE detecting a valid PD signature. See the *Typical Operating Circuits* and Figure 1a (Detection, Classification, and Power-Up Port Sequence). The MAX5965A/MAX5965B can probe and categorize different types of devices connected to the port such as: a valid PD, an open circuit, a low resistive load, a high resistive load, a high capacitive load, a positive DC supply, or a negative DC supply.

During detection, the MAX5965A/MAX5965B keep the external MOSFET off and force two probe voltages through the DET_ input. The current through the DET_ input is measured as well as the voltage at OUT_. A two-point slope measurement is used as specified by the IEEE 802.3af standard to verify the device connected to the port. The MAX5965A/MAX5965B implement appropriate settling times and a 100ms digital integration to reject 50Hz/60Hz power-line noise coupling.

An external diode, in series with the DET_ input, restricts PD detection to the first quadrant as specified by the IEEE 802.3af/at standard. To prevent damage to non-PD devices, and to protect themselves from an output short circuit, the MAX5965A/MAX5965B limit the current into DET_ to less than 2mA maximum during PD detection.

In midspan mode, the MAX5965A/MAX5965B wait 2.2s before attempting another detection cycle after every failed detection. The first detection, however, happens immediately after issuing the detection command.

High-Capacitance Detection

The CLC_EN bit in register R23h[5] enables the large capacitor detection feature for legacy PD devices. When CLC_EN = 1, the high-capacitance detection limit is extended up to 150µF. CLC_EN = 0 is the default condition for the normal capacitor size detection. See Table 1 and the *Register Map and Description* section.

Table 1. PSE PI Detection Modes Electrical Requirement (Table 33-2 of the IEEE 802.3af Standard)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}	—	30	V	In detection mode only
Short-Circuit Current	I_{SC}	—	5	mA	In detection mode only
Valid Test Voltage	V_{VALID}	2.8	10	V	
Voltage Difference Between Test Points	ΔV_{TEST}	1	—	V	
Time Between Any Two Test Points	t_{BP}	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	V_{SLEW}		0.1	V/µs	
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	
Open-Circuit Resistance	R_{OPEN}	500	—	kΩ	
Accept Signature Capacitance	C_{GOOD}	—	150	nF	
Reject Signature Capacitance	C_{BAD}	10	—	µF	
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	
Signature Offset Current Tolerance	I_{OS}	0	12	µA	

Powered Device Classification (PD Classification)

During the PD classification mode, the MAX5965A/MAX5965B force a probe voltage (-18V) at DET_ and measure the current into DET_. The measured current determines the class of the PD.

After each classification cycle, the device sets the CL_END_ bit (R04h/05h[7:4]) high and reports the classification results in the status registers R0Ch[6:4], R0Dh[6:4], R0Eh[6:4], and R0Fh[6:4]. The CL_END_ bit is reset to low when read through register R05h or after a port reset. Both events registers, R04h, and R05h are cleared after the port powers down. Table 2 shows the IEEE 802.3af requirement for a PSE classifying a PD at the power interface (PI).

The MAX5965A/MAX5965B support high power beyond the IEEE 802.3af standard by providing additional classifications (Class 5 and 2-event classification).

Class 5 PD Classification

During classification, if the MAX5965A/MAX5965B detect currents in excess of I_{CLASS} > 48mA, then the PD will be classified as a Class 5 powered device. Status registers R0Ch[6:4] or R0Dh[6:4] or R0Eh[6:4] or R0Fh[6:4] will report the Class 5 classification result.

2-Event (Class 6) PD Classification

When 2-event classification is activated, the classification cycle is repeated three times with 8ms wait time between each cycle (see Figure 1b). Between each classification cycle, the MAX5965A/MAX5965B do not reset the port voltage completely but keeps the output voltage at -9V. The EN_CL6 bits in R1Ch[7:4] enable 2-event classification on a per port basis.

Powered State

When the MAX5965A/MAX5965B enter a powered state, the t_{START} and t_{DISC} timers are reset. Before turning on the port power, the MAX5965A/MAX5965B check if any other port is not turning on and if the t_{FAULT} timer is zero. Another check is performed if the ACD_EN_ bit is set, in this case the OSC_FAIL bit must be low (oscillator is okay) for the port to be powered.

If these conditions are met, the MAX5965A/MAX5965B enter startup where it turns on power to the port. An internal signal, POK_, asserts high when $V_{OUT\_}$ is within 2V from V_{EE}. PGOOD_ status bits are set high if POK_ stays high longer than t_{PGOOD}. PGOOD_ immediately resets when POK_ goes low (see Figure 2).

The PG_CHG_ bit sets when a port powers up or down. PWR_EN_ sets when a port powers up and resets when a port shuts down. The port shutdown timer lasts 0.5ms and prevents other ports from turning off during that period, except in the case of emergency shutdowns ($\overline{RESET}$ = L, RESET_IC = H, V_{EEUVLO}, V_{DDUVLO}, and T_{SHD}).

The MAX5965A/MAX5965B always check the status of all ports before turning off. A priority logic system determines the order to prevent the simultaneous turn-on or turn-off of the ports. The port with the lesser ordinal number gets priority over the others (i.e., port 1 turns on first, port 2 second, port 3 third, and port 4 fourth). Setting PWR_OFF_ high turns off power to the corresponding port.

Table 2. PSE Classification of a PD (Refer to Table 33-4 of the IEEE 802.3af)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 and 1
8 to 13	Class 1
> 13 and < 16	May be Class 1 or 2
16 to 21	Class 2
> 21 and < 25	May be Class 2 or 3
25 to 31	Class 3
> 31 and < 35	May be Class 3 or 4
35 to 45	Class 4
> 45 and < 51	May be Class 4 or 5
51 to 68	Class 5

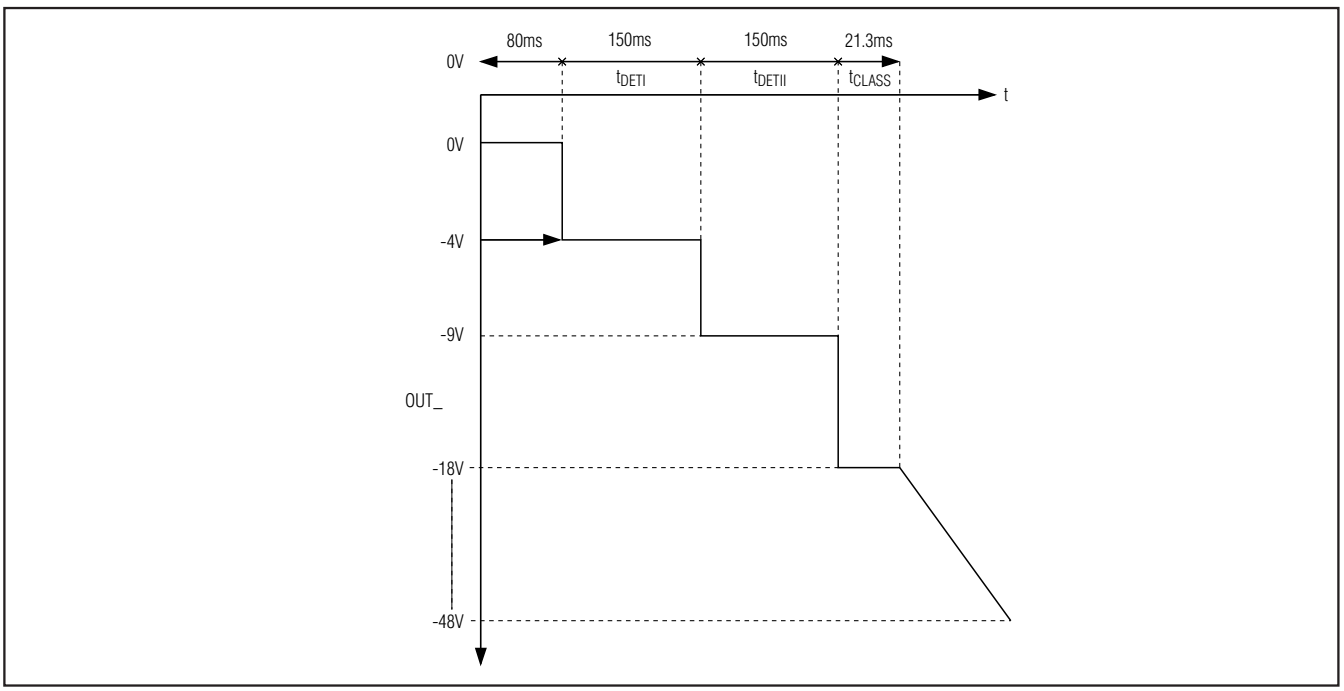


Figure 1a. Detection, Classification, and Power-Up Port Sequence

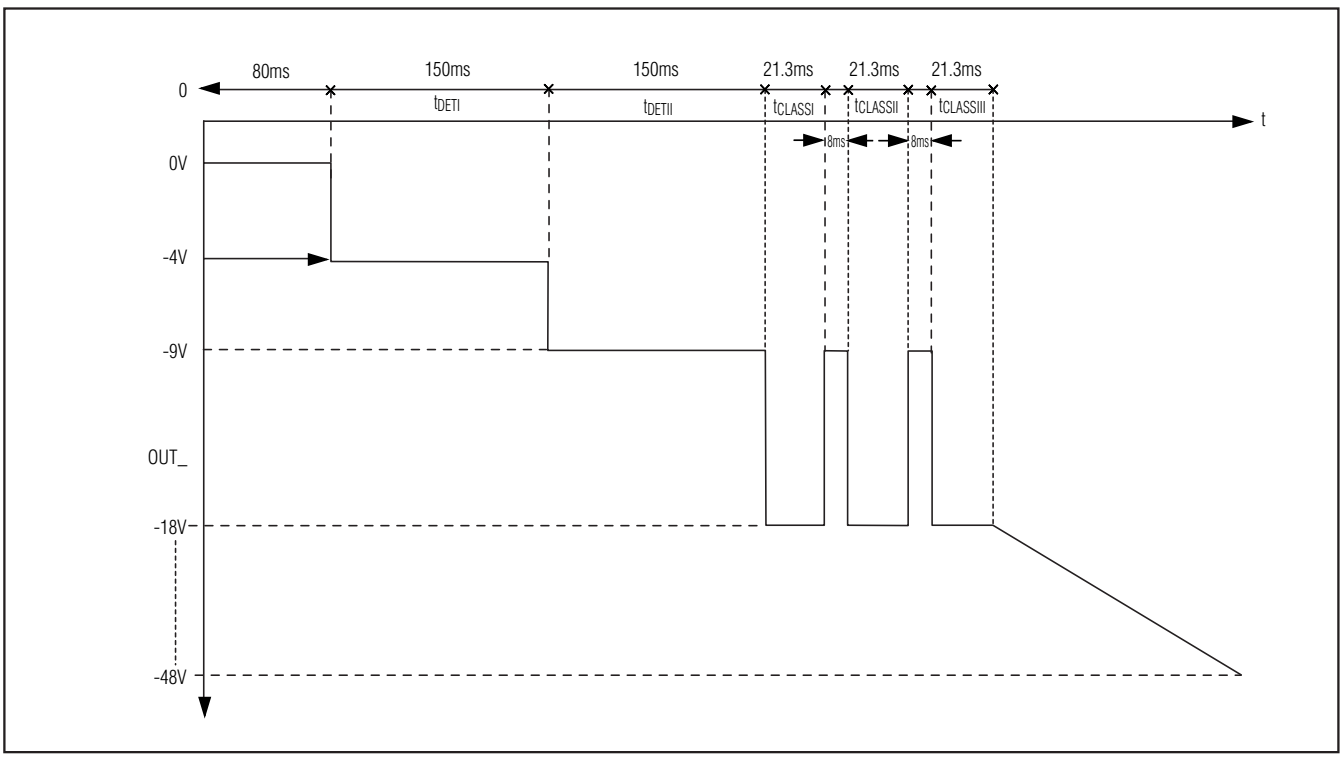


Figure 1b. Detection, 2-Event Classification, and Power-Up Port Sequence

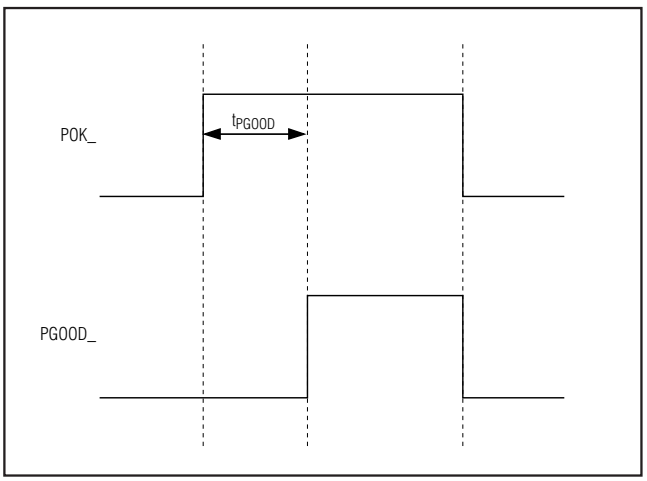


Figure 2. PGOOD_ Timing

Overcurrent Protection

A sense resistor R_S connected between SENSE_ and V_{EE} monitors the load current. Under normal operating conditions, the voltage across R_S (V_{RS}) never exceeds the threshold V_{SU_LIM}. If V_{RS} exceeds V_{SU_LIM}, an internal current-limiting circuit regulates the GATE_ voltage, limiting the current to $I_{LIM} = V_{SU\_LIM}/R_S$. During transient conditions, if V_{RS} exceeds V_{SU_LIM} by more than 1V, a fast pulldown circuit activates to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, t_{START}, times out, the port shuts off, and the STRT_FLT_ bit is set. In the normal powered state, the MAX5965A/MAX5965B check for overcurrent conditions as determined by V_{FLT_LIM} = ~88% of V_{SU_LIM}. The t_{FAULT} counter sets the maximum allowed continuous overcurrent period. The t_{FAULT} counter increases when V_{RS} exceeds V_{FLT_LIM} and decreases at a slower pace when V_{RS} drops below V_{FLT_LIM}. A slower decrement for the t_{FAULT} counter allows for detecting repeated short-duration overcurrents. When the counter reaches the t_{FAULT} limit, the MAX5965A/MAX5965B power off the port and assert the IMAX_FLT_ bit. For a continuous overstress, a fault latches exactly after a period of t_{FAULT}. V_{SU_LIM} is programmable through the ICUT registers R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], R2Bh[2:0], and the IVEE bits in register R29h[1:0]. See the *High-Power Mode* section for more information on the ICUT register.

After power-off due to an overcurrent fault, and if the RSTR_EN bit is set, the t_{FAULT} timer is not immediately reset but starts decrementing at the same slower pace. The MAX5965A/MAX5965B allow the port to be powered on only when the t_{FAULT} counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET avoiding overheating.

The MAX5965A/MAX5965B continuously flag when the current exceeds the maximum current allowed for the class as indicated in the CLASS status register. When class overcurrent occurs, the MAX5965A/MAX5965B set the IVC_ bit in register R09h.

ICUT Register and High-Power Mode

ICUT Register

The ICUT register determines the maximum current limits allowed for each port of the MAX5965A/MAX5965B. The 3 ICUT bits (R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], and R2Bh[2:0]) allow programming of the current-limit and overcurrent thresholds in excess of the IEEE standard limit (see Tables 34a, 34b, and 34c). The ICUT registers can be written to directly through the I^2C interface when CL_DISC (R17h[2]) is set to 0 (see Table 3). In this case, the current limit of the port is configured regardless of the status of the classification.

By setting the CL_DISC bit to 1, the MAX5965A/MAX5965B automatically set the ICUT register based upon the classification result of the port. See Table 3 and the *Register Map and Description* section.

High-Power Mode

When CL_DISC (R17h[2]) is set to 0, high-power mode is configured by setting the ICUT bits to any combination other than 000, 110, or 111 (note that 000 is the default value for the IEEE standard limit). See Table 3 and the *Register Map and Description* section.

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUT_ and reduces the current-limit value when ($V_{OUT\_}$ - V_{EE}) > 28V. The foldback function helps to reduce the power dissipation on the FET. The current limit eventually reduces down to 1/3 of I_{LIM} when ($V_{OUT\_}$ - V_{EE}) > 48V (see Figure 3a). For high-power mode, the foldback starts when ($V_{OUT\_}$ - V_{EE}) > 10V (see Figure 3b). In high-power mode, the current limit (I_{LIM}) is reduced down to minimum foldback current (V_{TH_FB}/R_S) when ($V_{OUT\_}$ - V_{EE}) > 48V.

Table 3. Automatic ICUT Programming

CL_DISC	PORT CLASSIFICATION RESULT	ENx_CL6	EN_HP_ALL	EN_HP_CL6	EN_HP_CL5	EN_HP_CL4	RESULTING ICUT REGISTER BITS
0	Any	X	X	X	X	X	User programmed
1	1	X	X	X	X	X	ICUT = 110
1	2	X	X	X	X	X	ICUT = 111
1	0, 3	X	X	X	X	X	ICUT = 000
1	4, 5	X	0	X	X	X	ICUT = 000
1	5	X	1	X	1	X	ICUT = R24h[6:4]
1	5	X	1	X	0	X	ICUT = 000
1	4	X	1	X	x	1	ICUT = R24h[6:4]
1	4	X	1	X	X	0	ICUT = 000
1	6 or Illegal	0	X	X	X	X	—
1	6 or Illegal	1	1	1	X	X	(See Table 35a)
1	6 or Illegal	1	1	0	X	X	ICUT = 000
1	6 or Illegal	1	0	X	X	X	ICUT = 000

MOSFET Gate Driver

Connect the gate of the external n-channel MOSFET to GATE_. An internal 50µA current source pulls GATE_ to (V_{EE} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE_ to V_{EE} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GD}}$$

where C_{GD} is the total capacitance between GATE and DRAIN of the external MOSFET. Current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the MAX5965A/MAX5965B manipulate the GATE_ voltage to control the voltage at SENSE_ (V_{RS}). A fast pulldown activates if V_{RS} overshoots the limit threshold (V_{SU_LIM}). The fast pulldown current increases with the amount of overshoot. The maximum fast pulldown current is 100mA.

During turn-off, when the GATE_ voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

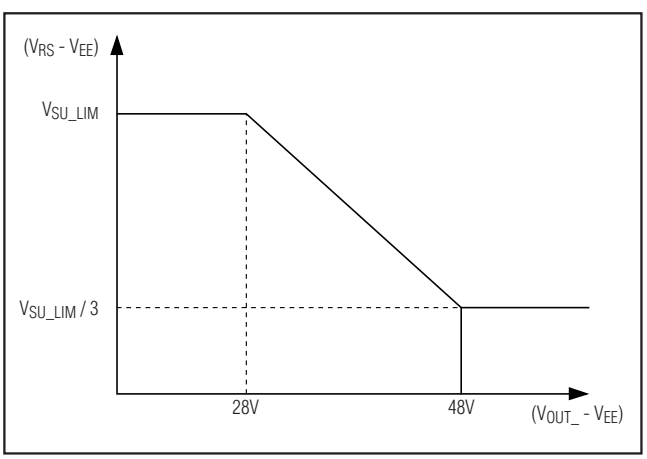


Figure 3a. Foldback Current Characteristics

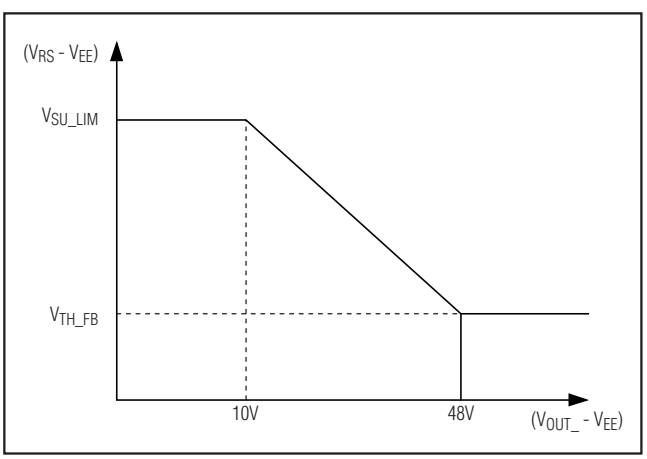


Figure 3b. Foldback Current Characteristics for High-Power Mode

Digital Logic

V_{DD} supplies power for the internal logic circuitry. V_{DD} ranges from +3.0V to +5.5V and determines the logic thresholds for the CMOS connections (SDAIN, SDAOUT, SCL, AUTO, $\overline{SHD\_}$, A_). This voltage range enables the MAX5965A/MAX5965B to interface with a nonisolated low-voltage microcontroller. The MAX5965A/MAX5965B check the digital supply for compatibility with the internal logic. The MAX5965A/MAX5965B also feature a V_{DD} undervoltage lockout (V_{DDUVLO}) of +2.0V. A V_{DDUVLO} condition keeps the MAX5965A/MAX5965B in reset and the ports shut off. Bit 0 in the supply event register shows the status of V_{DDUVLO} (Table 12) after V_{DD} has recovered. All logic inputs and outputs reference to DGND. For AC-disconnected detection, DGND and AGND must be connected together externally. Connect DGND to AGND at a single point in the system as close as possible to the MAX5965A/MAX5965B.

Hardware Shutdown

$\overline{SHD\_}$ shuts down the respective ports without using the serial interface. Hardware shutdown offers an emergency turn-off feature that allows a fast disconnect of the power supply from the port. Pull $\overline{SHD\_}$ low to remove power. $\overline{SHD\_}$ also resets the corresponding events and status register bits.

Interrupt

The MAX5965A/MAX5965B contain an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. R00h and R01h (Tables 6 and 7) contain the definitions of the interrupt registers. The mask register R01h determines events that trigger an interrupt. As a response to an interrupt, the controller reads the status of the event register to determine the cause of the interrupt and takes subsequent actions. Each interrupt event register also contains a Clear on Read (CoR) register. Reading through the CoR register address clears the interrupt. $\overline{INT}$ remains low when reading the interrupt through the read-only addresses. For example, to clear a startup fault on the port 4 read address 09h (see Table 11). Use the global pushbutton bit in register 1Ah (bit 7, Table 23) to clear interrupts, or use a software or hardware reset.

Undervoltage and Overvoltage Protection

The MAX5965A/MAX5965B contain several undervoltage and overvoltage protection features. Table 12 in the *Register Map and Description* section shows a detailed list of the undervoltage and overvoltage protection features. An internal V_{EE} undervoltage lockout (V_{EEUVLO}) circuit keeps the MOSFET off and the MAX5965A/MAX5965B in reset until V_{AGND} - V_{EE} exceeds 29V for more than 3ms. An internal V_{EE} overvoltage (V_{EE_OV}) circuit shuts down the ports when (V_{AGND} - V_{EE}) exceeds 60V. The digital supply also contains an undervoltage lockout (V_{DDUVLO}). The MAX5965A/MAX5965B also feature three other undervoltage and overvoltage interrupts: V_{EE} undervoltage interrupt (V_{EE_UV}), V_{DD} undervoltage interrupt (V_{DD_UV}), and V_{DD} overvoltage interrupt (V_{DD_OV}). A fault latches into the supply events register (Table 12), but the MAX5965A/MAX5965B does not shut down the ports with V_{EE_UV}, V_{DD_UV}, or V_{DD_OV}.

DC Disconnect Monitoring

Setting R13h[DCD_EN_] bits high enables DC load monitoring during a normal powered state. If V_{RS} (the voltage across R_S) falls below the DC load disconnect threshold, V_{DCTH}, for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port.

AC Disconnect Monitoring Features (MAX5965B)

The MAX5965B features AC load disconnect monitoring. Connect an external sine wave to OSC. The oscillator requirements are:

1) V_{P-P} x Frequency = 200V_{P-P} x Hz ±15%
2) Positive peak voltage > +2.2V
3) Frequency > 60Hz

A 100Hz ±10%, 2V_{P-P} ±5%, with +1.3V offset (V_{PEAK} = +2.3V typical) is recommended.

The MAX5965B buffers and amplifiers three times the external oscillator signal and sends the signal to DET_, where the sine wave is AC-coupled to the output. The MAX5965B senses the presence of the load by monitoring the amplitude of the AC current returned to DET_ (see the *Functional Diagram*).

Setting R13h[ACD_EN_] bits high enable AC load disconnect monitoring during a normal powered state. If the AC current peak at the DET_ input falls below I_{ACTH} for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port. I_{ACTH} is programmable using R23h[2:0].

An internal comparator checks for a proper amplitude of the oscillator input. If the positive peak of the input sinusoid falls below a safety value of 2V (typ), OSC_FAIL sets and the port shuts down. Power cannot be applied to the ports when ACD_EN_ is set high and OSC_FAIL is set high. Leave OSC unconnected or connect it to DGND when not using AC-disconnect detection.

Thermal Shutdown

If the MAX5965A/MAX5965B die temperature reaches +150°C, an overtemperature fault generates and the MAX5965A/MAX5965B shut down. The MOSFETs turn off. The die temperature of the MAX5965A/MAX5965B must cool down below +130°C to remove the overtemperature fault condition. After a thermal shutdown, the part is reset.

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Watchdog

The R1Eh and R1Fh registers control the watchdog operation. The watchdog function, when enabled, allows the MAX5965A/MAX5965B to gracefully take over control or securely shuts down the power to the ports in case of software/firmware crashes. Contact the factory for more details.

Address Inputs

A3, A2, A1, and A0 represent the 4 LSBs of the chip address. The complete chip address is 7 bits (see Table 4).

The 4 LSBs latch on the low-to-high transition of $\overline{RESET}$ or after a power-supply start (either on V_{DD} or V_{EE}). Address inputs default high through an internal 50kΩ pullup resistor to V_{DD}. The MAX5965A/MAX5965B also respond to the call through a global address 30h (see the *Global Addressing and Alert Response Protocol* section).

Table 4. MAX5965A/MAX5965B Address

0	1	0	A3	A2	A1	A0	R/$\overline{W}$

I²C-Compatible Serial Interface

The MAX5965A/MAX5965B operate as a slave that sends and receives data through an I²C-compatible, 2-wire or 3-wire interface. The interface uses a serial-data input line (SDAIN), a serial-data output line (SDAOUT), and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5965A/MAX5965B, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial-data line (SDA).

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The MAX5965A/MAX5965B SDAIN line operates as an input. The MAX5965A/MAX5965B SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDAOUT. The MAX5965A/MAX5965B SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

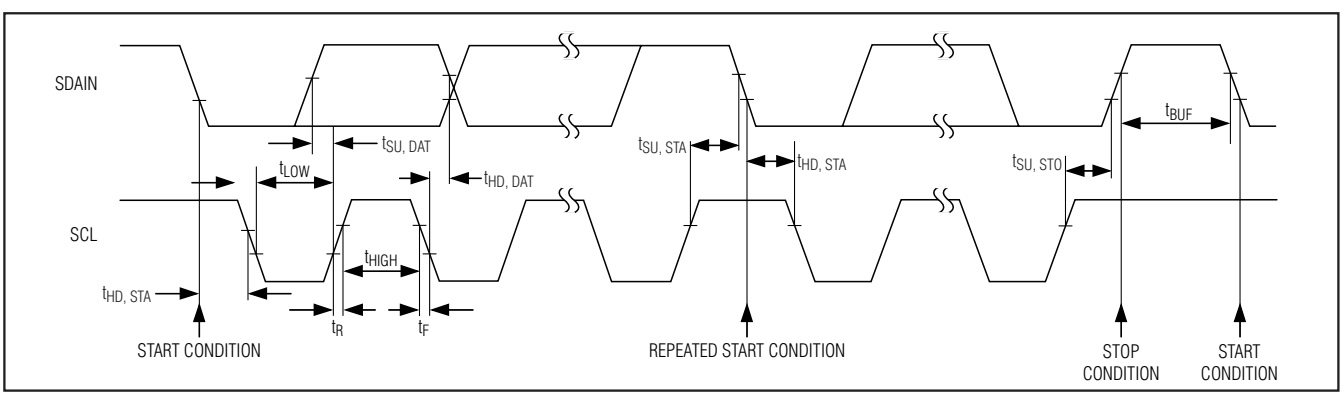

Figure 4. 2-Wire, Serial-Interface Timing Details

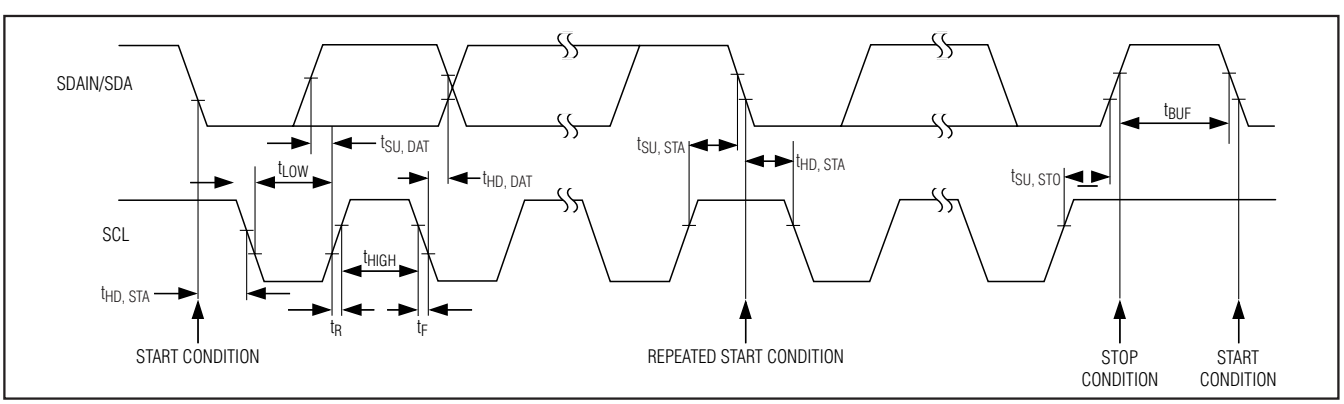

Figure 5. 3-Wire, Serial-Interface Timing Details

Serial Addressing

Each transmission consists of a START condition (Figure 6) sent by a master, followed by the MAX5965A/MAX5965B 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission.

Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus each byte effectively transferred requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA (or the SDAOUT in the 3-wire interface) during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5965A/MAX5965B, the MAX5965A/MAX5965B generate the acknowledge bit. When the MAX5965A/MAX5965B transmit to the master, the master generates the acknowledge bit.

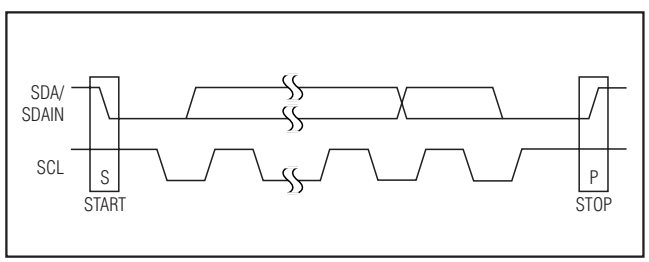

Figure 6. START and STOP Conditions

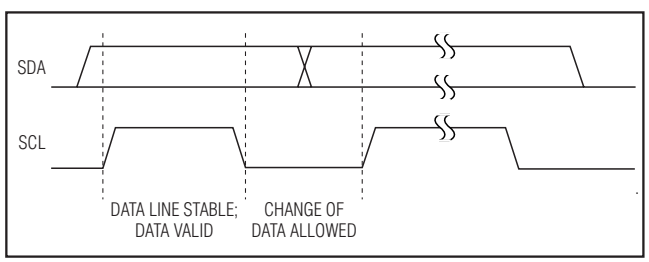

Figure 7. Bit Transfer

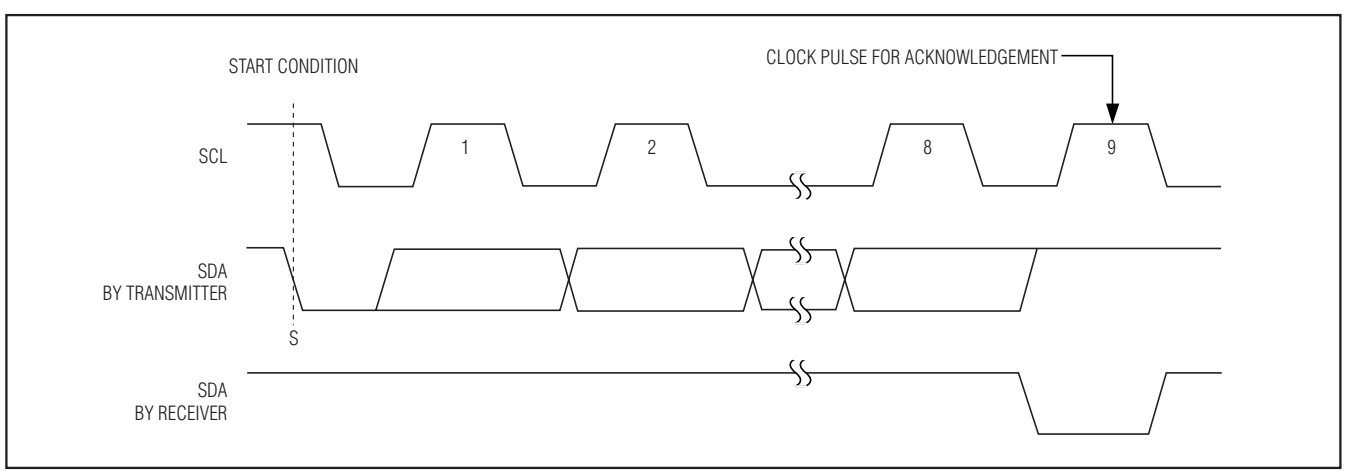

Figure 8. Acknowledge