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19-5128; Rev 0; 1/10

EVALUATION KIT AVAILABLE

0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

General Description

The MAX5970 dual hot-swap controller provides complete protection for systems with two supply voltages from 0V to +16V. The MAX5970 includes four programmable LED outputs. The two hot-swap channels can be configured to operate as independent hot-swap controllers, or as a pair operating together so that both channels shut down if either channel experiences a fault.

The MAX5970 provides two programmable levels of overcurrent circuit-breaker protection: a fast-trip threshold for a fast turn-off, and a lower slow-trip threshold for a delayed turn-off. The maximum overcurrent circuit-breaker threshold range is set independently for each channel with a trilevel logic input IRNG_, or by programming though the I²C interface.

The MAX5970 is an advanced hot-swap controller that monitors voltage and current with an internal 10-bit ADC which is continuously multiplexed to convert the output voltage and current of both hot-swap channels at 10ksps. Each 10-bit sample is stored in an internal circular buffer so that 50 past samples of each signal can be read back through the I²C interface at any time or after a fault condition.

The device includes five user-programmable digital comparators per hot-swap channel to implement overcurrent warning and two levels of overvoltage/undervoltage detection. When any of the measured values violates the programmable limits, an external $\overline{\text{ALERT}}$ output is asserted. In addition to the $\overline{\text{ALERT}}$ signal, the MAX5970 can be programmed to deassert the power-good signal and/or turn off the external MOSFET.

The MAX5970 features four I/Os that can be independently configured as general-purpose inputs/outputs (GPIOs) or as open-drain LED drivers with programmable blinking. These four I/Os can be configured for any mix of LED driver or GPIO function.

The MAX5970 is available in a 36-pin thin QFN-EP package and operates over the -40°C to +85°C extended temperature range.

Features

- **Two Independent Hot-Swap Controllers Operate from 0V to +16V**
- **10-Bit ADC Monitors Voltage and Current of Each Channel**
- **Circular Buffers Store 5ms of Current and Voltage Measurements**
- **Two Independent Internal Charge Pumps Generate n-Channel MOSFET Gate Drives**
- **Internal 500mA Gate Pulldown Current for Fast Shutdown**
- **VariableSpeed/BiLevel™ Circuit-Breaker Protection**
- **Independent Precision-Voltage Enable Inputs**
- **Alert Output Indicates Fault and Warning Conditions**
- **Independent Power-Good Outputs**
- **Independent Fault Outputs**
- **Four Open-Drain Outputs Sink 25mA to Directly Drive LEDs**
- **Programmable LED Flashing Function**
- **Autoretry or Latched Fault Management**
- **400kHz I²C Interface**
- **Small 6mm x 6mm, 36-Pin TQFN-EP Package**

Applications

Single PCI Express® Hot-Plug Slot

Blade Servers

Disk Drives/DASD/Storage Systems

Soft-Switch for ASICs, FPGAs, and Microcontrollers with Independent Core and I/O Voltages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5970ETX+	-40°C to +85°C	36 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

PCI Express is a registered trademark of PCI-SIG Corp.

0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

ABSOLUTE MAXIMUM RATINGS

IN, SENSE_, MON_, GATE_ to AGND ..... -0.3V to +30V
LED_ to AGND ..... -0.3V to +16V
ON_, SDA, SCL to AGND ..... -0.3V to +6V
REG, DREG, IRNG_, MODE, PROT, A_, PG_, ALERT, FAULT_ to AGND ..... -0.3V to +4V
REG to DREG ..... -0.3V to +0.3V
RETRY, HWEN, POL to AGND ..... -0.3V to (V_{REG} + 0.3V)
GATE1 to MON1, GATE2 to MON2 ..... -0.3V to +6V
GND_, DGND to AGND ..... -0.3V to +0.3V
SDA, ALERT Current ..... -20mA to +50mA
LED_ Current ..... -20mA to +100mA
GATE_, MON_, GND_ Current 750mA
All Other Pins Input/Output Current 20mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin, 6mm x 6mm TQFN
(derate 35.7mW/°C above +70°C) 2857mW**
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1) .. 28°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal consideration, refer to **www.maxim-ic.com/thermal-tutorial**.

**As per JEDEC51 Standard (Multilayer Board)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Input-Voltage Range	V_{IN}			2.7		16	V
Hot-Swap Voltage Range				0		16	V
Supply Current	I_{IN}				2.5	4	mA
Internal LDO Output Voltage	REG	I_{REG} = 0 to 5mA, V_{IN} = 2.7V to 16V		2.49	2.53	2.6	V
Undervoltage Lockout	UVLO	V_{IN} rising				2.7	V
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$				100		mV
CURRENT-MONITORING FUNCTION							
MON_, SENSE_ Input-Voltage Range				0		16	V
SENSE_ Input Current		$V_{SENSE\_}$, $V_{MON\_}$ = 16V			32	75	µA
MON_ Input Current		$V_{SENSE\_}$, $V_{MON\_}$ = 16V			180	280	µA
Current Measurement LSB Voltage		25mV range			24.34		µV
		50mV range			48.39		
		100mV range			96.77		
Current Measurement Error (25mV Range)		$V_{MON\_}$ = 0V	$V_{SENSE\_}$ - $V_{MON\_}$ = 5mV	-6.57		+6.22	% FS
			$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-6.71		+6.82	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 5mV	-9.71		+8.92	
			$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-10.24		+9.36	
Current Measurement Error (50mV Range)		$V_{MON\_}$ = 0V	$V_{SENSE\_}$ - $V_{MON\_}$ = 10mV	-4.24		+3.78	% FS
			$V_{SENSE\_}$ - $V_{MON\_}$ = 40mV	-4.53		+5.36	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 10mV	-4.50		+4.00	
			$V_{SENSE\_}$ - $V_{MON\_}$ = 40mV	-4.20		+4.50	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Measurement Error (100mV Range)		$V_{MON\_}$ = 0V	$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-2.70		+2.43	% FS
			$V_{SENSE\_}$ - $V_{MON\_}$ = 80mV	-3.63		+4.56	
		$V_{MON\_}$ = 2.5V to 16V	$V_{SENSE\_}$ - $V_{MON\_}$ = 20mV	-3.14		+3.19	
			$V_{SENSE\_}$ - $V_{MON\_}$ = 80mV	-3.80		+3.93	
Fast Current-Limit Threshold Error (25mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-2.106		+0.888	mV
			Circuit breaker, DAC = 255	-2.986		+0.641	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-3.000		+1.000	
			Circuit breaker, DAC = 255	-3.500		+1.500	
Fast Current-Limit Threshold Error (50mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-3.1188		+0.926	mV
			Circuit breaker, DAC = 255	-4.873		+0.3421	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-3.2668		+0.9228	
			Circuit breaker, DAC = 255	-4.7		+1.0212	
Fast Current-Limit Threshold Error (100mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-4.7987		+1.1812	mV
			Circuit breaker, DAC = 255	-8.9236		+0.202	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-4.9991		+0.6374	
			Circuit breaker, DAC = 255	-8.262		+1	
Slow Current-Limit Threshold Error (25mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-1.7965		+1.5496	mV
			Circuit breaker, DAC = 255	-1.86		+1.5916	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-2.149		+1.9868	
			Circuit breaker, DAC = 255	-2.2285		+1.9982	
Slow Current-Limit Threshold Error (50mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-2.3992		+1.8723	mV
			Circuit breaker, DAC = 255	-2.5146		+2.1711	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-2.4716		+2.181	
			Circuit breaker, DAC = 255	-2.7421		+2.1152	
Slow Current-Limit Threshold Error (100mV Range)		$V_{MON\_}$ = 0V	Circuit breaker, DAC = 102	-3.3412		+2.989	mV
			Circuit breaker, DAC = 255	-3.8762		+3.6789	
		$V_{MON\_}$ = 2.5V to 16V	Circuit breaker, DAC = 102	-3.2084		+2.7798	
			Circuit breaker, DAC = 255	-3.8424		+2.6483	
Fast Circuit-Breaker Response Time	t_{FCB}	Overdrive = 10% of current-sense range			2		µs
Slow Current-Limit Response Time	t_{SCB}	Overdrive = 4% of current-sense range			2.4		ms
		Overdrive = 8% of current-sense range			1.2		
		Overdrive = 16% of current-sense range			0.6		
THREE-STATE INPUTS							
A_, IRNG_, MODE, PROT Low Current	I_{IN_LOW}	Input voltage = 0.4V		-40			µA
A_, IRNG_, MODE, PROT T High Current	I_{IN_HIGH}	Input voltage = V_{REG} - 0.2V				40	µA
A_, IRNG_, MODE, PROT Open Current	I_{FLOAT}	Maximum source/sink current for open state		-4		+4	µA

0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
A_, IRNG_, MODE, PROT Low Voltage		Relative to AGND			0.4	V
A_, IRNG_, MODE, PROT High Voltage		Relative to REG	-0.24			V
TWO-STATE INPUTS						
ON_ Input Voltage	$V_{ON\_}$		0.582	0.592	0.602	V
ON_ Input Hysteresis	V_{ON_HYS}			4		%
ON_ Input Current			-100		+100	nA
TIMING						
MON_ to PG_ Delay		Register configurable (see Tables 31a and 31b)		50		ms
				100		
				200		
				400		
CHARGE PUMP (GATE_)						
Charge-Pump Output Voltage		Relative to MON_, I_{GATE} = 0	4.5	5.1	5.5	V
Charge-Pump Output Source Current	$I_{G(UP)}$		4	5	6	µA
GATE_ Discharge Current	$I_{G(DN)}$	$V_{GATE\_}$ - $V_{MON\_}$ = 2V		500		mA
OUTPUT ($\overline{FAULT}$_, PG_, $\overline{ALERT}$)						
Output-Voltage Low		I_{SINK} = 3.2mA			0.2	V
Output Leakage Current					1	µA
LED INPUT/OUTPUT						
LED_ Input Threshold Low Level	V_{IL}				0.4	V
LED_ Input Threshold High Level	V_{IH}		1.4			V
LED_ Output Low	V_{OL}	$I_{LED\_}$ = 25mA			0.7	V
LED_ Input Leakage Current (Open Drain)	I_{GPIO_IX}	$V_{LED\_}$ = 16V	-1		+1	µA
LED_ Weak Pullup Current	I_{PU_WEAK}	$V_{LED\_}$ = V_{IN} - 0.65V	2			µA
ADC PERFORMANCE						
Resolution				10		Bits
Maximum Integral Nonlinearity	INL			1		LSB
ADC Total Monitoring Cycle Time		Two voltage and two current-sense conversion	95	100	110	µs
MON_ LSB Voltage		16V range	15.23	15.49	15.69	mV
		8V range	7.655	7.743	7.811	
		4V range	3.811	3.875	3.933	
		2V range	1.899	1.934	1.966	
MON_ Code 000H to 001H Transition Voltage		16V range	10	25	41	mV
		8V range	4.7	12	21	
		4V range	2	6	12	
		2V range	0.5	3	5.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V to 16V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = +25°C.) (Note 2)

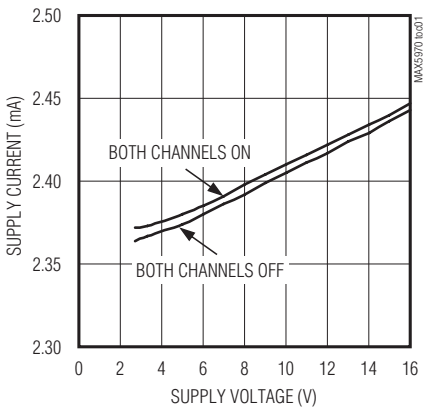
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C iNTERFACE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock High Period	t_{HIGH}		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	Transmit	100			ns
		Receive	300		900	
Output Fall Time	t_{OF}	C_{BUS} = 10pF to 400pF			250	ns
Pulse Width of Spike Suppressed	t_{SP}			50		ns
SDA, SCL Input High Voltage	V_{IH}		1.8			V
SDA, SCL Input Low Voltage	V_{IL}				0.8	V
SDA, SCL Input Hysteresis	V_{HYST}			0.22		V
SDA, SCL Input Current			-1		+1	µA
SDA, SCL Input Capacitance				15		pF
SDA Output Voltage	V_{OL}	I_{SINK} = 4mA			0.4	V

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the temperature range are guaranteed by design.

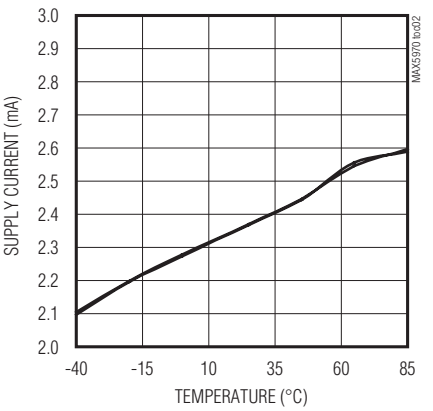
Typical Operating Characteristics

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

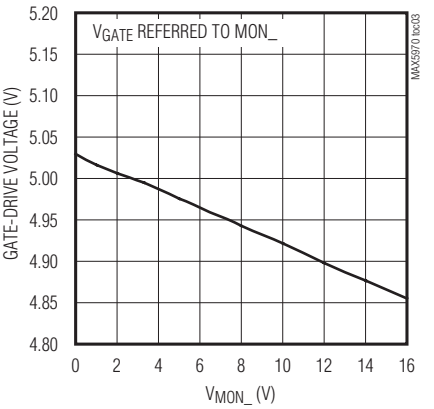
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



GATE-DRIVE VOLTAGE vs. $V_{MON\_}$

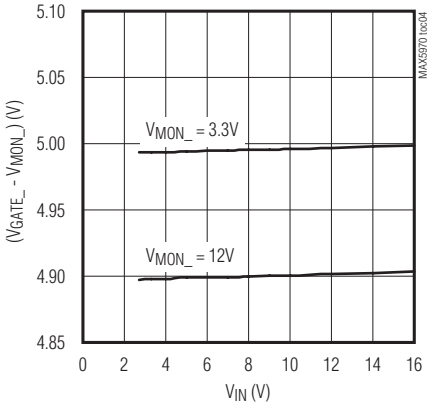


0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

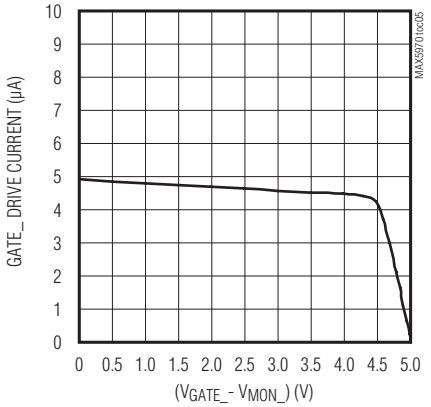
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

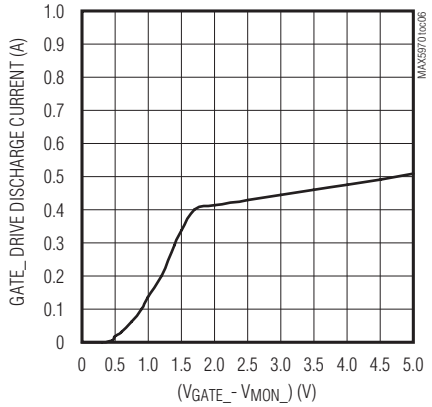
GATE_ DRIVE VOLTAGE vs. V_{IN}



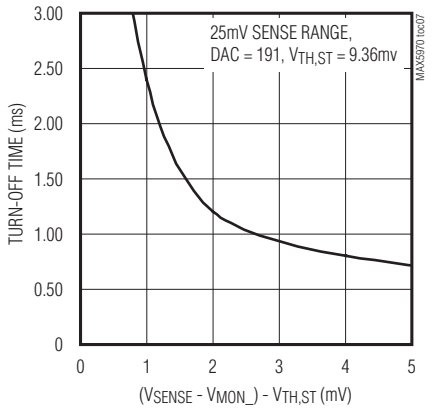
GATE_ DRIVE CURRENT vs. ($V_{GATE\_}$ - $V_{MON\_}$)



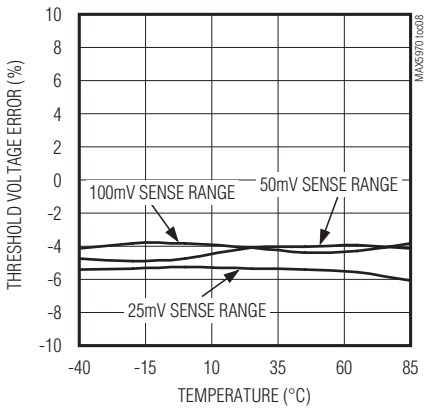
GATE_ DRIVE DISCHARGE CURRENT vs. ($V_{GATE\_}$ - $V_{MON\_}$)



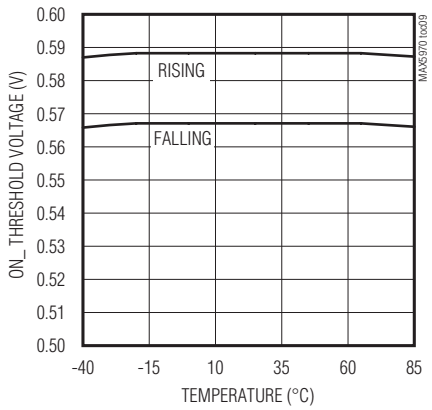
SLOW COMPARATOR TURN-OFF TIME vs. VOLTAGE OVERDRIVE



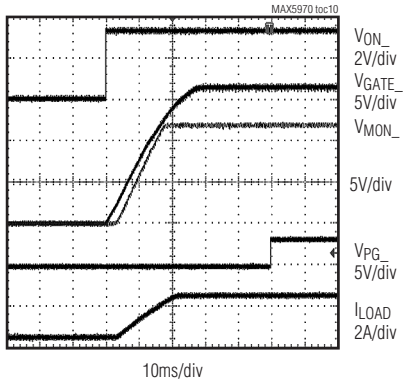
SLOW COMPARATOR THRESHOLD VOLTAGE ERROR vs. TEMPERATURE



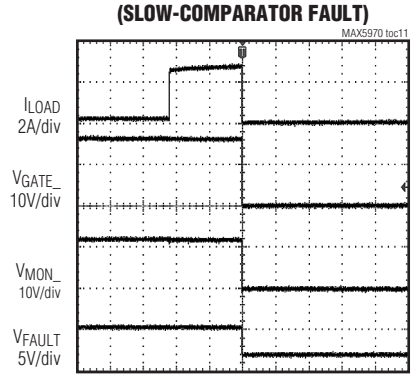
ON_ THRESHOLD VOLTAGE vs. TEMPERATURE



STARTUP WAVEFORM



TURN-OFF WAVEFORM (SLOW-COMPARATOR FAULT)

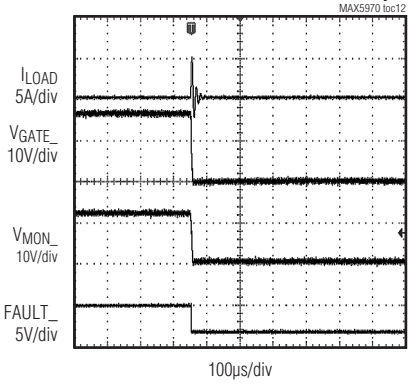


0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

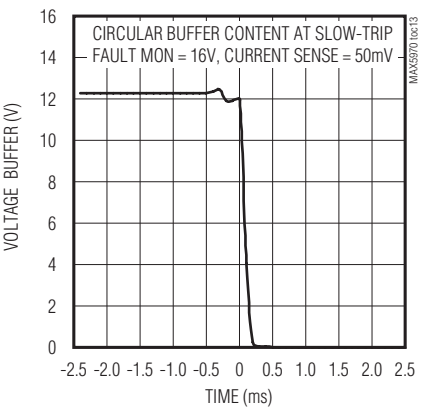
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

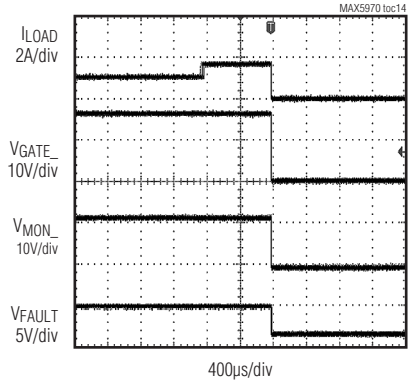
TURN-OFF WAVEFORM (FAST COMPARATOR FAULT/SHORT-CIRCUIT RESPONSE)



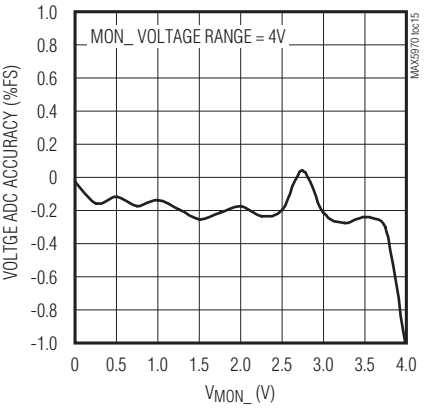
VOLTAGE BUFFER vs. TIME



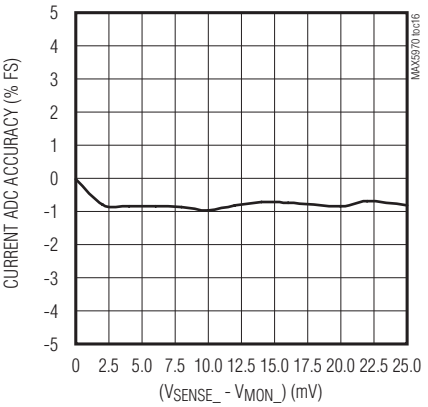
SLOW-COMPARATOR FAULT EVENT



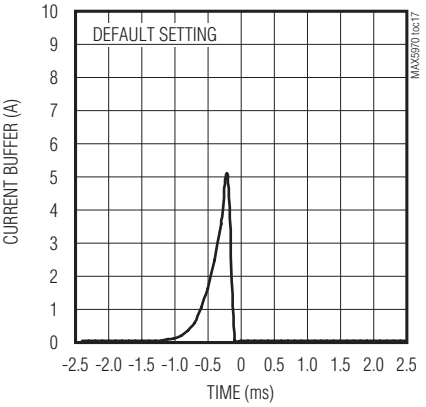
VOLTAGE ADC ACCURACY vs. MON_ VOLTAGE



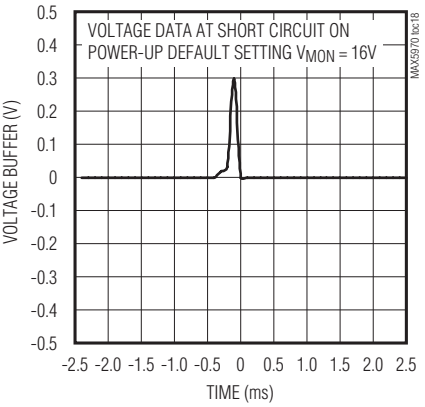
CURRENT ADC ACCURACY vs. ($V_{SENSE\_}$ - $V_{MON\_}$)



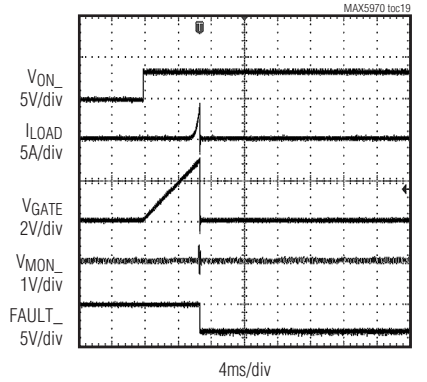
CURRENT BUFFER vs. TIME



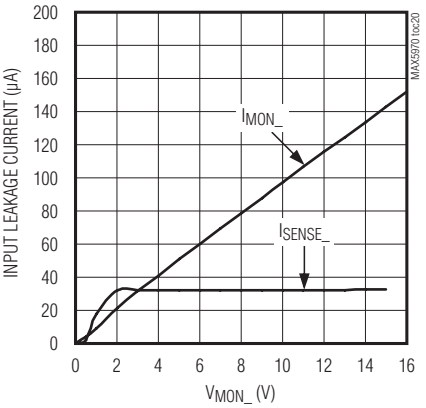
VOLTAGE BUFFER vs. TIME



STARTUP INTO SHORT LOAD

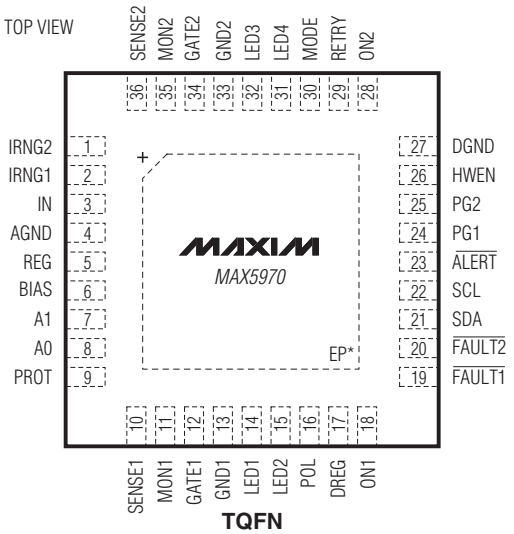


INPUT LEAKAGE CURRENT vs. MON_ VOLTAGE



0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor and 4 LED Drivers

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	IRNG2	Channel 2 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected.
2	IRNG1	Channel 1 Three-State Current-Sense Range Selection Input. Set the circuit-breaker threshold range by connecting to DGND, DREG, or leave unconnected.
3	IN	Power-Supply Input. Connect to a voltage from 2.7V to 16V. Bypass to AGND with a 1µF capacitor.
4	AGND	Analog Ground. Connect all GND_ and DGND to AGND externally using a star connection.
5	REG	Internal Regulator Output. Bypass to ground with a 1µF capacitor. Connect only to DREG. Do not use to power external circuitry.
6	BIAS	For normal operation, connect BIAS to REG.
7	A1	Three-State I^2C Address Input 1
8	A0	Three-State I^2C Address Input 0
9	PROT	Protection Behavior Input. Three-state input sets one of three different response options for undervoltage and overvoltage events.
10	SENSE1	Channel 1 Current-Sense Input. Connect SENSE1 to the source of an external MOSFET and to one end of R_{SENSE1}.
11	MON1	Channel 1 Voltage Monitoring Input
12	GATE1	Channel 1 Gate-Drive Output. Connect to the gate of an external n-channel MOSFET.
13	GND1	Channel 1 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.

Pin Description (continued)

PIN	NAME	FUNCTION
14	LED1	LED Driver 1
15	LED2	LED Driver 2
16	POL	Polarity Select Input. Connect to DREG for active-high power-good outputs (PG_). Connect to GND for active-low power-good outputs.
17	DREG	Logic Power-Supply Input. Connect to REG externally through a 10Ω resistor and to DGND with a 1µF ceramic capacitor.
18	ON1	Channel 1 Precision Turn-On Input
19	$\overline{FAULT1}$	Channel 1 Active-Low Open-Drain Fault Output. $\overline{FAULT1}$ goes low if an overcurrent occurs on channel 1.
20	$\overline{FAULT2}$	Channel 2 Active-Low Open-Drain Fault Output. $\overline{FAULT2}$ goes low if an overcurrent occurs on channel 2.
21	SDA	I^2C Serial-Data Input/Output
22	SCL	I^2C Serial-Clock Input
23	$\overline{ALERT}$	Open-Drain Alert Output. $\overline{ALERT}$ goes low during a fault to notify the system of an impending failure.
24	PG1	Channel 1 Open-Drain Power-Good Output
25	PG2	Channel 2 Open-Drain Power-Good Output
26	HWEN	Hardware Enable Input. Connect to DREG or DGND. State is read upon power-up as V_{IN} crosses the UVLO threshold and sets enable register bits with this value. After UVLO, this input becomes inactive until power is cycled.
27	DGND	Digital Ground. Connect all GND_ and DGND to AGND externally using a star connection.
28	ON2	Channel 2 Precision Turn-On Input
29	RETRY	Autoretry Fault Management Input. Connect to DREG to enable autoretry operation. Connect to DGND to enable latched-off operation.
30	MODE	Hot-Swap Two-State Mode Select Input. Connect MODE to DGND, DREG or leave it unconnected to operate the hot-swap channels independently or as a pair.
31	LED4	LED Driver 4
32	LED3	LED Driver 3
33	GND2	Channel 2 Gate Discharge Current Ground Return. Connect all GND_ and DGND to AGND externally using a star connection.
34	GATE2	Channel 2 Gate-Drive Output. Connect to gate of an external n-channel MOSFET.
35	MON2	Channel 2 Voltage Monitoring Input
36	SENSE2	Channel 2 Current-Sense Input. Connect SENSE2 to the source of an external MOSFET and to one end of R_{SENSE2}.
—	EP	Exposed Pad. EP is internally grounded. Connect externally to ground plane using a star connection.

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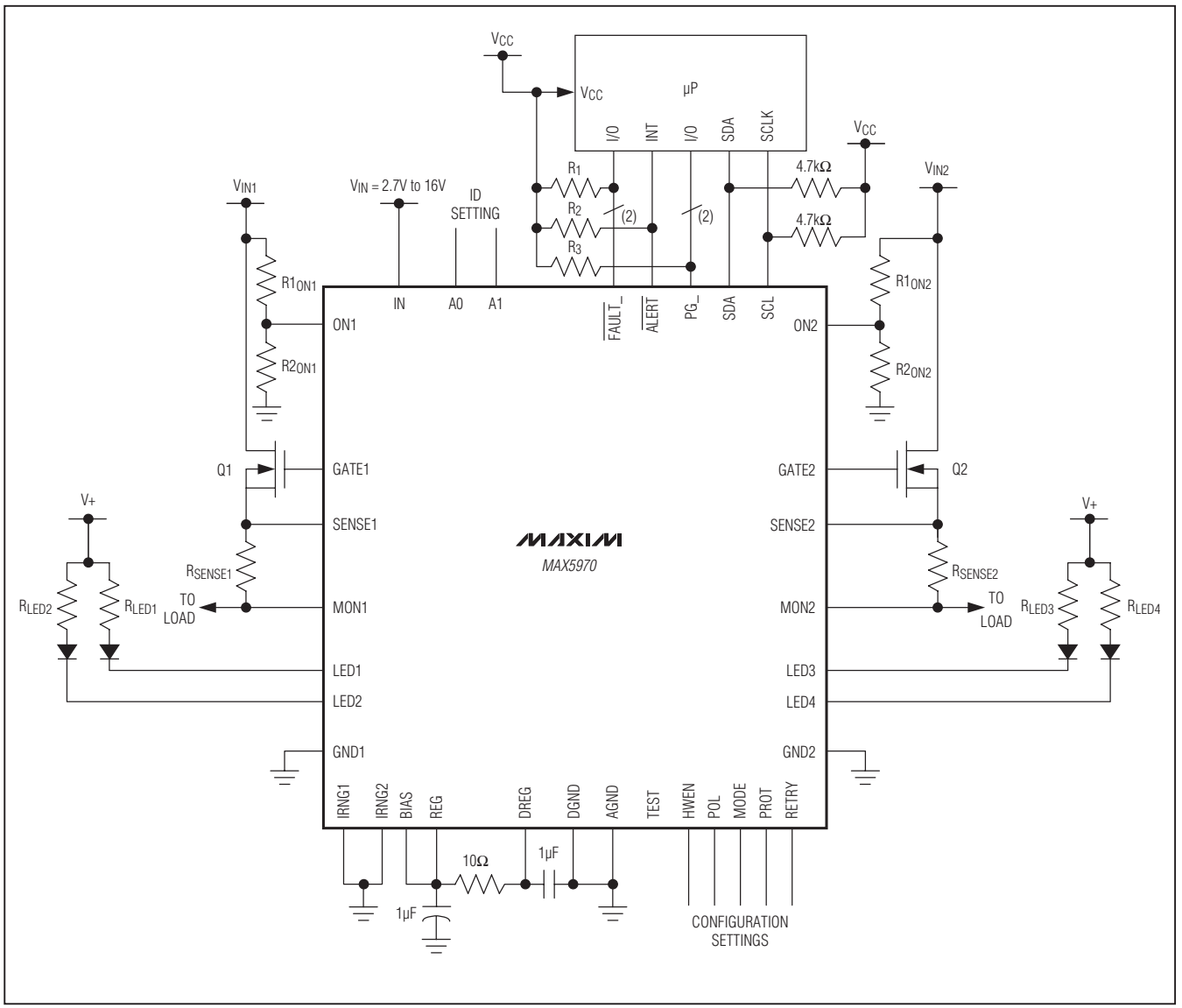
Typical Application Circuit



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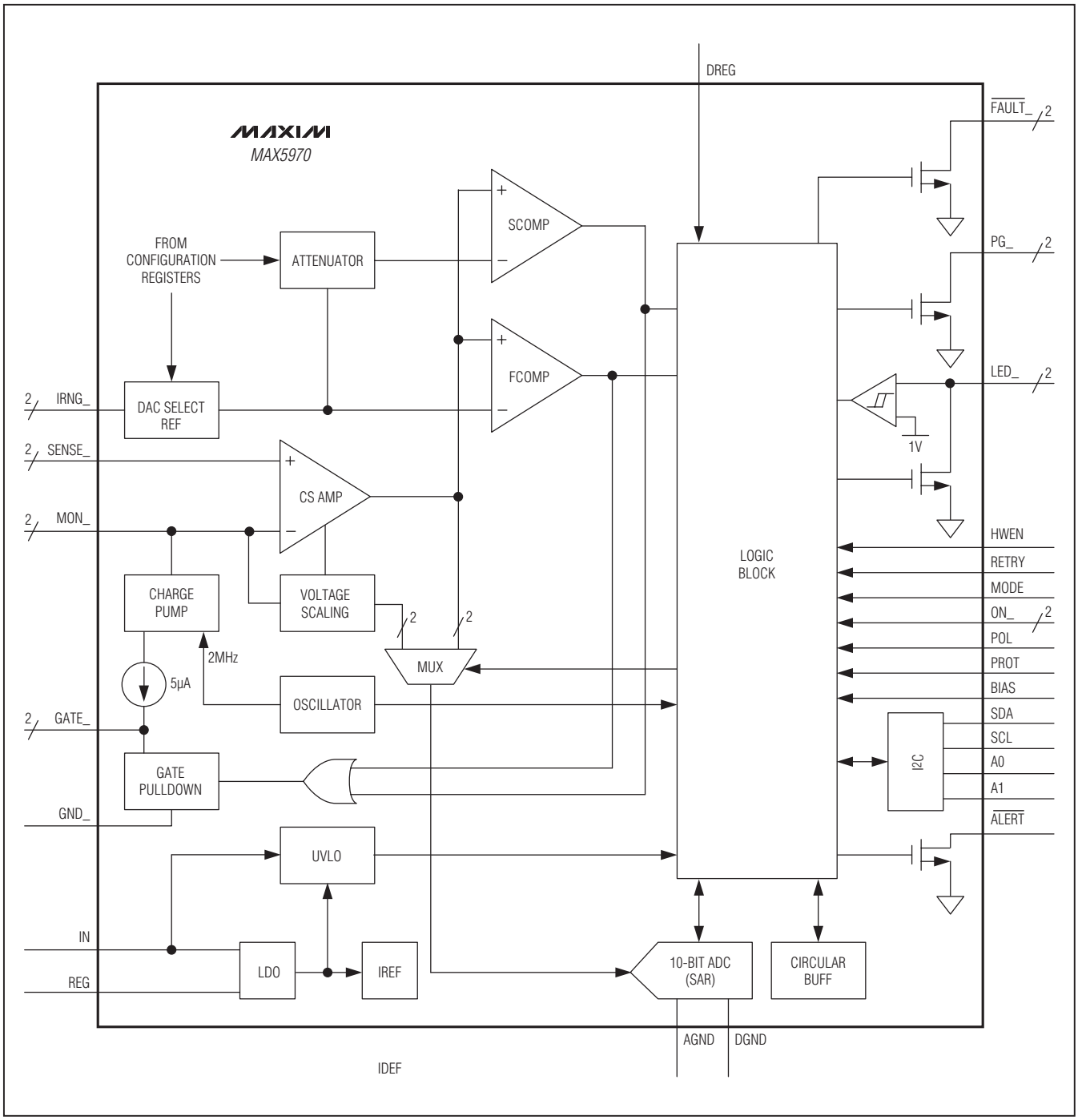
Block Diagram



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Detailed Description

The MAX5970 includes a set of registers that are accessed through the I²C interface. Some of the registers are read only and some of the registers are read and write that are updated to configure the MAX5970 for a specific operation. See Tables 1a and 1b for the registers map.

Table 1a. Register Address Map (Channel Specific)

REGISTER	DESCRIPTION	CHANNEL 1	CHANNEL 2	RESET VALUE	READ/ WRITE
adc_chx_cs_msb	High 8 bits ([9:2]) of latest current-signal ADC result	0x00	0x04	—	R
adc_chx_cs_lsb	Low 2 bits ([1:0]) of latest current-signal ADC result	0x01	0x05	—	R
adc_chx_mon_msb	High 8 bits ([9:2]) of latest voltage-signal ADC result	0x02	0x06	—	R
adc_chx_mon_ lsb	Low 2 bits ([1:0]) of latest voltage-signal ADC result	0x03	0x07	—	R
min_chx_cs_msb	High 8 bits ([9:2]) of current-signal minimum value	0x08	0x10	0xFF	R
min_chx_cs_ lsb	Low 2 bits ([1:0]) of current-signal minimum value	0x09	0x11	0x03	R
max_chx_cs_msb	High 8 bits ([9:2]) of current-signal maximum value	0x0A	0x12	0x00	R
max_chx_cs_ lsb	Low 2 bits ([1:0]) of current-signal maximum value	0x0B	0x13	0x00	R
min_chx_mon_msb	High 8 bits ([9:2]) of voltage-signal minimum value	0x0C	0x14	0xFF	R
min_chx_mon_ lsb	Low 2 bits ([1:0]) of voltage-signal minimum value	0x0D	0x15	0x03	R
max_chx_mon_msb	High 8 bits ([9:2]) of voltage-signal maximum value	0x0E	0x16	0x00	R
max_chx_mon_ lsb	Low 2 bits ([1:0]) of voltage-signal maximum value	0x0F	0x17	0x00	R
uv1thr _chx_msb	High 8 bits ([9:2]) of undervoltage warning (UV1) threshold	0x1A	0x24	0x00	R/W
uv1thr_chx_ lsb	Low 2 bits ([1:0]) of undervoltage warning (UV1) threshold	0x1B	0x25	0x00	R/W
uv2thr_chx_msb	High 8 bits ([9:2]) of undervoltage critical (UV2) threshold	0x1C	0x26	0x00	R/W
uv2thr_chx_ lsb	Low 2 bits ([1:0]) of undervoltage critical (UV2) threshold	0x1D	0x27	0x00	R/W
ov1thr_chx_msb	High 8 bits ([9:2]) of overvoltage warning (OV1) threshold	0x1E	0x28	0xFF	R/W
ov1thr_chx_ lsb	Low 2 bits ([1:0]) of overvoltage warning (OV1) threshold	0x1F	0x29	0x03	R/W

Table 1a. Register Address Map (Channel Specific) (continued)

REGISTER	DESCRIPTION	CHANNEL 1	CHANNEL 2	RESET VALUE	READ/ WRITE
ov2thr_chx_msb	High 8 bits ([9:2]) of overvoltage critical (OV2) threshold	0x20	0x2A	0xFF	R/W
ov2thr_chx_ lsb	Low 2 bits ([1:0]) of overvoltage critical (OV2) threshold	0x21	0x2B	0x03	R/W
oithr_chx_msb	High 8 bits ([9:2]) of overcurrent warning threshold	0x22	0x2C	0xFF	R/W
oithr_chx_ lsb	Low 2 bits ([1:0]) of overcurrent warning threshold	0x23	0x2D	0x03	R/W
dac_chx-fast	Fast-comparator threshold DAC setting	0x2E	0x2F	0xBF	R/W
cubf_ba_chx_v	Base address for block read of 50-sample voltage-signal data buffer	0x46	0x48	—	R
cubf_ba_chx_i	Base address for block read of 50-sample current-signal data buffer	0x47	0x49	—	R

Table 1b. Register Address Map (General)

REGISTER	DESCRIPTION	ADDRESS (HEX CODE)	RESET VALUE	READ/ WRITE
mon_range	MON input range setting	0x18	0x00	R/W
cbuf_chx_store	Selective enabling of circular buffer	0x19	0x0F	R/W
ifast2slow	Current threshold fast-to-slow ratio setting	0x30	0x0F	R/W
status0	Slow-trip and fast-trip comparators status register	0x31	0x00	R
status1	PROT, MODE, and ON_ inputs status register	0x32	—	R
status2	Fast-trip threshold maximum range setting bits, from IRNG_ three-state inputs	0x33	—	R/W
status3	LATCH, POL, $\overline{\text{ALERT}}$, and PG_ status register	0x34	—	R
fault0	Status register for undervoltage detection (warning or critical)	0x35	0x00	R/C
fault1	Status register for overvoltage detection (warning or critical)	0x36	0x00	R/C
fault2	Status register for overcurrent detection (warning)	0x37	0x00	R/C
pgdly	Delay setting between MON measurement and PG_ assertion	0x38	0x00	R/W
fokey	Load register with 0xA5 to enable force-on function	0x39	0x00	R/W
foset	Register that enables force-on function for a channel	0x3A	0x00	R/W
chxen	Channel enable bits	0x3B	—	R/W
dgl_i	OC deglitch enable bits	0x3C	0x00	R/W
dgl_uv	UV deglitch enable bits	0x3D	0x00	R/W
dgl_ov	OV deglitch enable bits	0x3E	0x00	R/W
cbufrd_hibyonly	Circular buffers readout mode: 8 bit or 10 bit	0x3F	0x0F	R/W
cbuf_dly_stop	Circular buffer stop-delay. Number of samples recorded to the circular buffer after channel shutdown.	0x40	0x19	R/W
peak_log_rst	Reset control bits for peak-detection registers	0x41	0x00	R/W
peak_log_hold	Hold control bits for peak-detection registers	0x42	0x00	R/W

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Table 1b. Register Address Map (General) (continued)

REGISTER	DESCRIPTION	ADDRESS (HEX CODE)	RESET VALUE	READ/ WRITE
LED_Flash	LED flash/GPIO enable register	0x43	0x00	R/W
LED_ph_pu	LED phase/weak pullup enable register	0x44	0x00	R/W
LED_state	LED pins voltage state register (LED pins set open)	0x45	0x00	R

Grouping Hot-Swap Channels

The MAX5970 can operate as either two independent hot-swap controllers or as a pair. See Table 2 for the configuration option based on the MODE logic level.

Hot-Swap Channels On-Off Control

Depending on the configuration of the Chx_EN1 and Chx_EN2 bits, when V_{IN} is above the V_{UVLO} threshold and the ON_ input reaches its internal threshold, the MAX5970 turns on the external n-channel MOSFET for the corresponding channel, allowing power to flow to the load. The channel is enabled depending on the output of a majority function. Chx_EN1, Chx_EN2, and ON_ are the inputs to the majority function and the channel is enabled when two or more of these inputs are 1.

(Channel enabled) = (Chx_EN1 x Chx_EN2) + (Chx_EN1 x ON_) + (Chx_EN2 x ON_)

The inputs ON_ and Chx_EN2 can be set externally; the initial state of the Chx_EN2 bits in register *chxen* is set by the state of the HWEN input when V_{IN} rises above V_{UVLO}. The ON_ inputs connect to internal precision analog comparators with a 0.6V threshold. Whenever $V_{ON\_}$ is above 0.6V, the corresponding ON_ bit in register *status1[0:1]* is set to 1. The inputs Chx_EN1 and Chx_EN2 can be set using the I^2C interface; the Chx_EN1 bits have a default value of 0. This makes it possible to enable or disable each of the MAX5970 channels independently with or without using the I^2C interface (see Tables 3, 4a, and 4b).

Table 2. Grouping Hot-Swap Channels

MODE INPUT	FUNCTION	DESCRIPTION
Low	Independent	Each channel operates as an independent hot-swap controller. A fault shutdown in one channel does not affect operation of other channel.
High/unconnected	Paired	Channel 0 and channel 1 operate together as one pair. A fault shutdown in one channel shuts down both channels in the pair. Both channels share the ADC monitoring capability.

Table 3. chxen Register Format

Description:	Channel enable bits, from HWEN input and Chx_EN1 bits
Register Title:	chxen
Register Address:	0x3B

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
				Ch2_EN2	Ch2_EN1	Ch1_EN2	Ch1_EN1	—
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 4a. status1 Register Function

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
0x32	[1:0]	**ON_ Inputs State** 1 = ON_ above 600mV channel enable threshold 0 = ON_ below 600mV channel enable threshold Bit 0: ON1 Bit 1: ON2
	[4]	**Channel Grouping Mode (MODE Input)** 0 = Grouped (MODE high or open) 1 = Independent (MODE low)
	[7:6]	**Voltage Critical Behavior (PROT Input)** 00 = Assert $\overline{ALERT}$ upon UV/OV critical (same as UV/OV warning behavior) 01 = Assert $\overline{ALERT}$ and deassert PG_ upon UV/OV critical 10 = Assert $\overline{ALERT}$, deassert PG_, and shutdown channel(s) upon UV/OV critical 11 = (Not possible)

Table 4b. status1 Register Format

Description:	Channel grouping (three-state MODE input), fault-detection behavior (three-state PROT input), and ON_ inputs status register
Register Title:	status1
Register Address:	0x32

R	R	R	R	R	R	R	R	RESET VALUE
prot[1]	prot[0]	—	mode[0]	—	—	ON2	ON1	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Figure 1 shows the detailed logic operation of the hot-swap enable signals Chx_EN1, Chx_EN2, and ON_, as well as the effect of various fault conditions.

An input undervoltage threshold control for enabling the hot-swap channel can be implemented by placing a resistive divider between the drain of the hot-swap MOSFET and ground, with the midpoint connected to ON_. The turn-on threshold voltage for the channel is then:

$$V_{EN} = 0.6V \times (R1 + R2)/R2$$

The maximum rating for the ON_ is 6V; do not exceed this value.

Startup

When all conditions for channel turn-on are met, the external n-channel MOSFET switch is fully enhanced with a typical gate-to-source voltage of 5V to ensure a low drain-to-source resistance. The charge pump at each GATE_ driver sources 5µA to control the output voltage turn-on voltage slew rate. An external capacitor can be added from GATE_ to GND_ to further reduce the voltage slew rate. Placing a 1kΩ resistor in series with this capacitance prevents the added capacitance from increasing the gate turn-off time. Total inrush current is the load current summed with the product of the gate voltage slew rate dV/dt and the load capacitance.

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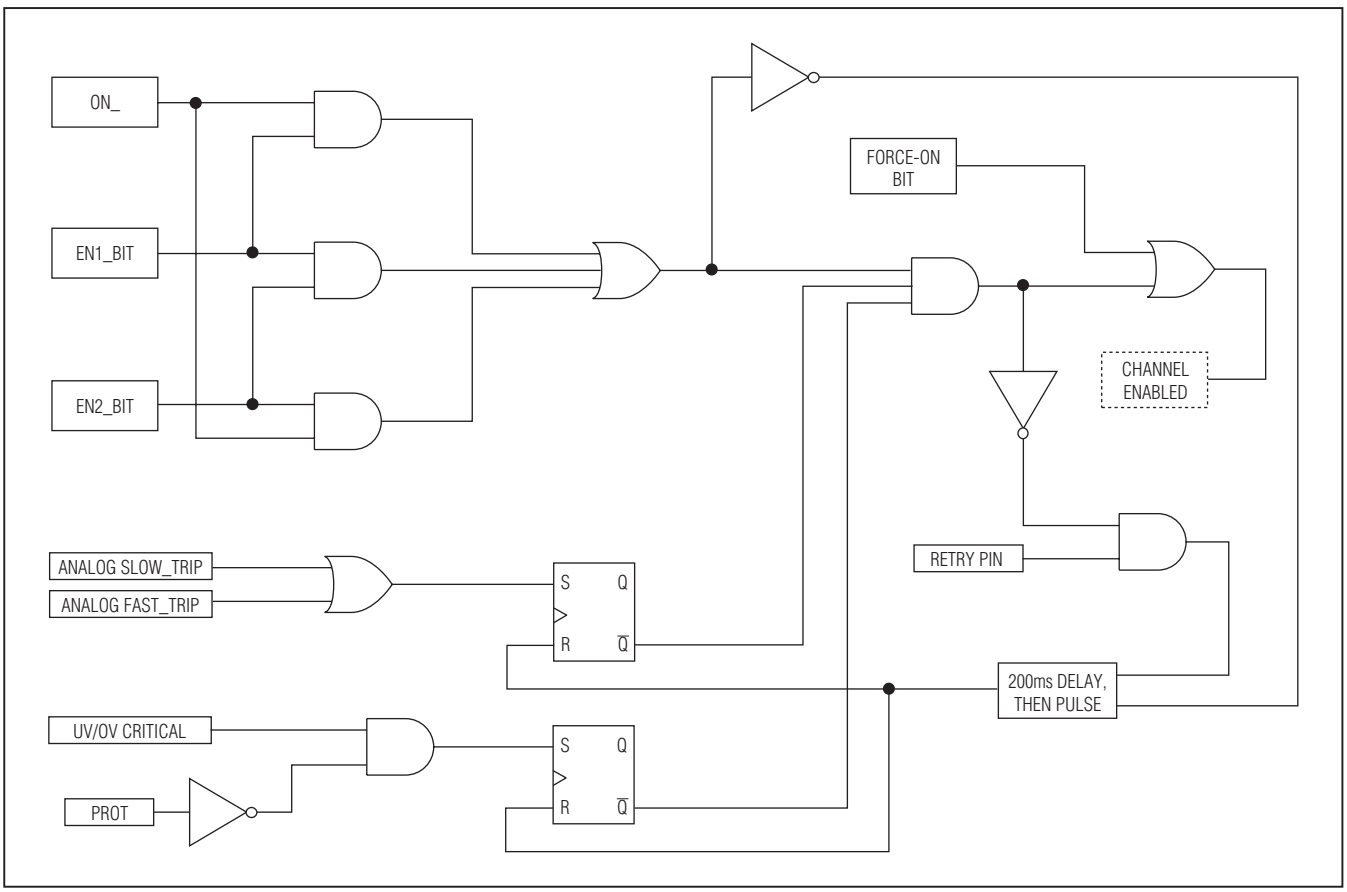

Figure 1. Channel On-Off Control Logic Functional Schematic

To determine the output dV/dt during startup, divide the GATE_ pullup current $I_{G(UP)}$ by the gate-to-ground capacitance. The voltage at the source of the external MOSFET follows the gate voltage, so the load dV/dt is the same as the gate dV/dt. Inrush current is the product of the dV/dt and the load capacitance. The time to start up t_{SU} is the hot-swap voltage VS_ divided by the output dV/dt.

Be sure to choose an external MOSFET that can handle the power dissipated during startup. The inrush current is roughly constant during startup, and the voltage drop across the MOSFET (drain to source) decreases linearly as the load capacitance charges. The resulting power dissipation is therefore roughly equivalent to a single pulse of magnitude (VS_ x Inrush current)/2 and duration t_{SU}. Refer to the thermal resistance charts in the MOSFET data sheet to determine the junction temperature rise during startup, and ensure that this does not exceed the maximum junction temperature for worst-case ambient conditions.

Circuit-Breaker Protection

As the channel is turned on and during normal operation, two analog comparators are used to detect an overcurrent condition by sensing the voltage across an external resistor connected between SENSE_ and MON_. If the voltage across the sense resistor is less than the slow-trip and fast-trip circuit-breaker thresholds, the GATE_ output remains high. If either of the thresholds is exceeded due to an overcurrent condition, the gate of the MOSFET is pulled down to MON_ by an internal 500mA current source.

The higher of the two comparator thresholds, the fast-trip, is set by an internal 8-bit DAC (see Table 8), within one of three configurable full-scale current-sense ranges: 25mV, 50mV, or 100mV (see Tables 7a and 7b). The 8-bit fast-trip threshold DAC can be programmed

Table 5a. ifast2slow Register Format

Description:	Current threshold fast to slow setting bits							
Register Title:	ifast2slow							
Register Address:	0x30							
R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**RESET VALUE**
—	—	—	—	Ch2_FS1	Ch2_FS0	Ch1_FS1	Ch1_FS0	0x0F
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 5b. Setting Fast-Trip to Slow-Trip Threshold Ratio

Chx_FS1	Chx_FS0	FAST-TRIP TO SLOW-TRIP RATIO (%)
0	0	125
0	1	150
1	0	175
1	1	200

from 40% to 100% of the selected full-scale current-sense range. The slow-trip threshold follows the fast-trip threshold as one of four programmable ratios, set by the ifast2slow register (see Tables 5a and 5b).

The fast-trip threshold is always higher than the slow-trip threshold, and the fast-trip comparator responds very quickly to protect the system against sudden, severe overcurrent events. The slower response of the slow-trip comparator varies depending upon the amount of overdrive beyond the slow-trip threshold. If the overdrive is small and short-lived, the comparator does not shut down the affected channel. As the overcurrent event increases in magnitude, the response time of the slow-trip comparator decreases. This scheme provides good rejection of noise and spurious overcurrent transients near the slow-trip threshold while aggressively protecting the system against larger overcurrent events that occur as a result of a load fault.

Setting Circuit-Breaker Thresholds

To select and set the MAX5970 slow-trip and fast-trip comparator thresholds, use the following procedure:

1) Select one of four ratios between the fast-trip threshold and the slow-trip threshold: 200%, 175%, 150%, or 125%. A system that experiences brief, but large transient load currents should use a higher ratio, whereas a system that operates continuously at higher average load currents might benefit from a smaller ratio to ensure adequate protection. The ratio is set by writing to the ifast2slow register. The default setting on power-up is 200%.
2) Determine the slow-trip threshold $V_{TH,ST}$ based on the anticipated maximum continuous load current during normal operation, and the value of the current-sense resistor. The slow-trip threshold should include some margin (possibly 20%) above the maximum load current to prevent spurious circuit-breaker shutdown and to accommodate passive component tolerances:

$$V_{TH,ST} = R_{SENSE} \times I_{LOAD,MAX} \times 120\%$$

3) Calculate the necessary fast-trip threshold $V_{TH,FT}$ based on the ratio set in step 1:

$$V_{TH,FT} = V_{TH,ST} \times (\text{ifast2slow ratio})$$

4) Select one of the four maximum current-sense ranges: 25mV, 50mV, or 100mV. The current-sense range is initially set upon power-up by the state of the associated IRNG_ input, but can be altered at any time by writing to the status2 register. For maximum accuracy and best measurement resolution, select the lowest current-sense range that is larger than the $V_{TH,FT}$ value calculated in Step 3.
5) Program the fast-trip and slow-trip thresholds by writing an 8-bit value to the dac_chx register. This 8-bit value is determined from the desired $V_{TH,ST}$ value that was calculated in Step 2, the threshold ratio from Step 1, and the current-sense range from Step 4:

$$DAC = V_{TH,ST} \times 255 \times (\text{ifast2slow ratio}) / (\text{IRNG\_ current-sense range})$$

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The MAX5970 provides a great deal of system flexibility because the current-sense range, DAC setting, and threshold ratio can be changed on the fly for systems that must protect a wide range of interchangeable load devices, or for systems that control the allocation of power to smart loads. Table 6 shows the specified ranges for the fast-trip and slow-trip thresholds for all combinations of current-sense range and threshold ratio.

When an overcurrent event causes the MAX5970 to shut down a channel, a corresponding open-drain $\overline{\text{FAULT\_}}$ output alerts the system. Figure 2 shows the operation and fault-management flowchart for one channel of the MAX5970.

Table 6. Specified Current-Sense and Circuit-Breaker Threshold Ranges

IRNG_ INPUT	FAST-TRIP DAC OUTPUT RANGE (mV)	GAIN (2-BIT) (V_{FAST}/V_{SLOW}) ifast2slow (DEFAULT = 11)	SLOW-TRIP THRESHOLD RANGE (mV)
Low	10 to 25	00 (125%)	8.00 to 20.00
		01 (150%)	6.67 to 16.67
		10 (175%)	5.71 to 14.29
		11 (200%)	5.00 to 12.50
High	20 to 50	00 (125%)	16.00 to 40.00
		01 (150%)	13.33 to 33.33
		10 (175%)	11.48 to 28.57
		11 (200%)	10.00 to 25.00
Unconnected	40 to 100	00 (125%)	32.00 to 80.00
		01 (150%)	26.67 to 66.67
		10 (175%)	22.86 to 57.14
		11 (200%)	20.00 to 50.00

Table 7a. IRNG Inputs Status Register Format

Description: Fast-trip threshold maximum range setting bits, from IRNG_ three-state inputs
Register Title: Status 2
Register Address: 0x33

				R/W	R/W	R/W	R/W	RESET VALUE
—	—	—	—	CH1_ IRNG1	CH1_ IRNG0	CH0_ IRNG1	CH0_ IRNG0	—
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 7b. Setting Current-Sense Range

IRNG_ PIN STATE	Chx_IRNG1	Chx_IRNG0	MAXIMUM CURRENT-SENSE SIGNAL (mV)
Low	1	0	25
High	0	1	50
Open	0	0	100

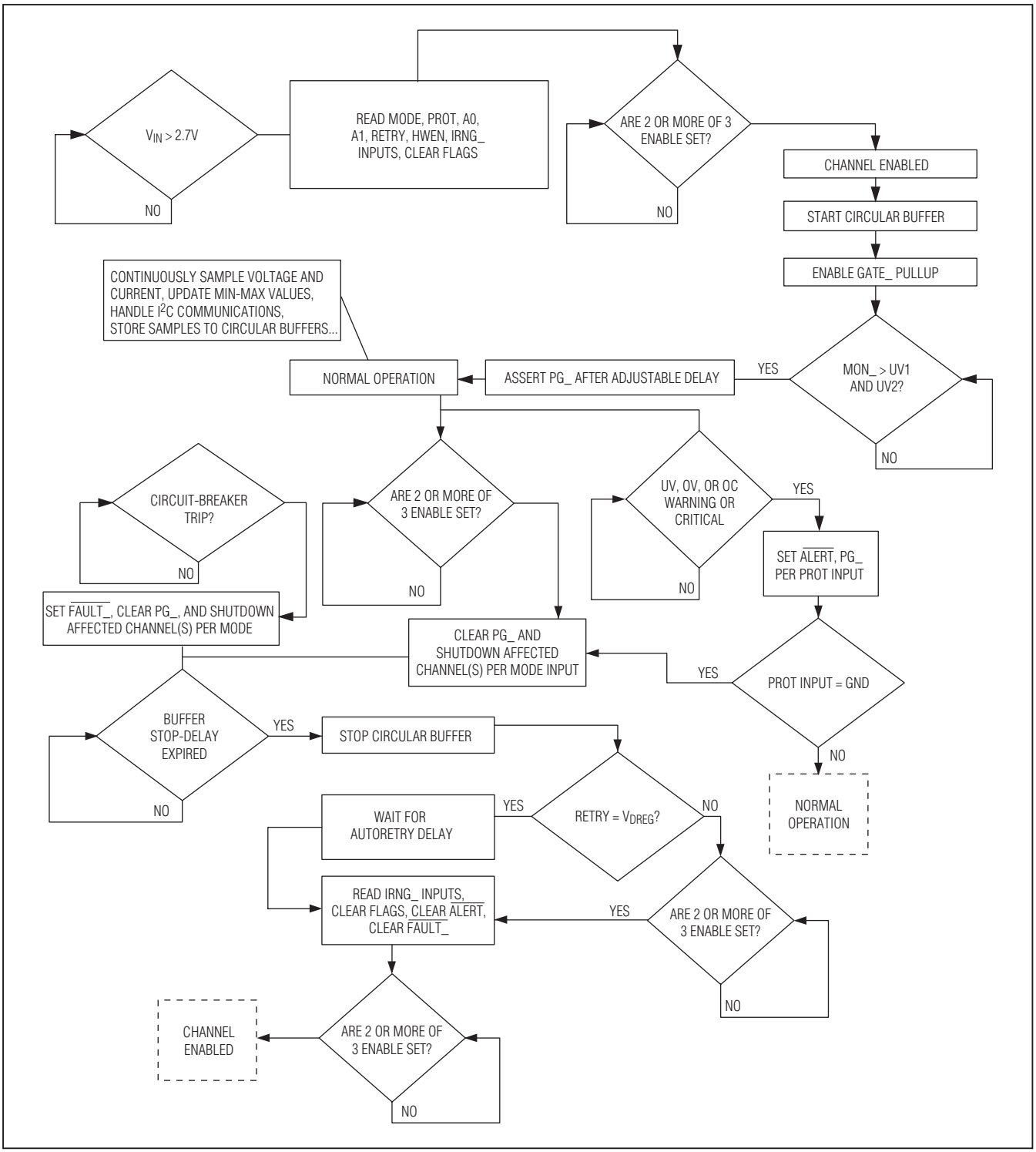

Figure 2. Operation and Fault-Management Flowchart for One Channel

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Table 8. dac_chx Register Format

Description:	Fast-comparator threshold DAC setting							
Register Title:	dac_ch0	dac_ch1						
Register Addresses:	0x2E	0x2F						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]	0xBF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Digital Current Monitoring

The two current-sense signals are sampled by the internal 10-bit 10ksps ADC, and the most recent results are stored in registers for retrieval through the I²C interface. The current conversion values are 10 bits wide, with the eight high-order bits written to one 8-bit register and the two low-order bits written to the next higher 8-bit register address (Tables 9 and 10). This allows use of just the high-order byte in applications where 10-bit precision is not required. This split 8-bit/2-bit storage scheme is used throughout the MAX5970 for all 10-bit ADC conversion results and 10-bit digital comparator thresholds.

Table 9. ADC Current Conversion Results Register Format (High-Order Bits)

Description:	Most recent current conversion result, high-order bits [9:2]							
Register Title:	adc_ch0_cs_msb	adc_ch1_cs_msb						
Register Addresses:	0x00	0x04						
R	R	R	R	R	R	R	R	RESET VALUE
inew_9	inew_8	inew_7	inew_6	inew_5	inew_4	inew_3	inew_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 10. ADC Current Conversion Results Register Format (Low-Order Bits)

Description:	Most recent current conversion result, low-order bits [0:1]							
Register Title:	adc_ch0_cs_ lsb	adc_ch1_cs_lsb						
Register Addresses:	0x01	0x05						
R	R	R	R	R	R	R	R	RESET VALUE
						inew_1	inew_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Once the PG_ output is asserted, the most recent current samples are continuously compared to the programmable overcurrent warning register values. If the measured current value exceeds the warning level, the $\overline{ALERT}$ output is asserted. The MAX5970 response to this digital comparator is not altered by the setting of the PROT input (Tables 11 and 12).

Minimum and Maximum Value Detection for Current Measurement Values

All current measurement values from the ADC are continuously compared with the contents of minimum- and maximum-value registers, and if the most recent measurement exceeds the stored maximum or is less than the stored minimum, the corresponding register is updated with the new value. These peak detection registers are read accessible through the I²C interface (Tables 13–16). The minimum-value registers are reset to 0x3FF, and the maximum-value registers are reset to 0x000. These reset values are loaded upon startup of a channel or at any time as commanded by register peak_log_rst (Table 36).

Table 11. Overcurrent Warning Threshold Register Format (High-Order Bits)

Description:	Overcurrent warning threshold high-order bits [9:2]							
Register Title:	oi_ch0_msb			oi_ch1_msb				
Register Addresses:	0x22			0x2C				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
oi_9	oi_8	oi_7	oi_6	oi_5	oi_4	oi_3	oi_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 12. Overcurrent Warning Threshold Register Format (Low-Order Bits)

Description:	Overcurrent warning threshold low-order bits [1:0]							
Register Title:	oi_ch0_ lsb			oi_ch1_lsb				
Register Addresses:	0x23			0x2D				
R	R	R	R	R	R	R/W	R/W	RESET VALUE
						oi_1	oi_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 13. ADC Minimum Current Conversion Register Format (High-Order Bits)

Description:	Minimum current conversion result high-order bits [9:2]							
Register Title:	min_ch0_cs_msb			min_ch1_cs_msb				
Register Addresses:	0x08			0x10				
R	R	R	R	R	R	R	R	RESET VALUE
imin_9	imin_8	imin_7	imin_6	imin_5	imin_4	imin_3	imin_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

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Table 14. ADC Minimum Current Conversion Register Format (Low-Order Bits)

Description:	Minimum current conversion result low-order bits [1:0]							
Register Title:	min_ch0_cs_ lsb				min_ch1_cs_ lsb			
Register Addresses:	0x09				0x11			
R	R	R	R	R	R	R	R	RESET VALUE
						imin_1	imin_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 15. ADC Maximum Current Conversion Register Format (High-Order Bits)

Description:	Maximum current conversion result high-order bits [9:2]							
Register Title:	max_ch0_cs_msb				max_ch1_cs_msb			
Register Addresses:	0x0A				0x12			
R	R	R	R	R	R	R	R	RESET VALUE
imax_9	imax_8	imax_7	imax_6	imax_5	imax_4	imax_3	imax_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 16. ADC Maximum Current Conversion Register Format (Low-Order Bits)

Description:	Maximum current conversion result low-order bits [1:0]							
Register Title:	max_ch0_cs_ lsb				max_ch1_cs_ lsb			
Register Addresses:	0x0B				0x13			
R	R	R	R	R	R	R	R	RESET VALUE
						imax_1	imax_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Digital Voltage Monitoring and Power-Good Outputs

The voltage at the load (MON_ inputs) is sampled by the internal ADC. The MON_ full-scale voltage for each channel can be set to 16V, 8V, 4V, or 2V by writing to register mon_range. The default range is 16V (Tables 17 and 18).

Table 17. ADC Voltage Monitor Settings Register Format

Description:	ADC voltage monitor full-scale range settings (for MON_ inputs)
Register Title:	mon_range
Register Addresses:	0x18

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
—	—	—	—	MON2_rng1	MON2_rng0	MON1_rng1	MON1_rng0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 18. ADC Full-Scale Voltage Setting

MONx_rng1	MONx_rng0	ADC FULL-SCALE VOLTAGE (V)
0	0	16
0	1	8
1	0	4
1	1	2

The most recent voltage conversion results can be read from the adc_chx_mon_msb and adc_chx_mon_lsb registers (see Tables 19 and 20).

Table 19. ADC Voltage Conversion Result Register Format (High-Order Bits)

Description:	Most recent voltage conversion result, high-order bits [9:2]	
Register Title:	adc_ch0_mon_msb	adc_ch1_mon_msb
Register Addresses:	0x02	0x06

R	R	R	R	R	R	R	R	RESET VALUE
vnew_9	vnew_8	vnew_7	vnew_6	vnew_5	vnew_4	vnew_3	vnew_2	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 20. ADC Voltage Conversion Result Register Format (Low-Order Bits)

Description:	Most recent voltage conversion result, low-order bits [1:0]	
Register Title:	adc_ch0_mon_lsb	adc_ch1_mon_lsb
Register Addresses:	0x03	0x07

R	R	R	R	R	R	R	R	RESET VALUE
						vnew_1	vnew_0	0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

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Digital Undervoltage and Overvoltage Detection Thresholds

The most recent voltage values are continuously compared to four programmable limits, comprising two undervoltage (UV) levels (see Tables 21–24) and two overvoltage (OV) levels (see Tables 25–28).

Table 21. Undervoltage Warning Threshold Register Format (High-Order Bits)

Description:	Undervoltage warning threshold high-order bits [9:2]							
Register Title:	uv1th_ch0_msb	uv1th_ch1_msb						
Register Addresses:	0xA1	0x1E						
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
	uv1_9	uv1_8	uv1_7	uv1_6	uv1_5	uv1_4	uv1_3	uv1_2	0x00
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 22. Undervoltage Warning Threshold Register Format (Low-Order Bits)

Description:	Undervoltage warning threshold low-order bits [1:0]							
Register Titles:	uv1th_ch0_lsb	uv1th_ch1_lsb						
Register Addresses:	0x1B	0x1F						
	R	R	R	R	R	R	R/W	R/W	RESET VALUE
							uv1_1	uv1_0	0x00
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 23. Undervoltage Critical Threshold Register Format (High-Order Bits)

Description:	Undervoltage critical threshold high-order bits [9:2]							
Register Title:	uv2th_ch0_msb	uv2th_ch1_msb						
Register Addresses:	0x1C	0x26						
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
	uv2_9	uv2_8	uv2_7	uv2_6	uv2_5	uv2_4	uv2_3	uv2_2	0x00
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 24. Undervoltage Critical Threshold Register Format (Low-Order Bits)

Description:	Undervoltage critical threshold low-order bits [1:0]							
Register Title:	uv2th_ch0_lsb	uv2th_ch1_lsb						
Register Addresses:	0x1D	0x27						
	R	R	R	R	R	R	R/W	R/W	RESET VALUE
							uv2_1	uv2_0	0x00
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 25. Overvoltage Warning Threshold Register Format (High-Order Bits)

Description:	Overvoltage warning threshold high-order bits [9:2]							
Register Title:	ov1thr_ch0_msb			ov1thr_ch1_msb				
Register Addresses:	0x1E			0x28				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ov1_9	ov1_8	ov1_7	ov1_6	ov1_5	ov1_4	ov1_3	ov1_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 26. Overvoltage Warning Threshold Register Format (Low-Order Bits)

Description:	Overvoltage warning threshold low-order bits [1:0]							
Register Title:	ov1thr_ch0_lsb			ov1thr_ch1_lsb				
Register Addresses:	0x1F			0x29				
R	R	R	R	R	R	R/W	R/W	RESET VALUE
						ov1_1	ov1_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 27. Overvoltage Critical Threshold Register Format (High-Order Bits)

Description:	Overvoltage critical threshold high-order bits [9:2]							
Register Title:	ov2thr_ch0_msb			ov2thr_ch1_msb				
Register Addresses:	0x20			0x2A				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE
ov2_9	ov2_8	ov2_7	ov2_6	ov2_5	ov2_4	ov2_3	ov2_2	0xFF
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	

Table 28. Overvoltage Critical Threshold Register Format (Low-Order Bits)

Description:	Overvoltage critical threshold low-order bits [1:0]							
Register Title:	ov2thr_ch0_lsb			ov2thr_ch1_lsb				
Register Addresses:	0x21			0x2B				
R	R	R	R	R	R	R/W	R/W	RESET VALUE
						ov2_1	ov2_0	0x03
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	