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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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EVALUATION KIT AVAILABLE

MAX5971B

Single-Port, 40W, IEEE 802.3af/at, PSE Controller with I²C

General Description

The MAX5971B is a single-port power controller designed for use in IEEE® 802.3af/at-compliant power-sourcing equipment (PSE). This device provides powered device (PD) discovery, classification, current limit, and DC and AC load-disconnect detections. The MAX5971B supports both fully automatic operation and software programmability, and features an integrated power MOSFET and sense resistor. The device supports detection and classification operation from a single 54V supply. In addition, it supports 2-event classification and new Class 5 classification of high-power PDs. The MAX5971B provides up to 40W to a single port (Class 5 enabled) and still provides high-capacitance detection for legacy PDs.

The device provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies a device connected to the port after initial software activation, but does not power the port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all port activities and securely turns off power to the port.

The IC features an I²C-compatible, 2-wire serial interface, and is fully software-configurable and programmable. The device provides instantaneous readout of port current through the I²C interface. The device's extensive programmability enhances system flexibility, enables field diagnosis and allows for uses in other, non standard applications.

The device provides input undervoltage lockout (UVLO), input undervoltage detection, input overvoltage lockout, overtemperature protection, output voltage slew-rate limit during startup, and LED status indication. The MAX5971B programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The device is available in a space-saving, 28-pin TQFN (5mm x 5mm) power package and is rated for the extended (-40°C to +105°C) temperature range.

Applications

Single-Port PSE End-Point Applications

Single-Port PSE Power Injectors (Midspan Applications)

Switches/Routers

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Features

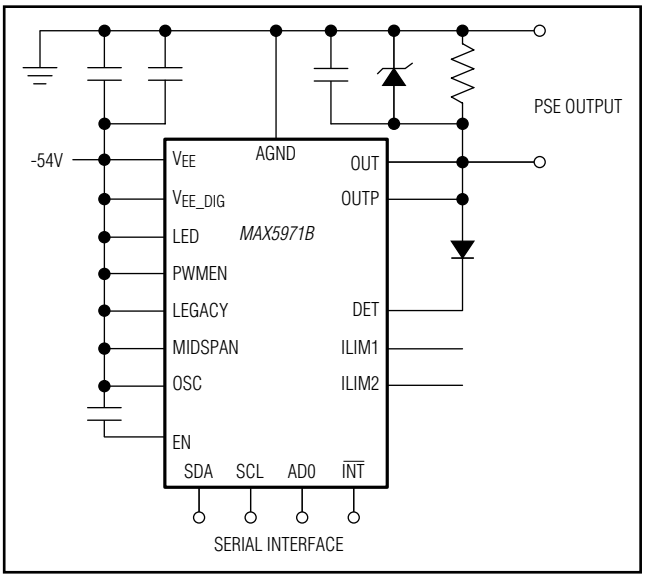
- **IEEE 802.3af/at Compliant**
- **Up to 40W for Single-Port PSE Applications**
- **Integrated Power MOSFET and Sense Resistor**
- **Supports 54V Single-Supply Operation**
- **PD Detection and Classification**
- **I²C-Compatible, 2-Wire Serial Interface**
- **Instantaneous Readout of Port Current Through I²C Interface**
- **Programmable Current Limit for Class 5 PDs**
- **High-Capacitance Detection for Legacy Devices**
- **Supports Both DC and AC Load Removal Detections**
- **Current Foldback and Duty-Cycle-Controlled Current Limit**
- **LED Indicator for Port Status**
- **Direct Fast-Shutdown Control Capability**
- **Space-Saving, 28-Pin TQFN (5mm x 5mm) Power Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5971BETI+	-40°C to +105°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5336; Rev 3; 3/16

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)

AGND, DET, LED ..... -0.3V to +80V
OUT ..... -0.3V to (V_{AGND} + 0.3V)
OUTP ..... -6V to (V_{AGND} + 0.3V)
V_{EE_DIG} ..... -0.3V to +0.3V
OSC ..... -0.3V to +6V
EN, PWMEN, MIDSPAN, LEGACY, ILIM1, ILIM2 ..... -0.3V to +4V
$\overline{INT}$, AD0, SCL, SDA ..... -0.3V to +6V
Maximum Current into $\overline{INT}$ and SDA 80mA
Maximum Current into LED 40mA
Maximum Current into OUT ..... Internally Regulated
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

28 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +105°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}		32		60	V
Supply Current	I_{EE}	V_{OUT} = V_{EE}, all logic inputs unconnected, measured at AGND in power mode			2.5	4	mA
CURRENT LIMIT							
Current Limit	I_{LIM}	Maximum I_{LOAD} allowed during current-limit conditions, V_{OUT} = 0V (Note 3)	ICUT = 010	98	126	155	mA
			ICUT = 011	185	223	265	
			Class 0, 1, 2, 3 or ICUT = 000	400	420	441	
			Class 4 or ICUT = 001	684	720	756	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = unconnected or ICUT = 101	807	850	893	
			Class 5 if ILIM1 = unconnected, ILIM2 = V_{EE} or ICUT = 110	855	900	945	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = V_{EE} or ICUT = 111	902	950	998	
Foldback Initial OUT Voltage	V_{FLBK_ST}	V_{AGND} - V_{OUT} below which the current limit starts folding back			27		V
Foldback Final OUT Voltage	V_{FLBK_END}	V_{AGND} - V_{OUT} below which the current limit reaches I_{TH_FB}			10		V
Minimum Foldback Current-Limit Threshold	I_{TH_FB}	V_{OUT} = V_{AGND}			166		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +105°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERCURRENT							
Overcurrent Threshold	I_{CUT}	Overcurrent threshold allowed for t ≤ t_{FAULT}, V_{OUT} = 0V (Note 3)	ICUT = 010	86	111	136	mA
			ICUT = 011	162	196	233	
			Class 0, 1, 2, 3 or ICUT = 000	351	370	389	
			Class 4 or ICUT = 001	602	634	666	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = unconnected or ICUT = 101	710	748	785	
			Class 5 if ILIM1 = unconnected, ILIM2 = V_{EE} or ICUT = 110	752	792	832	
			Class 5 if ILIM1 = V_{EE}, ILIM2 = V_{EE} or ICUT = 111	794	836	878	
INTERNAL POWER							
DMOS On-Resistance		Measured from OUT to V_{EE}, I_{OUT} = 100mA	T_A = +25°C		0.5	0.9	Ω
			T_A = +105°C		0.6	1.3	
Power-Off OUT Leakage Current	I_{OUT_LEAK}	V_{EN} = V_{EE}, V_{OUT} = V_{AGND}				10	µA
SUPPLY MONITORS							
V_{EE} Undervoltage Lockout	V_{EE_UVLO}	V_{AGND} - V_{EE}, V_{AGND} increasing			28.5		V
V_{EE} Undervoltage Lockout Hysteresis	V_{EE_UVLOH}	Port is shutdown if: V_{AGND} - V_{EE} < V_{EE_UVLO} - V_{EE_UVLOH}			3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} increasing			62.5		V
V_{EE} Overvoltage Lockout Hysteresis	V_{EE_OVH}				1		V
V_{EE} Undervoltage	V_{EE_UV}	V_{EE_UV} event bit sets if: V_{AGND} - V_{EE} < V_{EE_UV}, V_{EE} increasing			40		V
Thermal Shutdown Threshold	T_{SHD}	Port is shut down and device resets if the junction temperature exceeds this limit, temperature increasing			+150		°C
Thermal Shutdown Hysteresis	T_{SHDH}	Temperature decreasing			20		°C
OUTPUT MONITOR							
OUT Input Current	I_{BOUT}	V_{OUT} = V_{AGND}, probing phases				6	µA
Idle Pullup Current at OUT	I_{DIS}	OUTP discharge current, detection and classification off, port shutdown, V_{OUTP} = V_{AGND} - 2.8V		200		265	µA
Short to V_{EE} Detection Threshold	DCN_{TH}	V_{OUT} - V_{EE}, V_{OUT} decreasing, enabled during detection		1.5	2.0	2.5	V
Short to V_{EE} Detection Threshold Hysteresis	DCN_{HY}				220		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +105°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOAD DISCONNECT							
DC Load-Disconnect Threshold	I_{DC_TH}	Minimum load current allowed before disconnect (DC disconnect active), V_{OUT} = 0V		5	7.5	10	mA
AC Load-Disconnect Threshold (Note 4)	I_{AC_TH}	Current into DET, for $I_{DET} < I_{AC\_TH}$ the port powers off (AC disconnect active)		115	130	145	µA
Triangular Wave Peak-to-Peak Voltage Amplitude	AMP_{TRW}	Measured at DET, referred to AGND		3.85	4	4.2	V
OSC Pullup/Pulldown Currents	I_{OSC}	Measured at OSC		26	32	39	µA
ACD_EN Threshold	V_{ACD_EN}	V_{OSC} - V_{EE} > V_{ACD_EN} to activate AC disconnect		270	330	380	mV
Load-Disconnect Timer	t_{DISC}	Time from $I_{RSENSE} < I_{DC\_TH}$ (DC disconnect active) or $I_{DET} < I_{AC\_TH}$ (AC disconnect active) to gate shutdown (Note 5)		300		400	ms
DETECTION							
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - V_{DET} during the first detection phase		3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - V_{DET} during the second detection phase		9	9.3	9.6	V
Current-Limit Protection	I_{DLIM}	V_{DET} = V_{AGND} during detection, measure current through DET		1.50	1.75	2.00	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - V_{OUT} < V_{DCP} after the first detection phase a short circuit to AGND is detected.			1		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition			20		µA
Resistor Detection Window	R_{DOK}	(Note 6)		19		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values				15.5	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
Classification Probe Voltage	V_{CL}	V_{AGND} - V_{DET} during classification		16		20	V
Current-Limit Protection	I_{CILIM}	V_{DET} = V_{AGND}, during classification measure current through DET		65		80	mA
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes	Class 0, Class 1	5.5	6.5	7.5	mA
			Class 1, Class 2	13.0	14.5	16.0	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			Class 4 upper limit (Note 7)	45	48	51	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +105°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS
Mark Event Voltage	V_{MARK}	V_{AGND} - V_{DET} during mark event	8		10	V
Mark Event Current Limit	I_{MARK_LIM}	V_{DET} = V_{AGND} during mark event measure current through DET	55		80	mA
DIGITAL INPUTS/OUTPUTS (Voltages Referenced to V_{EE})						
Digital Input Low	V_{IL}				0.8	V
Digital Input High	V_{IH}		2.4			V
Internal Input Pullup Current	I_{PU}	Pullup current to internal digital supply to set default values	3	5	7	µA
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 10mA			0.4	V
Open-Drain Leakage	I_{OL}	Open-drain high impedance			2	µA
LED Output Low Voltage	V_{LED_LOW}	I_{LED} = 10mA, PWM disabled, port power-on			0.8	V
LED Output Leakage	I_{LED_LEAK}	PWM disabled, shutdown mode, V_{LED} = 60V			10	µA
PWM Frequency				25		kHz
PWM Duty Cycle				6.25		%
TIMING						
Startup Time	t_{START}	Time during which a current limit set to 420mA is allowed, starts when power is turned on (Note 8)	50	60	70	ms
Fault Time	t_{FAULT}	Maximum allowed time for an overcurrent condition set by I_{CUT} after startup (Note 8)	50	60	70	ms
Detection Reset Time	t_{ME}	Time allowed for the port voltage to reset before detection starts		80	90	ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed			330	ms
Midspan Mode Detection Delay	t_{DMID}		2	2.2	2.4	s
Classification Time	t_{CLASS}	Time allowed for classification		19	23	ms
Mark Event Time		Time allowed for mark event	7	9	11	ms
V_{EE_UVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EE_UVLO} thresholds before the device operates		5.2		ms
Restart Timer	$t_{RESTART}$	Time the device waits before turning on after an overcurrent fault (Note 8)		16 x t_{FAULT}		ms
Watchdog Clock Period		Rate of decrement of the watchdog time		164		ms
ADC PERFORMANCE (Power-On Mode)						
Resolution				9		Bits
Range				1		A
LSB Step Size				1.95		mA
Gain Error		T_A = +25°C			2	%
		T_A = -40°C to +105°C		3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} - V_{EE} = 32V to 60V, T_A = -40°C to +105°C, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} - V_{EE} = +54V, T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Absolute Accuracy		I_{OUT} = 400mA, T_A = +25°C	201	205	209	LSB
		I_{OUT} = 400mA, T_A = -40°C to +105°C		205		
Integral Nonlinearity	INL	T_A = +25°C		0.3	1.5	LSB
		T_A = -40°C to +105°C		0.3		
Differential Nonlinearity	DNL	T_A = +25°C		0.3	1.5	LSB
		T_A = -40°C to +105°C		0.3		
TIMING CHARACTERISTICS (For 2-Wire Fast Mode)						
Serial Clock Frequency	f_{SCL}		100		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time for a START Condition	$t_{HD,STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		150	ns
Data in Setup Time	$t_{SU,DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 9)	20 + 0.1C_B		300	ns
Fall Time of SDA Transmitting	t_F	(Note 9)			250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Note 9)		50		ns

Note 2: This device is production tested at T_A = +25°C. Limits to T_A = -40°C to +105°C are guaranteed by design.

Note 3: Default thresholds are set by the classification result in auto mode. The thresholds are manually software programmable through the ICUT Register (R2Ah[2:0]). If ILIM1 and ILIM2 are both unconnected, Class 5 detection is disabled. See the C*lass 5 PD Classification* section and Table 3 for details and settings.

Note 4: Default value. The AC load-disconnect threshold can be programmed through the AC_TH register (R23h[2:0]).

Note 5: Default value. The load-disconnect time, t_{DISC} can be programmed through the TDISC register (R16h[1:0]).

Note 6: R_{DOK} = (V_{OUT2} - V_{OUT1})/(I_{DET2} - I_{DET1}). V_{OUT1}, V_{OUT2}, I_{DET2}, and I_{DET1} represent the voltage at OUT and the current at DET during phase 1 and 2 of the detection, respectively.

Note 7: If Class 5 is enabled, this value is the classification current threshold from Class 4 to Class 5.

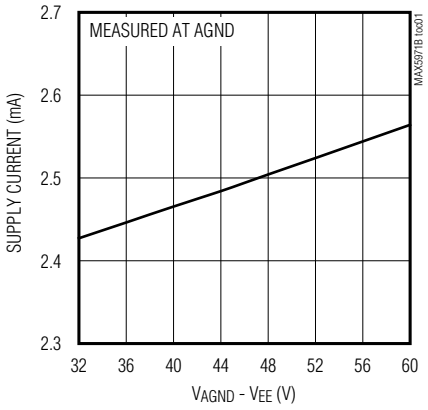
Note 8: Default values. The startup, fault, and restart timers can be programmed through the TSTART (R16h[5:4]), TFAULT (R16h[3:2]), and RSRT (R16h[7:6]) registers, respectively.

Note 9: Guaranteed by design. Not subject to production testing.

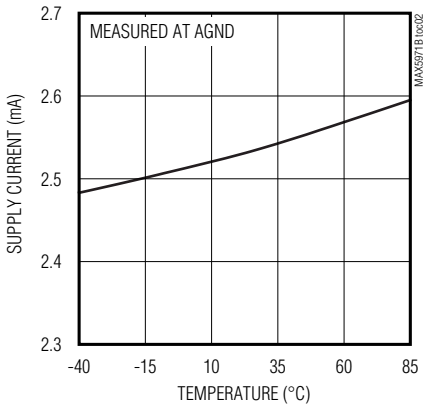
Typical Operating Characteristics

(V_{AGND} = 54V, V_{EE} = V_{EE_DIG} = 0V, T_A = +25°C, endpoint mode and default register settings with a Class 0 PD, unless otherwise otherwise noted.)

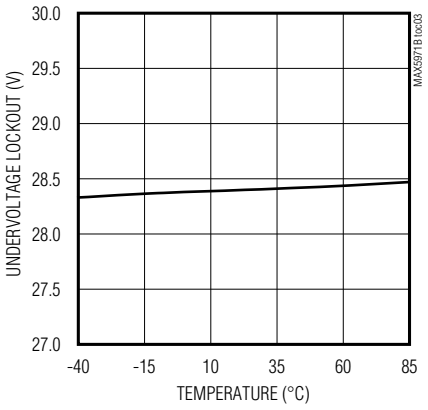
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



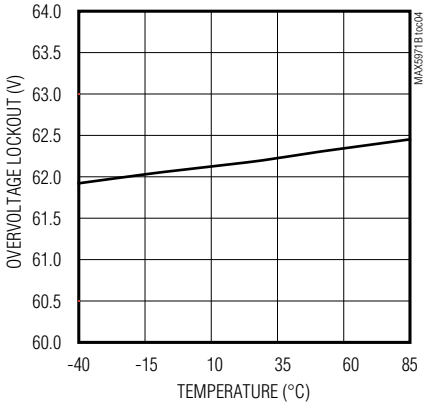
ANALOG SUPPLY CURRENT vs. TEMPERATURE



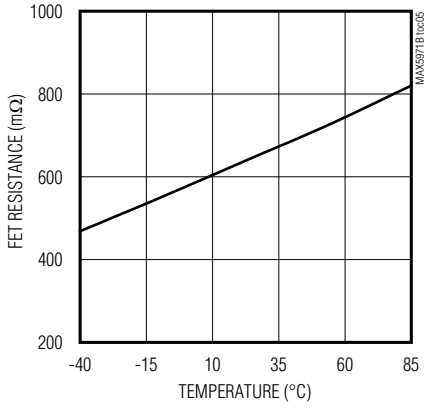
VEE UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



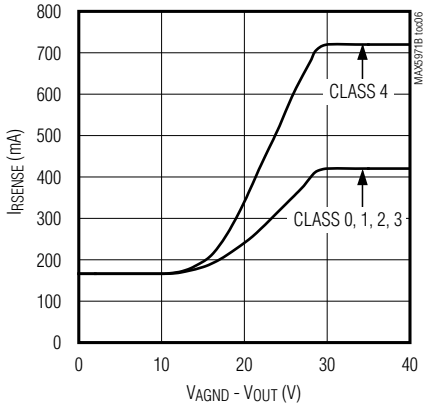
VEE OVERVOLTAGE LOCKOUT vs. TEMPERATURE



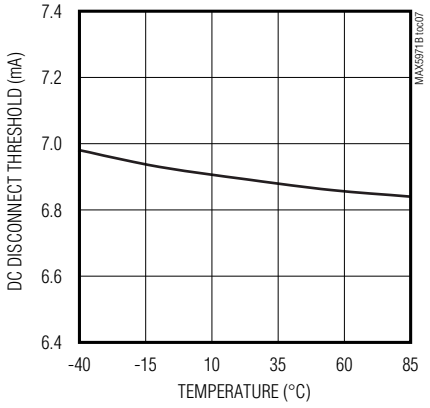
INTERNAL FET RESISTANCE vs. TEMPERATURE



FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



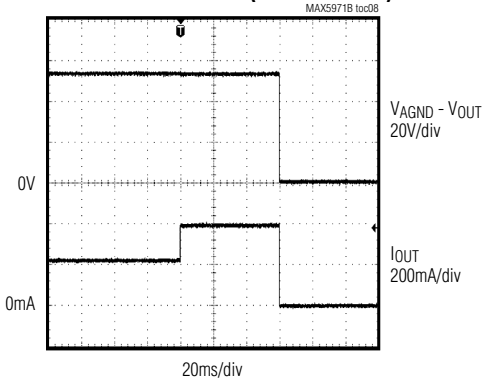
DC DISCONNECT THRESHOLD vs. TEMPERATURE



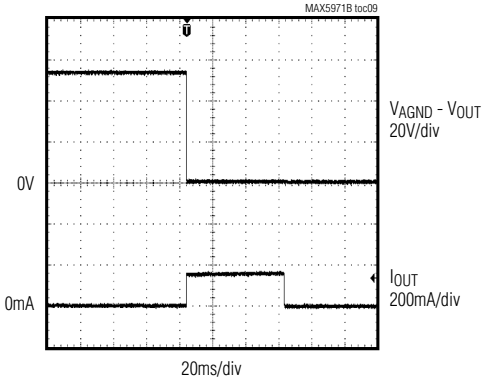
Typical Operating Characteristics (continued)

(V_{AGND} = 54V, V_{EE} = V_{EE_DIG} = 0V, T_A = +25°C, endpoint mode and default register settings with a Class 0 PD, unless otherwise otherwise noted.)

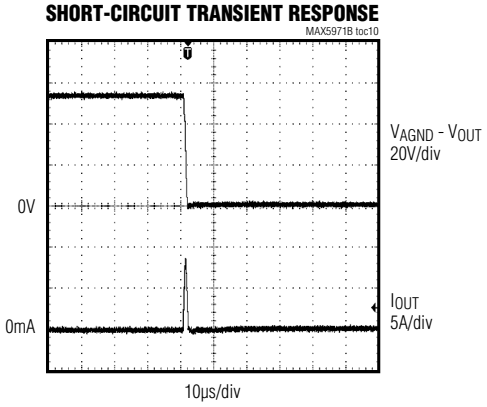
OVERCURRENT TIMEOUT (240Ω TO 138Ω)



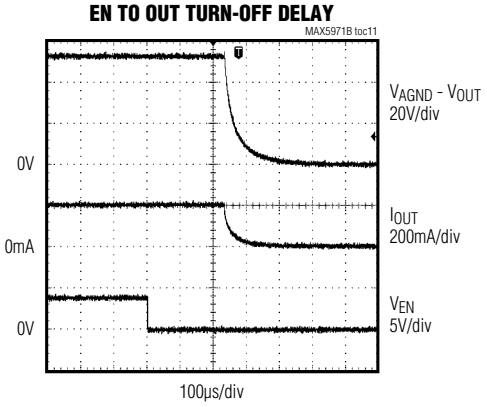
SHORT-CIRCUIT RESPONSE TIME



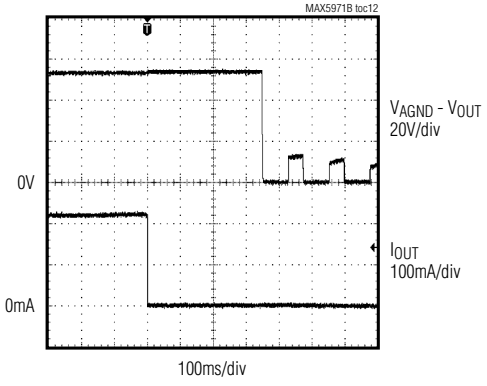
SHORT-CIRCUIT TRANSIENT RESPONSE



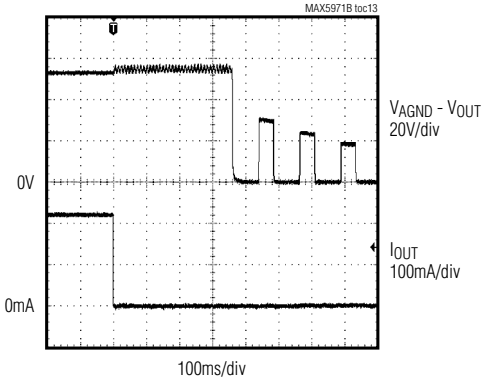
EN TO OUT TURN-OFF DELAY



ZERO-CURRENT DETECTION WAVEFORM WITH DC DISCONNECT ENABLED



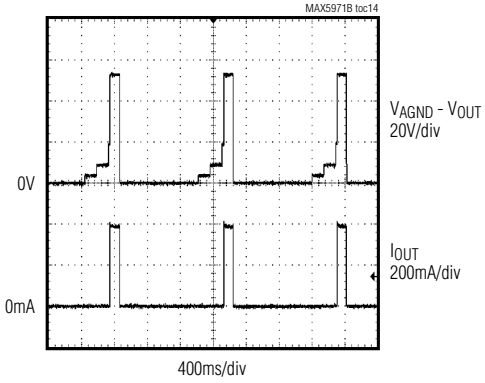
ZERO-CURRENT DETECTION WAVEFORM WITH AC DISCONNECT ENABLED



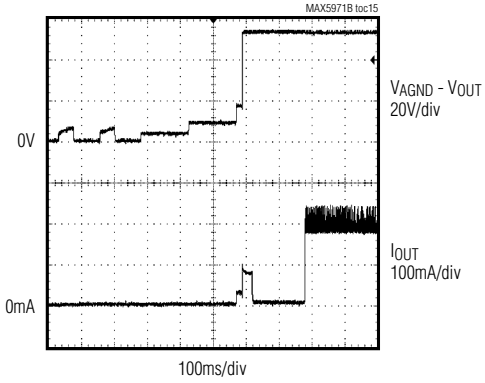
Typical Operating Characteristics (continued)

(V_{AGND} = 54V, V_{EE} = V_{EE_DIG} = 0V, T_A = +25°C, endpoint mode and default register settings with a Class 0 PD, unless otherwise otherwise noted.)

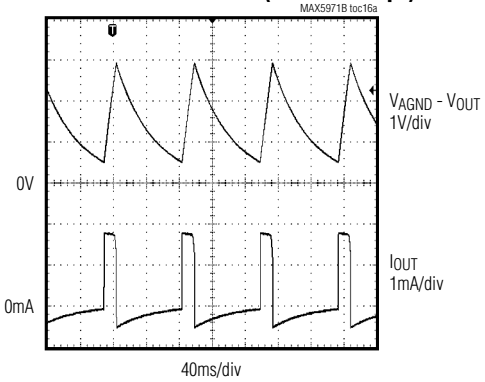
OVERCURRENT RESTART DELAY



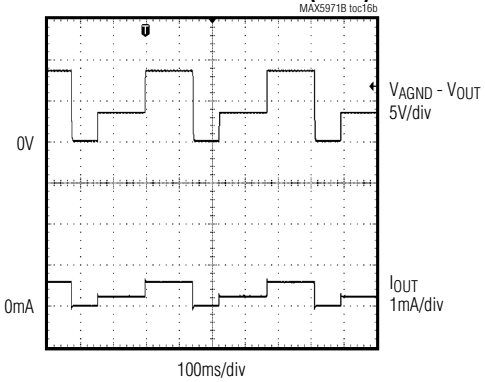
STARTUP WITH A VALID PD



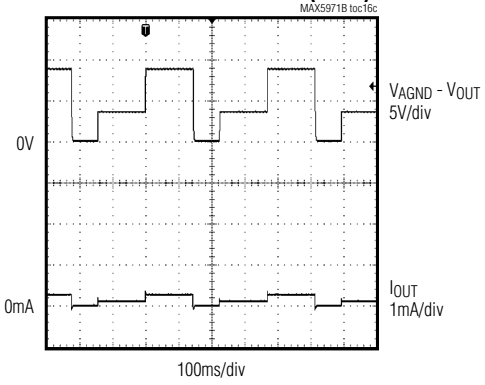
DETECTION WITH INVALID PD (25kΩ AND 10µF)



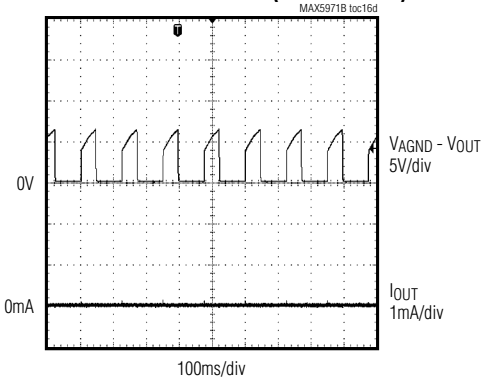
DETECTION WITH INVALID PD (15kΩ)



DETECTION WITH INVALID PD (33kΩ)



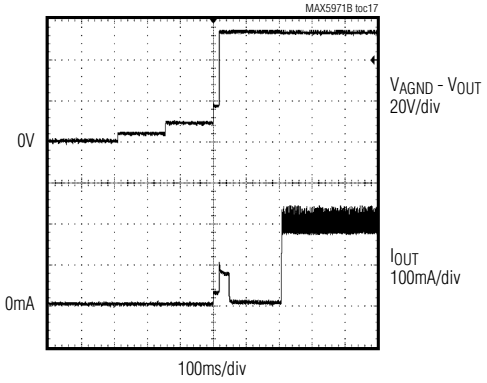
DETECTION WITH INVALID PD (OPEN CIRCUIT)



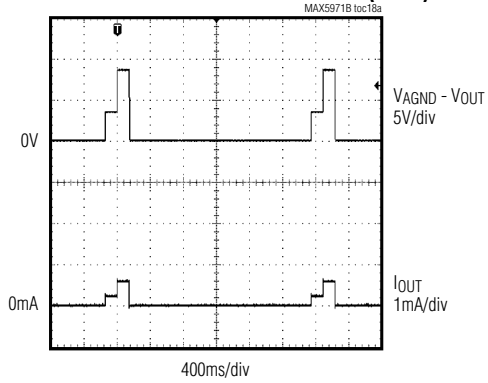
Typical Operating Characteristics (continued)

(V_{AGND} = 54V, V_{EE} = V_{EE_DIG} = 0V, T_A = +25°C, endpoint mode and default register settings with a Class 0 PD, unless otherwise otherwise noted.)

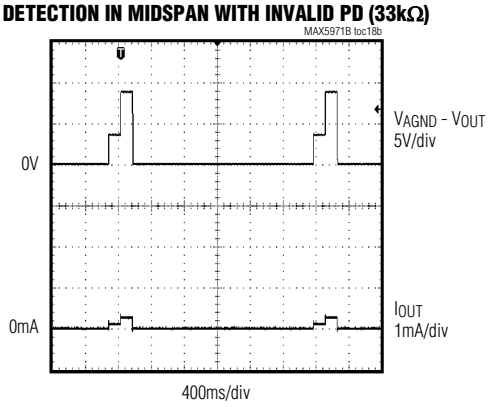
STARTUP IN MIDSPAN WITH A VALID PD



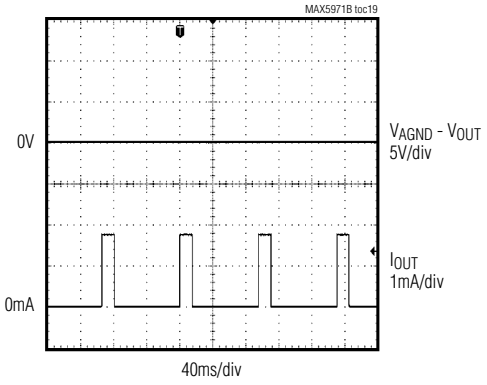
DETECTION IN MIDSPAN WITH INVALID PD (15kΩ)



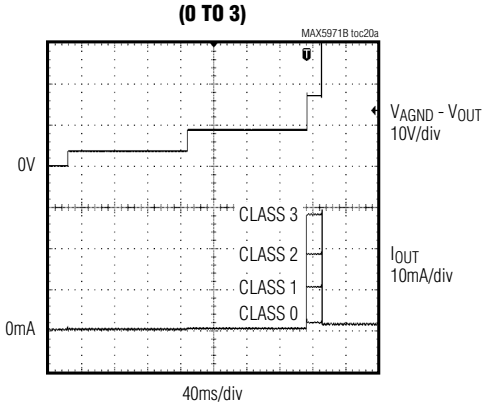
DETECTION IN MIDSPAN WITH INVALID PD (33kΩ)



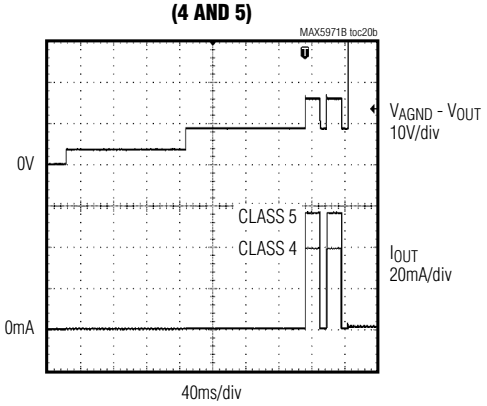
DETECTION WITH OUTPUT SHORTED TO AGND



CLASSIFICATION WITH DIFFERENT PD CLASSES (0 TO 3)



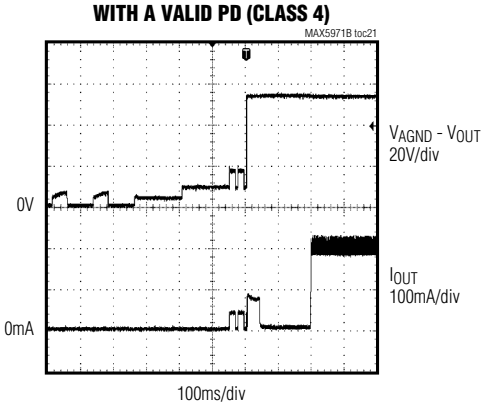
CLASSIFICATION WITH DIFFERENT PD CLASSES (4 AND 5)



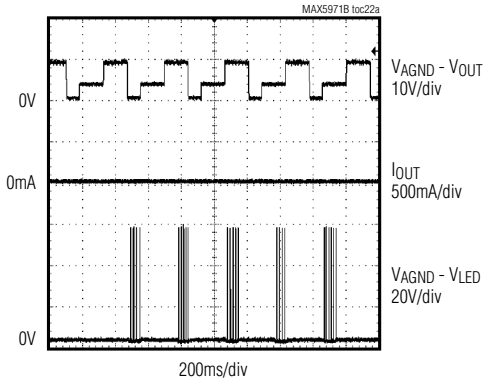
Typical Operating Characteristics (continued)

(V_{AGND} = 54V, V_{EE} = V_{EE_DIG} = 0V, T_A = +25°C, endpoint mode and default register settings with a Class 0 PD, unless otherwise otherwise noted.)

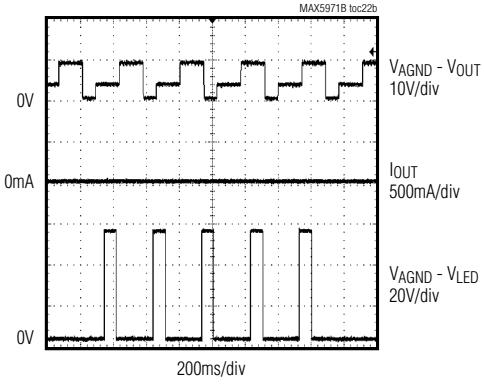
STARTUP USING 2-EVENT CLASSIFICATION WITH A VALID PD (CLASS 4)



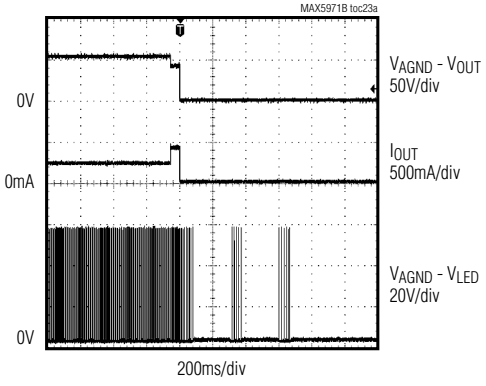
LED DETECTION FAULT WITH PWM ENABLED



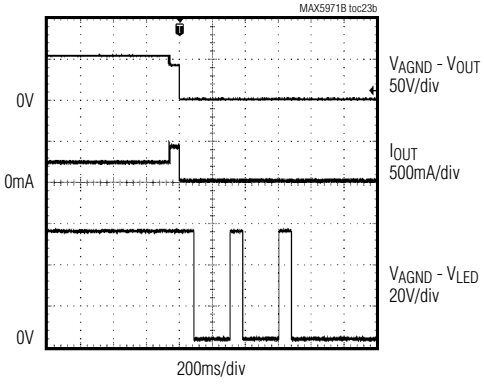
LED DETECTION FAULT WITH PWM DISABLED



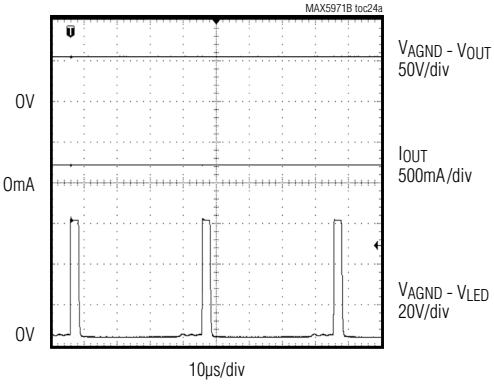
LED OVERCURRENT FAULT WITH PWM ENABLED



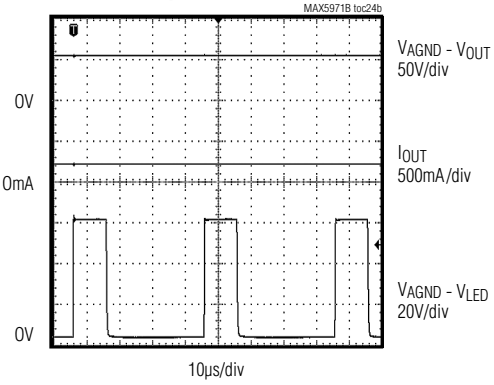
LED OVERCURRENT FAULT WITH PWM DISABLED



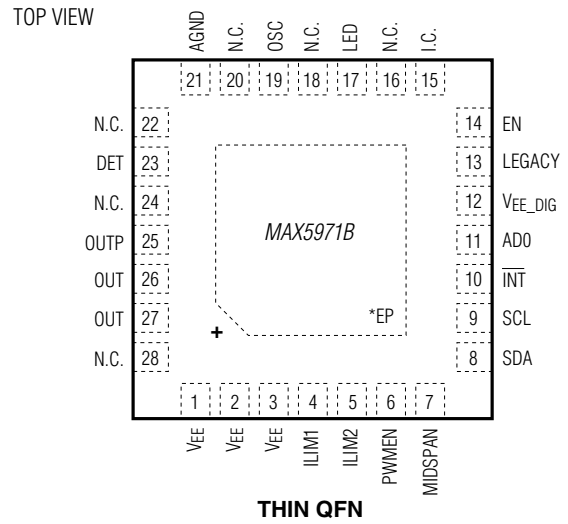
LED PWM TIMING: MINIMUM DUTY CYCLE (DEFAULT)



LED PWM TIMING: MAXIMUM DUTY CYCLE (PROGRAMMABLE)



Pin Configuration



THIN QFN

*CONNECT TO V_{EE}.

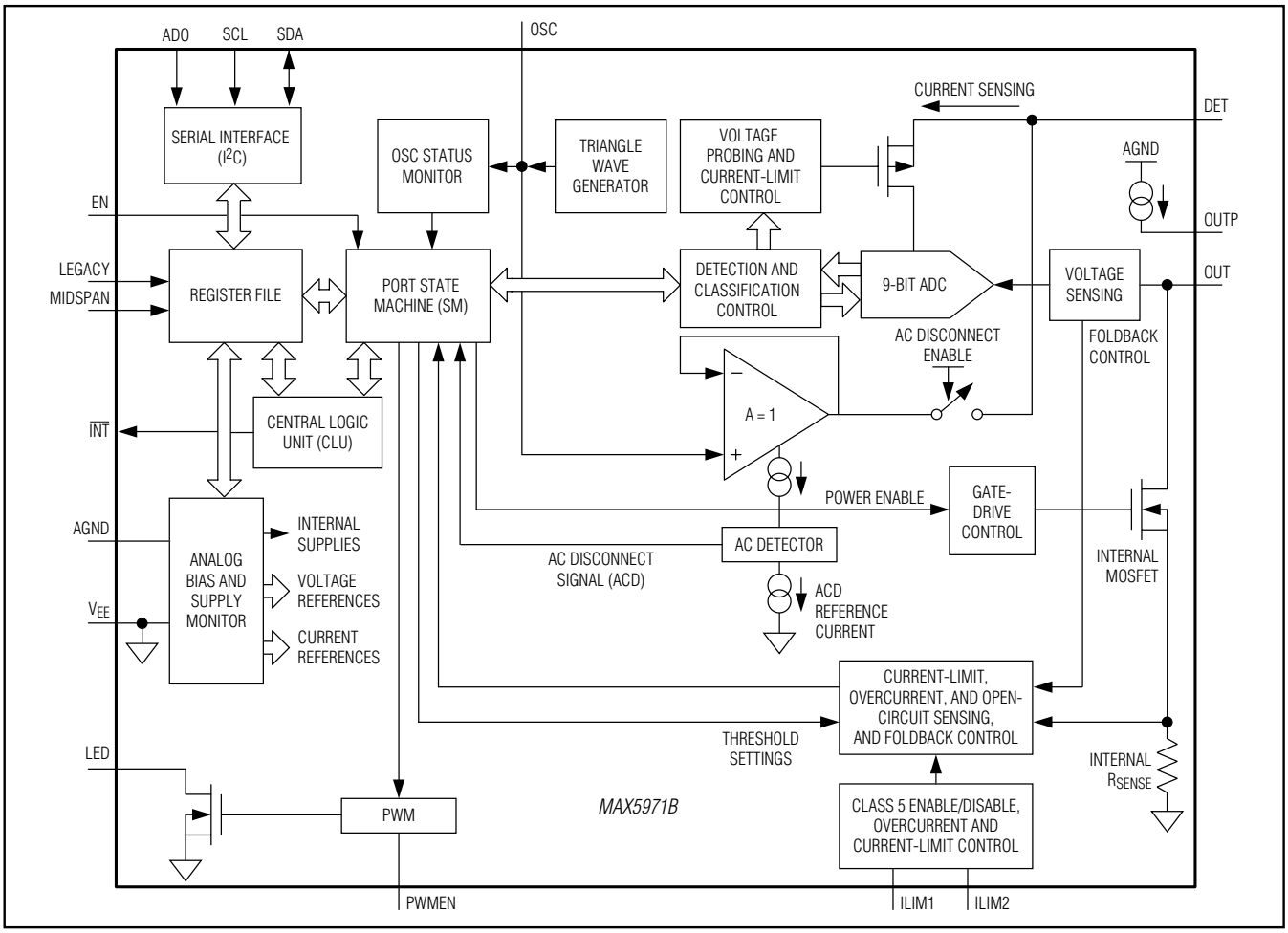
Pin Description

PIN	NAME	FUNCTION
1, 2, 3	V_{EE}	Analog Low-Side Supply Input. Bypass with an external 100V, 47µF capacitor in parallel with a 100V, 0.1µF ceramic capacitor between AGND and V_{EE}.
4	ILIM1	Class 5 Current-Limit Digital Adjust 1. Referenced to V_{EE}. ILIM1 is internally pulled up to the digital supply. Use ILIM1 with ILIM2 to enable Class 5 operation and to adjust the Class 5 current-limit value. See the *Electrical Characteristics* table and Table 3 in the *Class 5 PD Classification* section for details.
5	ILIM2	Class 5 Current-Limit Digital Adjust 2. Referenced to V_{EE}. ILIM2 is internally pulled up to the digital supply. Use ILIM2 with ILIM1 to enable Class 5 operation and to adjust the Class 5 current-limit value. See the *Electrical Characteristics* table and Table 3 in the *Class 5 PD Classification* section for details.
6	PWMEN	PWM Control Logic Input. Referenced to V_{EE}. PWMEN is internally pulled up to the digital supply. Leave unconnected to enable the internal PWM to drive the LED pin. Force low to disable the internal PWM.
7	MIDSPAN	Detection Collision Avoidance Logic Input. Referenced to V_{EE}. MIDSPAN is internally pulled up to the digital supply. Leave unconnected to activate the detection collision avoidance circuitry for midspan PSE systems. Force low to disable this function for an end-point PSE system. The MIDSPAN logic level latches after the device is powered up or after a reset condition.
8	SDA	2-Wire Serial Interface Input/Output Data Line. Referenced to V_{EE}. Connect to V_{EE} if the I^2C interface is not used.

Pin Description (continued)

PIN	NAME	FUNCTION
9	SCL	2-Wire Serial Interface Input Clock Line. Referenced to V_{EE}. Connect to V_{EE} if the I^2C interface is not used.
10	$\overline{INT}$	Open-Drain Interrupt Output. Referenced to V_{EE}. $\overline{INT}$ is pulled low whenever an interrupt is sent to the microcontroller. See the *Interrupt* section for details. Connect to V_{EE} if the I^2C interface is not used.
11	AD0	Address Input. Referenced to V_{EE}. AD0 is used to form the lower part of the device address. See the *Device Address (AD0)* section and Table 5 for details. Connect to V_{EE} if the I^2C interface is not used.
12	V_{EE_DIG}	Digital Low-Side Supply Input. Connect to V_{EE} externally.
13	LEGACY	Legacy Detection Logic Input. Referenced to V_{EE}. LEGACY is internally pulled up to the digital supply. Leave unconnected to activate the legacy PD detection. Force low to disable this function. The LEGACY logic level latches after the device is powered up or after a reset condition.
14	EN	Enable Input. Referenced to V_{EE}. EN is internally pulled up to the digital supply. Leave unconnected to enable the device. Force low for at least 40µs to reset the device. The MIDSPAN, OSC, and LEGACY states latch-in when the reset condition is removed (low-to-high transition). Bypass EN to V_{EE} with a 1nF ceramic capacitor.
15	I.C.	Internally Connected. Connect I.C. to V_{EE}.
16, 18, 20, 22, 24, 28	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.
17	LED	LED Indicator Open-Drain Output. Referenced to V_{EE}. LED can sink 10mA and can drive an external LED directly. Blinking functionality is provided to signal different conditions (see the *PWM and LED Signals* section). Connect LED to AGND externally (see Figures 15 and 16) or to an external supply (if available) through a series resistance.
19	OSC	AC-Disconnect Triangular Wave Output. Bypass with a 100nF (±10% tolerance) external capacitor to V_{EE} to enable the AC disconnect function. Connect OSC to V_{EE} to disable the AC disconnect function and to activate the DC disconnect function. The OSC state latches after the device is powered up or after a reset condition.
21	AGND	High-Side Supply Input
23	DET	Detection/Classification Voltage Output. DET is used to set the detection and classification probe voltages and for the AC current sensing when using the AC disconnect function. To use the AC disconnect function, place a 1kΩ and 0.47µF RC series in parallel with the external protection diode to OUTP (see Figure 16).
25	OUTP	Port Pullup Output. OUTP is used to pull up the port voltage to AGND when needed. If AC disconnect is used, connect OUTP to the anode of the AC-blocking diode. If AC disconnect is not used, connect OUTP to OUT (see Figures 15 and 17). Bypass OUTP to AGND with a 100V, 0.1µF ceramic capacitor.
26, 27	OUT	Integrated MOSFET Output. If DC disconnect is used, connect the port output to OUTP (see Figures 15 and 17). If the AC disconnect function is used, connect OUT to the cathode of the AC-blocking diode (see Figure 16).
—	EP	Exposed Pad. Connect EP to V_{EE} externally. See the *Layout Procedure* section for details.

Simplified Diagram



Detailed Description

The MAX5971B is a single-port power controller designed for use in IEEE 802.3af/802.3at-compliant PSE. This device provides PD discovery, classification, current limit, and DC and AC load-disconnect detections. The MAX5971B supports both fully automatic operation and software programmability, and features an integrated power MOSFET and sense resistor. The device also supports new Class 5 and 2-event classification for detection and classification of high-power PDs. The MAX5971B provides up to 40W to a single port (Class 5 enabled), and still provides high-capacitance detection for legacy PDs.

The MAX5971B features an I2C-compatible, 2-wire serial interface, and is fully software configurable and programmable. The device provides instantaneous readout of port current through the I2C interface. The MAX5971B provides input undervoltage lockout (UVLO), input undervoltage detection, input overvoltage lockout, overtemperature protection, output voltage slew-rate limit during startup, and LED status indication. The MAX5971B programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

Reset

The MAX5971B is reset by any of the following conditions:

1) Power-Up. Reset condition is cleared once V_{EE} rises above the UVLO threshold.
2) Hardware Reset. Reset occurs once the EN input is driven low (> 40µs, typ) any time after power-up. The device exits the reset condition once the EN input is driven high again.

3) Software Reset. To initiate a software reset, write a logical 1 to the RESET_IC register (R1Ah[4]) any time after power-up. Reset clears automatically and all registers are set to their default states.
4) Thermal Shutdown. The device enters thermal shutdown at 150°C. The device exits thermal shutdown and is reset once the temperature drops below 130°C.

At the end of a reset event, the MAX5971B latches in the state of MIDSPAN, LEGACY, and OSC. During normal operation, changes to the MIDSPAN and LEGACY inputs are ignored, and these inputs can be changed at any time prior to the end of a reset state. Changes to OSC input during normal operation can impact device functionality. Therefore, OSC is only changed while the device is held in a reset state (or powered down), and OSC then latches in when the reset state ends (other schematic modifications may be needed, see Figures 15 and 16).

Port Reset

Set RESET_P (R1Ah[0]) high anytime during normal operation to turn off port power and clear the port event and status registers. Port reset does not initiate a global device reset.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the port waits between 2s and 2.4s before attempting to detect again. Midspan mode is activated by setting MIDSPAN high and then powering or resetting the device. Alternatively, midspan mode is software enabled by setting BCKOFF (R15h[0], Table 23) to a logical 1. By default, the MIDSPAN input is internally pulled high, enabling cadence timing. Force MIDSPAN low to disable this function.

Operation Modes

The MAX5971B provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies a device connected to the port after initial software activation, but does not power up the port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the port.

Switching between auto, semiautomatic, and manual mode does not interfere with the operation of the output port. When the port is set into shutdown mode, all port operations are immediately stopped and the port remains idle until shutdown mode is exited.

Auto (Automatic) Mode

By default, the MAX5971B enters auto mode after the reset condition is cleared. To manually place the MAX5971B into auto mode from any other mode, set P_M[1:0] (R12h[1:0]) to [11] during normal operation (see Tables 19 and 20).

In auto mode, the MAX5971B performs detection and classification, and powers up the port automatically if a valid PD is connected to the port. If a valid PD is not connected at the port, the MAX5971B repeats the detection routine continuously until a valid PD is connected.

When entering auto mode, the DET_EN and CLASS_EN bits (R14h[0] and R14h[4], Table 22) are set to high and stay high unless changed by software. Using software to set DET_EN and/or CLASS_EN low causes the MAX5971B to skip detection and/or classification. As a protection, disabling the detection routine in auto mode does not allow the corresponding port to power up, unless the DET_BY bit (R23h[4], Table 33) is set to 1.

Semiautomatic (Semi) Mode

The MAX5971B is put into semiautomatic mode by setting P_M[1:0] (R12h[1:0]) to [10] during normal operation (see Tables 19 and 20). In semi mode, the MAX5971B, upon request, performs detection and/or classification repeatedly but does not power up the port. To power the port, set the PWR_ON bit (R19h[0], Table 27) to 1. This immediately terminates the detection/classification routine and turns on power to the port.

DET_EN and CLASS_EN (R14h[0] and R14h[4], Table 22) default to low in semiautomatic mode. Use software to set DET_EN (R14h[0]) to 1 to start the detection routine and CLASS_EN (R14h[4]) to 1 to enable classification routine. They are reset every time the software commands a power-off of the port, either through a reset event or by writing a 1 to the PWR_OFF bit (R19h[4]). In any other case, the status of the bits is left unchanged (including when the state machine turns off the power when a load disconnect or a fault condition is encountered).

Manual Mode

The MAX5971B is placed in manual mode by setting P_M[1:0] (R12h[1:0]) to [01] during normal operation (see Tables 19 and 20). Manual mode allows the software to dictate the sequence of operation. Write a 1 to both R14h[0] (DET_EN) and R14h[4] (CLASS_EN) to start detection and classification operations, respectively, and in that priority order. In manual mode, after

execution, the command is cleared from the register(s). PWR_ON has highest priority. Setting PWR_ON to 1 at any time causes the device to immediately enter the powered mode. Setting DET_EN and CLASS_EN to 1 at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN or CLASS_EN commands.

When switching to manual mode from another mode, DET_EN and CLASS_EN default to low. These bits become pushbutton rather than configuration bits. Writing 1 to these bits while in manual mode commands the device to execute one cycle of detection and/or classification. They are reset back to 0 at the end of the execution.

Shutdown Mode

To put the MAX5971B into shutdown mode, set P_M[1:0] (R12h[1:0]) to [00] during normal operation (see Table 19 and Table 20). Putting the MAX5971B into shutdown mode immediately turns off port power, clears the event and status bits, and halts all port operations. In shutdown mode the serial interface is still fully active, however, all DET_EN, CLASS_EN, and PWR_ON commands are ignored.

PD Detection

During normal operation, the MAX5971B probes the output for a valid PD. A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af/802.3at standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature.

After each detection cycle, the MAX5971B sets DET_END (R04h[0] and R05h[0]) to 1 and reports the detection results in the detection status bits, DET_ST[2:0] (R0Ch[2:0], see Table 14). The DET_END registers are reset to 0 when read through the CoR (clear-on-read) register R05h[0], or after a reset event.

During detection, the MAX5971B keeps the internal MOSFET off and forces two probe voltages through DET. The current through DET is measured as well as the voltage at OUT. A two-point slope measurement is used, as specified by the IEEE 802.3af/802.3at standard, to verify the device connected to the port. By default, The MAX5971B load stability check is disabled. Set LSC_EN (R29h[4], Table 36) to 1 to enable the load stability check. The MAX5971B implements appropriate settling times to reject 50Hz/60Hz power-line noise coupling.

An external diode, in series with the DET input, restricts PD detection to the first quadrant as specified by the IEEE 802.3af/802.3at standard. To prevent damage to non-PD devices, and to protect itself from an output short circuit, the MAX5971B limits the current into DET to less than 2mA (max) during PD detection.

In midspan mode, after every failed detection cycle, the MAX5971B waits at least 2.0s before attempting another detection cycle. The first detection, however, still happens immediately after exiting a reset condition.

High-Capacitance Detection

High-capacitance detection for legacy PDs is both software and pin programmable (LEGACY). To use software to enable high-capacitance detection, set CLC_EN (R23h[5]) to 1 during normal operation. Alternatively, the status of the LEGACY input is latched and written to CLC_EN during power-up or after reset condition is cleared. The LEGACY input is internally pulled

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}		30	V	In detection mode only
Short-Circuit Current	I_{SC}		5	mA	In detection mode only
Valid Test Voltage	V_{VALID}	2.8	10	V	
Voltage Difference Between Test Points	ΔV_{TEST}	1		V	
Time Between Any Two Test Points	t_{BP}	2		ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	V_{SLEW}		0.1	V/µs	
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	
Open-Circuit Resistance	R_{OPEN}	500		kΩ	
Accept Signature Capacitance	C_{GOOD}		150	nF	
Reject Signature Capacitance	C_{BAD}	10		µF	
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	
Signature Offset Current Tolerance	I_{OS}	0	12	µA	

high, enabling high-capacitance detection. Unless high-capacitance detection is needed, connect LEGACY to V_{EE} to disable this function. If high-capacitance detection is enabled, PD signature capacitances up to 47µF (typ) are accepted.

Powered Device Classification (PD Classification)

During PD classification, the MAX5971B forces a probe voltage (-18V, typ) at DET and measures the current into DET. The measured current determines the class of the PD.

After each classification cycle, the MAX5971B sets CL_END (R04h[4] and R05h[4]) to 1 and reports the classification results in the classification status bits, CLASS[2:0] (R0Ch[6:4], see Table 14). The CL_END "registers are reset to 0 when read through the CoR (clear- on-read) register, R05h, or after a reset event.

If ILIM1 and ILIM2 are both left unconnected, the MAX5971B classifies the PD based on Table 33.9 of the IEEE 802.3at standard (see Table 2). If the measured current exceeds 51mA, the MAX5971B does not power the PD, but returns to idle state before attempting a new detection cycle.

Table 2. PSE Classification of a PD (Table 33.9 of the IEEE 802.3at Standard)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	Can be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

Class 5 PD Classification

The MAX5971B supports high power beyond the IEEE 802.3at standard by providing an additional classification (Class 5) if needed. To enable Class 5 detection and select the corresponding current-limit/overcurrent thresholds, ILIM1 and ILIM2 must be set based on the combinations detailed in Table 3. Once Class 5 is enabled, during classification, if the MAX5971B detects currents in excess of the Class 4 upper limit threshold, the PD is classified as a Class 5 powered device. The PD is guaranteed to be classified as a Class 5 device for any classification current from 51mA up to the classification current-limit threshold.

The Class 5 overcurrent threshold and current limit is set with ILIM1 and ILIM2. ILIM1 and ILIM2 are both referenced to V_{EE} and are internally pulled up to the digital supply. Leave ILIM1 and ILIM2 unconnected to disable Class 5 detection and to be fully compliant to IEEE 802.3at standard classification. Class 5 detection is enabled, and the corresponding overcurrent threshold and current limit is adjusted, by connecting one or both to V_{EE} (see Table 3).

2-Event PD Classification

If the result of the first classification event is Class 0 through Class 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 or Class 5 (when enabled), the device performs a second classification event as shown in Figure 2. Between the classification cycles, the MAX5971B performs a first and second mark event as required by the IEEE 802.3at standard, forcing a -9.3V probing voltage at DET.

Table 3. Class 5 Overcurrent Threshold and Current-Limit Settings

ILIM1 CONFIGURATION	ILIM2 CONFIGURATION	OVERCURRENT THRESHOLD (mA)	CURRENT LIMIT (mA)
Unconnected	Unconnected	Class 5 disabled	Class 5 disabled
V_{EE}	Unconnected	748	850
Unconnected	V_{EE}	792	900
V_{EE}	V_{EE}	836	950

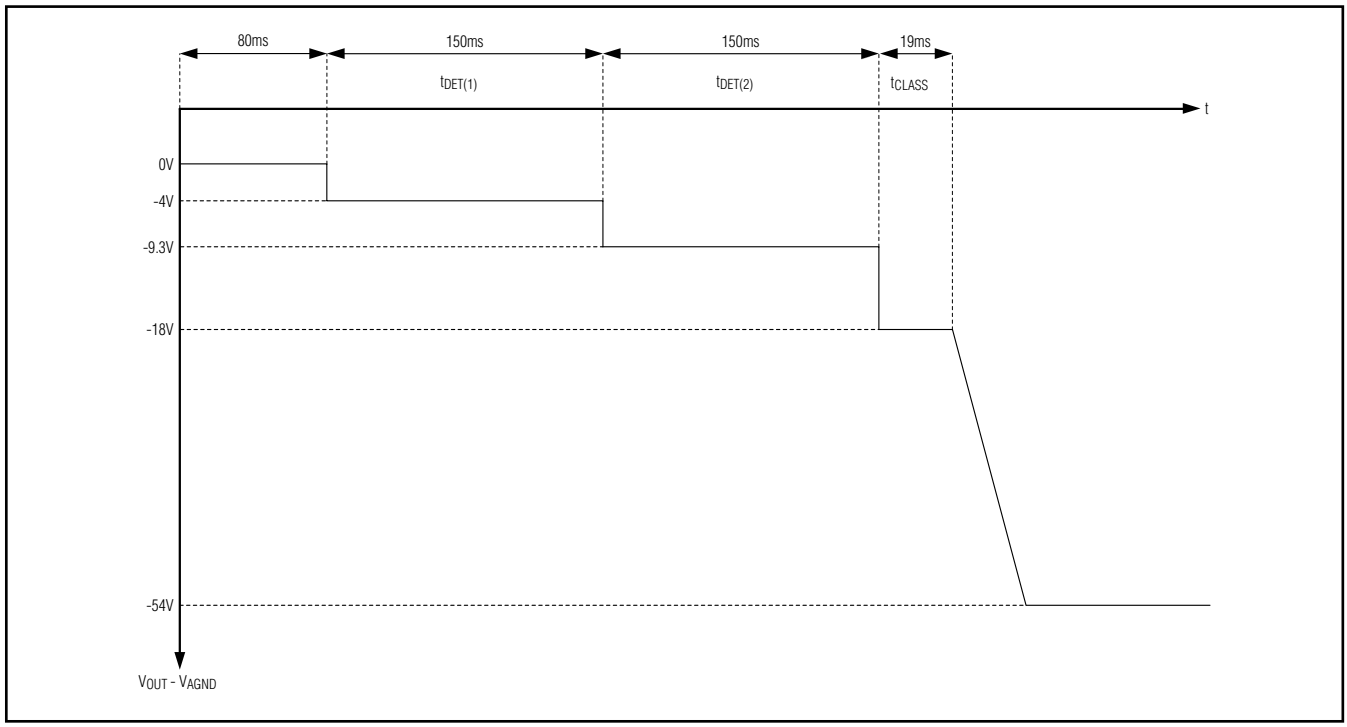


Figure 1. Detection, Classification, and Port Power-Up Sequence

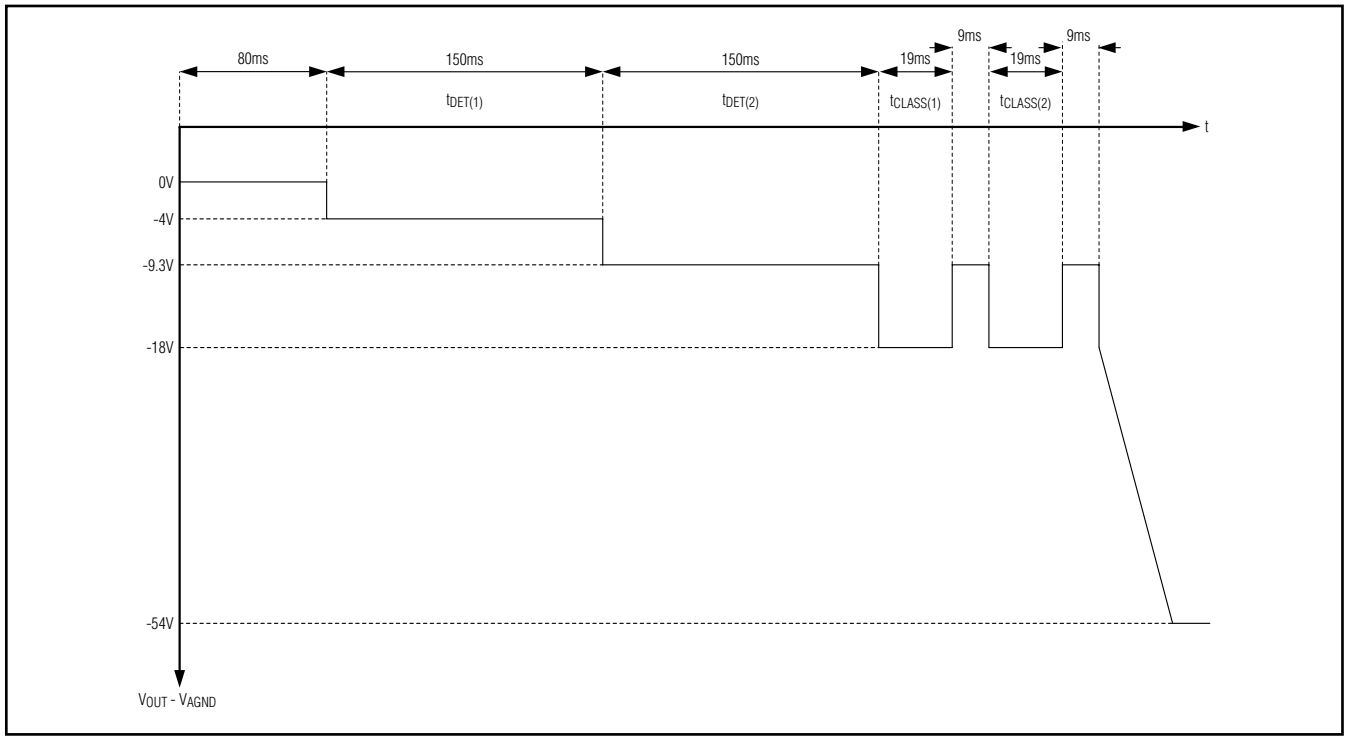


Figure 2. Detection, 2-Event Classification, and Port Power-Up Sequence

Powered State

When the MAX5971B enters a powered state, the t_{FAULT} and t_{DISC} timers are reset. When the startup timer (t_{START}) has timed out, the device enters a normal powered condition, allowing power delivery to the PD. PGOOD (R10h[4], Table 17) is set to 1 when the device enters the normal powered condition. PGOOD immediately resets to 0 whenever the power to the port is turned off. The power-good change bits, PG_CHG (R02h[4] and R03h[4], Table 9) are set both when the port powers up and when it powers down. PWR_EN (R10h[0], Table 17) is set to 1 when the port powers up and resets to 0 when a port shuts down. Set PWR_OFF (R19h[4], Table 27) to 1 to immediately turn off power to the port.

Overcurrent Protection

The MAX5971B has an internal sense resistor, R_{SENSE} (see the *Simplified Diagram*), connected between the source of the internal MOSFET and V_{EE} to monitor the load current. Under normal operating conditions, the current through R_{SENSE} (I_{RSENSE}) never exceeds the threshold I_{LIM}. If I_{RSENSE} exceeds I_{LIM}, an internal current-limiting circuit regulates the gate voltage of the internal MOSFET, limiting the current. During transient conditions, if I_{RSENSE} exceeds I_{LIM} by more than 2A, a fast pulldown circuit activates to quickly recover from the current overshoot.

In the normal powered state, the MAX5971B checks for overcurrent conditions, as determined by I_{CUT} = ~88% of I_{LIM}. The t_{FAULT} counter sets the maximum-allowed continuous overcurrent period. This timer is incremented both in startup and in normal powered state, but under different conditions. During startup it increases when I_{RSENSE} exceeds I_{LIM}, while in the normal powered state the counter increases when I_{RSENSE} exceeds I_{CUT}. It decreases at a slower pace when I_{RSENSE} drops below I_{LIM} or I_{CUT}. A slower decrement for the t_{FAULT} counter allows for detection of repeated short-duration overcurrent events. When the counter reaches the t_{FAULT} limit, the MAX5971B powers down the port and asserts the IMAX_FLT bits (R06h[0] and R07h[0]). For a continuous overstress, a fault occurs exactly after a period of t_{FAULT}. The timing is software programmable through the timing register (R16h, Table 24).

After a power-off due to an overcurrent fault, the t_{FAULT} timer is not immediately reset but starts decrementing. The MAX5971B allows the port to be powered on only when the t_{FAULT} counter reaches zero. This feature sets an automatic port power duty-cycle protection to the internal MOSFET to avoid overheating. Through programmable registers, the MAX5971B allows the rate of decrement to be adjusted or for the restart timeout to be disabled entirely (see Tables 24 and 25).

In the normal powered state, the I_{LIM} and I_{CUT} thresholds are set automatically according to the classification result (see Table 4 for classification results based on detection current, and the *Electrical Characteristics* table for the corresponding thresholds). The thresholds can also be set manually by programming the ICUT register (R2Ah[2:0]). During startup, I_{LIM} is always set to 420mA regardless of the detected class.

The ICUT Register

The ICUT register determines the maximum current limit allowed for the MAX5971B during the powered state. The ICUT bits (R2Ah[2:0]) allow manual programming of the current limit (I_{LIM}) and overcurrent (I_{CUT}) thresholds (see Tables 37 and 38). The ICUT register can be written to directly through the I²C interface when the automatic ICUT programming bit, CL_DISC (R17h[2]), is set to 1 (see Table 4). In this case, the current limit of the port is configured regardless of the status of the classification. By setting the CL_DISC bit to 0 (default), the MAX5971B automatically sets the ICUT register based upon the classification result (see Tables 4, 37, and 38 in the *Register Map and Description* section).

Table 4. Automatic ICUT Programming

CL_DISC (R17h[2])	PORT CLASSIFICATION RESULT	ILIM1 SETTING	ILIM2 SETTING	RESULTING ICUT REGISTER BITS (R2Ah[2:0])	CURRENT LIMIT (mA)
1	Any	—	—	User programmed	—
0	0, 1, 2, 3	—	—	ICUT = 000	420
0	4	—	—	ICUT = 001	720
0	5	V_{EE}	Unconnected	ICUT = 101	850
0	5	Unconnected	V_{EE}	ICUT = 110	900
0	5	V_{EE}	V_{EE}	ICUT = 111	950

Foldback Current

During startup and normal operation, an internal circuit senses the port voltage and reduces the current-limit value and the overcurrent threshold when (V_{AGND} - V_{OUT}) < 27V. The foldback function helps to reduce the power dissipation on the internal MOSFET. The current limit eventually reduces down to I_{TH_FB} (166mA, typ) when (V_{AGND} - V_{OUT}) < 10V (see Figure 3).

Digital Logic

The MAX5971B internally generates digital supplies (referenced to V_{EE}) to power the internal logic circuitry. All logic inputs and outputs are referenced to V_{EE}. See the *Electrical Characteristics* table for digital input thresholds. If digital logic inputs are driven externally, the nominal digital logic level is 3.3V.

Interrupt

The MAX5971B contains an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. The interrupt register (R00h, Table 7) contains the interrupt flag bits and the interrupt mask register (R01h, Table 8) determines which events can trigger an interrupt. When an event occurs, the appropriate interrupt event register bits (in R02h through R0Bh) and the corresponding interrupt (in R00h) are set to 1 and $\overline{INT}$ is asserted low (unless masked).

As a response to an interrupt, the controller can read the status of the event register(s) to determine the cause of the interrupt and take appropriate action. Each interrupt event register is paired with a clear-on-read (CoR) register. When an interrupt event register is read through the corresponding CoR register, the interrupt register is reset to 0. $\overline{INT}$ remains low and the interrupt is not reset when the interrupt event register is read through the read-only addresses. For example, to clear a supply event fault, read R0Bh (CoR) not R0Ah (read only, see Table 13). Use the CLR_INT bit (R1Ah[7]) to clear an interrupt, or the RESET_IC (R1Ah[4]) or RESET_P (R1Ah[0]) bit to initiate a software reset (see Table 28).

Undervoltage and Overvoltage Protection

The MAX5971B contains both undervoltage and overvoltage protection features. Table 13 in the *Register Map and Description* section shows a detailed list of the undervoltage and overvoltage protection features. An internal V_{EE} undervoltage lockout (V_{EE_UVLO}) circuit keeps the port off and the MAX5971B in reset until V_{AGND} - V_{EE} exceeds 28.5V (typ) for more than 2.5ms. An internal V_{EE} overvoltage (V_{EE_OV}) circuit shuts down the port when V_{AGND} - V_{EE} exceeds 62.5V (typ). The MAX5971B also features a V_{EE} undervoltage interrupt (V_{EE_UV}) that triggers when V_{AGND} - V_{EE} drops below

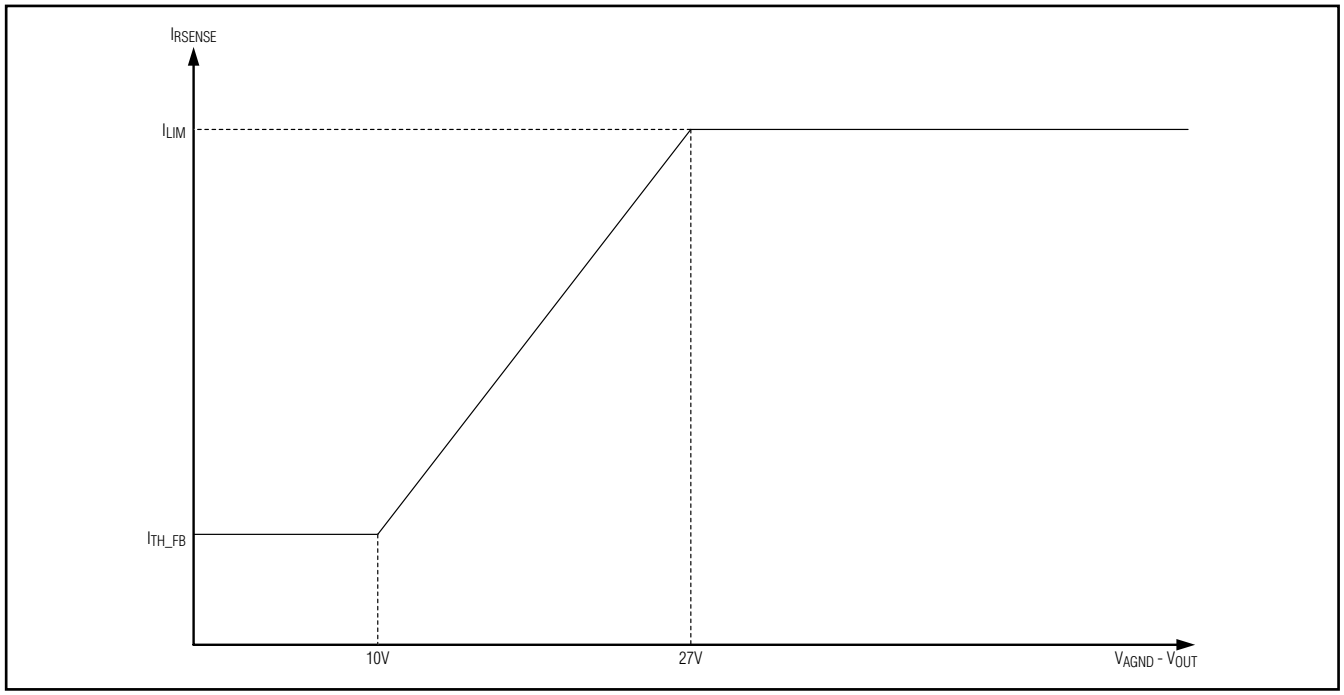


Figure 3. Foldback Current Characteristics

40V (typ). A fault latches into the supply event register V_{EE_UV} (R0Ah[2] and R0Bh[2], Table 13) but the MAX5971B does not power down the port in this case.

DC Disconnect Monitoring

Force OSC to V_{EE} and power or reset the device to activate DC load-disconnect monitoring. DCD_EN (R13h[0]) is set to 1 to enable DC load disconnect. If I_{RSENSE} (the current across R_{SENSE}) falls below the DC load-disconnect threshold, I_{DC_TH}, for more than t_{DISC}, the device turns off port power and sets LD_DISC in the fault event registers (R06h[4] and R07h[4]) to 1.

AC Disconnect Monitoring

The MAX5971B features AC load-disconnect monitoring. Bypass OSC with a 100nF (±10% tolerance) external capacitor to V_{EE} and power or reset the device to automatically enable AC disconnect. ACD_EN (R13h[4]) is set to 1 to enable AC disconnect (the bypass from OSC to V_{EE} must be in place as well). When AC disconnect is enabled, a blocking diode in series to OUT and an RC circuit in parallel to the DET diode must be used, as shown in the typical operating circuit of Figure 16.

The AC disconnect uses an internal triangle-wave generator to supply the probing signal. Then the resulting $4V_{P-P}$ amplitude wave is forced on DET. The common mode of the output signal probed on DET is 5V below AGND. If the AC current peak at DET falls below I_{AC_TH} for more than t_{DISC}, the device powers down the port and asserts LD_DISC (R06h[4] and R07h[4]). The AC load-disconnect threshold (I_{AC_TH}) is programmable using the AC_TH[2:0] bits (R23h[2:0], see Table 33 for settings).

PWM and LED Signals

The MAX5971B includes a multifunction LED driver to inform the user of the port status. LED is an open-drain, multifunction output referenced to V_{EE} and can sink 10mA (typ) while driving an external LED. The LED is turned on when the port is connected to a valid PD and powered. If the port is not powered or is disconnected, the LED is off.

For two other conditions, the MAX5971B blinks a code to communicate the port status. A series of two flashes indicates an overcurrent fault occurred during port power-on, and has a timing characteristic detailed by Figure 4. A series of five flashes indicates that during detection an invalid low or high discovery signature resistance was detected, and has a timing characteristic detailed by Figure 5.

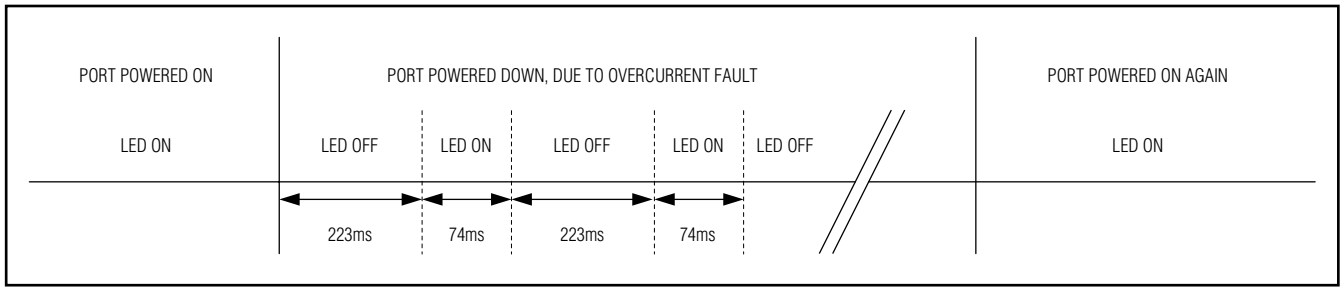


Figure 4. LED Code Timing for Overcurrent Fault During Port Power-On

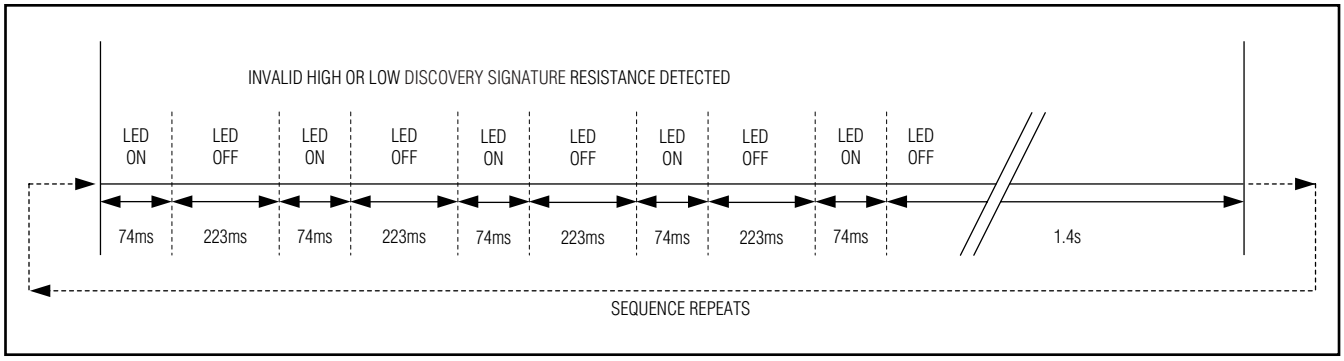


Figure 5. LED Code Timing for Detection Fault Due to High- or Low-Discovery Signature Resistance

The MAX5971B also contains an internal square wave, PWM signal generator. The PWM runs at a typical frequency of 25kHz with a default duty cycle of 6.25%. The duty cycle is programmable from 6.25% up to 25% through the PWM_TH[1:0] bits (R24h[5:4], Tables 34 and 35). PWMEN is used to enable or disable the PWM. PWMEN is internally pulled up to the digital supply, and can be left unconnected to enable the internal PWM. When enabled, the LED pulses are driven by the PWM to reduce the power dissipation and increase the system efficiency. Force PWMEN low to disable the internal PWM; LED is then driven directly.

Thermal Shutdown

If the MAX5971B die temperature reaches +150°C (typ), an overtemperature fault is generated and the device shuts down. The die temperature must cool down below 130°C (typ) to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset.

Watchdog

The R1Eh and R1Fh registers control the watchdog operation. The watchdog function, when enabled, allows the MAX5971B to automatically take over control and securely shut down the power to the port in case of software/firmware crashes. See the *Register Map and Description* section for register configuration and settings (Tables 30, 31, and 32).

Device Address (AD0)

The MAX5971B is programmable to one of four unique slave addresses. To program the device address, connect AD0 to V_{EE}, SCL, SDA or to an external V_{CC} supply referenced to V_{EE}. This external V_{CC} (at AD0) must exceed the digital input logic-high threshold (V_{CC} > 2.4V, see Table 5), but should not exceed 5.5V. An external regulated 3.3V or 5V supply is recommended for V_{CC}.

I²C-Compatible Serial Interface

The MAX5971B operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5971B, and generates the SCL clock that synchronizes the data transfer (see Figure 6).

The MAX5971B SDA line operates as both an input and an output. A pullup resistor, typically 4.7kΩ, may be required on SDA. The MAX5971B SCL line operates only as an input. A pullup resistor may be required (typically 4.7kΩ) on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

Table 5. Programmable Device Address Settings

AD0	DEVICE ADDRESS						
	A7	A6	A5	A4	A3	A2	A1
VEE	0	1	0	0	0	0	0
VCC	0	1	0	0	0	0	1
SCL	0	1	0	0	0	1	0
SDA	0	1	0	0	0	1	1

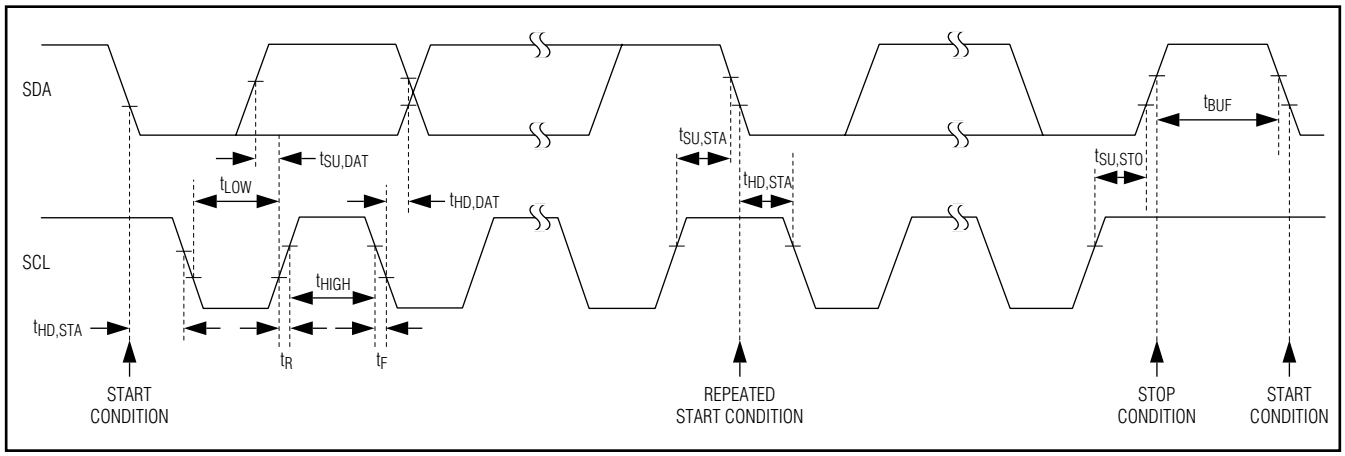


Figure 6. 2-Wire Serial Interface Timing Details

Serial-Addressing

Each transmission consists of a START condition sent by a master, followed by the MAX5971B 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission (see Figure 7).

Bit Transfer

Each clock pulse transfers one data bit (Figure 8). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 9), which the recipient uses to handshake receipt of each byte of data. Thus each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5971B, the device generates the acknowledge bit. When the MAX5971B transmits to the master, the master generates the acknowledge bit.

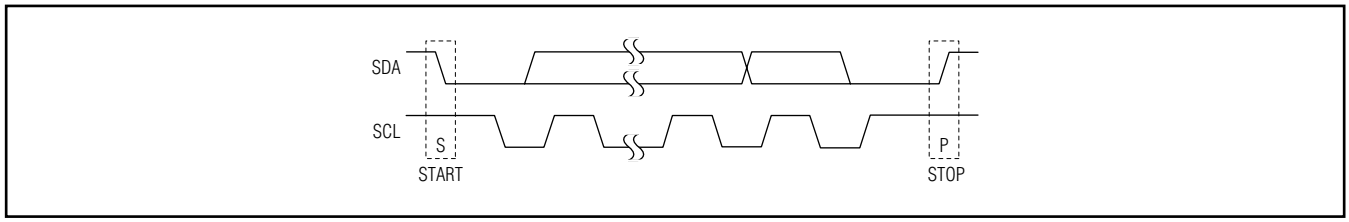


Figure 7. START and STOP Conditions

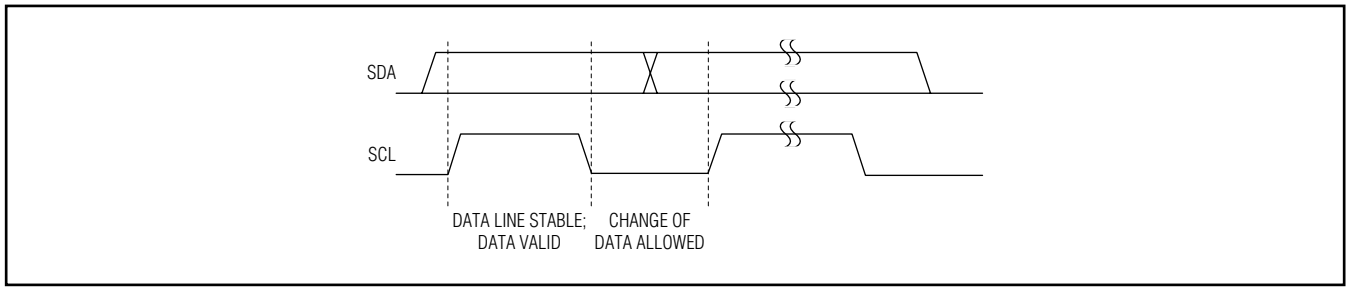


Figure 8. Bit Transfer

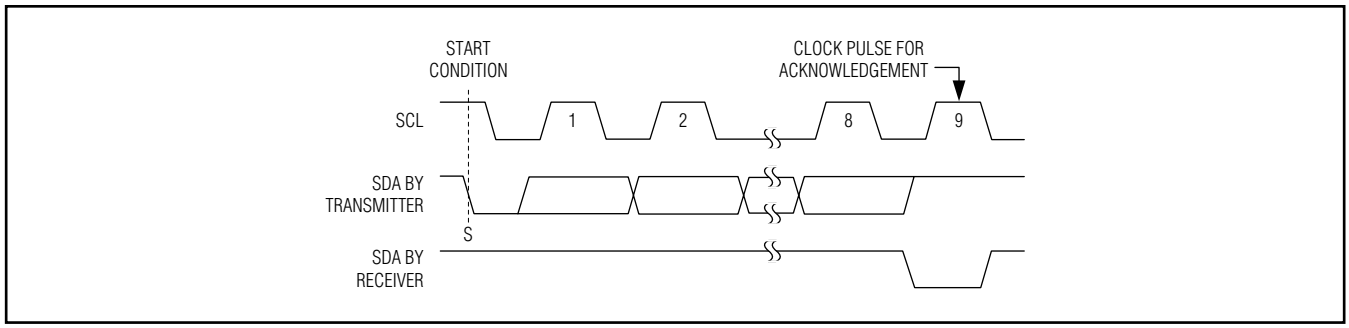


Figure 9. Acknowledge

Slave Address

The MAX5971B has a 7-bit long slave address (Figure 10). The bit following the 7-bit slave address (bit 8) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The upper five bits of the slave address cannot be changed and are always [01000]. Using the AD0 input, the lowest two bits can be programmed to assign the MAX5971B one of 4 unique slave addresses (see Table 5). The MAX5971B monitors the bus continuously, waiting for a START condition followed by the MAX5971B's slave address. When a MAX5971B recognizes its slave address, it acknowledges and is then ready for continued communication.

Global Addressing and Alert Response Protocol

The global address call is used in writing mode to write the same register to multiple devices (address 0x60). In read mode (address 0x61), the global address call is used as the alert response address. When responding to a global call, the MAX5971B puts out on the data line its own address whenever its interrupt is active (as does every other device connected to the SDA line that has an active interrupt). After every bit transmitted, the MAX5971B checks that the data line effectively corresponds to the data it is delivering. If it is not, it then backs off and frees the data line. This litigation protocol always allows the part with the lowest address to complete the transmission. The microcontroller then responds to that interrupt and takes proper action. The MAX5971B does not reset its own interrupt at the end of the alert response protocol. The microcontroller has to do it by clearing the event register through their CoR addresses or activating the CLR_INT pushbutton (R1Ah[7]).

General Call

In compliance with the I2C specification, the MAX5971B responds to the general call through the global address 30h.

Message Format for Writing the MAX5971B

A write to the MAX5971B comprises the device slave address transmission with the R/$\overline{W}$ bit set to 0, followed by at least one byte of information. The first byte of information is the command byte (Figure 11). The command byte determines which register of the MAX5971B is written to by the next byte, if received. If the MAX5971B detects a STOP condition after receiving the command byte but before receiving any data, then the MAX5971B takes no further action beyond storing the command byte.

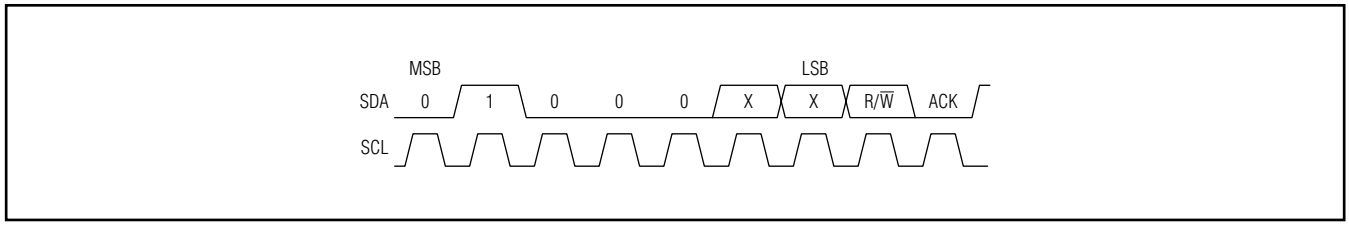


Figure 10. Slave Address

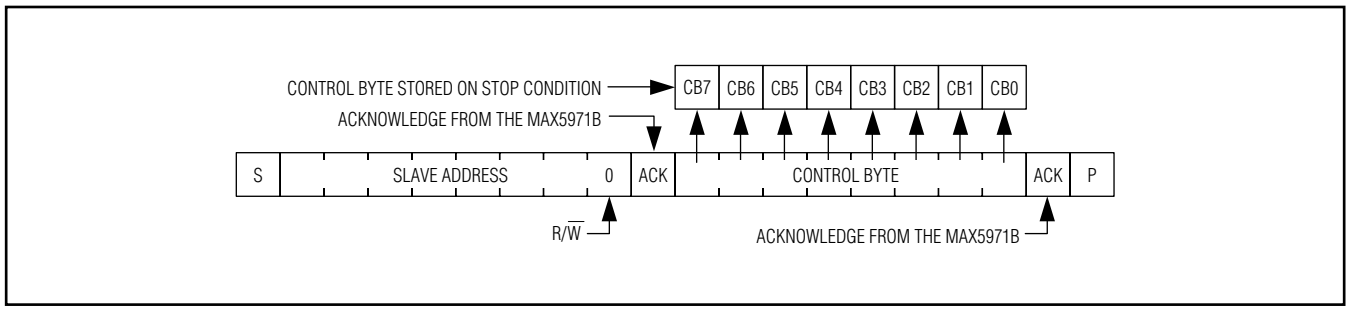


Figure 11. Write Format: Control Byte Received

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX5971B selected by the command byte (Figure 12). The control byte address then autoincrements, if possible (see Table 6), and then waits for the next data byte or a STOP condition.

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are stored in subsequent MAX5971B internal registers as the control byte address autoincrements (Figure 13). If the control byte address can no longer increment, any subsequent data sent continues to write to that address.

Message Format for Reading

A read command for the MAX5971B comprises the device slave address transmission with the R/$\overline{W}$ bit set to 1, followed by at least one byte of information. As with a write command, the first byte of information is the command byte. The MAX5971B then reads using the internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. This pointer autoincrements after reading each data byte using the same rules as for a write, though the master now sends the acknowledge bit after each read receipt (Figure 14). When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address autoincrements after the write.

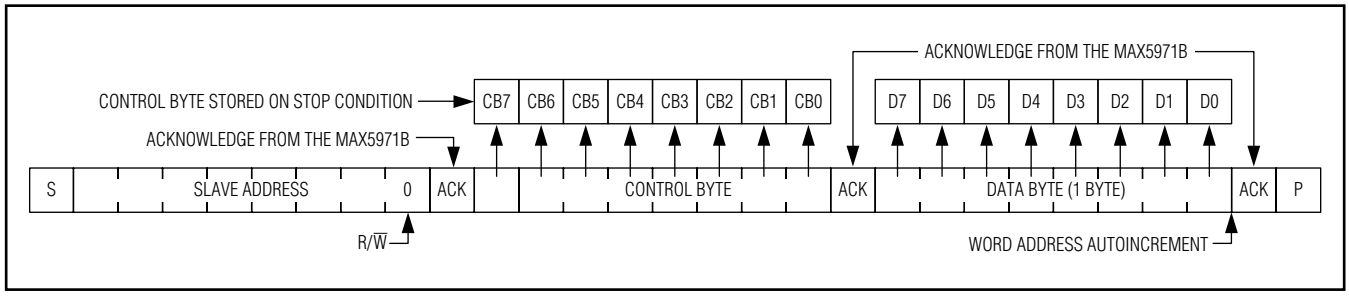


Figure 12. Write Format: Control and Single Data Byte Written

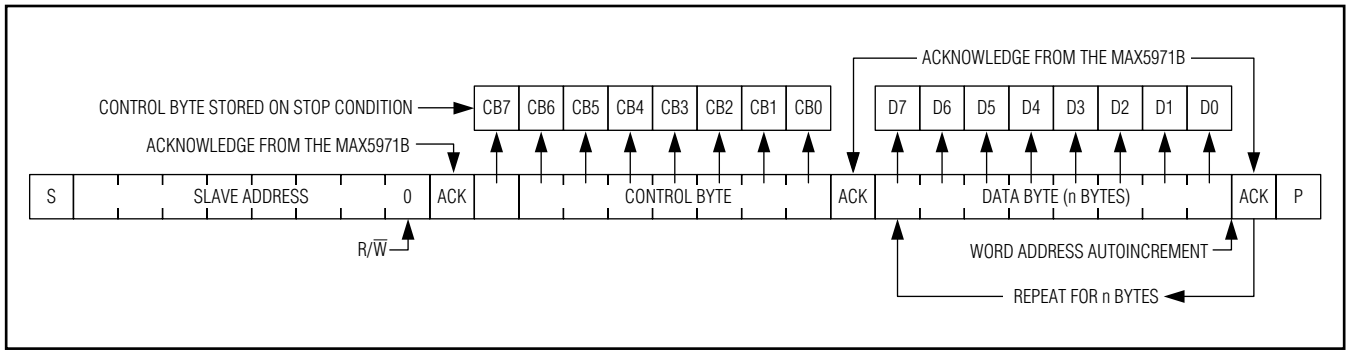


Figure 13. Write Format: Control and n Data Bytes Written

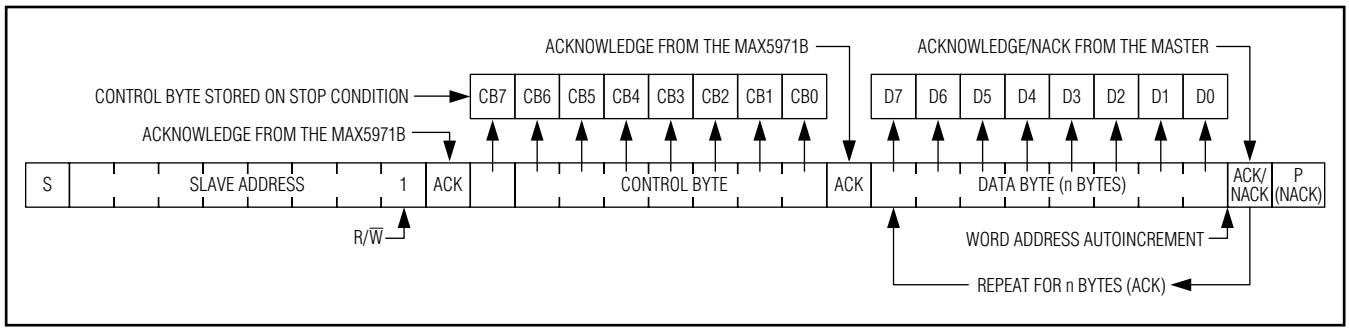


Figure 14. Read Format: Control and n Data Bytes Read