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19-5568; Rev 1; 9/11

Quad, IEEE 802.3at/af PSE Controller for Power-over-Ethernet

General Description

The MAX5980 is a quad, power-sourcing equipment (PSE) power controller designed for use in IEEE® 802.3at/af-compliant PSE. This device provides powered device (PD) discovery, classification, current limit, and load disconnect detection. The device supports both fully automatic operation and software programmability. The device also supports new 2-event classification and Class 5 for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 70W to each port (Class 5 enabled), and still provides high-capacitance detection for legacy PDs.

The device features an I²C-compatible, 3-wire serial interface, and is fully software configurable and programmable. The device provides instantaneous readout of port current and voltage through the I²C interface. The device's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other, nonstandard applications.

The device is available in a space-saving, 32-pin TQFN (5mm x 5mm) power package and is rated for the automotive (-40°C to +105°C) temperature range.

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Features

- **IEEE 802.3at/af Compliant**
- **0.25Ω Current-Sensing Resistor**
- **Up to 70W per Port for PSE Applications**
- **9-Bit Port Current and Voltage Monitoring**
- **I²C-Compatible, 3-Wire Serial Interface**
- **Supports Single-Supply Operation**
- **High-Capacitance Detection for Legacy Devices**
- **Supports DC Load-Removal Detections**
- **Space-Saving, 32-Pin TQFN (5mm x 5mm) Power Package**

Applications

PSE-ICM

Power-Sourcing Equipment (PSE)

Switches/Routers

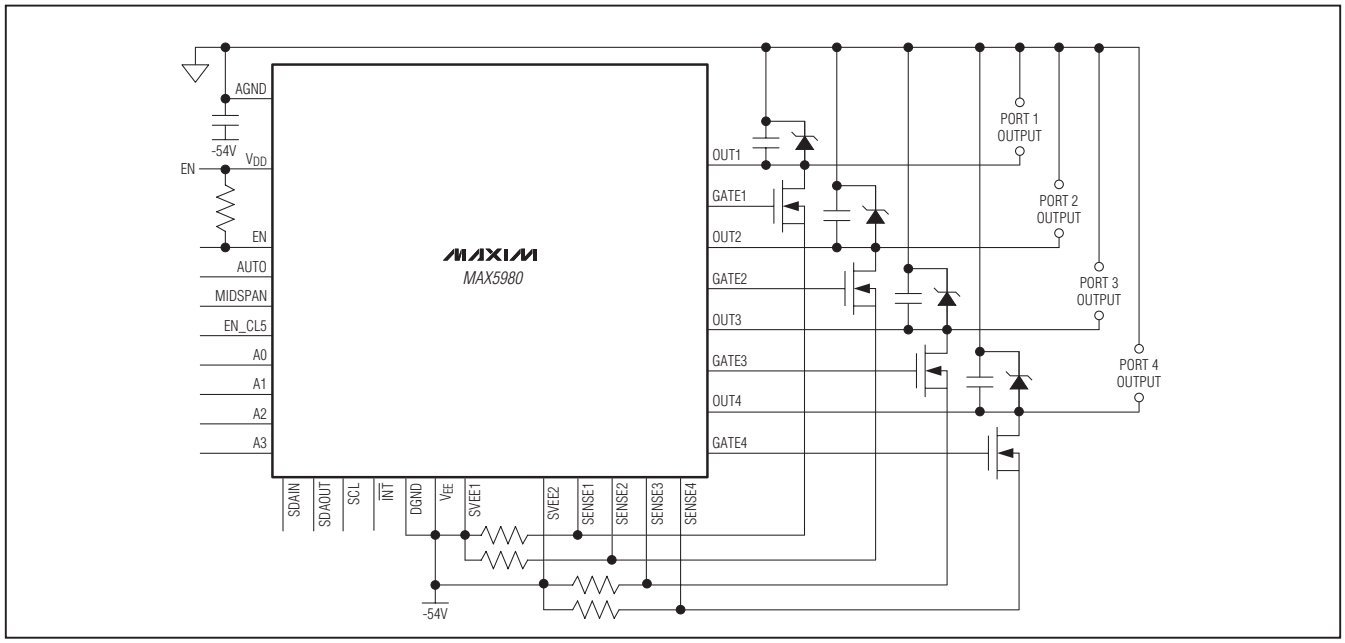
Midspan Power Injectors

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5980GTJ+	-40°C to +105°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Operating Circuit



Quad, IEEE 802.3at/af PSE Controller for Power-over-Ethernet

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)

AGND .....-0.3V to +80V
DGND, SVEE_ .....-0.3V to +0.3V
V_{DD} ..... -0.3V to the lower (V_{AGND} + 0.3V) and +4V
OUT_ .....-0.3V to (V_{AGND} + 0.3V)
GATE_, SENSE_ .....-0.3V to +22V
A3, A2, A1, A0, MIDSPAN, EN_CL5, AUTO, $\overline{INT}$, SCL, SDAIN, SDAOUT, EN to DGND .....-0.3V to +6V
Maximum Current into $\overline{INT}$ and OUT 20mA
Maximum Current into OUT_.....Internally Regulated

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C)....2758.6mW
Package Thermal Resistance (Note 1)
θ_{JA}..... +29°C/W
θ_{JC} ..... +1.7°C/W
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}		32		60	V
Supply Currents	I_{EE}	$V_{OUT\_}$ = $V_{SENSE\_}$ = V_{EE}; $\overline{INT}$, SDAOUT, and all logic inputs unconnected; V_{SCL} = V_{SDAIN} = V_{DD}; measured at AGND in power mode after GATE_ pullup			5	7	mA
GATE DRIVER AND CLAMPING							
GATE_ Pullup Current	I_{PU}	Power mode, gate drive on, $V_{GATE\_}$ = V_{EE}		-40	-50	-60	µA
GATE_ Pulldown Current	I_{PDW}	Port SHDN mode enabled; $V_{GATE\_}$ = V_{EE} + 10V			40		µA
Strong Pulldown Current	I_{PDS}	$V_{SENSE\_}$ = 500mV, $V_{GATE\_}$ = V_{EE} + 2V			25		mA
External Gate Drive	V_{GS}	$V_{GATE\_}$ - V_{EE}, power mode, gate-drive on		8.5	9.5	10.5	V
CURRENT LIMIT AND OVERCURRENT							
Current-Limit Clamp Voltage	V_{SU_LIM}	Maximum $V_{SENSE\_}$ allowed during current-limit conditions, $V_{OUT\_}$ = 0V (Note 3)	$I_{LIM\_}$ register set to 80h, Class 0–3	101	106.25	111.5	mV
			$I_{LIM\_}$ register set to C0h, Class 4	200	212.5	225	
			$I_{LIM\_}$ register set to C0h, Class 5	405	430	455	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Overcurrent Threshold after Startup	V_{CUT}	Overcurrent $V_{SENSE\_}$ threshold allowed for $t \le t_{FAULT}$ after startup, $V_{OUT\_}$ = 0V	$I_{CUT\_}$ register set to 14h, Class 0 and 3	89	93.75	98.5	mV
			$I_{CUT\_}$ register set to 22h, Class 4	178	187.5	197	
			$I_{CUT\_}$ register set to 22h, Class 5	356	375	394	
Foldback Initial Voltage	V_{FLBK_ST}	V_{AGND} - $V_{OUT\_}$ above which the current-limit trip voltage starts folding back	I_{LIM} register set to 80h		32		V
			I_{LIM} register set to C0h		18		
Foldback Final Voltage	V_{FLBK_END}	V_{AGND} - $V_{OUT\_}$ above which the current limit reaches V_{TH_FB}			46		V
Minimum Foldback Current-Limit Threshold	V_{TH_FB}	$V_{OUT\_}$ = V_{AGND} = 60V			35		mV
SENSE_ Input Bias Current		$V_{SENSE\_}$ = V_{EE}				-2	µA
SUPPLY MONITORS							
V_{EE} Undervoltage Lockout	V_{EE_UVLO}	V_{AGND} - V_{EE}, V_{AGND} - V_{EE} increasing			29		V
V_{EE} Undervoltage Lockout Hysteresis	V_{EE_UVLOH}	Ports shut down if: V_{AGND} - V_{EE} < V_{EE_UVLO} - V_{EE_UVLOH}			3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	Ports shut down if: V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} - V_{EE} increasing			62		V
V_{EE} Overvoltage-Lockout Hysteresis	V_{EE_OVH}				1		V
V_{EE} Undervoltage	V_{EE_UV}	V_{EE_UV} event bit sets if: V_{AGND} - V_{EE} < V_{EE_UV}, V_{AGND} - V_{EE} increasing			40		V
V_{DD} Output Voltage	V_{DD}	I_{DD} = 0 to 10mA		3.0	3.3	3.6	V
V_{DD} Undervoltage Lockout	V_{DD_UVLO}				2		V
Thermal-Shutdown Threshold	T_{SHD}	Port is shut down and device resets if the junction temperature exceeds this limit, temperature increasing (Note 4)			+140		°C
Thermal-Shutdown Hysteresis	T_{SHDH}	Temperature decreasing (Note 4)			20		°C
OUTPUT MONITOR							
OUT_ Input Current	I_{BOUT}	$V_{OUT\_}$ = V_{AGND}, during idle				2	µA
		V_{AGND} - V_{EE} = 48V, $V_{OUT\_}$ = V_{EE}, during power-on mode				-70	
Idle Pullup Resistance at OUT_	R_{DIS}	Detection and classification off, port shut down		0.7	1	1.25	MΩ
PGOOD High Threshold	PG_{TH}	$V_{OUT\_}$ - V_{EE}, OUT_ decreasing		1.5	2.0	2.5	V

Quad, IEEE 802.3at/af PSE Controller for Power-over-Ethernet

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Hysteresis	PG_{HYS}				220		mV
PGOOD Low-to-High Glitch Filter	t_{PGOOD}	Time $V_{OUT\_}$ - V_{EE} has to exceed PGTH to set the PGOOD_ bit in register 10h		2		4	ms
LOAD DISCONNECT							
DC Load Disconnect Threshold	V_{DCTH}	Minimum $V_{SENSE\_}$ allowed before disconnect (DC disconnect active), $V_{OUT\_}$ = 0V		1.25	1.875	2.5	mV
Load Disconnect Time	t_{DISC}	Time from $V_{SENSE\_}$ < V_{DCTH} to gate shutdown (Note 5)		300		400	ms
DETECTION							
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - V_{DET} during the first detection phase		3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - V_{DET} during the second detection phase		8.8	9.1	9.4	V
Current-Limit Protection	I_{DLIM}	$V_{OUT\_}$ = V_{AGND}, current measured through OUT_ during detection		1.50		2	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - $V_{OUT\_}$ < V_{DCP} after the first detection phase, a short circuit to AGND is detected			1.5		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition			12.5		µA
Resistor Detection Window	R_{DOK}	(Note 5)		19		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values				15.2	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
Classification Probe Voltage	V_{CL}	V_{AGND} - $V_{OUT\_}$ during classification		15.5		20	V
Current-Limit Protection	I_{CL_LIM}	$V_{OUT\_}$ = V_{AGND}, current measured through OUT_		65	75	86	mA
Classification Event Timing	t_{CL_E}			14	18	22	ms
Mark Event Voltage	V_{MARK}	V_{AGND} - V_{DET} during mark event		8		9.6	V
Mark Event Current Limit	I_{MARK_LIM}	V_{DET} = V_{AGND}, during mark event measure current through DET		34	40	46	mA
Mark Event Timing	t_{MARK_E}			7	9	11	ms
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes	Class 0, Class 1	5.5	6.5	7.5	mA
			Class 1, Class 2	13.0	14.5	16.0	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			Class 4 upper limit (Note 6)	45	48	51	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS (Voltages Referenced to V_{EE})							
Digital Input Low	V_{IL}					0.8	V
Digital Input High	V_{IH}			2			V
Internal Input Pullup/Pulldown Resistor	R_{DIN}	Pullup (pulldown) resistor to V_{DD} (DGND) to set default level		25	50	75	kΩ
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 10mA				0.4	V
Open-Drain Leakage	I_{OL}	Open-drain high impedance, $V_{OUT\_}$ = 3.3V				1	µA
SCL, SDAIN Input Leakage	I_{DL}	Input connected to the pull voltage				1	µA
Hardware Reset Pulse Width		Minimum low pulse duration on EN to lead to a hardware reset event		120			µs
TIMING							
Startup Time	t_{START}	Time during which a current limit set by V_{SU_LIM} is allowed, starts when the GATE_ is turned on		50	60	70	ms
Fault Time	t_{FAULT}	Time allowed for an overcurrent fault set by V_{FLT_LIM} after startup		50	60	70	ms
Current Limit	t_{LIM}	Time during after startup (Note 7)		50	60	70	ms
Port_ Turn-Off Time	t_{OFF}	Minimum delay between any port turn-off, does not apply in a reset case			0.1		ms
Detection Reset Time		Time allowed for the port voltage to reset before detection starts			80		ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed				330	ms
Midspan Mode Detection Delay	t_{DMID}			2			s
Classification Time	t_{CLASS}	Time allowed for classification			19	25	ms
V_{EE_UVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EE_UVLO} threshold before the device operates		2		4	ms
Restart Timer	$t_{RESTART}$	Time the device waits before turning on after an overcurrent fault, MIDSPAN disabled		0.8	0.96	1.1	s
Startup Sequence Delay	t_{SEQ}	Time between any port power-up in auto mode			0.5		s
ADC PERFORMANCE (Power-On Mode)							
Resolution					9		Bits
Offset Error		Voltage reading	T_A = -5°C to +85°C			2.5	LSB
			T_A = -40°C to +105°C			3	
		Current reading	T_A = -5°C to +85°C			2.5	
			T_A = -40°C to +105°C			3	

Quad, IEEE 802.3at/af PSE Controller for Power-over-Ethernet

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error		Gain error voltage	T_A = -5°C to +85°C	-0.5		+4	%
			T_A = -40°C to +105°C	-1		+4.5	
		Gain error current	T_A = -5°C to +85°C	-2		+2	
			T_A = -40°C to +105°C	-2.5		+2.5	
V_{EE} Voltage Accuracy		V_{AGND} - V_{EE} = 48V	T_A = -5°C to +85°C	-0.5		+4.5	%
			T_A = -40°C to +105°C	-0.5		+5	
Integral Nonlinearity	INL					1	LSB
Differential Nonlinearity	DNL					1	LSB
Current Reading Range		Classes 0–4			1		A
		Class 5			2		
Current LSB Step Size		Classes 0–4			1.956		mA
		Class 5			3.912		
Voltage Reading Range		All classes			95.6		V
Voltage LSB Step Size		All classes			187		mV
TIMING CHARACTERISTICS (3-Wire Fast Mode)							
Serial Clock Frequency	f_{SCL}			10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}			1.3			µs
Hold Time for a START Condition	$t_{HD, STA}$			0.6			µs
Low Period of the SCL Clock	t_{LOW}			1.3			µs
High Period of the SCL Clock	t_{HIGH}			0.6			µs
Setup Time	$t_{SU, STA}$	START and STOP conditions		0.6			µs
Data Hold Time	$t_{HD, DAT}$	Receive		0			ns
		Transmit		100		300	
Data in Setup Time	$t_{SU, DAT}$			100			ns
Cumulative Clock Low Extend Time	t_{LOW_EXT}					25	ms
Fall Time of SDAOUT Transmitting	t_F	(Note 8)				250	ns
Setup Time for STOP Condition	$t_{SU, STO}$			0.6			µs
Pulse Width of Spike Suppressed	t_{SP}	(Note 8)			30		ns

Note 2: Production testing done at +25°C. Overtemperature limits are guaranteed by design and not production tested.

Note 3: The current-limit thresholds are programmed through the I^2C interface (see the *Register Map and Description* section and Table 41).

Note 4: Functional test is performed over thermal shutdown entering test mode.

Note 5: R_{DOK} = (V_{OUT2} - V_{OUT1})/(I_{OUT2} - I_{OUT1}). V_{OUT1}, V_{OUT2}, I_{OUT1}, and I_{OUT2} represent the voltage at OUT_ and the current into OUT_ during phase 1 and 2 of the detection, respectively.

Note 6: If Class 5 is enabled, this value is the classification current threshold from Class 4 to Class 5, and classification currents between 51mA and I_{CL_LIM} will be classified as Class 5.

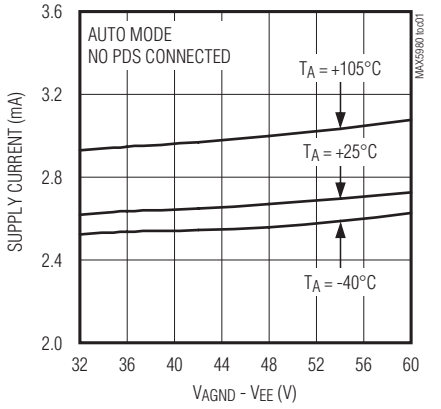
Note 7: Default value. The fault timer can be reprogrammed through the I^2C interface (TLIM_[3:0]).

Note 8: Guaranteed by design. Not subject to production testing.

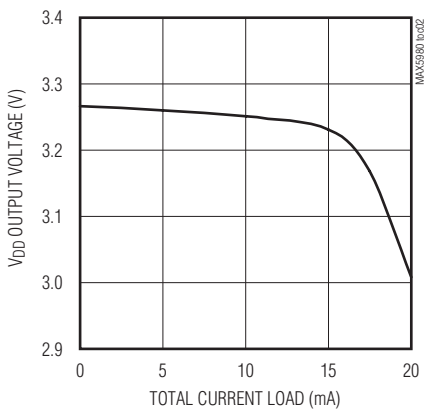
Typical Operating Characteristics

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

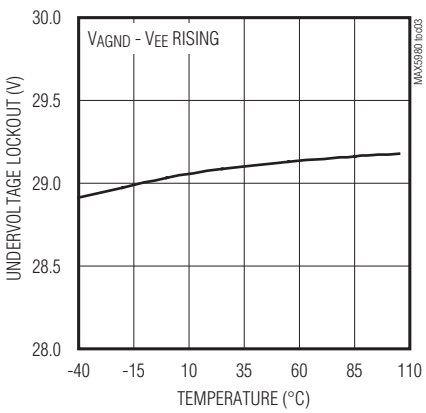
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



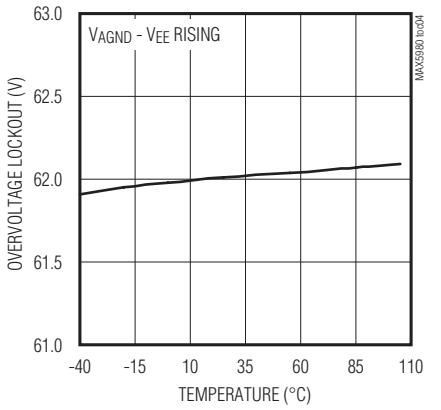
DIGITAL SUPPLY REGULATED VOLTAGE vs. LOAD CURRENT



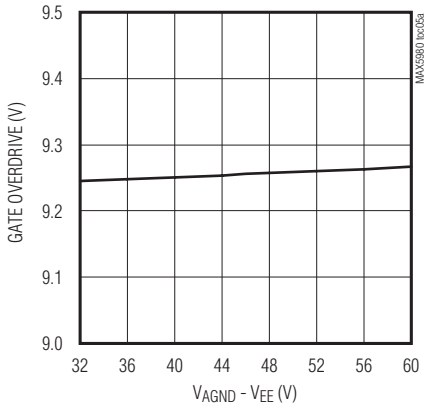
ANALOG SUPPLY UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



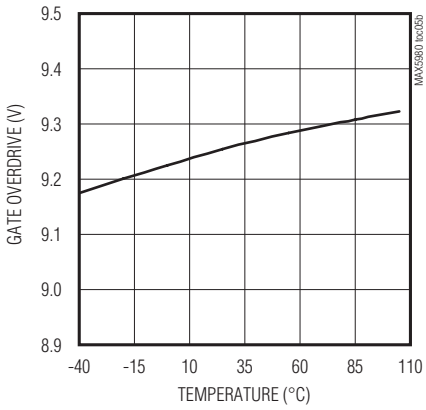
ANALOG SUPPLY OVERVOLTAGE LOCKOUT vs. TEMPERATURE



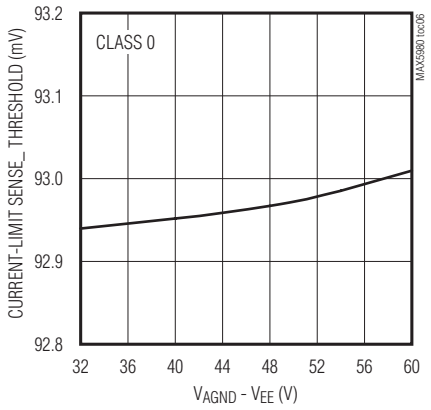
GATE OVERDRIVE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



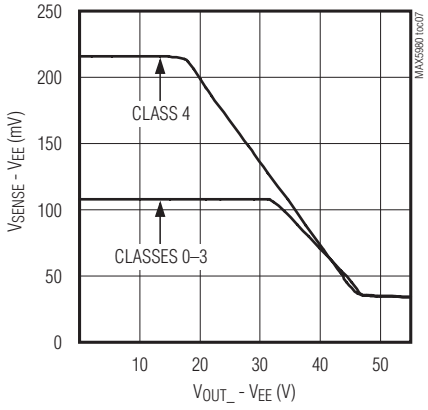
GATE OVERDRIVE VOLTAGE vs. TEMPERATURE



CURRENT-LIMIT SENSE_ THRESHOLD vs. ANALOG SUPPLY VOLTAGE



FOLDBACK CURRENT-LIMIT SENSE_ THRESHOLD vs. PORT OUTPUT VOLTAGE

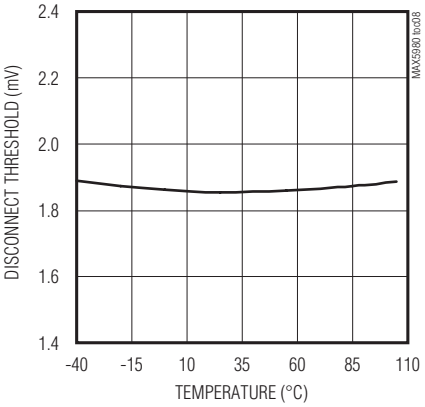


Quad, IEEE 802.3at/af PSE Controller for Power-over-Ethernet

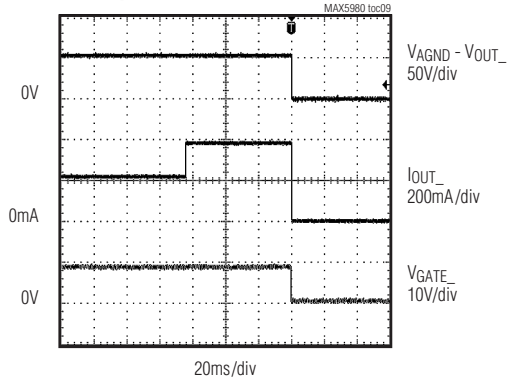
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

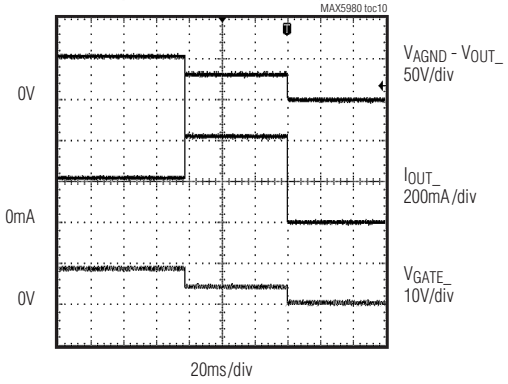
DC LOAD DISCONNECT SENSE_ THRESHOLD vs. TEMPERATURE



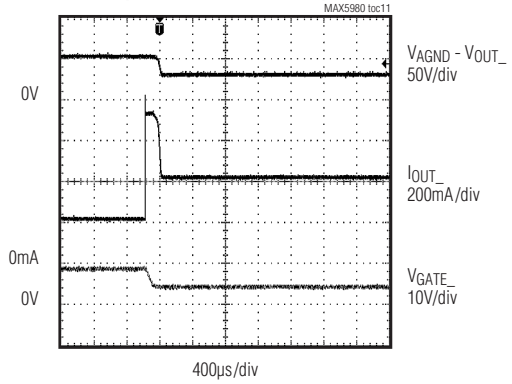
OVERCURRENT TIMEOUT (R_{LOAD} = 240Ω TO 140Ω)



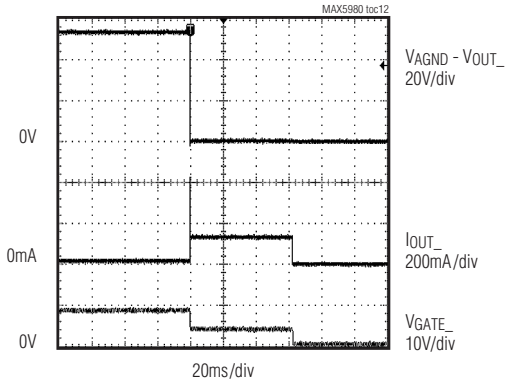
CURRENT-LIMIT TIMEOUT (R_{LOAD} = 240Ω TO 75Ω)



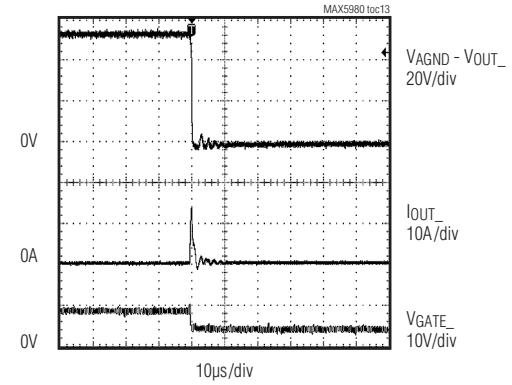
CURRENT-LIMIT TRANSIENT RESPONSE (R_{LOAD} = 240Ω TO 75Ω)



OUTPUT SHORT-CIRCUIT TIMEOUT



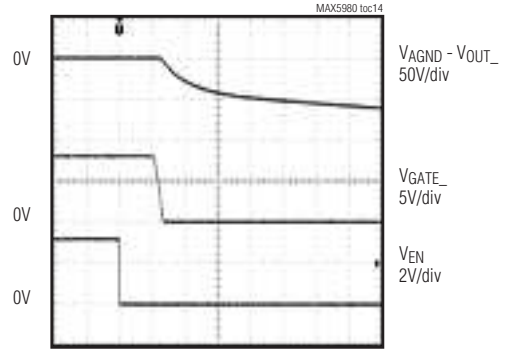
OUTPUT SHORT-CIRCUIT RESPONSE TIME



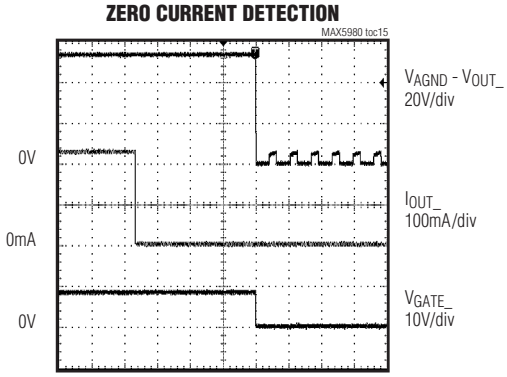
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

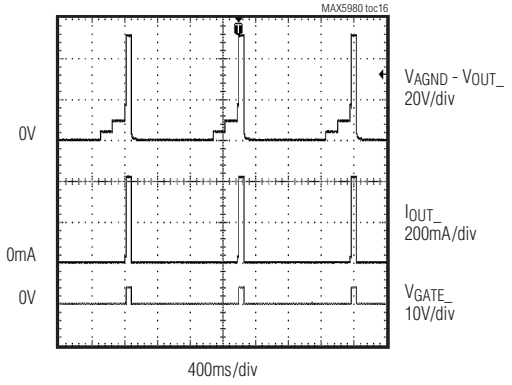
EN TO HARDWARE POWER-DOWN DELAY



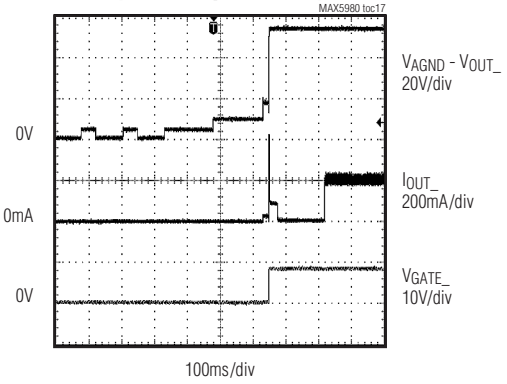
ZERO CURRENT DETECTION



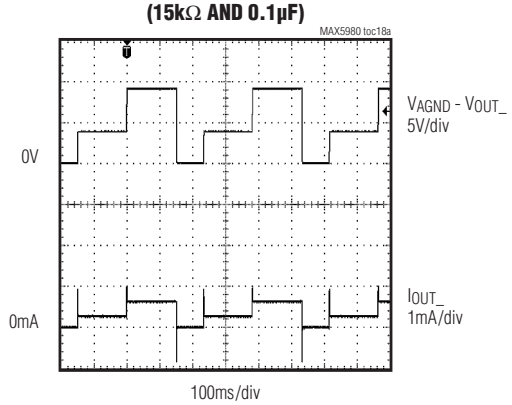
OVERCURRENT RESTART DELAY



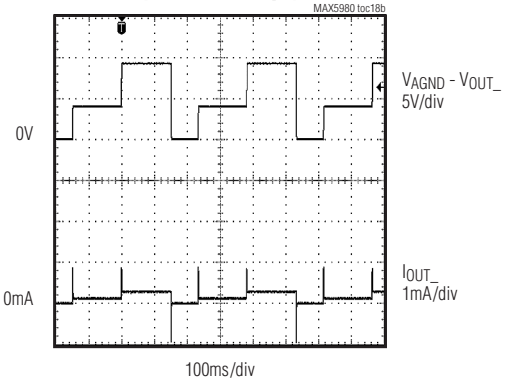
STARTUP WITH VALID PD (25kΩ, 0.1µF, CLASS 3)



DETECTION WITH INVALID PD (15kΩ AND 0.1µF)



DETECTION WITH INVALID PD (33kΩ AND 0.1µF)



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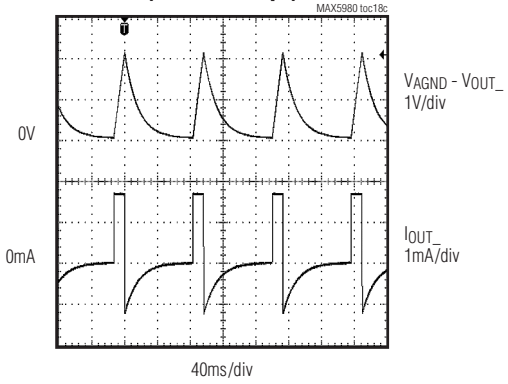
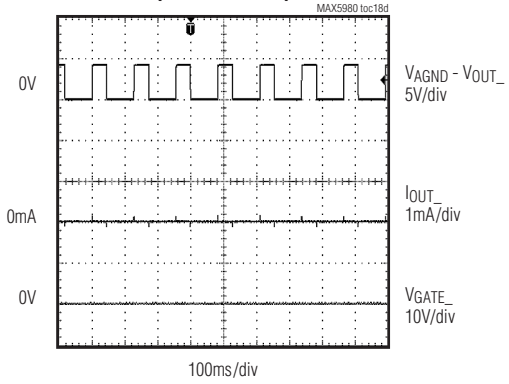
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

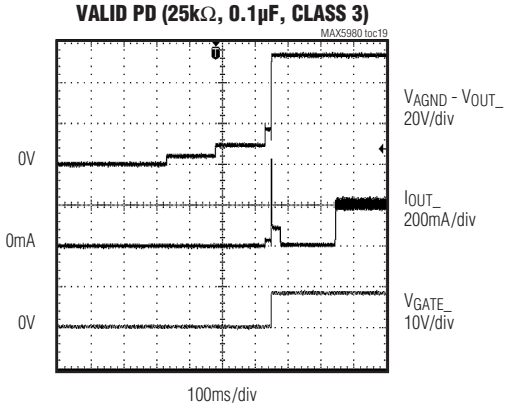
DETECTION WITH INVALID PD (25kΩ AND 10µF)



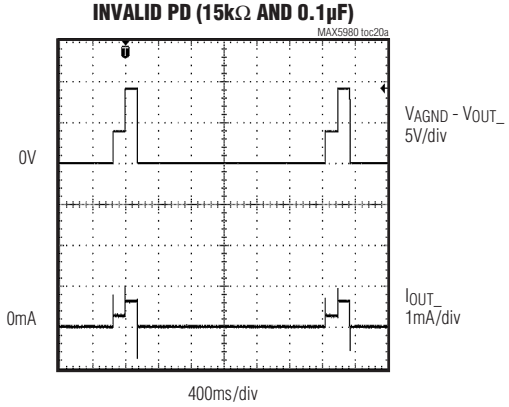
DETECTION WITH INVALID PD (OPEN CIRCUIT)



STARTUP IN MIDSPAN MODE WITH VALID PD (25kΩ, 0.1µF, CLASS 3)



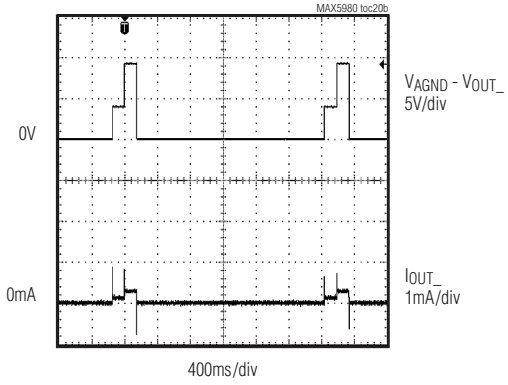
DETECTION IN MIDSPAN MODE WITH INVALID PD (15kΩ AND 0.1µF)



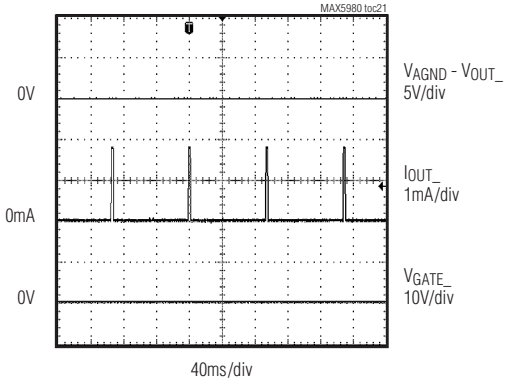
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

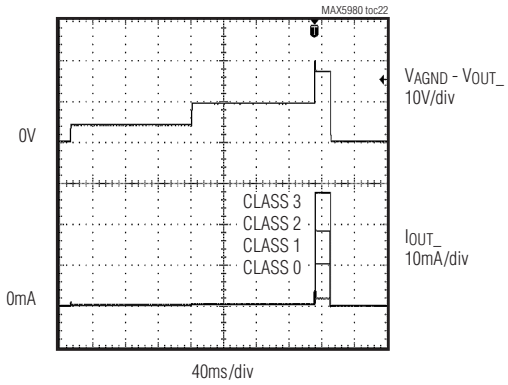
DETECTION IN MIDSPAN MODE WITH INVALID PD (33kΩ AND 0.1µF)



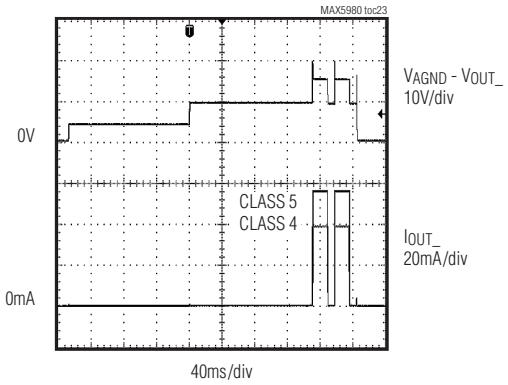
DETECTION WITH OUT_ SHORTED TO AGND



CLASSIFICATION WITH CLASS 0 TO 3 PDs



2-EVENT CLASSIFICATION WITH CLASS 4 AND 5 PDs



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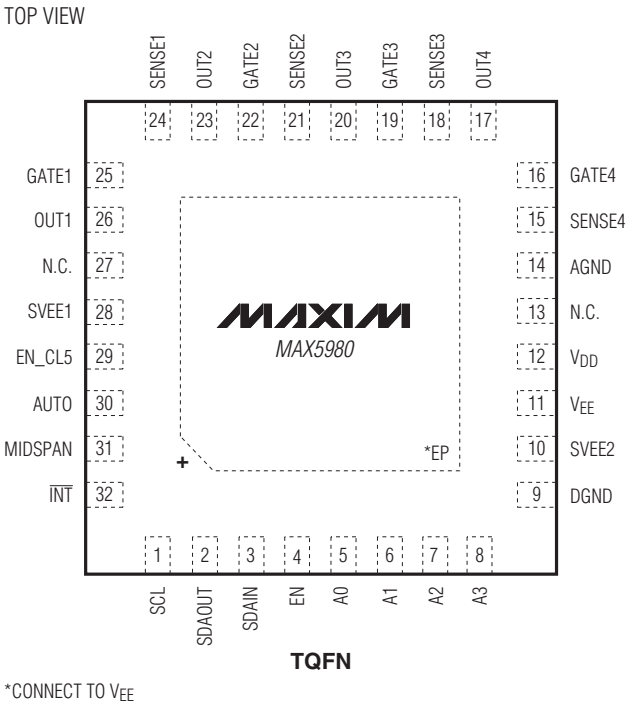
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SCL	3-Wire Serial Interface Input Clock Line. Referenced to DGND. Connect to DGND if the I²C interface is not used.
2	SDAOUT	Serial Interface Data Line Output. Referenced to DGND. Connect to DGND if the I²C interface is not used.
3	SDAIN	Serial Interface Data Line Input. Referenced to DGND. Connect to DGND if the I²C interface is not used.
4	EN	EN Input. Referenced to DGND. Connect EN to V_{DD} externally through a pullup resistor to enable normal operation. See the *Hardware Power-Down* section for details.
5, 6, 7, 8	A0, A1, A2, A3	Slave Address Bits 0, 1, 2, 3 (Respectively). Referenced to DGND. The slave address bits are used to form bits 3, 2, 1, and 0 of the device address (0:1:0:A3:A2:A1:A0; see Table 3). The slave address bits are internally pulled up to V_{DD}. Leave them unconnected to use the default device address (0101111). Connect one or more to DGND to change the device address. The slave address is latched-in after the device is powered up or after a reset condition.
9	DGND	Digital Low-Side Supply Input. Connect to V_{EE} externally.
10	SVEE2	Port 3/4 Current-Sense Negative Terminal Input. Use Kelvin-sensing technique in PCB layout for best accuracy current sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
11	V_{EE}	Analog Low-Side Supply Input. Bypass with an external 100V, 0.1µF ceramic capacitor between AGND and V_{EE}.
12	V_{DD}	Digital High-Side Supply Output. Bypass with an external RC network; see the *V_{DD} Power Supply* section for details.
13, 27	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.
14	AGND	Analog High-Side Supply Input
15, 18, 21, 24	SENSE4, SENSE3, SENSE2, SENSE1	Current-Sense Positive Terminal Inputs. Connect to the source of the external power MOSFET and connect a 0.25Ω current-sense resistor between SENSE_ and SVEE_. Use Kelvin-sensing technique in PCB layout for best accuracy current sensing.
16, 19, 22, 25	GATE4, GATE3, GATE2, GATE1	Port_ MOSFET Gate Drivers. Connect GATE_ to the gate of the external power MOSFET (see the *Typical Operating Circuit*).
17, 20, 23, 26	OUT4, OUT3, OUT2, OUT1	Port Output Voltage Senses. Connect OUT_ to the port output.
28	SVEE1	Port 1/2 Current-Sense Negative Terminal Input. Use Kelvin sensing technique in PCB layout for best accuracy current sensing.
29	EN_CL5	Class 5 Enable Input. Referenced to DGND. EN_CL5 is internally pulled down to DGND. Leave unconnected to disable the classification for Class 5 devices (IEEE 802.3at-compliant mode). Connect EN_CL5 to V_{DD} to enable the classification of Class 5 devices. EN_CL5 is latched in after the device is powered up or after a reset condition.
30	AUTO	Auto/Shutdown Mode Input. Referenced to DGND. AUTO is internally pulled up to V_{DD}. Leave unconnected to put the device into auto mode by default. Connect AUTO to DGND instead to set the default mode to shutdown. In either configuration, the software can change the operating mode of the device. AUTO is latched in after the device is powered up or after a reset condition.
31	MIDSPAN	Detection Collision Avoidance Logic Input. Referenced to DGND. MIDSPAN is internally pulled up to V_{DD}. Leave unconnected to activate midspan mode, or connect to DGND to disable this function. MIDSPAN is latched in after the device is powered up or after a reset condition.
32	$\overline{INT}$	Open-Drain Interrupt Output. Referenced to DGND. $\overline{INT}$ is pulled low whenever an interrupt is sent to the microcontroller. See the *Interrupt* section for details. Connect to DGND if the I^2C interface is not used.
—	EP	Exposed Pad. EP is internally connected to V_{EE}. Connect EP to V_{EE} externally.

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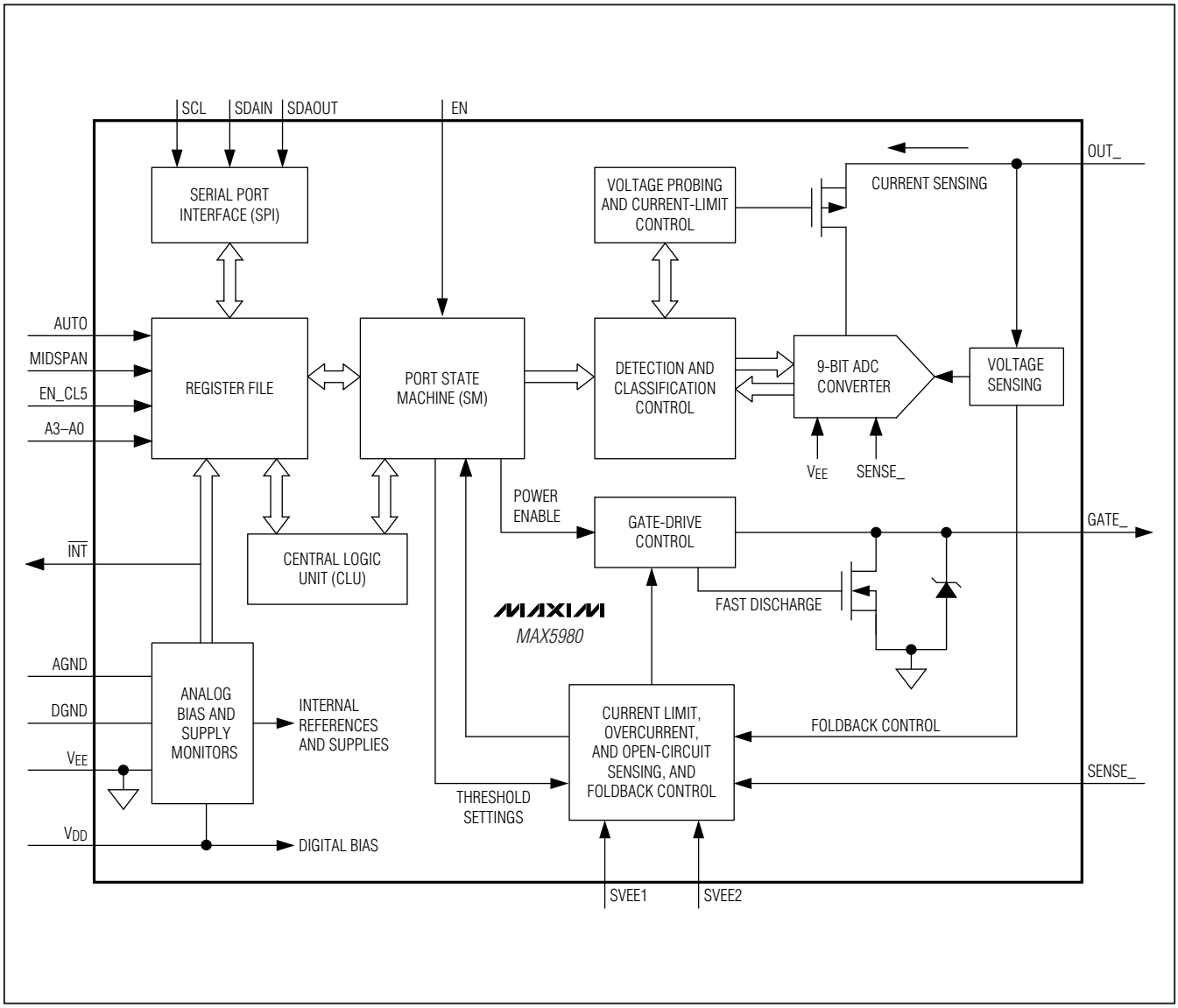
Functional Diagram



Detailed Description

The MAX5980 is a quad PSE power controller designed for use in IEEE 802.3at/af-compliant PSE. This device provides PD discovery, classification, current limit, and load disconnect detections. The device supports both fully automatic operation and software programmability. The device also supports new 2-event classification and Class 5 for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 70W to each port (Class 5 enabled), and still provides high-capacitance detection for legacy PDs.

The device features an I²C-compatible, 3-wire serial interface, and is fully software configurable and programmable. The device provides instantaneous readout of port current and voltage through the I²C interface. The device provides input undervoltage lockout (UVLO), input overvoltage lockout (OVLO), overtemperature protection, and output voltage slew-rate limit during startup.

Reset

The device is reset by any of the following conditions:

1) Power-up/down. Reset condition is asserted once V_{EE} falls below the UVLO threshold.
2) Hardware reset. To initiate a hardware reset, pull EN low to DGND for at least 100µs. Hardware reset clears once, EN returns high to V_{DD}, and all registers are set to their default states.
3) Software reset. To initiate a software reset, write a logical 1 to the RESET_IC register (R1Ah[4]) any time after power-up. Reset clears automatically, and all registers are set to their default states.
4) Thermal shutdown. The device enters thermal shutdown at +140°C. The device exits thermal shutdown and is reset once the temperature drops below 120°C.

During normal operation, changes to the address inputs, MIDSPAN, EN_CL5, and AUTO are ignored, and they can be changed at any time prior to a reset state. At the end of a reset event, the device latches in the state of these inputs.

Port Reset

Set RESET_P_ (R1Ah[3:0]) high anytime during normal powered operation to turn off port_, disable detection and classification, and clear the Port_ Event and Status registers. If a port is not powered, setting RESET_P_ high for that port has no effect. Individual port reset does not initiate a global device reset.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the ports wait at least 2s before attempting to detect again. Midspan mode is activated by setting MIDSPAN high and then powering or resetting the device. Alternatively, midspan mode can be software programmed individually for each port by setting MIDSPAN_ (R15h[3:0], Table 23) to a logical 1. By default, the MIDSPAN input is internally pulled high, enabling cadence timing. Force MIDSPAN low to disable this function.

Operation Modes

The device provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies devices connected to the ports, but does not power a port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

Switching between auto, semiautomatic, and manual mode does not interfere with the operation of an output port. When a port is set into shutdown mode, all port operations are immediately stopped and the port remains idle until shutdown mode is exited.

Auto (Automatic) Mode

By default, when the auto input is unconnected, the device enters auto mode after power-up or when the reset condition is cleared. To manually place a port into auto mode from any other mode, set the corresponding port mode bits (R12h[7:0]) to [11] (Table 19).

In auto mode, the device performs detection, classification, and powers up the port automatically if a valid PD is connected to the port. If a valid PD is not connected at the port, the device repeats the detection routine continuously until a valid PD is connected.

When entering auto mode after a reset condition (state of AUTO input), the DET_EN_ and CLASS_EN_ bits (R14h[7:0], Table 22) are set to high and stay high, unless changed by software. When entering auto mode from any other mode due to a software command (programmed with R12h[7:0], Table 19, the DET_EN_ and CLASS_EN_ bits retain their previous state.

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Semiautomatic (Semi) Mode

Enter semiautomatic mode by setting the port operating mode (R12h, Table 19) to [10]. When entering semi mode, the DET_EN_ and CLASS_EN_ bits retain their previous states. When the DET_EN_ and/or CLASS_EN_ bits are set to 1, the MAX5980 performs detection and/or classification repeatedly, but do not power up the port(s) automatically.

Setting R19h[3:0] (PWR_ON_, Table 26) high turns on power to the port(s) if detection and classification has successfully completed. If a port is powered down while in semiautomatic mode, the corresponding DET_EN_ and CLASS_EN_ bits are reset to 0.

Manual Mode

Enter manual mode by setting the port operating mode (R12h, Table 19) to [01]. Manual mode allows the software to dictate any sequence of operation. In manual mode, the Detection/Classification register (R14h, Table 22) is set to 00h, and DET_EN_/CLASS_EN_ become pushbutton bits. A port will only perform a single detection/classification cycle when DET_EN_/CLASS_EN_ are set high, and they are reset low after execution.

PWR_ON_ (R19h[3:0], Table 26) has the highest priority, and setting PWR_ON_ high at any time causes the device to immediately enter the powered mode. Setting DET_EN_ and CLASS_EN_ high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ and CLASS_EN_ commands.

Shutdown Mode

To put a port into shutdown mode, set the corresponding port mode bits (R12h, Table 19) to [00]. Putting a port into shutdown mode immediately turns off port power, clears the event and status bits, and halts all port operations. In shutdown mode the serial interface is still fully active; however, all DET_EN_, CLASS_EN_, and PWR_ON_ commands are ignored.

PD Detection

During normal operation, the device probes the output for a valid PD. A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3at/af standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature.

After each detection cycle, the device sets DET_ (R04h[3:0] and R05h[3:0], Table 9) to 1 and reports the detection results in the detection status bits (see Table 13). The DET_ bits are reset to 0 when read through the CoR (clear on read) register (R05h), or after a reset event.

During detection, the device keeps the external MOSFET off and forces two probe voltages through OUT_. The current through OUT_ is measured, as well as the voltage difference from AGND to OUT_. A two-point slope measurement is used, as specified by the IEEE 802.3at/af standard, to verify the device connected to the port. The device implements appropriate settling times to reject 50Hz/60Hz power-line noise coupling.

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}	—	30	V	In detection mode only
Short-Circuit Current	I_{SC}	—	5	mA	In detection mode only
Valid Test Voltage	V_{VALID}	2.8	10	V	—
Voltage Difference Between Test Points	ΔV_{TEST}	1	—	V	—
Time Between Any Two Test Points	t_{BP}	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	V_{SLEW}	—	0.1	V/µs	—
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	—
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	—
Open-Circuit Resistance	R_{OPEN}	500	—	kΩ	—
Accept Signature Capacitance	C_{GOOD}	—	150	nF	—
Reject Signature Capacitance	C_{BAD}	10	—	µF	—
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	—
Signature Offset Current Tolerance	I_{OS}	0	12	µA	—

To prevent damage to non-PD devices, and to protect itself from an output short circuit, the device limits the current into OUT_ to less than 2mA (max) during PD detection. In midspan mode, after every failed detection cycle, the device waits at least 2.0s before attempting another detection cycle.

High-Capacitance Detection

High-capacitance detection for legacy PDs is software programmable. To use the software to enable high-capacitance detection, set LEG_EN_ (Port GPMD registers, Table 39) to 1 during normal operation. If high-capacitance detection is enabled, PD signature capacitances up to 100µF (typ) are accepted.

Power Device Classification (PD Classification)

During PD classification, the device forces a probe voltage between 15V and 20V at OUT_ and measures the current into OUT_. The measured current determines the class of the PD.

After each classification cycle, the device sets CLS_ (R04h[7:4] and R05h[7:4], Table 9) to 1 and reports the classification results in the classification status bits (see Table 13). The CLS_ bits are reset to 0 when read through the CoR (clear on read) register (R05h) or after a reset event.

If EN_CL5 is left unconnected, the device will classify the PD based on Table 33-9 of the IEEE 802.3at standard (see Table 2). If the measured current exceeds 51mA, the device will not power the PD, but will report an overcurrent classification result and will return to IDLE state before attempting a new detection cycle.

Class 5 PD Classification

The device supports high power beyond the IEEE 802.3at standard by providing an additional classification (Class 5) if needed. To enable Class 5, connect EN_CL5 to V_{DD} and initiate a global reset or use the software to individually enable Class 5 classification for each port (R1Ch[3:0], Table 29). Once Class 5 is enabled, during classification, if the device detects currents in excess of the Class 4 upper-limit threshold, the PD will be classified as a Class 5 powered device. The PD is guaranteed to be classified as a Class 5 device for any classification current from 51mA up to the classification current-limit threshold. The Class 5 overcurrent threshold and current limit will be set automatically with ICUT_[5:0] and ILIM_ (see Tables 40 and 41). Leave EN_CL5 unconnected to disable Class 5 detection and to be fully compliant to IEEE 802.3at standard classification.

Table 2. PSE Classification of a PD (Table 33-9 of the IEEE 802.3at Standard)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

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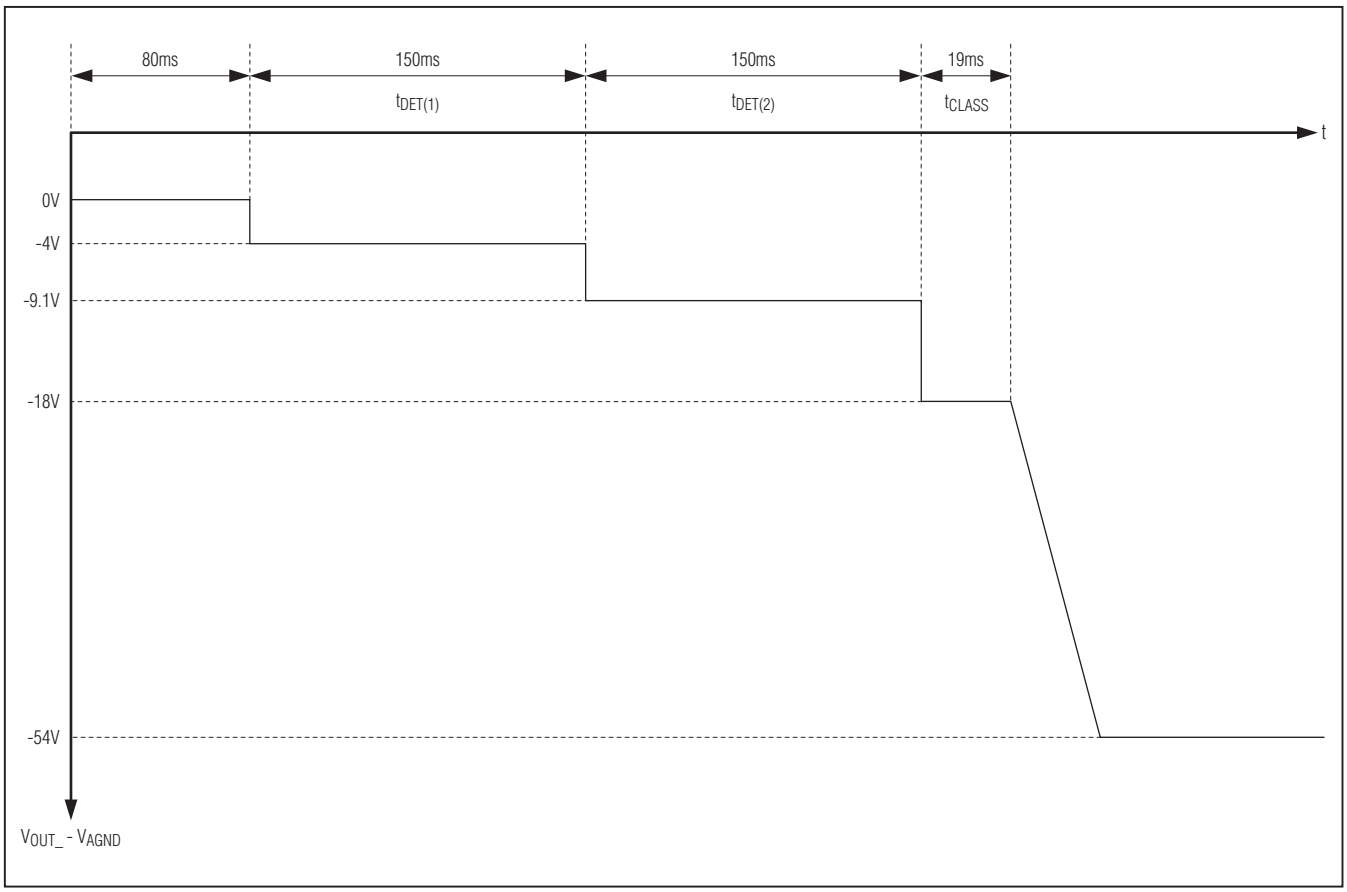

Figure 1. Detection, Classification, and Port Power-Up Sequence

2-Event PD Classification

If the result of the first classification event is Class 0 to 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 (or Class 5), the device will perform a second classification event as shown in Figure 2. Between the classification cycles, the device performs a first and second mark event as required by the IEEE 802.3at standard, forcing a -9.3V probing voltage at OUT_.

Powered State

When the device enters a powered state, the t_{FAULT} timer is reset and power is delivered to the PD. PGOOD_ (R10h[7:4], Table 16) is set to 1 when the device enters the normal power condition. PGOOD_ immediately resets to 0 whenever the power to the port is turned off. The power-good change bits, PG_CHG_ (R02h[3:0], Table 8) are set both when the port powers up and when it powers down.

Overcurrent Protection

A sense resistor, $R_{SENSE\_}$, connected between SENSE_ and SVEE_ monitors the load current. Under normal operating conditions, the voltage across $R_{SENSE\_}$ ($V_{RSENSE\_}$) never exceeds the current-limit threshold, V_{SU_LIM}. If $V_{RSENSE\_}$ exceeds V_{SU_LIM}, an internal current-limiting circuit regulates the GATE_ voltage, limiting the current to $I_{LIM} = V_{SU\_LIM}/R_{SENSE\_}$. During transient conditions, if $V_{RSENSE\_}$ exceeds V_{SU_LIM} by more than 500mV, a fast pulldown circuit activates to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, t_{START}, times out, the port shuts off, and the TSTART_ bit is set (R08h[3:0] and R09h[3:0], Table 11).

In the normal powered state, the device checks for overcurrent conditions as determined by V_{CUT}. The t_{FAULT} counter sets the maximum allowed continuous overcurrent period. The t_{FAULT} counter increases when

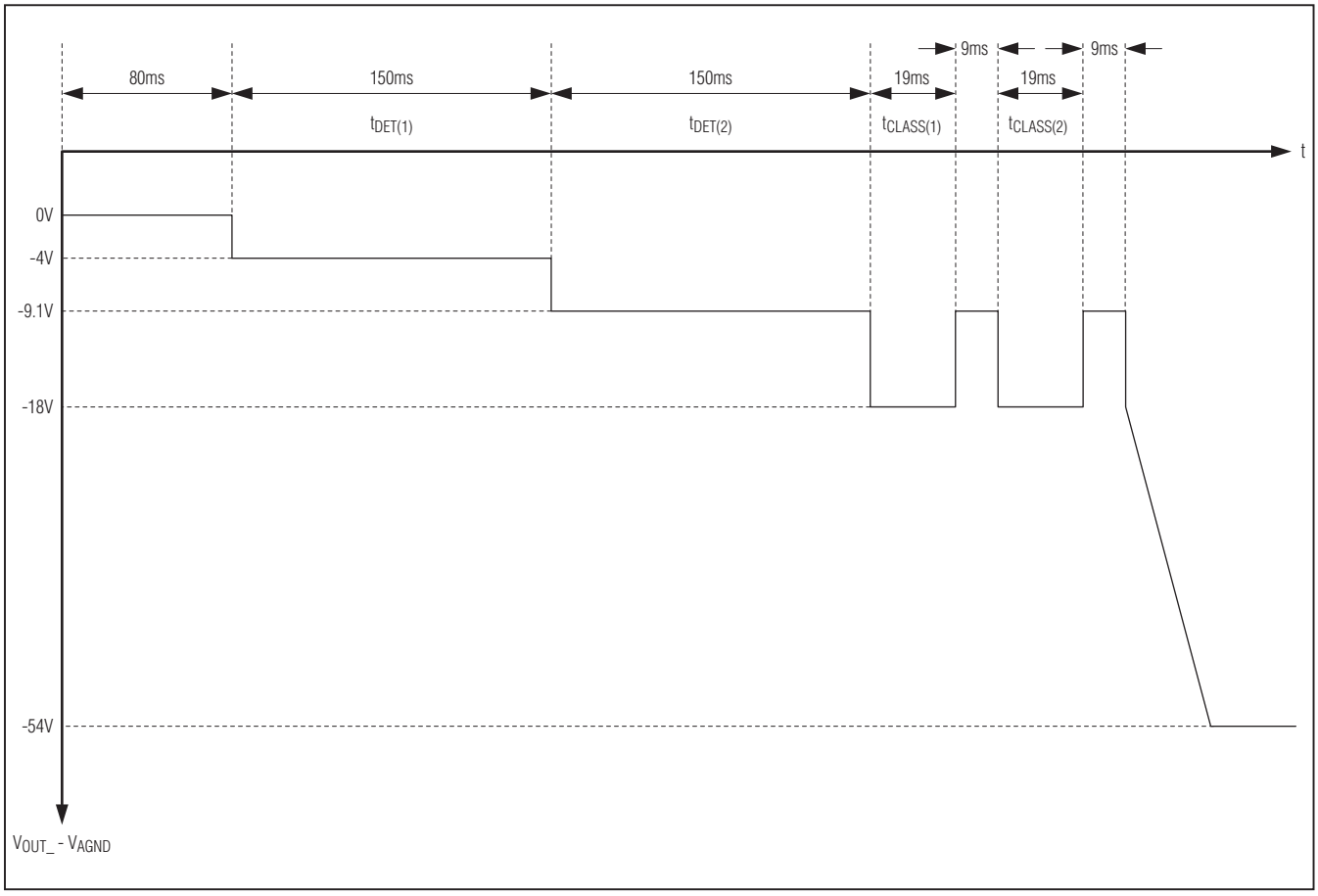

Figure 2. Detection, 2-Event Classification, and Port Power-Up Sequence

$V_{RSENSE\_}$ exceeds V_{CUT} and decreases at a slower pace when $V_{RSENSE\_}$ drops below V_{CUT}. A slower decrement for the t_{FAULT} counter allows for detecting repeated short-duration overcurrent conditions. When the counter reaches the t_{FAULT} limit, the device powers the port down and asserts the corresponding TCUT_ bit (R06h[3:0] and R07h[3:0], Table 10). For a continuous overstress, a fault latches exactly after a period of t_{FAULT}. V_{CUT} is programmable through the ICUT_ registers (Table 40). If a port is powered down due to a current-limit condition, during normal operation, the device asserts the corresponding ICV_ bit (R08h[7:4] and R09h[7:4], Table 11)

After power-off due to an overcurrent fault, the t_{FAULT} timer is not immediately reset but starts decrementing at the same slower pace. The device allows a port to be powered on only when the t_{FAULT} counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET to avoid overheating.

High-Power Mode

The device features individual, port programmable high-power settings. To enable the high-power configuration for a port, set the corresponding HP_EN_ bit (R44h[3:0], Table 38) to 1. By default, if AUTO = 1, the HP_EN_ bits will be set to 1 automatically after a reset event. When enabled, each port's high-power settings can be individually configured using the corresponding Port GPMD, Port Overcurrent (ICUT), Port Current-Limit (ILIM_), and Port High-Power Status registers (see the *Register Map and Description* section, Tables 39–42).

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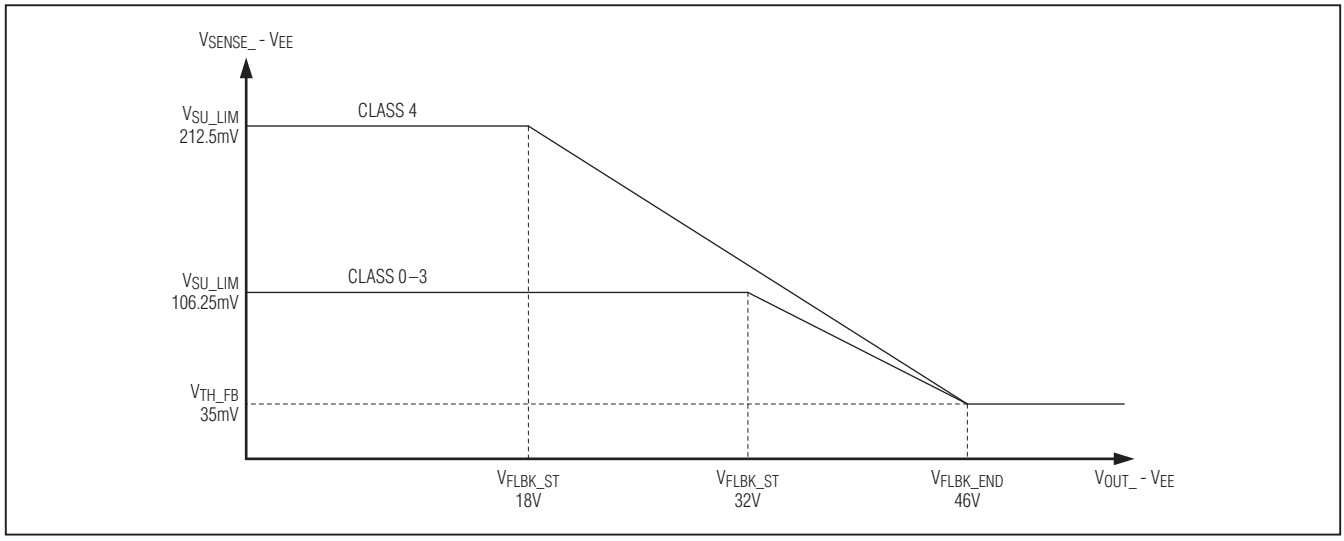

Figure 3. Foldback Current Characteristics

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUT_ and when necessary reduces the current-limit clamp voltage (V_{SU_LIM}) to help reduce the power dissipation through the external FET. When $I_{LIM\_}$ = 80h (Classes 0–3), foldback begins when $V_{OUT\_} - V_{EE} > 32V$; and when $I_{LIM\_}$ = C0h (Classes 4 and 5), foldback begins when $V_{OUT\_} - V_{EE} > 18V$. The V_{SU_LIM} eventually reduces down to the minimum current-limit threshold (V_{TH_FB} = 35mV) when $V_{OUT\_} - V_{EE} > 46V$ (Figure 3).

MOSFET Gate Driver

Connect the gate of the external n-channel MOSFET to GATE_. An internal 50µA current source pulls GATE_ to (V_{EE} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE_ to V_{EE} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT\_}}{\Delta t} = \frac{I_{GATE\_}}{C_{GD}}$$

where C_{GD} is the total capacitance between the gate and the drain of the external MOSFET. The current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the device manipulates the GATE_ voltage to control the voltage at SENSE_ ($V_{RSENSE\_}$). A fast pulldown activates if $V_{RSENSE\_}$ overshoots the limit threshold (V_{SU_LIM}). The fast pulldown current increases with the amount of overshoot, and the maximum fast pulldown current is 50mA.

During turn-off, when the GATE_ voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

Interrupt

The device contains an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. The Interrupt register (R00h, Table 6) contains the interrupt flag bits and the Interrupt Mask register (R01h, Table 7) determines which events can trigger an interrupt. When an event occurs, the appropriate Interrupt Event register bits (in R02h to R0Bh) and the corresponding interrupt (in R00h) are set to 1 and $\overline{INT}$ is asserted low (unless masked). If the master device on the I^2C bus sends out an Alert Response Address, any MAX5980 device on the bus that has $\overline{INT}$ asserted will respond (see the *Global Addressing and the Alert Response Address (ARA)* section).

As a response to an interrupt, the controller can read the status of the event register(s) to determine the cause of the interrupt and take appropriate action. Each interrupt event register is paired with a Clear-on-Read (CoR) register. When an interrupt event register is read through the corresponding CoR register, the corresponding event register is reset to 0 (clearing that interrupt event). $\overline{INT}$ remains low and the interrupt is not reset when the Interrupt Event register is read through the read-only address. For example, to clear a supply event fault read R0Bh (CoR) not R0Ah (read-only, see Table 12). Use the INT_CLR bit (R1Ah[7], Table 27) to clear an interrupt, or the RESET_IC bit (R1Ah[4]) to initiate software resets.

Undervoltage and Overvoltage Protection

The device contains undervoltage and overvoltage protection features, and the flag bits can be found in the Supply Event register (R0Ah and R0Bh, Table 12) and the Watchdog register (R42h, Table 36). An internal V_{EE} undervoltage lockout circuit keeps the MOSFET off and the device in reset until V_{AGND} - V_{EE} exceeds 28.5V for more than 3ms. An internal V_{EE} overvoltage circuit shuts down the ports when V_{AGND} - V_{EE} exceeds 62.5V. The digital supply also contains an undervoltage lockout that triggers when V_{DD} - $V_{EE} \leq 2V$.

DC Disconnect Monitoring

The DC disconnect monitoring settings are found in the Disconnect Enable register (R13h, Table 21). To enable DC disconnect, set either the ACD_EN_ or DCD_EN_ bit for the corresponding port to 1. To disable the DC disconnect monitoring, both the ACD_EN_ and DCD_EN_ bit for that port must be set to 0. When enabled, if $V_{RSENSE\_}$ (the voltage across $R_{SENSE\_}$) falls below the DC load disconnect threshold, V_{DCTH}, for more than t_{DISC}, the device turns off power and asserts the DIS_ bit for the corresponding port (R06h[7:4] and R07h[7:4], Table 10).

V_{DD} Power Supply

The device has an internally regulated, 3.3V digital supply that powers the internal logic circuitry. V_{DD} has an undervoltage lockout (V_{DD_UVLO}) of 2V, and an undervoltage condition on V_{DD} keeps the device in reset and the ports shut off. When V_{DD} has recovered and the reset condition clears, the VDD_UVLO bit in the Supply Event registers is set to 1 (R0Ah[5] and R0Bh[5], Table 12). The digital address inputs, AUTO, and MIDSPAN are internally pulled up to V_{DD}, and all digital inputs are referenced to DGND. V_{DD} can also be used to source up to 10mA for external circuitry. For internal regulator stability, connect a 1.8kΩ resistor in parallel with a 33nF capacitor at the V_{DD} output (Figure 4). If an external load is to be shared among multiple MAX5980 devices, isolate the external supply bus with a series resistor (50Ω for 3 devices, 75Ω for 4 devices), and place a single 1µF capacitor on the bus.

Hardware Power-Down

The EN digital input is referenced to DGND and is used for hardware level control of device power management. During normal operation, EN should be externally pulled directly up to V_{DD}, the 3.3V internal regulator output (see the *Typical Operating Circuit*).

To initiate a hardware reset and port power-down, pull EN to DGND for at least 100µs. While EN is held low, the device remains in reset and the ports remain securely powered down. Normal device operation resumes once EN is pulled up to the V_{DD}.

Thermal Shutdown

If the device's die temperature reaches +140°C (typ), an overtemperature fault is generated and the device shuts down. The die temperature must cool down below +120°C (typ) to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset and the TSD event bit is set to a logical 1 (R0Ah[7]/R0Bh[7], Table 12).

Watchdog

The Watchdog register (R42h, Table 36) is used to monitor device status, and to enable and monitor the watchdog functionality. On a power-up or after a reset condition, this register is set to a default value of 16h. WD_DIS[3:0] is set by default to 1011, disabling the watchdog timeout. Set WD_DIS[3:0] to any other value to enable the watchdog. The watchdog monitors the SCL line for activity. If there are no transitions for 2.5s (typ), the WD_STAT bit is set to 1 and all ports are powered down (using the individual port reset protocol). WD_STAT must be reset before any port can be reenabled.

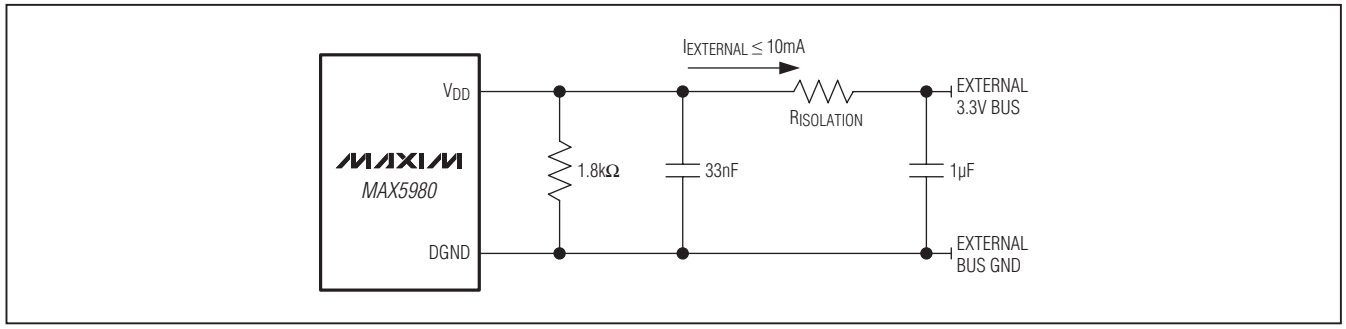

Figure 4. V_{DD} External Power Sourcing

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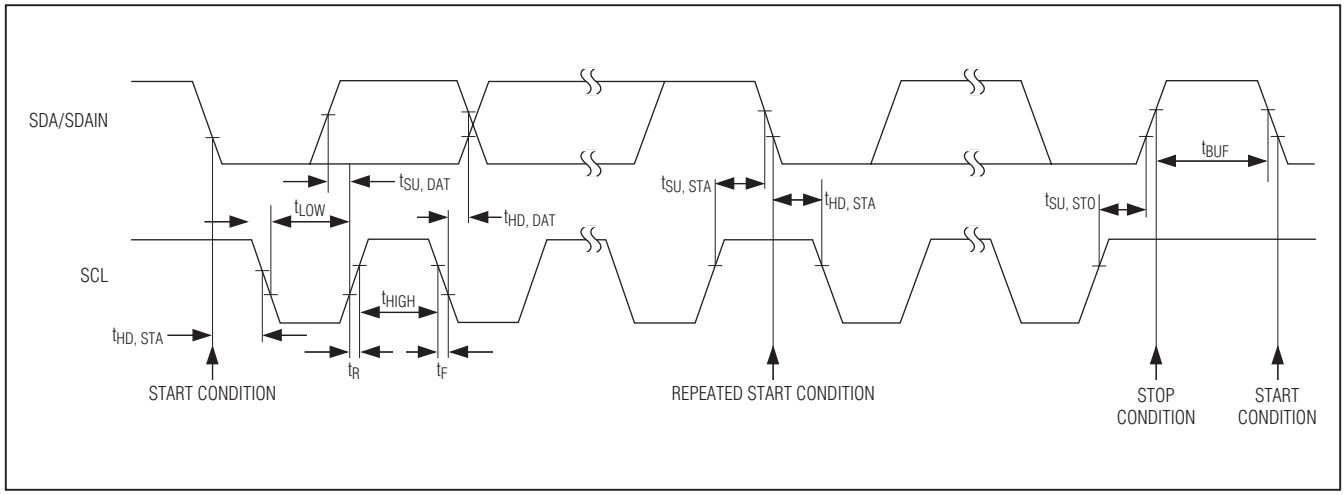

Figure 5. Serial Interface Timing Details

Table 3. Programmable Device Address Settings

DEVICE ADDRESS						
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**
0	1	0	A3	A2	A1	A0

Device Address (AD0)

The MAX5980 is programmable to 1 of 16 unique slave device addresses. The three MSBs of the device address are always [010]. The 4 LSBs of the device address are programmable, and are formed by the states of the Slave Address Inputs (A0, A1, A2, and A3; see Table 3). To program the device address, connect A0, A1, A2, and A3 to a combination of V_{DD} (logical 1) and DGND (logical 0), and initiate a device reset.

I²C-Compatible Serial Interface

The device operates as a slave that sends and receives data through an I²C-compatible, 2-wire or 3-wire interface. The interface uses a serial-data input line (SDAIN), a serial-data output line (SDAOUT), and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial-data line (SDA). Most of the figures shown label the bus as SDA.

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The device's SDAIN line operates as an input and SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDAOUT (3-wire mode) or SDA (2-wire mode). The SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

Serial Addressing

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus R/W bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission (see Figure 6).

Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5980, the device generates the acknowledge bit. When the device transmits to the master, the master generates the acknowledge bit.

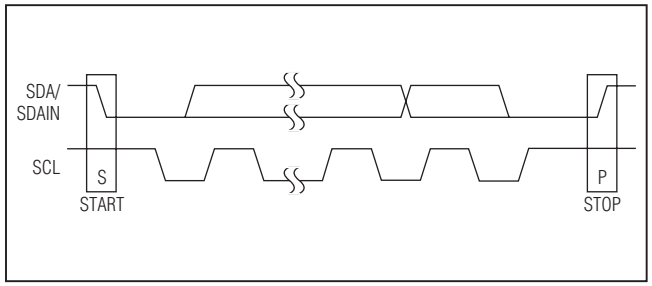

Figure 6. START and STOP Conditions

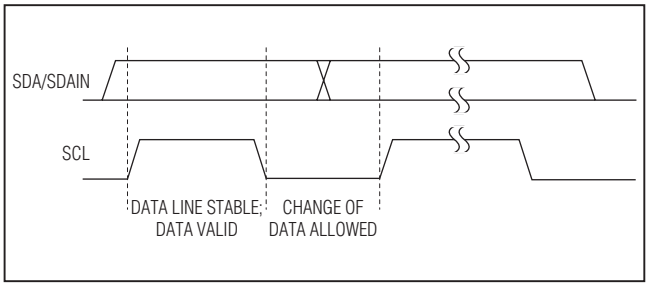

Figure 7. Bit Transfer

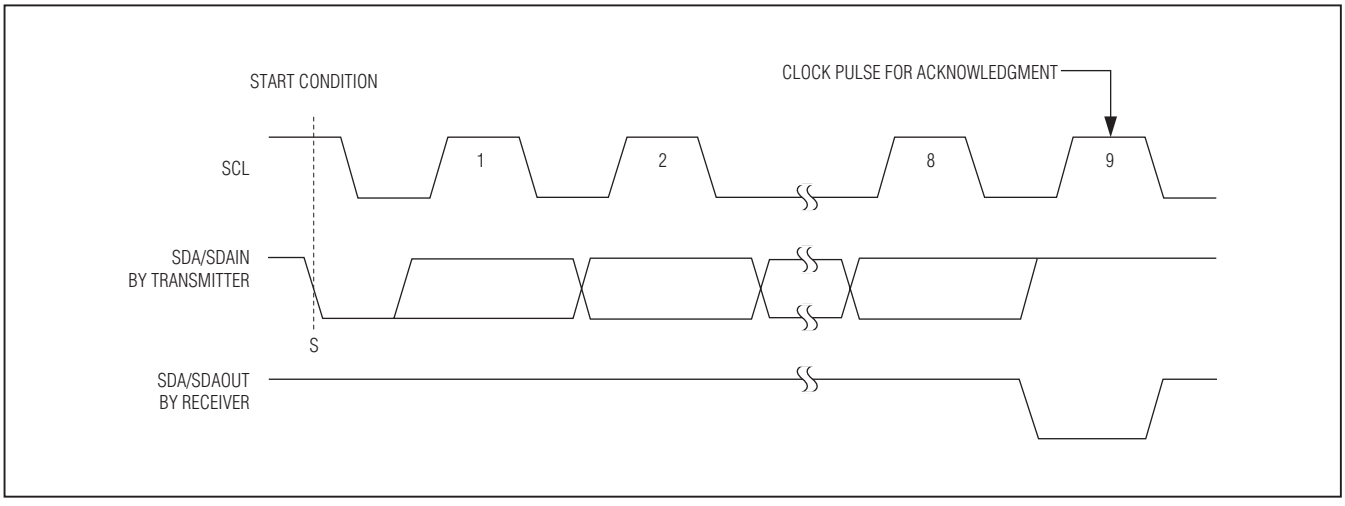

Figure 8. Acknowledge

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Slave Address

The device has a 7-bit long slave address (Figure 9). The bit following the 7-bit slave address (bit eight) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The upper five bits of the slave address cannot be changed and are always [01000]. Using the AD0 input, the lowest two bits can be programmed to assign the device one of four unique slave addresses (see Table 3). The device monitors the bus continuously, waiting for a START condition followed by the device's slave address. When a device recognizes its slave address, it acknowledges and is then ready for continued communication.

Global Addressing and the Alert Reponse Address (ARA)

The global address call is used in write mode to write to the same register to multiple devices (address 60h). The global address call can also be used in read mode (61h) in the same way as the alert response address (ARA). The actual alert response address (ARA) is 0Ch. The MAX5980 slave device only responds to the ARA if its $\overline{INT}$ (interrupt) output is asserted. All MAX5980 devices in which the $\overline{INT}$ output is not asserted ignore the ARA.

When responding to the ARA, the device transmits a byte of data on SDAOUT containing its own address in the top 7 bits, and a 1 in the LSB (as does every other device connected to the SDAIN line that has an active interrupt). As each bit in the byte is transmitted, the device determines whether to continue transmitting the remainder of the byte or terminate transmission. The device terminates the transmission if it sees a 0 on SDA at a time when it is attempting to send a 1; otherwise it continues transmitting bits until the entire byte has been sent. This litigation protocol always allows the part with the lowest address to complete the transmission, and the microcontroller can respond to that interrupt. The device deasserts $\overline{INT}$ if it completes the transmission of the entire byte. If the device did not have the lowest address, and terminates the transmission early, the $\overline{INT}$ output remains asserted. In this way, the microcontroller can continue to send ARA read cycles until all slave devices successfully transmit their addresses, and all interrupt requests are resolved.

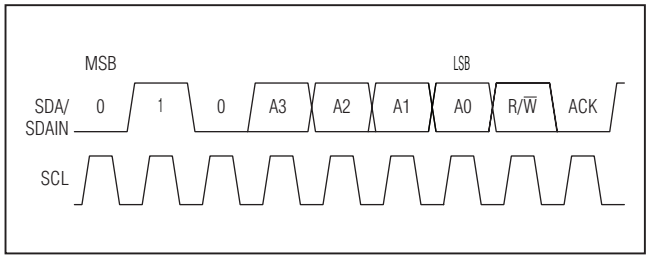

Figure 9. Slave Address

General Call

In compliance with the I²C specification, the device responds to the general call through global address 30h.

Message Format for Writing to the MAX5980

A write to the device comprises the device slave address transmission with the R$\overline{W}$ bit set to 0, followed by at least 1 byte of information. The first byte of information is the command byte (Figure 10). The command byte determines which register of the device is written to by the next byte, if received. If the device detects a STOP condition after receiving the command byte but before receiving any data, then the device takes no further action beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the device selected by the command byte (Figure 11). The control byte address then autoincrements (if possible; see Table 4) and then waits for the next data byte or a STOP condition.

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are stored in subsequent MAX5980 internal registers as the control byte address autoincrements (Figure 12). If the control byte address can no longer increment, any subsequent data sent continues to write to that address.

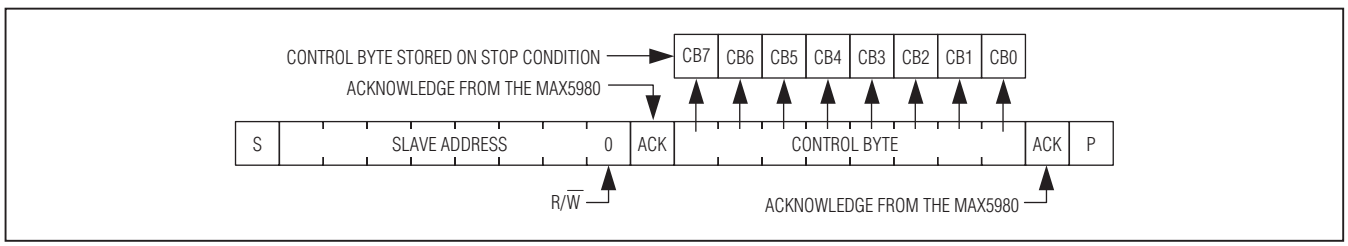

Figure 10. Write Format, Control Byte Received

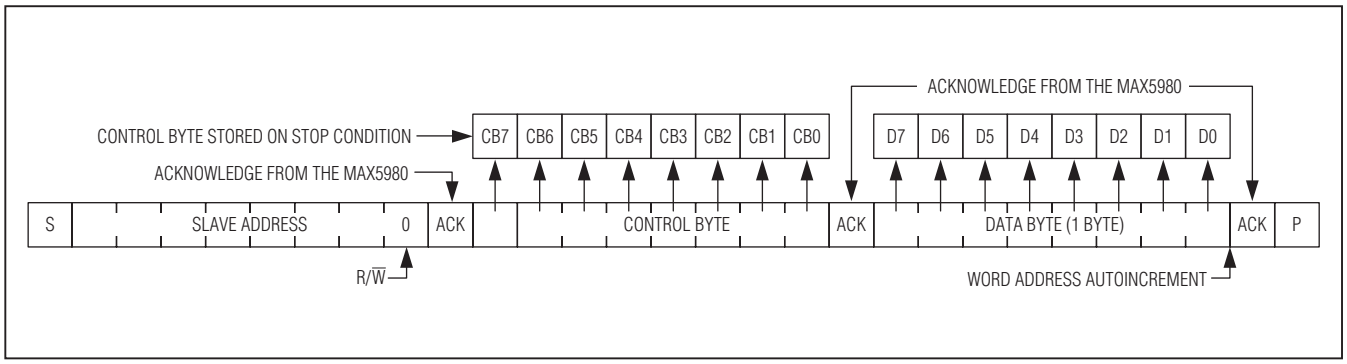

Figure 11. Write Format, Control, and Single Data Byte Written

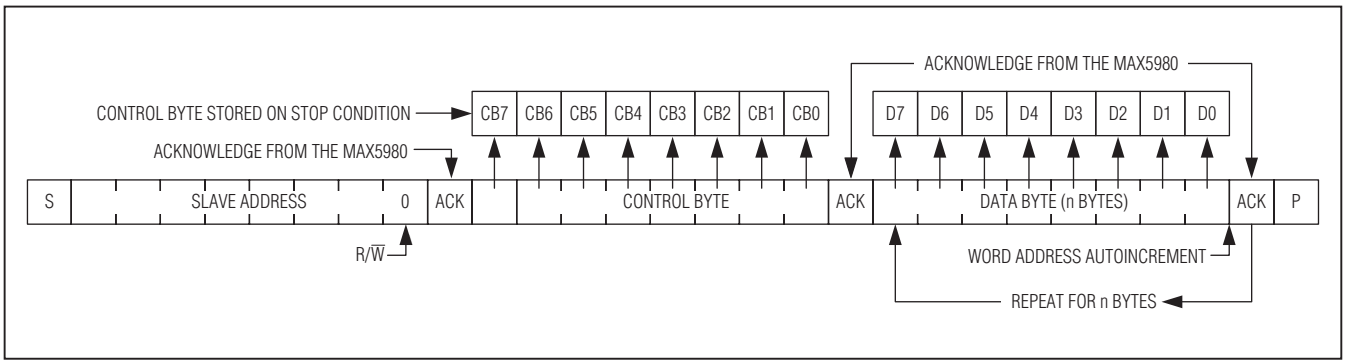

Figure 12. Write Format, Control, and n Data Bytes Written

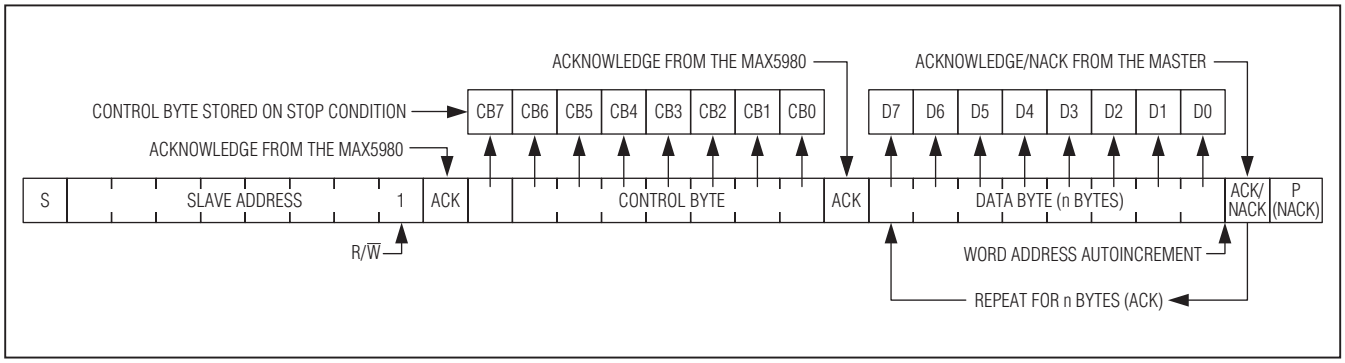

Figure 13. Read Format, Control, and n Data Bytes Read

Message Format for Reading

A read command for the device comprises the device slave address transmission with the R/$\overline{W}$ bit set to 1, followed by at least 1 byte of information. As with a write command, the first byte of information is the command byte. The device then reads using the internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. This pointer autoincrements after reading each data byte using the same rules as for a write, though the master now sends the acknowledge bit after each read receipt (Figure 13). When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address autoincrements after the write.