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MAXIM

# I²C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller



## General Description

The MAX6917 provides all the features of a real-time clock (RTC) plus a microprocessor (µP) supervisory circuit, NV RAM controller, and backup-battery monitor function. In addition, 96 x 8 bits of static RAM are available for scratchpad storage. The MAX6917 communicates with a µP through an I²C-bus-compatible serial interface.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap years through 2099. The clock operates in either 24hr or 12hr format with an AM/PM indicator. A time/date-programmable alarm function is provided with an open-drain, active-low alarm output.

The µP supervisory circuit features an open-drain, active-low reset available in three different reset thresholds. A manual reset input and a watchdog function are included as well.

The NV RAM controller provides power for external SRAM from a backup battery plus chip-enable gating. The backup battery also provides data retention of the on-board 96 x 8 bits of RAM. An open-drain, active-low, battery-on signal alerts the system when operating from a battery.

The battery-test circuitry periodically tests the backup battery for a low-battery condition. An optional external resistor network selects different battery thresholds. A freshness seal prevents battery drain until the first $V_{CC}$ power-up.

The MAX6917 has a crystal-fail-detect circuit and a data-valid bit. The MAX6917 is available in a 20-pin QSOP package and is guaranteed to operate over the extended (-40°C to +85°C) temperature range.

## Applications

Point-of-Sale Equipment

Programmable Logic Controllers

Intelligent Instruments

Fax Machines

Digital Thermostats

Industrial Control

***Pin Configuration and Selector Guide appear at end of data sheet.***

## Features

- **Real-Time Clock Counts**
  **Seconds, Minutes, Hours, Date, Month, Day of Week, and Year with Leap-Year Compensation Through 2099**
- **Fast (400kHz) I²C-Bus-Compatible Interface**
- **96 x 8 Bits of RAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 6pF Load, Watch Crystal**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or RAM**
- **Battery Monitor and Low-Battery Warning Output**
  **Internal Default for Lithium Backup-Battery Testing**
  **Pins Available for Other Backup-Battery Testing Configurations**
- **Dual Power-Supply Pins for Primary and Backup Power**
- **Battery-On Output**
- **NV RAM Controller**
  **Chip-Enable Gating (Control of $\overline{CE}$ with Reset and Power Valid)**
  **$V_{OUT}$ for SRAM Power**
- **Microprocessor Supervisor with Watchdog Input**
- **Programmable Time/Date Alarm Output**
- **Data Valid Bit (Loss of All Voltage Alerts User of Corrupt Data)**
- **Crystal-Fail Detect**
- **Reference Output Frequencies—1Hz and 32.768kHz**
- **Small, 20-Pin, QSOP Surface-Mount Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| MAX6917EO30+ | -40°C to +85°C | 20 QSOP | E20-2 |
| MAX6917EO33+ | -40°C to +85°C | 20 QSOP | E20-2 |
| MAX6917EO50+ | -40°C to +85°C | 20 QSOP | E20-2 |

*+Denotes lead-free package.*

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

## ABSOLUTE MAXIMUM RATINGS

$V_{BATT}$, $V_{CC}$ to GND .....-0.3V to +6.0V
All Other Pins to GND .....-0.3V to ($V_{CC}$ + 0.3V)
All Other Pins to GND .....-0.3V to ($V_{BATT}$ + 0.3V)
Input Currents
$V_{CC}$ .....200mA
$V_{BATT}$ .....20mA
GND .....20mA
All Other Pins .....±20mA
Output Currents
$V_{OUT}$ Continuous .....200mA
All Other Outputs .....20mA
Continuous Power Dissipation
20-Pin QSOP (derate 9.1mW/°C over $T_A$ = +70°C) .....727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range (Note 3) | $V_{CC}$ | MAX6917EO30 | | 2.7 | 3.0 | 3.3 | V |
| | | MAX6917EO33 | | 3.0 | 3.3 | 3.6 | |
| | | MAX6917EO50 | | 4.5 | 5.0 | 5.5 | |
| Operating Voltage Range BATT (Note 4) | $V_{BATT}$ | MAX6917EO30 | | 2.0 | | 5.5 | V |
| | | MAX6917EO33 | | 2.0 | | 5.5 | |
| | | MAX6917EO50 | | 2.0 | | 5.5 | |
| Timekeeping Current $V_{BATT}$ (Note 5) | $I_{BATT}$ | 1Hz, 32kHz outputs disabled; XTAL FAIL disabled | $V_{BATT}$ = 2V, $V_{CC}$ = 0 | | | 1 | µA |
| | | | $V_{BATT}$ = 3V, $V_{CC}$ = 0 | | | 1.4 | |
| | | | $V_{BATT}$ = 3.6V, $V_{CC}$ = 0 | | | 1.9 | |
| | | | $V_{BATT}$ = 5.5V, $V_{CC}$ = 0 | | | 3.8 | |
| | | 1Hz, 32kHz outputs disabled; XTAL FAIL enabled | $V_{BATT}$ = 2V, $V_{CC}$ = 0 | | | 1.23 | |
| | | | $V_{BATT}$ = 3V, $V_{CC}$ = 0 | | | 1.61 | |
| | | | $V_{BATT}$ = 3.6V, $V_{CC}$ = 0 | | | 2.3 | |
| | | | $V_{BATT}$ = 5.5V, $V_{CC}$ = 0 | | | 4.08 | |
| | | 1Hz, 32kHz enabled, outputs open; XTAL FAIL disabled | $V_{BATT}$ = 2V, $V_{CC}$ = 0 | | | 2.82 | |
| | | | $V_{BATT}$ = 3V, $V_{CC}$ = 0 | | | 4.7 | |
| | | | $V_{BATT}$ = 3.6V, $V_{CC}$ = 0 | | | 6.1 | |
| | | | $V_{BATT}$ = 5.5V, $V_{CC}$ = 0 | | | 10.6 | |
| Active Supply Current $V_{CC}$ (Note 6) | $I_{CCA}$ | 1Hz, 32kHz enabled, outputs open; XTAL FAIL enabled | $V_{CC}$ = 3.3V, $V_{BATT}$ = 0 | | | 0.1 | mA |
| | | | $V_{CC}$ = 3.6V, $V_{BATT}$ = 0 | | | 0.12 | |
| | | | $V_{CC}$ = 5.5V, $V_{BATT}$ = 0 | | | 0.2 | |
| | | 1Hz, 32kHz outputs disabled; XTAL FAIL disabled | $V_{CC}$ = 3.3V, $V_{BATT}$ = 0 | | | 0.9 | |
| | | | $V_{CC}$ = 3.6V, $V_{BATT}$ = 0 | | | 0.11 | |
| | | | $V_{CC}$ = 5.5V, $V_{BATT}$ = 0 | | | 0.18 | |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Standby Current $V_{CC}$ (Note 5) | $I_{CCS}$ | 1Hz, 32kHz enabled, outputs open; XTAL FAIL enabled | $V_{CC}$ = 3.3V, $V_{BATT}$ = 0 | | | 27 | µA |
| | | | $V_{CC}$ = 3.6V, $V_{BATT}$ = 0 | | | 30 | |
| | | | $V_{CC}$ = 5.5V, $V_{BATT}$ = 0 | | | 81 | |
| | | 1Hz, 32kHz outputs disabled; XTAL FAIL disabled | $V_{CC}$ = 3.3V, $V_{BATT}$ = 0 | | | 20 | |
| | | | $V_{CC}$ = 3.6V, $V_{BATT}$ = 0 | | | 25 | |
| | | | $V_{CC}$ = 5.5V, $V_{BATT}$ = 0 | | | 76 | |
| **$V_{OUT}$** | | | | | | | |
| $V_{OUT}$ in $V_{CC}$ Mode (Note 4) | $V_{OUT}$ | $V_{CC}$ = 2.7V, $V_{BATT}$ = 0, $I_{OUT}$ = 35mA | | $V_{CC}$ - 0.2 | | | V |
| | | $V_{CC}$ = 3.0V, $V_{BATT}$ = 0, $I_{OUT}$ = 35mA | | $V_{CC}$ - 0.2 | | | |
| | | $V_{CC}$ = 4.5V, $V_{BATT}$ = 0, $I_{OUT}$ = 70mA | | $V_{CC}$ - 0.2 | | | |
| $V_{OUT}$ in Battery-Backup Mode (Notes 4, 7) | $V_{OUT}$ | $V_{BATT}$ = 2V, $V_{CC}$ = 0, $I_{OUT}$ = 400µA | | $V_{BATT}$ - 0.02 | | | V |
| | | $V_{BATT}$ = 3V, $V_{CC}$ = 0, $I_{OUT}$ = 800µA | | $V_{BATT}$ - 0.03 | | | |
| | | $V_{BATT}$ = 4.5V, $V_{CC}$ = 0, $I_{OUT}$ = 1.5mA | | $V_{BATT}$ - 0.05 | | | |
| $V_{BATT}$-to-$V_{CC}$ Switchover Threshold | $V_{TRU}$ | Power-up ($V_{CC}$ < $V_{RST}$) switch from $V_{BATT}$ to $V_{CC}$ (Note 7) | | | $V_{BATT}$ + 0.1 | | V |
| $V_{CC}$-to-$V_{BATT}$ Switchover Threshold | $V_{TRD}$ | Power-down ($V_{CC}$ < $V_{RST}$) switch from $V_{CC}$ to $V_{BATT}$ (Note 7) | | | VBATT - 0.1 | | V |
| **$\overline{CE\_IN}$ AND $\overline{CE\_OUT}$ (Figures 10, 14, 15, 16)** | | | | | | | |
| $\overline{CE\_IN}$ Leakage Current | IIL, IIH | Disabled, $V_{CC}$ < $V_{RST}$, $V_{\overline{CE\_IN}}$ = VCC or GND | | -1 | | +1 | µA |
| $\overline{CE\_IN}$-to-$\overline{CE\_OUT}$ Resistance | | $V_{CC}$ = $V_{CC(MIN)}$, $V_{IH}$ = 0.9$V_{CC}$, $\overline{CE\_OUT}$ connected to GND; VIL = 0.1VCC, $\overline{CE\_OUT}$ connected to VCC | | | 46 | 140 | Ω |
| $\overline{CE\_IN}$-to-$\overline{CE\_OUT}$ Propagation Delay | $t_{CED}$ | 50Ω source-impedance driver, $C_{LOAD}$ = 10pF, $V_{CC}$ = $V_{CC(MIN)}$, $V_{IH}$ = 0.9$V_{CC}$, $V_{IL}$ = 0.1$V_{CC}$ (Note 8); measured from 50% point on $\overline{CE\_IN}$ to the 50% point of $\overline{CE\_OUT}$ | | | 10 | 20 | ns |
| $\overline{RESET}$ Active to $\overline{CE\_OUT}$ High Delay | $t_{RCE}$ | $\overline{MR}$ high to low | | 2 | 10 | 50 | µs |

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $\overline{CE\_OUT}$ Active-Low Delay After $V_{CC} > V_{RST}$ | $t_{RP}$ | | 140 | 200 | 280 | ms |
| $\overline{CE\_OUT}$ High Voltage | $V_{OH}$ | $I_{OH}$ = -100µA, $V_{BATT}$ = 2V, $V_{CC}$ = 0, $\overline{RESET}$ = low | 0.8 x $V_{BATT}$ | | | V |
| **$\overline{MR}$ INPUT (Figure 10)** | | | | | | |
| $\overline{MR}$ Input Voltage | $V_{IL}$ | | | | 0.8 | V |
| | $V_{IH}$ | | 2.0 | | | |
| $\overline{MR}$ Pullup Resistance | | Internal pullup resistor | | 50 | | kΩ |
| $\overline{MR}$ Minimum Pulse Width | | | 1 | | | µs |
| $\overline{MR}$ Glitch Immunity | $t_{GW}$ | | | | 35 | ns |
| $\overline{MR}$ to $\overline{RESET}$ Delay | $t_{RD}$ | $V_{CC}$ = $V_{CC(MIN)}$, $V_{BATT}$ = 0 | | 450 | 600 | ns |
| **WDI INPUT (Figure 12)** | | | | | | |
| WDI Initial Timeout Period | | $V_{CC} > V_{RST}$ from rising edge of $\overline{RESET}$ | 1.00 | 1.6 | 2.25 | s |
| Watchdog Timeout Period | $t_{WDL}$ | Long watchdog timeout period | 1.00 | 1.6 | 2.25 | s |
| | $t_{WDS}$ | Short watchdog timeout period | 140 | 200 | 280 | ms |
| Minimum WDI Input Pulse Width | $t_{WDI}$ | | 100 | | | ns |
| WDI Input Threshold | $V_{IL}$ | | | | 0.8 | V |
| | $V_{IH}$ | | 2.0 | | | |
| WDI Input-Leakage Current | | $V_{WDI}$ = $V_{CC}$ or GND | -100 | | +100 | nA |
| $V_{CC}$ Standby Current with WDI Max Frequency | $I_{CCSW}$ | Watchdog frequency = 1MHz, $V_{CC}$ = $V_{CC(MAX)}$, 1Hz, 32kHz outputs disabled (Note 5) | | | 450 | µA |
| **BATTERY TEST AND TRIP (Figures 17, 18, and 19)** | | | | | | |
| $V_{BATT}$ Trip Point | $V_{BTP}$ | Internal mode | 2.45 | 2.6 | 2.70 | V |
| TRIP Input Threshold | $V_{TRIP}$ | $V_{CC}$ = $V_{CC(MAX)}$, $V_{BATT}$ = 2V, external mode | 1.14 | 1.24 | 1.31 | V |
| TRIP Input Comparator Hysteresis | $V_{TRIP\_HYST}$ | | | 10 | | mV |
| TRIP Input Current | $I_{TRIP\_LKG}$ | External mode | -100 | | +100 | nA |
| Battery Test Load | $R_{LOAD\_INT}$ | Internal | 0.50 | 0.91 | 1.30 | MΩ |
| TEST Output-High Voltage | $V_{TEST\_HIGH}$ | $I_{TEST}$ = -5mA | $V_{OUT}$ - 0.3V | | | V |
| TEST Output-Low Voltage | $V_{TEST\_LOW}$ | $I_{TEST}$ = 5mA | | | 0.3 | V |
| **$\overline{BATT\_LO}$, $\overline{ALM}$ OUTPUT** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $V_{BATT}$ = 2V, $V_{CC}$ = 0, $I_{OL}$ = 5mA | | | 0.5 | V |
| | | $V_{CC}$ = 2.7V, $V_{BATT}$ = 0, $I_{OL}$ = 10mA | | | 0.5 | |
| | | $V_{CC}$ = 4.5V, $V_{BATT}$ = 0, $I_{OL}$ = 20mA | | | 0.5 | |
| Off-Leakage | $I_{LKG}$ | | -100 | | +100 | nA |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$\overline{BATT}$_$\overline{ON}$ OUTPUT** | | | | | | | |
| Output Low Voltage | $V_{OL}$ | $V_{BATT}$ = 2V, $V_{CC}$ = 0, $I_{OL}$ = 5mA | | | | 0.5 | V |
| | | $V_{BATT}$ = 2.7V, $V_{CC}$ = 0, $I_{OL}$ = 10mA | | | | 0.5 | |
| | | $V_{BATT}$ = 4.5V, $V_{CC}$ = 0, $I_{OL}$ = 20mA | | | | 0.5 | |
| Off-Leakage | $I_{LKG}$ | | | -100 | | +100 | nA |
| **$\overline{RESET}$** | | | | | | | |
| $\overline{RESET}$ Threshold Voltage | $V_{RST}$ | MAX6917EO30 | | 2.5 | 2.63 | 2.7 | V |
| | | MAX6917EO33 | | 2.8 | 2.93 | 3.0 | |
| | | MAX6917EO50 | | 4.1 | 4.38 | 4.5 | |
| $V_{RST}$ Hysteresis | $V_{HYST}$ | | | | 30 | | mV |
| $V_{CC}$ Falling-Reset Delay | $t_{RPD}$ | $V_{CC}$ falling from $V_{RST(MAX)}$ to $V_{RST(MIN)}$, measured from the beginning of $V_{CC}$ falling to $\overline{RESET}$ low | MAX6917EO30 | | 27 | 75 | µs |
| | | | MAX6917EO33 | | 37 | 90 | |
| | | | MAX6917EO50 | | 50 | 120 | |
| Main Reset Active-Timeout Period | $t_{RP}$ | | | 140 | 200 | 280 | ms |
| $\overline{RESET}$ Output Voltage | $V_{OL}$ | $\overline{RESET}$ asserted, $I_{OL}$ = 1.6mA, $V_{BATT}$ = 2V, $V_{CC}$ = 0 | | | | 0.2 | V |
| Off-Leakage | $I_{LKG}$ | | | -100 | | +100 | nA |
| **I²C DIGITAL INPUTS SCL, SDA** | | | | | | | |
| Input High Voltage | $V_{IH}$ | | | 0.7 x $V_{CC}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | | 0.3 x $V_{CC}$ | V |
| Input Hysteresis | $V_{HYS}$ | | | | 0.05 x $V_{CC}$ | | V |
| Input Leakage Current | | $V_{IN}$ = 0 to $V_{CC}$ | | -100 | | +100 | nA |
| Input Capacitance | | (Note 8) | | | | 10 | pF |
| SDA Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4mA, $V_{CC}$ = $V_{CC(MIN)}$ | | | | 0.4 | V |
| **FREQUENCY OUTPUTS (32kHz and 1Hz)** | | | | | | | |
| 32kHz and 1Hz OUT Low Voltage | $V_{OL}$ | $V_{CC}$ = 0, $V_{BATT}$ = 2V, $I_{OL}$ = 100µA | | | | 0.2 | V |
| | | $V_{CC}$ = 2.7V, $V_{BATT}$ = 0, $I_{OL}$ = 1mA | | | | 0.4 | |
| | | $V_{CC}$ = 4.5V, $V_{BATT}$ = 0, $I_{OL}$ = 2mA | | | | 0.5 | |

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| 32kHz and 1Hz OUT High Voltage | $V_{OH}$ | $V_{CC}$ = 0, $V_{BATT}$ = 2V, $I_{OH}$ = -100µA | $V_{OUT}$ - 0.1V | | | V |
| | | $V_{CC}$ = 2.7V, $V_{BATT}$ = 0, $I_{OH}$ = -1mA | $V_{OUT}$ - 0.3V | | | |
| | | $V_{CC}$ = 4.5V, $V_{BATT}$ = 0, $I_{OH}$ = -2mA | $V_{OUT}$ - 0.4V | | | |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FAST I²C-BUS TIMING (Figure 2 (Note 9))** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | (Note 10) | 800 | | 400,000 | Hz |
| Bus Timeout | $t_{TIMEOUT}$ | | 1 | | 2 | s |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time After (Repeated) START Conditions | $t_{HD:STA}$ | After this period, the first clock is generated | 0.6 | | | µs |
| Repeated START Condition Setup Time | $t_{HD:STA}$ | | 0.6 | | | µs |
| STOP Condition Setup Time | $t_{SU:STO}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD:DAT}$ | (Notes 11, 14) | 0 | | 0.9 | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| SCL Low Period | $t_{LOW}$ | | 1.3 | | | µs |
| SCL High Period | $t_{HIGH}$ | | 0.6 | | | µs |
| SCL/SDA Rise Time (Receiving) | $t_R$ | (Note 12) | $20 + 0.1 \times C_b$ | | 300 | ns |
| SCL/SDA Fall Time (Receiving) | $t_F$ | (Notes 12, 13) | $20 + 0.1 \times C_b$ | | 300 | ns |
| SCL/SDA Fall Time (Transmitting) | $t_F$ | (Notes 12, 13) | $20 + 0.1 \times C_b$ | | 250 | ns |
| Pulse Width of Spike Suppressed | $t_{SP}$ | | 0 | | 50 | ns |
| Capacitive Load for Each Bus Line | $C_b$ | | | | 400 | pF |
| **BATTERY-TEST TIMING (Figure 18)** | | | | | | |
| Battery Test to $\overline{BATT\_LO}$ Active | $t_{BL}$ | (Note 8) | | | 1 | s |
| Battery-Test Cycle—Normal | $t_{BTCN}$ | (Note 8) | | 24 | | hr |
| Battery-Test Pulse Width | $t_{BTPW}$ | (Note 8) | | | 1 | s |

**Note 1:** $V_{RST}$ is the reset threshold for $V_{CC}$. See the *Selector Guide* section.

**Note 2:** All parameters are 100% tested at $T_A$ = +85°C. Limits overtemperature are guaranteed by design and are not production tested.

## AC ELECTRICAL CHARACTERISTICS (continued)

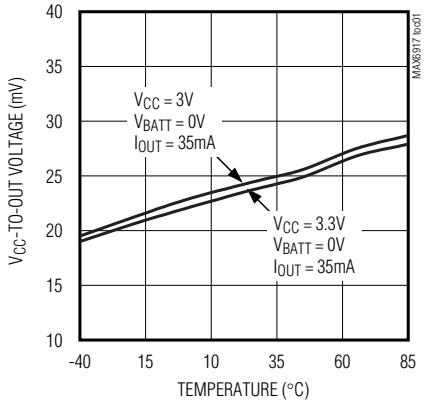
($V_{CC}$ = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

**Note 3:** $I^2C$ serial interface is operational for $V_{CC}$ > $V_{RST}$.
**Note 4:** See the *Detailed Description* section ($V_{OUT}$ function).
**Note 5:** $I_{BATT}$ is specified with SDA = SCL = $V_{CC}$, $\overline{CE\_IN}$ = WDI = GND, $V_{OUT}$ , $\overline{CE\_OUT}$, and $\overline{MR}$ floating. $I_{CCS}$ is specified with SDA = SCL = $V_{CC}$, $\overline{CE\_IN}$ = WDI = GND, $V_{OUT}$, $\overline{CE\_OUT}$, and $\overline{MR}$ floating.
**Note 6:** $I^2C$ serial interface operating at 400kHz, SDA pulled high, and WDI = $V_{CC}$ or GND, $V_{OUT}$ and $\overline{CE\_OUT}$ floating.
**Note 7:** For OUT switchover to BATT, $V_{CC}$ must fall below $V_{RST}$ and $V_{BATT}$. For OUT switchover to $V_{CC}$, $V_{CC}$ must be above $V_{RST}$ or above $V_{BATT}$.
**Note 8:** Guaranteed by design. Not subject to production testing.
**Note 9:** All values are referred to $V_{IH\ (MIN)}$ and $V_{IL(MAX)}$ levels.
**Note 10:** Minimum SCL clock frequency is limited by the MAX6917 bus timeout feature, which resets the serial bus interface if either SDA or SCL is held low for 1s to 2s. When using the burst read or write command, all 96 bytes of RAM must be read/written within the timeout period. See the *Timeout Feature* section.
**Note 11:** A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
**Note 12:** $C_b$ is the total capacitance of one bus line in pF.
**Note 13:** The maximum $t_F$ for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage $t_F$ is specified at 250ns. This allows series-protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_F$.
**Note 14:** The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal.

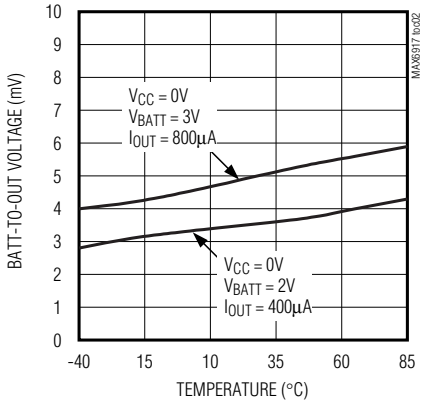
## Typical Operating Characteristics

($V_{CC}$ = 3V, $V_{BATT}$ = 3V, $T_A$ = +25°C, unless otherwise noted.)

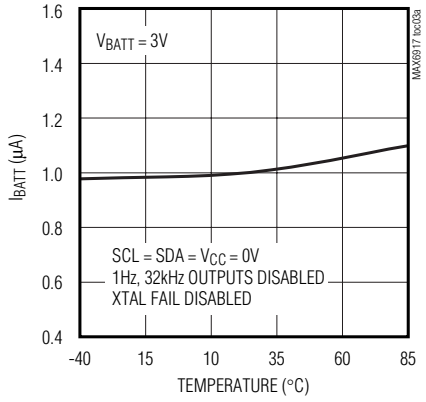
**$V_{CC}$-TO-OUT VOLTAGE vs. TEMPERATURE**



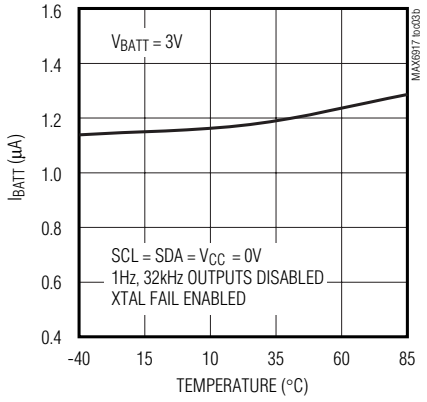

**BATT-TO-OUT VOLTAGE vs. TEMPERATURE**




**TIMEKEEPING CURRENT vs. TEMPERATURE**




**TIMEKEEPING CURRENT vs. TEMPERATURE**

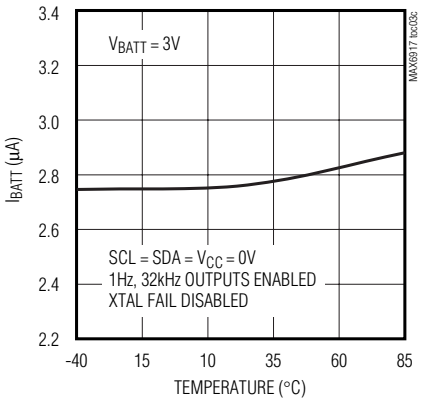


# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

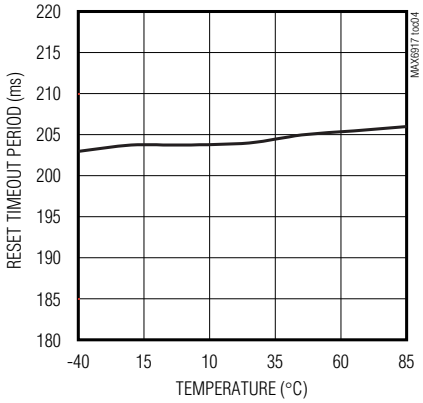
## Typical Operating Characteristics (continued)

($V_{CC}$ = 3V, $V_{BATT}$ = 3V, $T_A$ = +25°C, unless otherwise noted.)

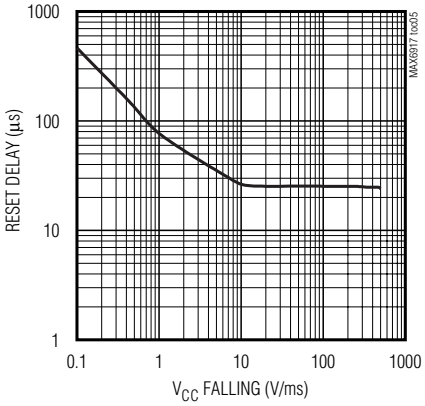
**TIMEKEEPING CURRENT vs. TEMPERATURE**



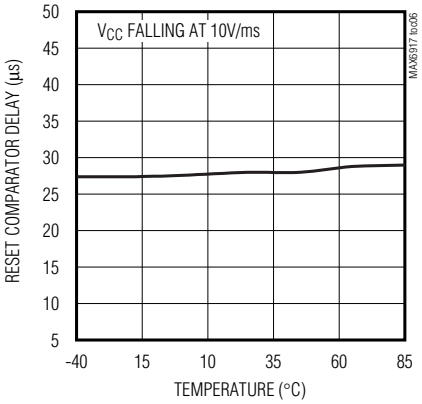

**RESET TIMEOUT PERIOD vs. TEMPERATURE**



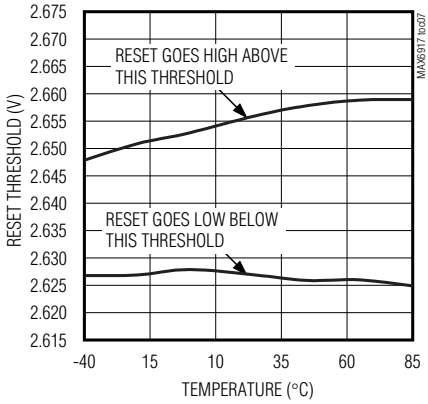

**RESET COMPARATOR DELAY vs. $V_{CC}$ FALLING**



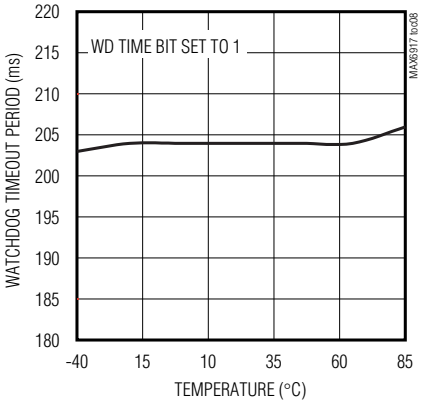

**RESET COMPARATOR DELAY vs. TEMPERATURE**



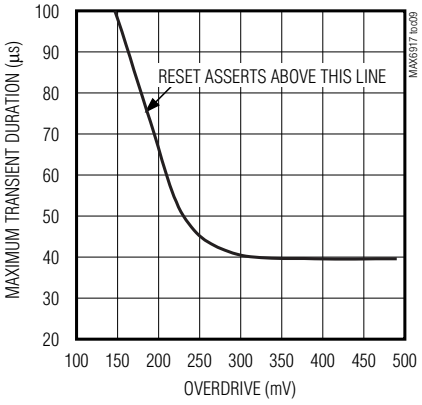

**RESET THRESHOLD vs. TEMPERATURE (MAX6917E030)**



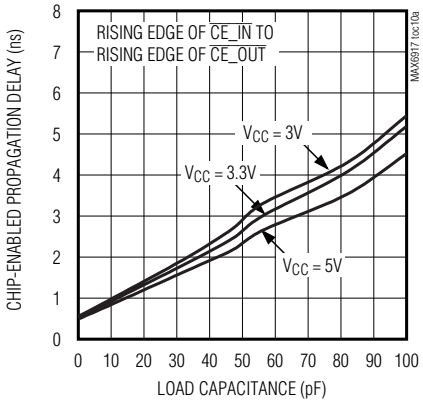

**WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE**



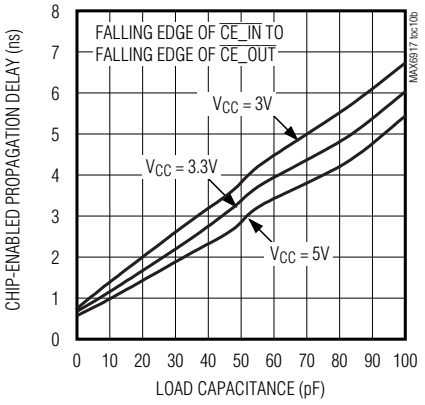

**MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE**




**CHIP-ENABLED PROPAGATION DELAY vs. CE_OUT LOAD CAPACITANCE**



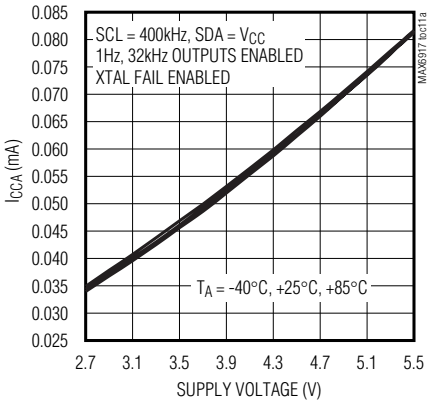

**CHIP-ENABLED PROPAGATION DELAY vs. CE_OUT LOAD CAPACITANCE**



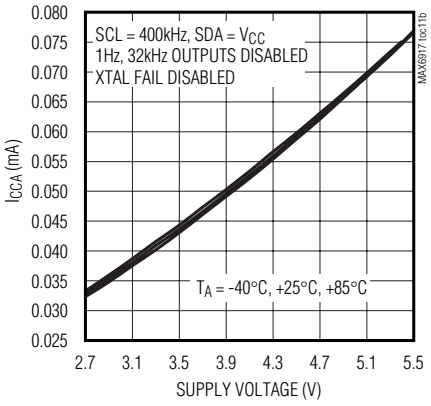
## Typical Operating Characteristics (continued)

($V_{CC}$ = 3V, $V_{BATT}$ = 3V, $T_A$ = +25°C, unless otherwise noted.)

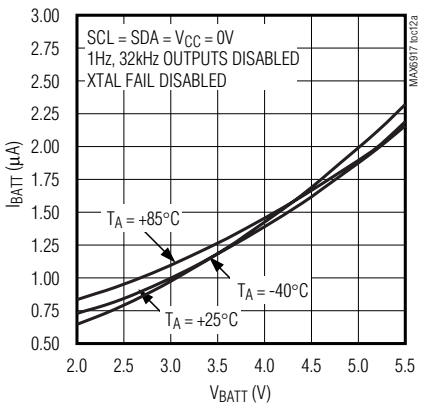
**ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE**



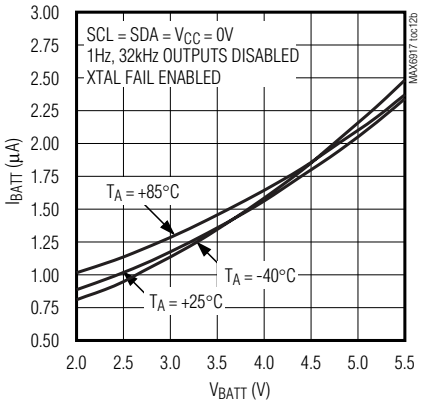

**ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE**



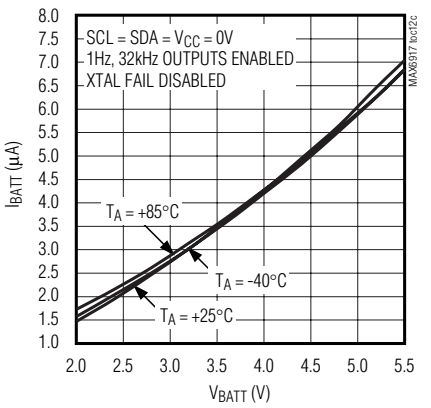

**TIMEKEEPING CURRENT vs. SUPPLY VOLTAGE**



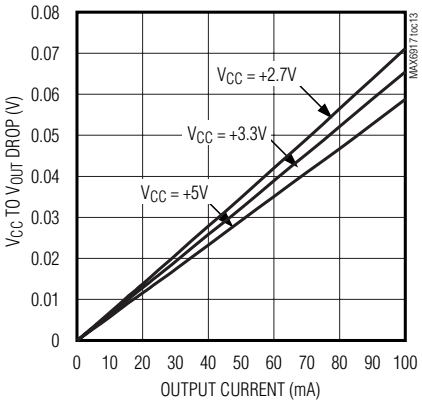

**TIMEKEEPING CURRENT vs. SUPPLY VOLTAGE**



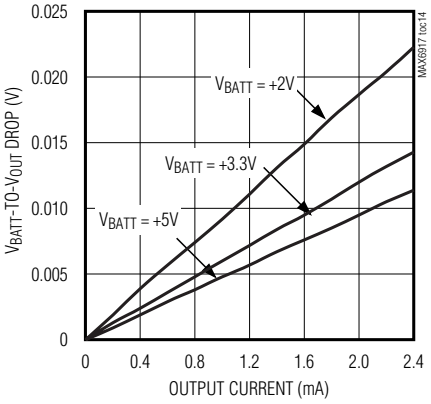

**TIMEKEEPING CURRENT vs. SUPPLY VOLTAGE**




**VCC TO VOUT vs. OUTPUT CURRENT (NORMAL MODE)**




**VBATT-TO-VOUT vs. OUTPUT CURRENT (BATTERY BACKUP MODE)**



# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{OUT}$ | Supply Output for External SRAM or Other ICs Requiring Use of Backup-Battery Power. When $V_{CC}$ rises above the reset threshold or above $V_{BATT}$, $V_{OUT}$ is connected to $V_{CC}$. When $V_{CC}$ falls below $V_{RESET}$ and $V_{BATT}$, $V_{BATT}$ is connected to $V_{OUT}$. Connect a 0.1µF low-leakage bypass capacitor from $V_{OUT}$ to GND. Leave open if not used. |
| 2 | TEST | External Battery Test. Active high for 1s during each battery test. Intended to drive an external MOSFET or bipolar transistor for an external battery-test configuration. External test must be selected in the control register to use TEST; otherwise, it remains low. Leave open if not used. |
| 3 | TRIP | External Trip Set. If a different battery-low threshold is desired other than the internal POR default of $V_{BTP}$, then connect $R_{SET+}$ between $V_{BATT}$ and TRIP and $R_{SET-}$ between TRIP and the drain or collector of an external transistor whose base or gate is connected to TEST; Figure 17 (see the *Battery Test* section). External test must be selected in the control register to use TRIP. Leave open if not used. |
| 4 | $\overline{BATT\_ON}$ | Open-Drain Battery-On Indicator. $\overline{BATT\_ON}$ is active low when the MAX6917 is powered from $V_{BATT}$. |
| 5 | $\overline{CE\_IN}$ | Chip-Enable Input. The input to the chip-enable gating circuitry. Connect $\overline{CE\_IN}$ to GND if unused. |
| 6 | $\overline{MR}$ | Manual-Reset Input. A logic low on $\overline{MR}$ asserts $\overline{RESET}$. $\overline{RESET}$ remains asserted as long as $\overline{MR}$ is low and for $t_{RP}$ after $\overline{MR}$ returns high. The active-low $\overline{MR}$ input has an internal pullup resistor. $\overline{MR}$ can be driven from a TTL or CMOS-logic line or shorted to ground with a switch. Internal debouncing circuitry ensures noise immunity. Leave $\overline{MR}$ open if unused. |
| 7 | WDI | Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and $\overline{RESET}$ is asserted. The internal watchdog timer clears while $\overline{RESET}$ is asserted or when WDI sees a rising or falling edge. The watchdog function can be disabled from the control register. The timeout period is configurable in the control register for 200ms or 1.6s. |
| 8 | GND | Ground |
| 9 | X1 | 32.768kHz Crystal-Oscillator Input |
| 10 | X2 | 32.768kHz Crystal-Oscillator Output |

# I²C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 11 | 32KHZ | 32.768kHz Output. Buffered push-pull output that is enabled from the FOUT configuration register. |
| 12 | 1HZ | 1Hz Output. Buffered push-pull output that is enabled from the FOUT configuration register. |
| 13 | SDA | Open-Drain Data Input/Output. I²C bus serial data input/output connection. |
| 14 | SCL | Serial Clock Input. I²C bus clock for input/output data transfers. |
| 15 | $\overline{ALM}$ | Open-Drain, Active-Low Alarm Output. $\overline{ALM}$ goes low when RTC time matches alarm thresholds set in the alarm threshold registers. $\overline{ALM}$ stays low until cleared by reading or writing to the alarm configuration register or to any of the alarm threshold registers. |
| 16 | $\overline{CE\_OUT}$ | Chip-Enable Output. $\overline{CE\_OUT}$ goes low only when $\overline{CE\_IN}$ is low and $\overline{RESET}$ is not asserted. If $\overline{CE\_IN}$ is low when $\overline{RESET}$ is asserted, $\overline{CE\_OUT}$ remains low for $t_{RCE}$ or until $\overline{CE\_IN}$ goes high, whichever occurs first. $\overline{CE\_OUT}$ is pulled to $V_{OUT}$. |
| 17 | $\overline{BATT\_LO}$ | Open-Drain, Battery-Low Indicator. $\overline{BATT\_LO}$ is active low when the $V_{BATT}$ input is tested below $V_{BTP}$ if the internal trip is selected in the control register (POR default). If external trip is selected in the control register, then $\overline{BATT\_LO}$ is active low when TRIP is less than $V_{TRIP}$. |
| 18 | $\overline{RESET}$ | Open-Drain, Active-Low Reset Output. $\overline{RESET}$ pulses low for $t_{RP}$ when triggered, and stays low whenever $V_{CC}$ is below the reset threshold or when $\overline{MR}$ is logic low. $\overline{RESET}$ remains low for $t_{RP}$ after either $V_{CC}$ rises above the reset threshold or $\overline{MR}$ goes from low to high. |
| 19 | $V_{CC}$ | Main Supply Input. Connect a 0.1µF bypass capacitor from $V_{CC}$ to GND. |
| 20 | $V_{BATT}$ | Backup-Battery Input. When $V_{CC}$ falls below the reset threshold and $V_{BATT}$, $V_{OUT}$ switches from $V_{CC}$ to $V_{BATT}$. When $V_{CC}$ rises above $V_{BATT}$ or the reset threshold, $V_{OUT}$ reconnects to $V_{CC}$. $V_{BATT}$ may exceed $V_{CC}$. Connect $V_{BATT}$ to GND if no backup-battery supply is used. Connect a 0.1µF low-leakage bypass capacitor from $V_{BATT}$ to GND. |

## Detailed Description

### Functional Description

The MAX6917 contains eight 8-bit timekeeping registers, seven 8-bit alarm threshold registers, one status register, one control register, one alarm-configuration register, and 96 x 8 bits of SRAM. In addition to single-byte reads and writes to registers and RAM, there is a burst timekeeping register read/write command, a burst RAM read/write command, and a battery-test command that allows software-commanded testing of the backup battery at any time. An I²C-bus-compatible interface allows serial communication with a µP. When $V_{CC}$ is less than the reset threshold, the serial interface is disabled to prevent erroneous data from being written to the MAX6917. A µP supervisory section and an NVRAM controller are provided for ease of implementation with µP-based systems. A crystal fail-detect circuit and a data-valid bit can be used to guarantee RAM data integrity and valid timekeeping data. Two reference frequencies outputs, 32.768kHz and 1Hz, are provided for external device clocking. Time and calendar data are stored in a binary-coded decimal (BCD) format. Figure 1 shows the functional diagram of the MAX6917.

### Real-Time Clock

The RTC provides seconds, minutes, hours, day, date, month, and year information. The end of the months is automatically adjusted for months with fewer than 31 days, including corrections for leap years through 2099.

### Crystal Oscillator

The MAX6917 uses an external, standard 6pF load watch crystal. No other external components are required for this timekeeping oscillator. Power-up oscillator start time is dependent mainly upon applied $V_{CC}$ and ambient temperature. The MAX6917, because of its low timekeeping current, exhibits a typical startup time of 1s to 2s.

### I²C-Compatible Interface

The I²C bus allows bidirectional, 2-wire communication between different ICs. The two lines are serial data line (SDA) and serial clock line (SCL). Both lines must be connected to a positive supply through individual pullup resistors (see the *Typical Application Circuit)*. Data transfer can only be initiated when the bus is not busy (both SDA and SCL are high). Figure 2 shows a timing diagram for I²C communication.

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

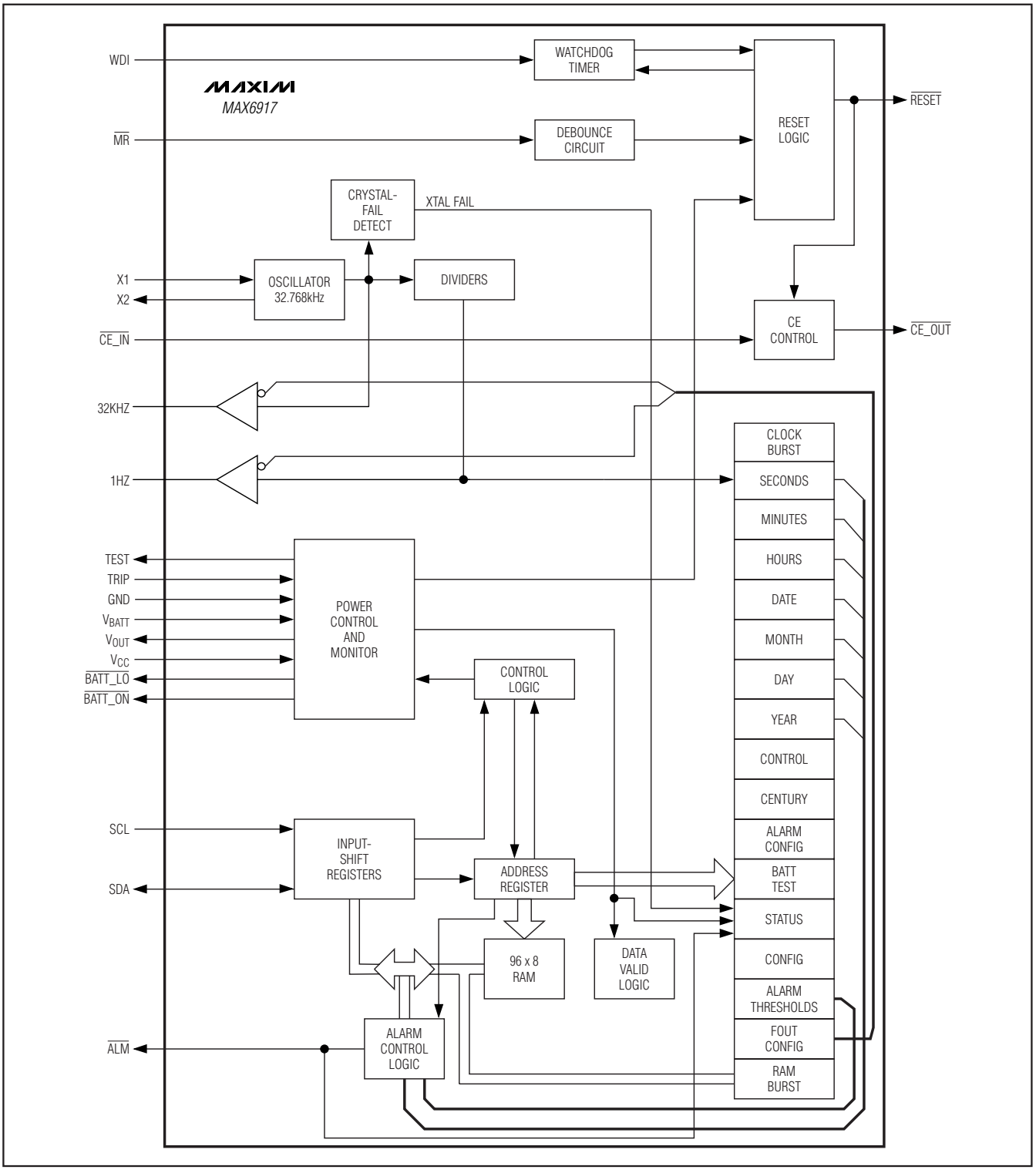



*Figure 1. Functional Diagram*

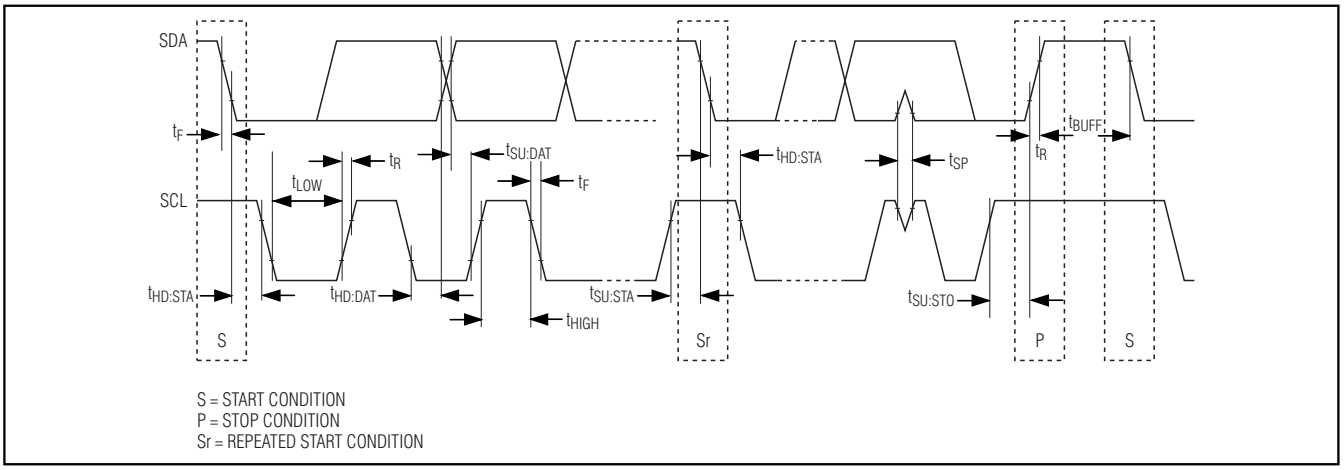



*Figure 2. I²C Communication Timing Diagram*

To maximize battery life and prevent erroneous data from being entered into the MAX6917, the serial bus interface is disabled when $V_{CC}$ is below $V_{RST}$. If the SDA or SCL serial interface lines are held low for longer than 1s to 2s, the serial bus interface resets and awaits for a new START condition (see the *START and STOP Conditions* section).

### I²C System Configuration

A device on the I²C-compatible bus that generates a message is called a transmitter and a device that receives the message is called a receiver. The device that controls the message is the master and the devices that are controlled by the master are called slaves (Figure 3). The word message refers to data in the form of three 8-bit bytes for a single read or write. The first byte is the slave ID byte, the second byte is the address/command byte, and the third is the data.

### START and STOP Conditions

Data transfer can only be initiated when the bus is not busy (both SDA and SCL are high). A high-to-low transition of SDA while SCL is high defines a START (S) condition; low-to-high transition of SDA while SCL is high defines a STOP (P) condition (Figures 2, 4). Any time a START condition occurs, the slave ID must follow immediately, regardless of completion of a previous data transfer.

### Bit Transfer

After the START condition occurs, 1 bit of data is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal (Figure 5).

### Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 6). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high portion of the clock pulse. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the SDA high to enable the master to generate a STOP condition. If a STOP condition is received before the current byte of data transfer is completed in burst mode, the last incomplete byte is ignored if it is a burst transaction to RAM or the whole burst transaction is ignored if it is a burst transaction to the timekeeping registers. There is no limit to the number of bytes that can be transmitted between a START and a STOP condition.

### Slave Address

Before any data is transmitted on the I²C-bus-compatible serial interface, the device that is expected to respond must be addressed first. The first byte sent after the START (S) condition is the address byte or 7-bit slave ID. The MAX6917 acts as a slave transmitter/receiver. Therefore, SCL is only an input clock signal and SDA is a bidirectional data line. The slave address for the MAX6917 is shown in Figure 7.

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

### Address/Command Byte

The second byte of data sent after the START condition is the address/command byte (Figure 8). Each data transfer is initiated by an address/command byte. Bits 7–1 specify the designated register or RAM location to be read or written to, and the LSB (bit 0) specifies a write operation if logic zero or a read operation if logic one. The command byte is always input starting with the MSB (bit 7).

### Reading from the Timekeeping Registers

The timekeeping registers (seconds, minutes, hours, date, month, day, and year) and the control register can be read either with a single read or a burst read (Figure 9). Since the RTC runs continuously and a read takes a finite amount of time, there is the possibility that the clock counters could change during a read operation, thereby reporting inaccurate timekeeping data. In the MAX6917, each clock counter's data is buffered by a latch. Clock counter data is latched by the I2C bus read command (on the falling edge of SCL when the slave acknowledge bit is sent, after the address/command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a seconds counter update to ensure accurate time data is being read. This avoids time-data changes during a read operation. The clock counters continue to count and keep accurate time during the read operation.

If single reads are used to read each of the timekeeping registers individually, then it is necessary to do some error checking on the receiving end. An error can occur when the seconds counter increments before all the other registers are read out. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single-read operations of the timekeeping registers. Then the net data could become 14:59:59, which is erroneous real-time data. To prevent this with single-read operations, read the seconds register first (initial seconds) and store this value for future comparison. When the remaining timekeeping registers have been read out, read the seconds register again (final seconds). If the initial seconds value is 59, check that the final-seconds value is still 59; if not, repeat the entire single-read process for the timekeeping registers. A comparison of the initial-seconds value with the final-seconds value can indicate if there was a bus-delay problem in reading the timekeeping data (difference should always be 1s or less). Using a 100kHz bus speed, and sequential single reads, it would take under 2.5ms to read all seven of the timekeeping registers plus a second read of the seconds register.

The most accurate way to read the timekeeping registers is to perform a burst read. With burst reads, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are read sequentially, in the order listed with the seconds register first. They must be all read out as a group of

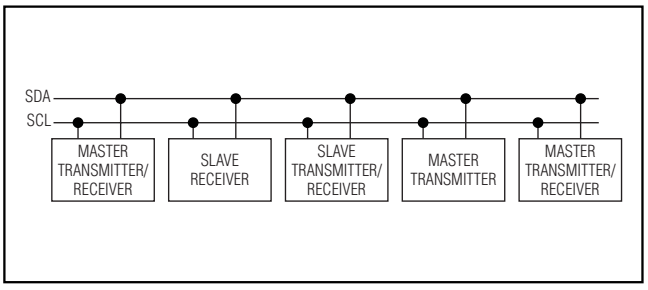



*Figure 3. I2C System Configuration*

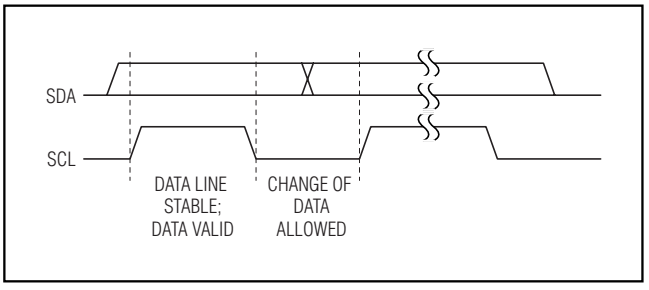



*Figure 5. Bit Transfer*

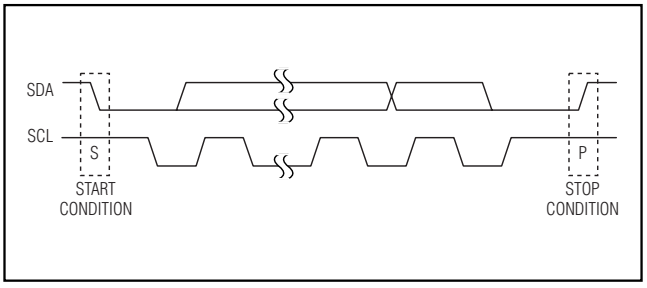



*Figure 4. START and STOP Conditions*

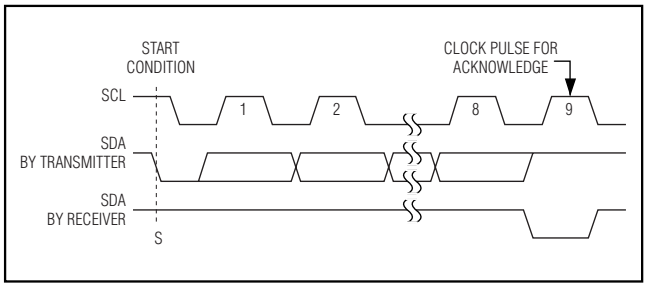



*Figure 6. Acknowledge*

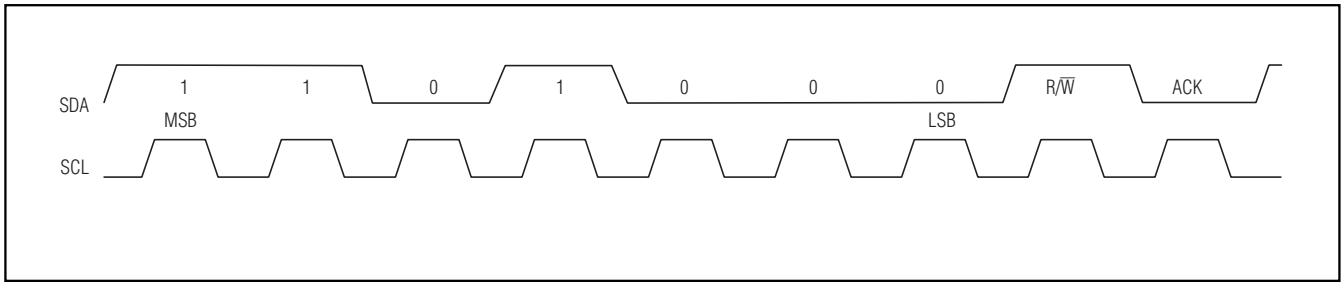



*Figure 7. MAX6917 Slave Address*

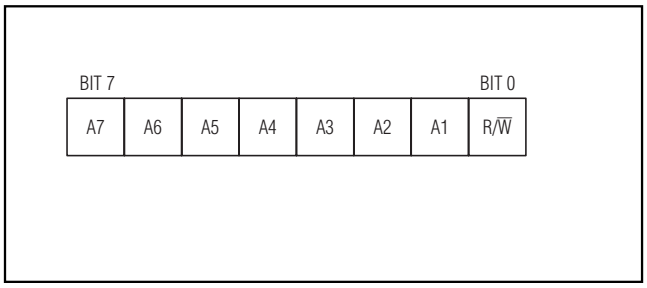



*Figure 8. Address/Command Byte*

eight registers, with 8 bytes each, for proper execution of the burst-read function. All seven timekeeping registers are latched upon the receipt of the burst-read command. The worst-case error that can occur between the actual time and the read time is 1s.

***Writing to the Timekeeping Registers***

The time and date can be set by writing to the timekeeping registers (seconds, minutes, hours, date, month, day, year, and century). To avoid changing the

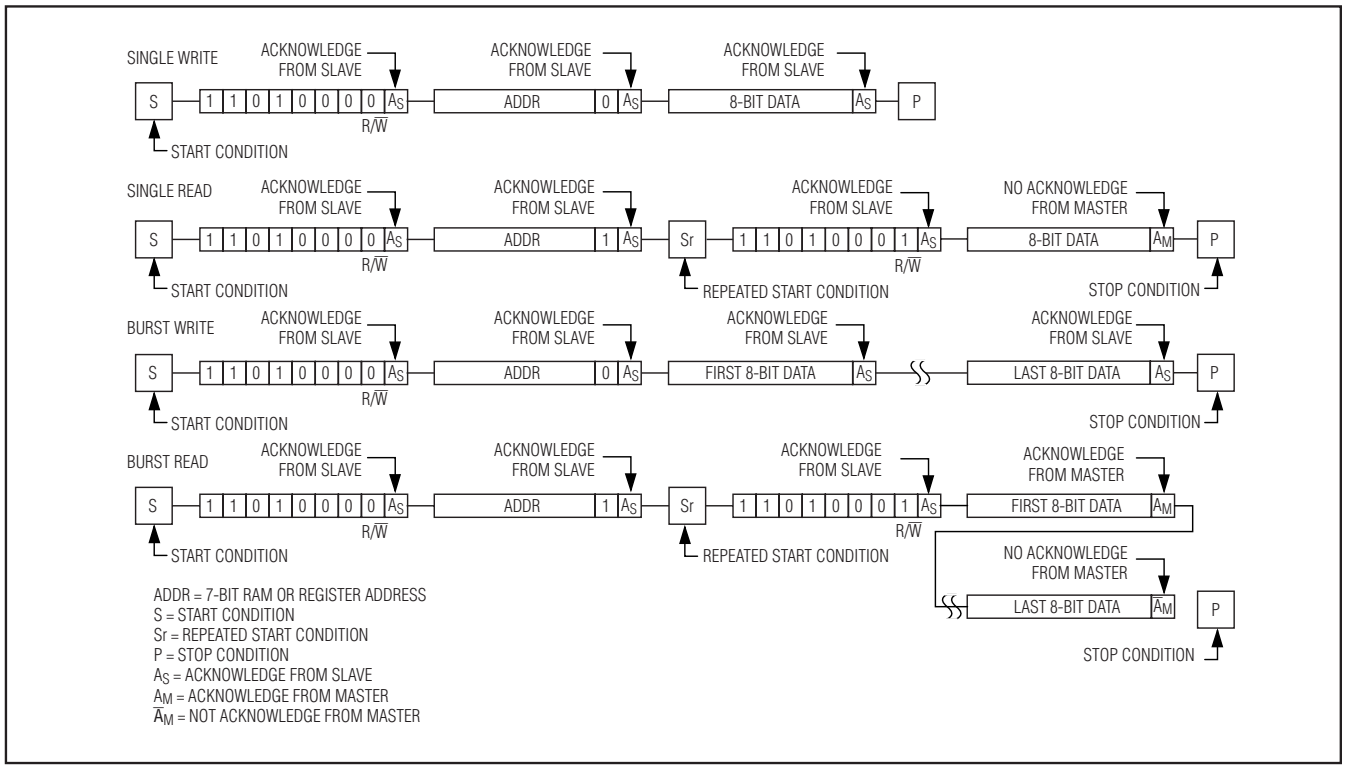



*Figure 9. Read and Write Operations*

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

current time by an incomplete write operation, the current time value is buffered from being written directly to the clock counters. The new data sent replaces the current contents of this input buffer. This time update data is loaded into the clock counters after the stop bit at the end of the I²C bus write operation. Collision-detection circuitry ensures that this does not happen coincident with a seconds-counter update to guarantee that accurate time data is being written. This avoids time data changes during a write operation. An incomplete write operation aborts the time-update procedures and the contents of the input buffer are discarded. The clock counters reflect the new time data beginning with the first 1s clock cycle after the stop bit. The clock counter is reset immediately after a write to the seconds register or a burst write to the timekeeping registers. This ensures that 1s clock tick is synchronous to timekeeping writes.

If single-write operations (Figure 9) are used to write to each of the timekeeping registers, then error checking is needed. If the seconds register is the one to be updated, update it first and then read it back and store its value as the initial seconds. Update the remaining timekeeping registers and then read the seconds register again (final seconds). If initial seconds was 59, ensure it is still 59. If initial seconds was not 59, ensure that final seconds is within 1s of initial seconds. If the seconds register is not to be written to, then read the seconds register first and save it as initial seconds. Write to the required timekeeping registers and then read the seconds register again (final seconds). If initial seconds was 59, ensure it is still 59. If initial seconds was not 59, ensure that final seconds is within 1s of initial seconds.

Although both single writes and burst writes are possible, the most accurate way to write to the timekeeping counters is to do a burst write (Figure 9). In the burst write, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are written sequentially. They must be all written to as a group of eight registers, with 8 bytes each, for proper execution of the burst-write function. All seven timekeeping registers and the control register are simultaneously loaded into the input buffer at the end of the 2-wire bus write operation. The worst-case error that can occur between the actual time and the write time update is 1s.

To avoid rollover issues when writing time data to the MAX6917, the remaining time and date registers must be written within 1s of updating the seconds register when using single writes. For burst writes, all eight registers must be written within this period (1s).

The weekday data in the day register increments at midnight. Values that correspond to the day of the week are user defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). If invalid values are written to the timekeeping registers, the operation becomes undefined.

### *Timeout Feature*

The purpose of the bus timeout feature is to reset the serial bus interface and change the SDA line of the MAX6917 from an output to an input, which puts the SDA line into a high-impedance state. This is necessary when the MAX6917 is transmitting data and becomes stuck at a logic-low level. If the SDA line is stuck low, any other device on the bus is not able to communicate.

The timeout feature looks for a valid START and STOP condition to determine whether SDA has been stuck low. A valid START condition initiates the timeout counter in reference to the internal 1Hz clock. Counting begins on the first rising edge of the 1Hz clock after a valid START condition. If a valid STOP condition is detected before the next rising edge of the 1Hz clock, the timeout counter is stopped and awaits a new valid START condition. If a valid STOP condition is not detected before the next rising edge of the 1Hz clock, the I²C interface resets to the idle state and waits for a new I²C transaction. Depending on the occurrence of the START condition, that initiates the timeout counter, in reference to the internal 1Hz clock, the timeout period can be 1s to 2s. The lower limit of the timeout period (1s) imposes a limit on the SCL frequency of the MAX6917 because a burst read/write requires up to 96 bytes of information to be transmitted in between a START and STOP condition.

### Registers

Tables 1 and 2 show the register map, as well as the register descriptions for the MAX6917.

#### Control Register

The control register contains bits for configuring the MAX6917 for custom applications. Bit D0 (BATT ON BLINK) and D1 (BATT LO BLINK) are used to enable a 1Hz blink rate on $\overline{BATT\_ON}$ and $\overline{BATT\_LO}$ when they are active; see the *Battery Test* section for details. D2 (WD TIME) and D3 (WD EN) are used to enable the watchdog function and select its timeout. For details, see the *Watchdog Input* section. D5 (INT/EXT TEST) sets whether the internal resistor ratio or an external resistor ratio is to be used to check for the low-battery condition; see the *Battery Test* section for details. D6 (XTAL EN) enables the crystal-fail-detect circuitry when set. See the *Crystal-Fail Detect* section for details. D7 (WP) is the write protect bit. Before any write operation to the registers (except the control register) or RAM, bit 7 must be zero. When set to one, the write-protect bit prevents write operations to any register (except the control register) or RAM location.

#### Timekeeping and Alarm Thresholds Registers

Time and date data is stored in the timekeeping and alarm threshold registers in BCD format as shown in Table 1. The weekday data in the day register is user defined (a common format is 1 = Sunday, 2 = Monday, etc.)

#### AM/PM and 12hr/24hr Mode

For both timekeeping and alarm threshold registers (Table 1), D7 of the hours register is defined as the 12hr or 24hr mode-select bit. When set to one, the 12hr mode is selected. In the 12hr mode, D5 is the $\overline{AM}$/PM bit with logic one being PM. In the 24hr mode, D5 is the second 10hr bit (20hr to 23hr).

#### Clock-Burst Mode

Addressing the clock-burst register specifies burst-mode operation. In this mode, the first eight clock/calendar registers (seven timekeeping and the control register) can be consecutively read or written to by using the address/command byte 00h for a write or 01h for a read (Table 1). If the write-protect bit is set to one when a write-clock/calendar-burst mode is specified, no data transfer occurs to any of the seven timekeeping registers or the control register. When writing to the clock/calendar registers in the burst mode, the first eight registers must be written to for the data to be transferred.

#### RAM

The static RAM consists of 96 x 8 bits addressed consecutively in the RAM address/command space. Even address/commands (3Eh to FCh) are used for RAM writes and odd address/commands (3Fh to FDh) are used for RAM reads (Table 2).

#### RAM-Burst Mode

Sending the RAM-burst address/command (FEh for write, FFh for read) specifies burst-mode operation. In this mode, the 96 RAM locations can be consecutively read or written to starting with bit 7 of address/command 3Eh for writes, and 3Fh for reads. A burst read outputs all 96 bytes of RAM. When writing to RAM in burst mode, it is not necessary to write all 96 bytes for the data to transfer; each complete byte written is transferred to the RAM. When reading from RAM, data are output until all 96 bytes have been read, or until the data transfer is stopped by the I2C master.

#### Status Register

The status register contains individual bits for monitoring the status of several functions of the MAX6917. Bits D0–D3 are unused and always read zero (Table 1). D4 (ALM OUT) reflects the state of the alarm function; see the *Alarm-Generation Function* section for details. D5 (BATT LO) indicates the state of the battery connected to $V_{BATT}$; see the *Battery Test* section for more information. D6 (DATA VALID) alerts the user if all power was lost. See the *Data Valid Bit* section for details. D7 (XTAL FAIL) is the output of the crystal-fail detect circuit. See the *Crystal-Fail Detect* section for details.

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## Table 1. Register Map

| FUNCTION | REGISTER ADDRESS A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | VALUE | REGISTER FUNCTION D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLOCK BURST | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | | | | | | | | | |
| SEC | 1 | 0 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 0–59 | 0 | 10 SEC | | | 1 SEC | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MIN | 0 | 1 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 0–59 | 0 | 10 MIN | | | 1 MIN | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HR | 1 | 1 | 0 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 00–23<br>01–12 | 12/$\overline{24}$ | 0 | 10 HR<br>$\overline{AM}$/PM | 10 HR | 1 HR | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DATE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 01–28/29<br>01–30/31 | 0 | 0 | 10 DATE | | 1 DATE | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| MONTH | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 01–12 | 0 | 0 | 0 | 10 M | 1 MONTH | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| DAY | 0 | 1 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 01–07 | 0 | 0 | 0 | 0 | 0 | WEEKDAY | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| YEAR | 1 | 1 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 00–99 | 10 YEAR | | | | 1 YEAR | | | |
| | | | | | | | | | POR STATE | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| CONTROL | 0 | 0 | 0 | 1 | 0 | 0 | 0 | R/$\overline{W}$ | | WP | XTAL EN | INT/EXT TEST | 0 | WD EN | WD TIME | BATT LO BLINK | BATT ON BLINK |
| | | | | | | | | | POR STATE | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| CENTURY | 1 | 0 | 0 | 1 | 0 | 0 | 0 | R/$\overline{W}$ | 00–99 | 1000 YEAR | | | | 100 YEAR | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| ALARM CONFIGURATION | 0 | 1 | 0 | 1 | 0 | 0 | 0 | R/$\overline{W}$ | | ONE SEC | YEAR | DAY | MONTH | DATE | HR | MIN | SEC |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FOUT CONFIGURATION | 0 | 0 | 0 | 1 | 0 | 1 | 1 | R/$\overline{W}$ | | 32kHz $V_{CC}$ EN | 1kHz $V_{CC}$ EN | 32kHz $V_{BATT}$ EN | 1kHz $V_{BAT}$ EN | 0 | 0 | 0 | 0 |
| | | | | | | | | | POR STATE | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| STATUS | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R/$\overline{W}$ | | XTAL FAIL | DATA VALID | BATT LO | ALM OUT | 0 | 0 | 0 | 0 |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**POR STATE** DEFINES THE POWER-ON RESET STATE OF THE REGISTER.

## Table 1. Register Map (continued)

| FUNCTION | REGISTER ADDRESS A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | VALUE | REGISTER FUNCTION D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BATT TEST | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | | | | | |
| ALARM THRESHOLDS: | | | | | | | | | | | | | | | | | |
| SEC | 0 | 0 | 0 | 1 | 1 | 1 | 0 | R/$\overline{W}$ | 0–59 | 0 | 10 SEC | | | 1 SEC | | | |
| | | | | | | | | | POR STATE | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| MIN | 0 | 0 | 0 | 1 | 1 | 1 | 1 | R/$\overline{W}$ | 0–59 | 0 | 10 MIN | | | 1 MIN | | | |
| | | | | | | | | | POR STATE | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| HR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ | 00–23 | 12/$\overline{24}$ | 0 | 10 HR / $\overline{AM}$/PM | 10 HR | 1 HR | | | |
| | | | | | | | | | 01–12 | | | | | | | | |
| | | | | | | | | | POR STATE | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| DATE | 0 | 0 | 1 | 0 | 0 | 0 | 1 | R/$\overline{W}$ | 01–28/29 01–30/31 | 0 | 0 | 10 DATE | | 1 DATE | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| MONTH | 0 | 0 | 1 | 0 | 0 | 1 | 0 | R/$\overline{W}$ | 01–12 | 0 | 0 | 0 | 10 M | 1 MONTH | | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| DAY | 0 | 0 | 1 | 0 | 0 | 1 | 1 | R/$\overline{W}$ | 01–07 | 0 | 0 | 0 | 0 | 0 | WEEK DAY | | |
| | | | | | | | | | POR STATE | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| YEAR | 0 | 0 | 1 | 0 | 1 | 0 | 0 | R/$\overline{W}$ | 00–99 | 10 YEAR | | | | 1 YEAR | | | |
| | | | | | | | | | POR STATE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TEST CONFIGURATION (FACTORY RESERVED) | 0 | 0 | 1 | 0 | 1 | 0 | 1 | R/$\overline{W}$ | POR STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **RAM REGISTERS:** | | | | | | | | | | | | | | | | | |
| RAM 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | R/$\overline{W}$ | RAM DATA 0 00h-FFh | X | X | X | X | X | X | X | X |
| ⋮ | | | | | | | | | ⋮ | | | | | | | | |
| RAM 95 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | R/$\overline{W}$ | RAM DATA 95 00h-FFh | X | X | X | X | X | X | X | X |
| RAM BURST | 1 | 1 | 1 | 1 | 1 | 1 | 1 | R/$\overline{W}$ | | | | | | | | | |

**POR STATE** DEFINES THE POWER-ON RESET STATE OF THE REGISTER.

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

### Power Control

$V_{BATT}$ provides power as a battery backup. $V_{CC}$ provides the primary power in dual-supply systems where $V_{BATT}$ is connected as a backup source to maintain timekeeping in the absence of primary power. When $V_{CC}$ rises above the reset threshold, $V_{RST}$, $V_{CC}$ powers the MAX6917. When $V_{CC}$ falls below the reset threshold, $V_{RST}$, and is less than $V_{TRD}$, $V_{BATT}$ powers the MAX6917. If $V_{CC}$ falls below the reset threshold, $V_{RST}$, and is more than $V_{TRU}$, $V_{CC}$ still powers the MAX6917. $V_{CC}$ slew rate in power-down is limited to 10V/ms (max) for proper data retention.

### VOUT Function

$V_{OUT}$ is an output supply voltage for battery-backed-up devices such as SRAM. When $V_{CC}$ rises above the reset threshold or is greater than $V_{BATT}$, $V_{OUT}$ connects to $V_{CC}$ (Figure 19). When $V_{CC}$ falls below $V_{RST}$ and $V_{BATT}$, $V_{OUT}$ connects to $V_{BATT}$. There is a typical ±100mV hysteresis associated with the switching between $V_{CC}$ and $V_{BATT}$ on the $V_{OUT}$ output. Connect a 0.1µF capacitor from $V_{OUT}$ to GND.

### Power-On Reset (POR)

The MAX6917 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Once either $V_{CC}$ or $V_{BATT}$ rises above 1.6V (typ), the POR circuit releases the registers for normal operation. When $V_{CC}$ or $V_{BATT}$ drops to less than 0.9V (typ), the MAX6917 resets all register contents to the POR defaults.

### Oscillator Start Time

The MAX6917 oscillator typically takes 1s to 2s to begin oscillating. To ensure the oscillator is operating correctly, the system software should validate proper timekeeping. This is accomplished by reading the seconds register. Any reading with more than 0s, from the POR value of 0s, is a validation of proper startup.

### Alarm-Generation Function

The alarm function is configured using the alarm-configuration register and the alarm-threshold registers (Table 1). Writing a one to D7 (ONE SEC) in the alarm-configuration register sets the alarm function to occur once every second, regardless of any other setting in the alarm-configuration register or in any of the alarm-threshold registers. When the alarm is triggered, D4 (ALM OUT) in the status register is set to one and the open-drain alarm output $\overline{ALM}$ goes low. The alarm is cleared by reading or writing to the alarm-configuration register or by reading or writing to any of the alarm-threshold registers. This resets the $\overline{ALM}$ output to a high and the ALM OUT bit to zero.

When D7 (ONE SEC) is set to zero in the alarm-configuration register, then the alarm function is set by the remaining bits in the alarm-configuration register and the contents of the respective alarm-threshold register. For example, writing 01h (0000 0001) to the alarm-configuration register causes the alarm to trigger every time the seconds-timekeeping register matches the seconds alarm-threshold register (i.e., once every minute on a specific second). Writing 02h (0000 0010) to the alarm configuration register causes the alarm to trigger on a minutes match (i.e., once every hour). Writing a 4Fh (0100 1111) to the alarm configuration register causes the alarm to be triggered on a specific second, of a specific minute, of a specific hour, of a specific date, of a specific year.

When setting the alarm-threshold registers, ensure that both the hour-timekeeping register and the hour-alarm-threshold register are using the same-hour format (either 12hr or 24hr format).

The alarm function, as well as the $\overline{ALM}$ output, is operational in both $V_{CC}$ and battery-backup mode.

## Table 2. Hex Register Address and Description

| WRITE ADDRESS/COMMAND (HEX) | READ ADDRESS/COMMAND (HEX) | DESCRIPTION | POR SETTING (HEX) |
|---|---|---|---|
| 00 | 01 | Clock burst | N/A |
| 02 | 03 | Seconds | 00 |
| 04 | 05 | Minutes | 00 |
| 06 | 07 | Hour | 00 |
| 08 | 09 | Date | 01 |
| 0A | 0B | Month | 01 |
| 0C | 0D | Day | 01 |
| 0E | 0F | Year | 70 |
| 10 | 11 | Control | 48 |
| 12 | 13 | Century | 00 |
| 14 | 15 | Alarm configuration | 19 |
| 16 | 17 | FOUT configuration | C0 |
| 18 | 19 | Status | 00 |
| 1A | N/A | Battery test | N/A |
| 1C | 1D | Seconds alarm threshold | 7F |
| 1E | 1F | Minutes alarm threshold | 7F |
| 20 | 21 | Hours alarm threshold | BF |
| 22 | 23 | Date alarm threshold | 3F |
| 24 | 25 | Month alarm threshold | 1F |
| 26 | 27 | Day alarm threshold | 07 |
| 28 | 29 | Year alarm threshold | FF |
| 2A | 2B | Test configuration | 00 |
| 3E | 3F | RAM 0 | Indeterminate |
| 40 | 41 | RAM 1 | Indeterminate |
| 42 | 43 | RAM 2 | Indeterminate |
| 44 | 45 | RAM 3 | Indeterminate |
| 46 | 47 | RAM 4 | Indeterminate |
| • | • | • | • |
| • | • | • | • |
| • | • | • | • |
| F4 | F5 | RAM 91 | Indeterminate |
| F6 | F7 | RAM 92 | Indeterminate |
| F8 | F9 | RAM 93 | Indeterminate |
| FA | FB | RAM 94 | Indeterminate |
| FC | FD | RAM 95 | Indeterminate |
| FE | FF | RAM BURST | Indeterminate |

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

### Crystal-Fail Detect

The crystal-fail detect circuit looks for a loss of oscillation from the 32.768kHz oscillator for 30 cycles (typ) or more. Both the control register and the status register are used in the crystal-failure detection scheme (Table 1).

The crystal-fail detect circuit sets the XTAL FAIL bit in the status register to one for a crystal failure and to zero for normal operation. Once the status register is read, the XTAL FAIL bit is reset to zero, if it was previously one. If the crystal-fail-detect circuit continues to sense a failed crystal, then the XTAL FAIL bit is set again.

On initial power-up, the crystal-fail detect circuit is enabled. Since it takes a while for the low-power, 32.768kHz oscillator to start, the XTAL FAIL bit in the status register can be set to one indicating a crystal failure. The XTAL FAIL bit should be polled a number of times to see if it is set to zero for successive polls. If the polling is far enough apart, a few polled results could guarantee that a maximum of 10s had elapsed since power-on, at which time the oscillator would be considered truly failed if the XTAL FAIL bit remains one.

On subsequent power-ups, when XTAL EN is set to one, if XTAL FAIL is set to one, time data should be considered suspect.

The crystal-fail-detection circuit functions in both $V_{CC}$ and $V_{BATT}$ modes when the XTAL EN bit is set in the control register.

### Manual Reset Input

A logic low on $\overline{MR}$ asserts $\overline{RESET}$. $\overline{RESET}$ remains asserted while $\overline{MR}$ is low, and for $t_{RP}$ after it returns high (Figure 10). $\overline{MR}$ has an internal pullup resistor, so it can be left open if it is not used. Internal debounce circuitry requires a minimum low time on the $\overline{MR}$ input of 1µs with 35ns maximum glitch immunity.

### Reset Output

A µP's reset input starts the µP in a known state. The MAX6917's µP supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. The $\overline{RESET}$ output is guaranteed to be active for $0V < V_{CC} < V_{RST}$, provided $V_{BATT}$ is greater than $V_{BATT}$ (min). If $V_{CC}$ drops below and then exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ active for the reset timeout period $t_{RP}$; after this interval, $\overline{RESET}$ becomes inactive high. This condition occurs at either power-up or after a $V_{CC}$ brownout.

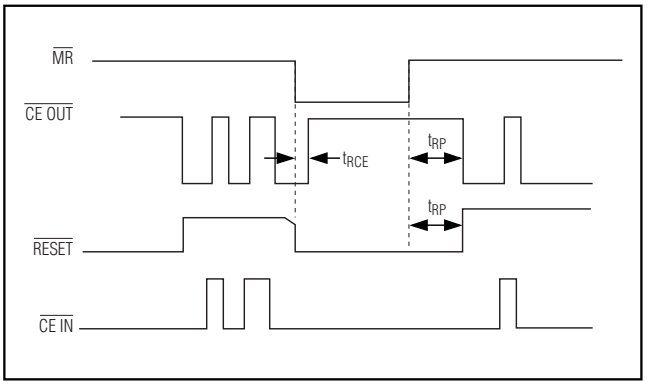


*Figure 10. Manual-Reset Timing Diagram*

The $\overline{RESET}$ output is also activated when the watchdog interrupt function is enabled but no transition is detected on the WDI input. In this case, $\overline{RESET}$ is active for the period $t_{RP}$ before becoming inactive again. When $\overline{RESET}$ is active, all inputs—WDI, $\overline{MR}$, $\overline{CE\_IN}$, SDA, and SCL—are disabled.

The MAX6917EO30 is optimized to monitor 3.0V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until $V_{CC}$ falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the power supply falls below 2.5V (3.0V - 15%).

The MAX6917EO33 is optimized to monitor 3.3V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until $V_{CC}$ falls below 3.0V (3.0V is just above 3.3V - 10%), but is guaranteed to occur before the power supply falls below 2.8V (3.3V - 15%).

The MAX6917EO50 is optimized to monitor 5.0V ±10% power supplies. Except when $\overline{MR}$ is asserted, $\overline{RESET}$ is not active until $V_{CC}$ falls below 4.5V (5.0V - 10%), but is guaranteed to occur before the power supply falls below 4.1V (4.1V is just below 5.0V - 15%).

### Negative-Going $V_{CC}$ Transients

The MAX6917 is relatively immune to short-duration negative transients (glitches) while issuing resets to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when $V_{CC}$ experiences only small glitches is usually not recommended. Typically, a $V_{CC}$ transient that goes 150mV below the reset threshold and lasts for 90µs or less does not cause a reset pulse to be issued. A 0.1µF capacitor mounted close to the $V_{CC}$ pin provides additional transient immunity.

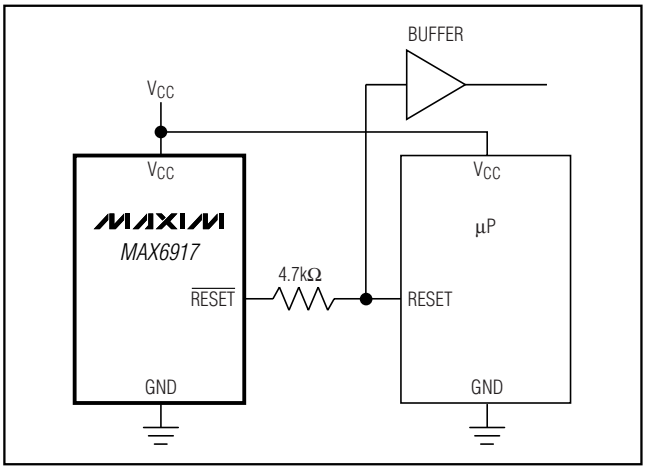


Figure 11. Interfacing to µP with Bidirectional Reset I/O

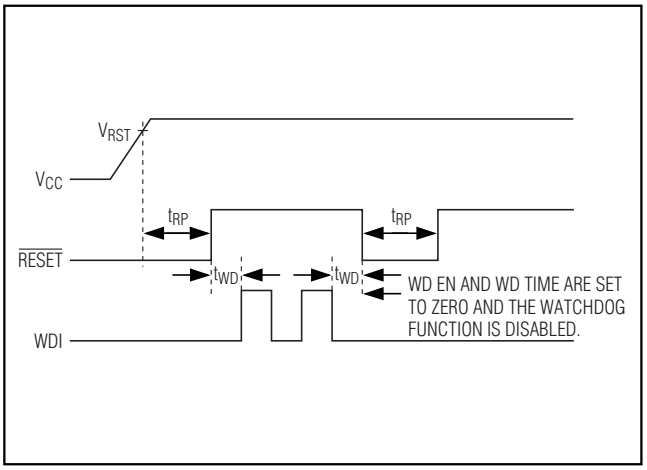


Figure 12. Watchdog Timing Diagram

### Interfacing to µPs with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX6917 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels can result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O as shown in Figure 11. Buffer the $\overline{RESET}$ output to other system components.

### Battery-On Output

The battery-on output, $\overline{BATT\_ON}$, is an open-drain output that indicates when the MAX6917 is powered from the backup-battery input, $V_{BATT}$. When $V_{CC}$ falls below the reset threshold, $V_{RST}$, and below $V_{BATT}$, $V_{OUT}$ switches from $V_{CC}$ to $V_{BATT}$ and $\overline{BATT\_ON}$ becomes low. When $V_{CC}$ rises above the reset threshold, $V_{RST}$, $V_{OUT}$ reconnects to $V_{CC}$ and $\overline{BATT\_ON}$ becomes high (open-drain output with pullup resistor). If desired, the $\overline{BATT\_ON}$ output can be register selected, through the BATT ON BLINK bit in the control register, to toggle on and off 0.5s on, 0.5s off when active. The POR default is logic zero for no blink.

### Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within the register-selectable watchdog-timeout period, $\overline{RESET}$ is asserted for $t_{RP}$. At the same time, the WD EN and WD TIME bits in the control register (Table 1) are reset to zero and can only be set again by writing the appropriate command to the control register. Thus, once a $\overline{RESET}$ is asserted due to a watchdog timeout, the watchdog function is disabled (Figure 12).

WDI can detect pulses as short as $t_{WDI}$. Data bit D2 in the control register controls the selection of the watchdog-timeout period. The power-up default is 1.6s (D2 = 0). A reset condition returns the timeout to 1.6s (D2 = 0). If D2 is set to one, then the watchdog-timeout period is changed to 200ms. Data bit D3 in the control register is the watchdog-enable function. A logic zero disables the watchdog function, while a logic one enables it. The POR state of WD EN is logic one, or the watchdog function is enabled. Disable the watchdog function by writing a zero to the WD EN bit in the control register, within the 1.6s POR default timeout after power-up.

WDI does not include a pulldown or pullup feature. For this reason, WDI should not be left floating. When the WD EN bit in the control register is set to zero, WDI should be connected to $V_{CC}$ or GND. WDI is disabled and does not draw cross-conduction current when $V_{CC}$ falls below $V_{RST}$.

### Watchdog Software Considerations

There is a way to help the watchdog-timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 13 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset to be issued.

# I2C-Compatible RTC with Microprocessor Supervisor, Alarm, and NV RAM Controller

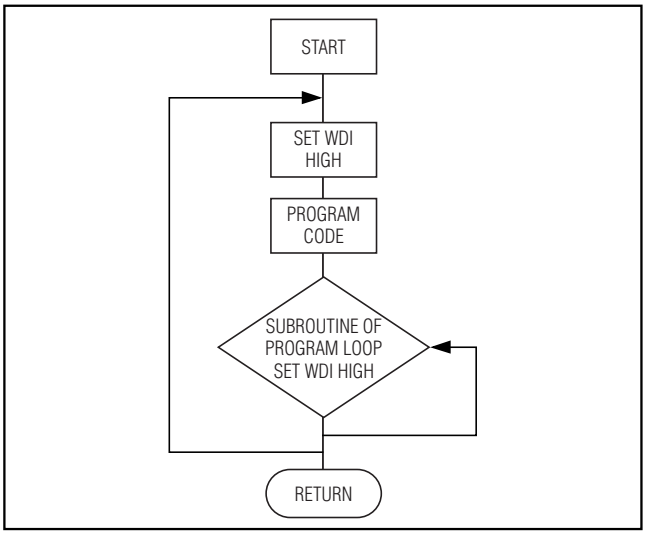


*Figure 13. Watchdog Flow Diagram*

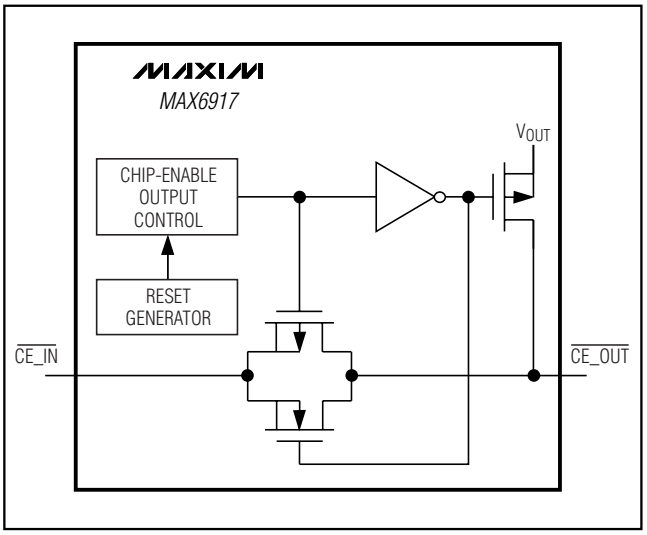


*Figure 14. Chip-Enable Gating*

### Chip-Enable Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting external SRAM in the event of an undervoltage condition. The MAX6917 uses a transmission gate from $\overline{CE\_IN}$ to $\overline{CE\_OUT}$ (Figure 14). During normal operation ($\overline{RESET}$ inactive), the transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the external SRAM. The short CE propagation delay from $\overline{CE\_IN}$ to $\overline{CE\_OUT}$ enables the MAX6917 to be used with most µPs. If $\overline{CE\_IN}$ is low when reset asserts, $\overline{CE\_OUT}$ remains low for $t_{RCE}$ to permit completion of the current write cycle.

### Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE\_IN}$ is high impedance (disabled mode) while $\overline{RESET}$ is active. During a power-down sequence when $V_{CC}$ passes the reset threshold, the CE transmission gate disables and $\overline{CE\_IN}$ immediately becomes high impedance if the voltage at $\overline{CE\_IN}$ is high. If $\overline{CE\_IN}$ is low when $\overline{RESET}$ becomes active, the CE transmission gate disables at the moment $\overline{CE\_IN}$ goes high or $t_{RCE}$ after $\overline{RESET}$ is active, whichever occurs first (see the *Chip-Enable Timing* diagram). This permits the current write cycle to complete during power-down. The CE transmission gate remains disabled and $\overline{CE\_IN}$ remains high impedance (regardless of $\overline{CE\_IN}$ activity) for most of the reset-timeout period ($t_{RST}$) any time a $\overline{RESET}$ is generated. When the CE transmission gate is enabled, the impedance of $\overline{CE\_IN}$ appears as a 46Ω (typ) load in series with the load at $\overline{CE\_OUT}$.

The propagation delay through the CE transmission gate depends on $V_{CC}$, the source impedance of the driver connected to $\overline{CE\_IN}$, and the loading on $\overline{CE\_OUT}$ (see the Chip-Enable Propagation Delay vs. $\overline{CE\_OUT}$ Load Capacitance graph in the *Typical Operating Characteristics*). For minimum propagation delay, the capacitive load at $\overline{CE\_OUT}$ should be minimized, and a low-output-impedance driver should be used on $\overline{CE\_IN}$ (Figure 15).

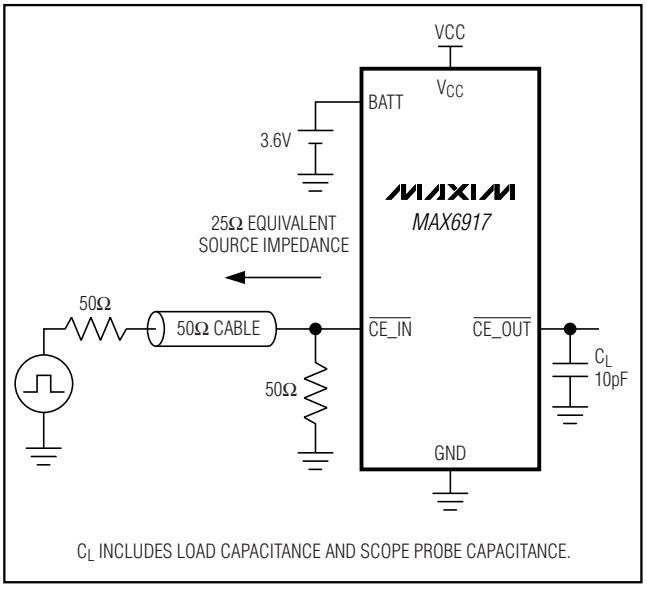


*Figure 15. Propagation Delay Test Circuit*

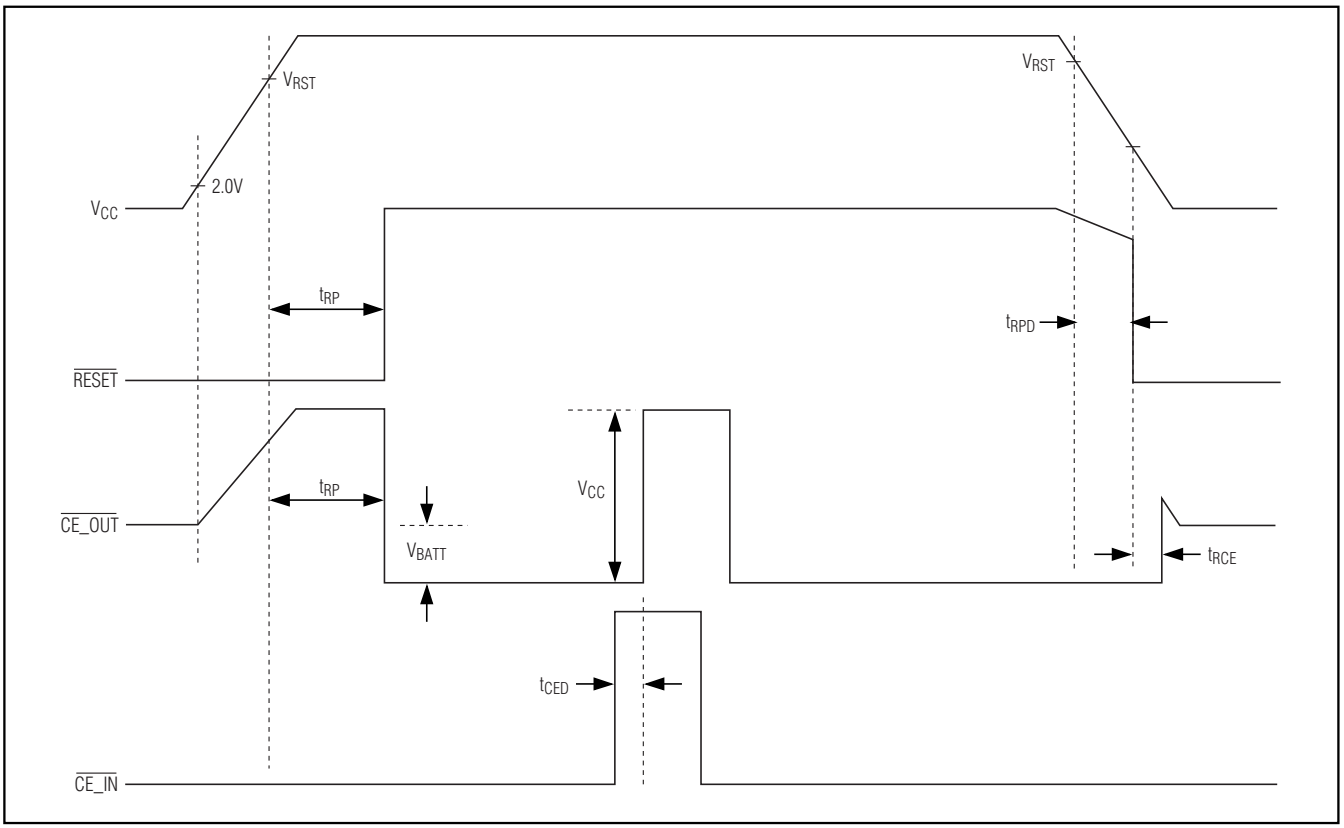


*Figure 16. Chip-Enable Timing Diagram*

### Chip-Enable Output

When the CE transmission gate is enabled, the impedance seen at $\overline{CE\_OUT}$ is equivalent to a 46Ω (typ) resistor in series with the source driving $\overline{CE\_IN}$. In the disabled mode, the transmission gate is off and an active pullup connects $\overline{CE\_OUT}$ to $V_{OUT}$ (see Figures 14, 16). This pullup turns off when the transmission gate is enabled.

### Test Configuration Register

This is a read-only register.

### Data Valid Bit

DATA VALID has a POR setting of zero, indicating that the data in the MAX6917 RTC is not guaranteed to be valid (Table 1). A read of the status register sets the DATA VALID bit to one, indicating valid data in the MAX6917 RTC. In a system that uses a backup power supply, the DATA VALID bit should be set to one by the system software on first system power-up by reading the status register. After that, any time the system recovers from a reset condition caused by $V_{CC} < V_{RST}$, the DATA VALID bit can be read to see if the data stored during operation from the backup power supply is still valid (i.e., the backup power supply did not drop out). A one indicates valid data and a zero indicates corrupted data. Any time the internal supply to the MAX6917 (either $V_{BATT}$ or $V_{CC}$ depending upon the operating conditions) drops below 1.5V to 1.6V (typ), the DATA VALID bit is set to zero even if it has recently been set by a read of the status register.