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EVALUATION KIT AVAILABLE

MAX6955

2-Wire Interfaced, 2.7V to 5.5V LED Display Driver with I/O Expander and Key Scan

General Description

The MAX6955 is a compact display driver that interfaces microprocessors to a mix of 7-segment, 14-segment, and 16-segment LED displays through an I²C-compatible 2-wire serial interface. The MAX6955 drives up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, or 128 discrete LEDs, while functioning from a supply voltage as low as 2.7V. The driver includes five I/O expander or general-purpose I/O (GPIO) lines, some or all of which can be configured as a key-switch reader. The key-switch reader automatically scans and debounces a matrix of up to 32 switches.

Included on chip are full 14- and 16-segment ASCII 104-character fonts, a hexadecimal font for 7-segment displays, multiplex scan circuitry, anode and cathode drivers, and static RAM that stores each digit. The maximum segment current for the display digits is set using a single external resistor. Digit intensity can be independently adjusted using the 16-step internal digital brightness control. The MAX6955 includes a low-power shutdown mode, a scan-limit register that allows the user to display from 1 to 16 digits, segment blinking (synchronized across multiple drivers, if desired), and a test mode, which forces all LEDs on. The LED drivers are slew-rate limited to reduce EMI.

For an SPI™-compatible version, refer to the MAX6954 data sheet. An evaluation kit (EV kit) for the MAX6955 is available.

Applications

Set-Top Boxes	Automotive
Panel Meters	Bar Graph Displays
White Goods	Audio/Video Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6955AAX	-40°C to +125°C	36 SSOP	A36-2
MAX6955ATL+	-40°C to +125°C	40 TQFN-EP*	T4066-5

**EP = Exposed paddle.*

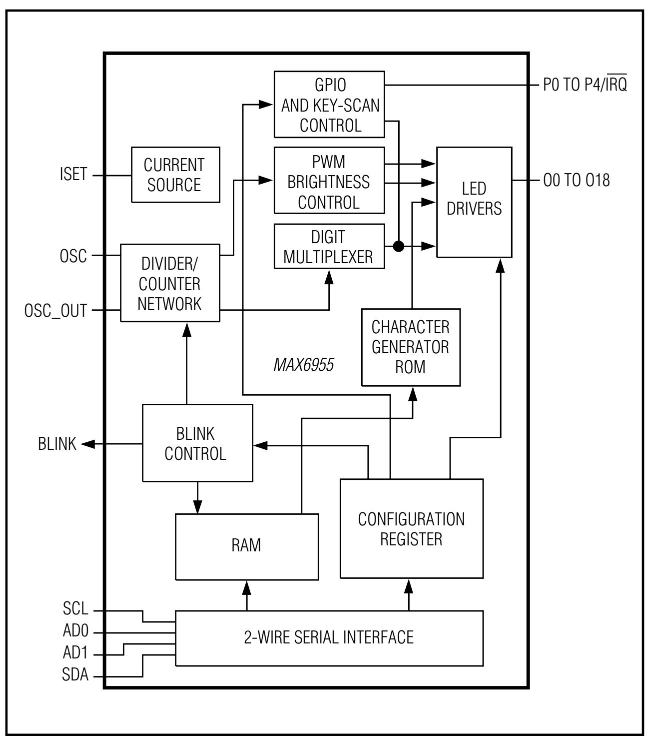
+Denotes a lead-free package.

Pin Configurations and Typical Operating Circuits appear at end of data sheet.

Features

- ♦ **400kbps 2-Wire I²C-Compatible Interface**
- ♦ **2.7V to 5.5V Operation**
- ♦ **Drives Up to 16 Digits 7-Segment, 8 Digits 14-Segment, 8 Digits 16-Segment, 128 Discrete LEDs, or a Combination of Digit Types**
- ♦ **Drives Common-Cathode Monocolor and Bicolor LED Displays**
- ♦ **Built-In ASCII 104-Character Font for 14-Segment and 16-Segment Digits and Hexadecimal Font for 7-Segment Digits**
- ♦ **Automatic Blinking Control for Each Segment**
- ♦ **10µA (typ) Low-Power Shutdown (Data Retained)**
- ♦ **16-Step Digit-by-Digit Digital Brightness Control**
- ♦ **Display Blanked on Power-Up**
- ♦ **Slew-Rate-Limited Segment Drivers for Lower EMI**
- ♦ **Five GPIO Port Pins Can Be Configured as Key-Switch Reader to Scan and Debounce Up to 32 Switches with n-Key Rollover**
- ♦ **IRQ Output when a Key Input is Debounced**
- ♦ **36-Pin SSOP and 6mm x 6mm 40-Pin TQFN Packages**
- ♦ **Automotive Temperature Range Standard**

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Voltage (with Respect to GND)
- V+ ....-0.3V to +6V
- SCL, SDA, AD0, AD1 ....-0.3V to +6V
- All Other Pins....................................-0.3V to (V+ + 0.3V)

Current
- O0–O7 Sink Current....................................935mA
- O0–O18 Source Current 55mA
- SCL, SDA, AD0, AD1, BLINK, OSC, OSC_OUT, ISET....20mA
- P0, P1, P2, P3, P4/$\overline{IRQ}$....................................40mA
- GND 1A

Continuous Power Dissipation (T_A = +70°C)
- 36-Pin SSOP (derate at 11.8mW/°C above +70°C) 941mW
- 40-Pin TQFN (derate at 25.6mW/°C above +70°C)....2051.3mW

Operating Temperature Range
- (T_{MIN} to T_{MAX}) ....-40°C to +125°C

Junction Temperature....................................+150°C
Storage Temperature Range....................................-65°C to +150°C
Lead Temperature (soldering, 10s)....................................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Shutdown mode, all digital inputs at V+ or GND	T_A = +25°C		10	35	µA
			T_A = T_{MIN} to T_{MAX}			40	
Operating Supply Current	I+	All segments on, all digits scanned, intensity set to full, internal oscillator, no display or OSC_OUT load connected	T_A = +25°C		22	30	mA
			T_A = T_{MIN} to T_{MAX}			35	
Master Clock Frequency	f_{OSC}	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			4		MHz
		OSC driven externally		1		8	
Dead Clock Protection Frequency	f_{OSC}				95		kHz
OSC Internal/External Detection Threshold	V_{OSC}				1.7		V
OSC High Time	t_{CH}			50			ns
OSC Low Time	t_{CL}			50			ns
Slow Segment Blink Period	$f_{SLOWBLINK}$	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			1		s
Fast Segment Blink Period	$f_{FASTBLINK}$	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			0.5		s
Fast or Slow Segment Blink Duty Cycle				49.5		50.5	%

DC ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Segment Drive Source Current	I_{SEG}	V_{LED} = 2.2V, V+ = 3.3V	T_A = +25°C	-32	-40	-48	mA
		V_{LED} = 2.2V, V+ = 2.7V					
Segment Current Slew Rate	$\Delta I_{SEG}/\Delta t$	T_A = +25°C, V+ = 3.3V			11		mA/µs
Segment Drive Current Matching	ΔI_{SEG}	T_A = +25°C, V+ = 3.3V			5		%
LOGIC INPUTS AND OUTPUTS							
Input High Voltage SDA, SCL, AD0, AD1	V_{IH}			0.7 x V+			V
Input Low Voltage SDA, SCL, AD0, AD1	V_{IL}					0.3 x V+	V
Input Leakage Current SDA, SCL, AD0, AD1, OSC, P0, P1, P2, P3, P4/$\overline{IRQ}$	I_{IH}, I_{IL}			-1		+1	µA
SDA Output Low Voltage	V_{OLSDA}	I_{SINK} = 6mA				0.4	V
Port Logic-High Input Voltage P0, P1, P2, P3, P4/$\overline{IRQ}$	V_{IHP}			0.7 x V+			V
Port Logic-Low Input Voltage P0, P1, P2, P3, P4/$\overline{IRQ}$	V_{ILP}					0.3 x V+	V
Port Hysteresis Voltage P0, P1, P2, P3, P4/$\overline{IRQ}$	ΔV_{IP}				0.03 x V+		V
Port Input Pullup Current from V+	I_{IPU}	P0 to P3 configured as key-scan inputs, V+ = 3.3V			75		µA
Port Output Low Voltage	V_{OLP}	I_{SINK} = 8mA			0.3	0.5	V
Blink Output Low Voltage	V_{OLBK}	I_{SINK} = 0.6mA			0.1	0.3	V
OSC_OUT Output High Voltage	V_{OHOSC}	I_{SOURCE} = 1.6mA		V+ - 0.4			V
OSC_OUT Output Low Voltage	V_{OLOSC}	I_{SINK} = 1.6mA				0.4	V

TIMING CHARACTERISTICS

(Typical Operating Circuit, V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

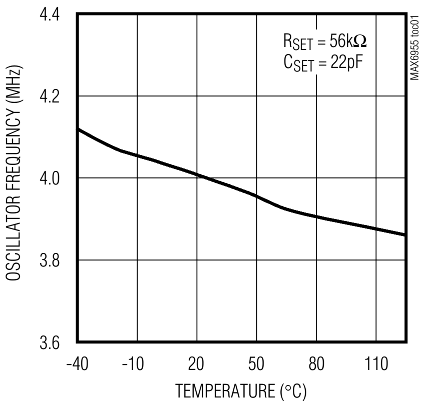
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	t_{HD}, t_{STA}		0.6			µs
Repeated START Condition Setup Time	t_{SU}, t_{STA}		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Data Hold Time	t_{HD}, t_{DAT}	(Note 3)			0.9	µs
Data Setup Time	t_{SU}, t_{DAT}		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		20 + $0.1C_B$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		20 + $0.1C_B$	300	ns
Fall Time of SDA Transmitting	t_F, t_X	(Notes 2, 5)		20 + $0.1C_B$	300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 2, 6)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 2)		400		pF

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL}- of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 4: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 5: $I_{SINK} \leq 6mA$. C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

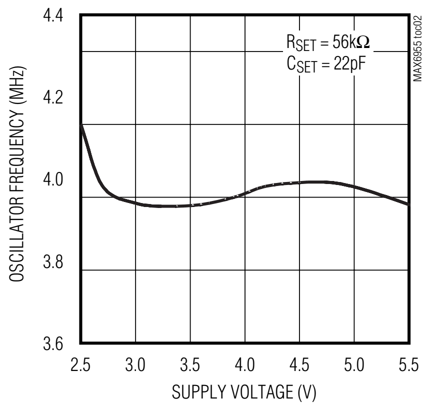
Typical Operating Characteristics

(V+ = 3.3V, LED forward voltage = 2.4V, Typical Application Circuit, T_A = +25°C, unless otherwise noted.)

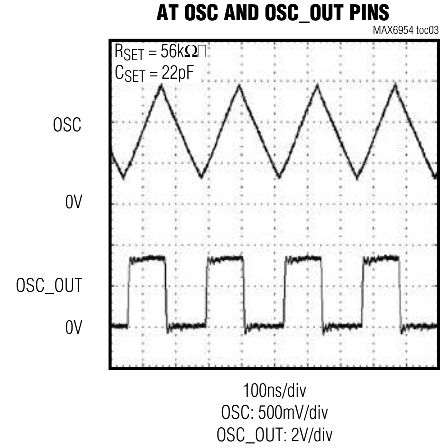
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



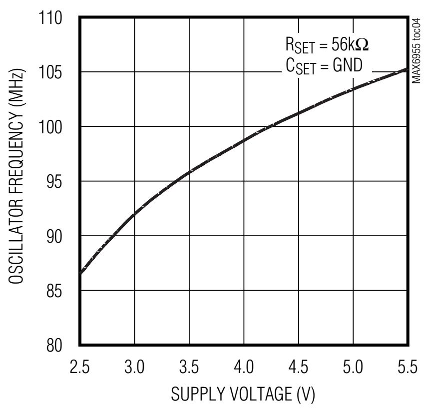
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



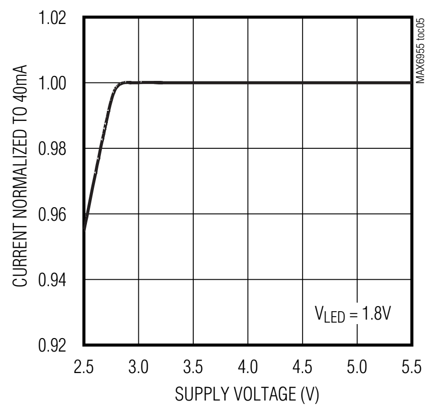
INTERNAL OSCILLATOR WAVEFORM AT OSC AND OSC_OUT PINS



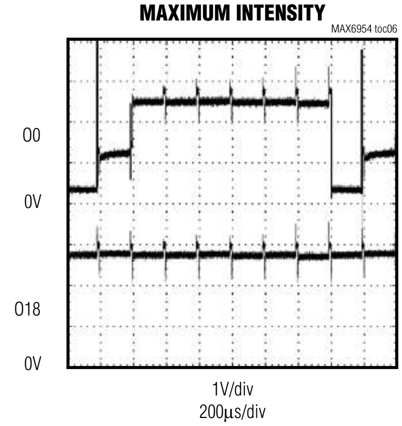
DEAD CLOCK OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



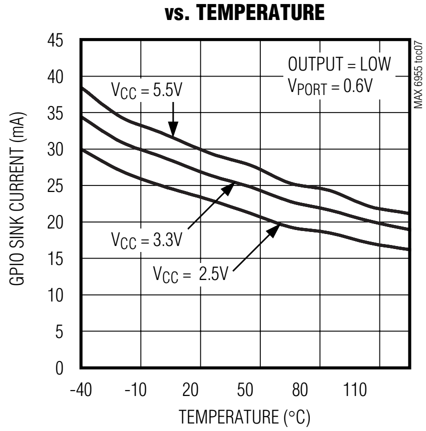
SEGMENT SOURCE CURRENT vs. SUPPLY VOLTAGE



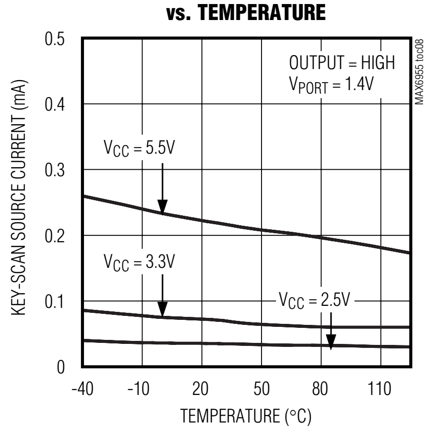
WAVEFORM AT PINS O0 AND O18, MAXIMUM INTENSITY



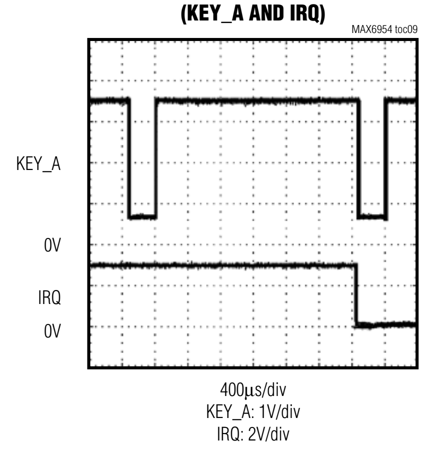
GPIO SINK CURRENT vs. TEMPERATURE



PORT INPUT PULLUP CURRENT vs. TEMPERATURE



KEY-SCAN OPERATION (KEY_A AND IRQ)



Pin Description

PIN		NAME	FUNCTION
SSOP	TQFN-EP		
1, 2, 34, 35	36, 37, 33, 34	P0–P3	General-Purpose I/O Ports (GPIOs). GPIO can be configured as logic inputs or open-drain outputs. Enabling key scanning configures some or all ports P0–P3 as key-switch matrix inputs with internal pullup (Key_A through Key_D).
3	38	AD0	Address Input 0. Sets device slave address. Connect to GND, V+, SCL, or SDA to give four logic combinations. See Table 5.
4	39	SDA	I^2C-Compatible Serial Data I/O
5	40	SCL	I^2C-Compatible Serial Clock Input
6	1	AD1	Address Input 1. Sets device slave address. Connect to GND, V+, SCL, or SDA to give four logic combinations. See Table 5.
7–15, 22–31	2–10, 21–30	O0–O18	Digit/Segment Drivers. When acting as digit drivers, outputs O0 to O7 sink current from the display common cathodes. When acting as segment drivers, O0 to O18 source current to the display anodes. O0 to O18 are high impedance when not being used as digit or segment drivers.
16, 18	12, 13, 15	GND	Ground
17	14	ISET	Segment Current Setting. Connect ISET to GND through series resistor R_{SET} to set the peak current.
19, 21	16, 18, 19	V+	Positive Supply Voltage. Bypass V+ to GND with a 47µF bulk capacitor and a 0.1µF ceramic capacitor.
20	17	OSC	Multiplex Clock Input. To use internal oscillator, connect capacitor C_{SET} from OSC to GND. To use external clock, drive OSC with a 1MHz to 8MHz CMOS clock.
32	31	BLINK	Blink Clock Output. Output is open drain.
33	32	OSC_OUT	Clock Output. OSC_OUT is a buffered clock output to allow easy blink synchronization of multiple MAX6955s. Output is push-pull.
36	35	P4/$\overline{IRQ}$	General-Purpose I/O Port. Also functions as IRQ output when key scanning is enabled.
—	11, 20	N.C.	Not Internally Connected
—	—	EP	Exposed Paddle. Internally connected to GND. Connect to a large ground plane to improve thermal performance.

Detailed Description

The MAX6955 is a serially interfaced display driver that can drive up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, 128 discrete LEDs, or a combination of these display types. Table 1 shows the drive capability of the MAX6955 for monocolor and bicolor displays.

The MAX6955 includes 104-character ASCII font maps for 14-segment and 16-segment displays, as well as the hexadecimal font map for 7-segment displays. The characters follow the standard ASCII font, with the addition of the following common symbols: £, €, ¥, °, µ, ±, ↑, and ↓. Seven bits represent the 104-character font map; an 8th bit is used to select whether the decimal point (DP) is lit. Seven-segment LED digits can be controlled directly or use the hexadecimal font. Direct segment control allows the MAX6955 to be used to drive bar graphs and discrete LED indicators.

Tables 2, 3, and 4 list the connection schemes for 16-, 14-, and 7-segment digits, respectively. The letters in Tables 2, 3, and 4 correspond to the segment labels shown in Figure 1. (For applications that require mixed display types, see Tables 38–41.)

Serial Interface

Serial Addressing

The MAX6955 operates as a slave that sends and receives data through an I^2C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a

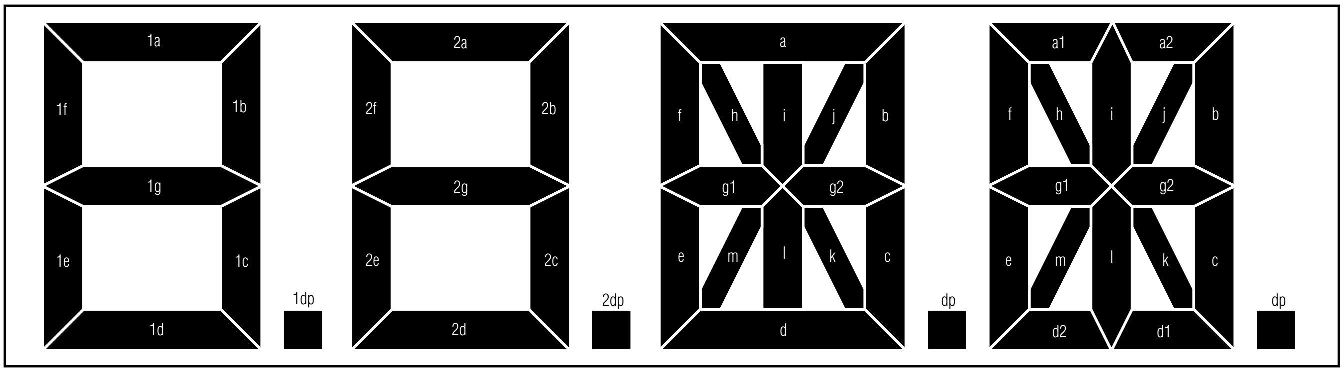


Figure 1. Segment Labeling for 7-Segment Display, 14-Segment Display, and 16-Segment Display

Table 1. MAX6955 Drive Capability

DISPLAY TYPE	7 SEGMENT (16-CHARACTER HEXADECIMAL FONT)	14 SEGMENT/ 16 SEGMENT (104-CHARACTER ASCII FONT MAP)	DISCRETE LEDs (DIRECT CONTROL)
Monocolor	16	8	128
Bicolor	8	4	64

serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6955, and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX6955 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on the SDA. The MAX6955 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX6955 7-bit slave address plus R/$\overline{W}$ bit (Figure 4), a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 5).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 6). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX6955, the MAX6955 generates the acknowledge bit because the MAX6955 is the recipient. When the MAX6955 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX6955 has a 7-bit-long slave address (Figure 4). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, high for a read command.

The first 3 bits (MSBs) of the MAX6955 slave address are always 110. Slave address bits A3, A2, A1, and A0 are selected by the address input pins AD1 and AD0. These two input pins can be connected to GND, V+, SDA, or SCL. The MAX6955 has 16 possible slave addresses (Table 5) and therefore a maximum of 16 MAX6955 devices can share the same interface.

Table 2. Connection Scheme for Eight 16-Segment Digits

DIGIT	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0	CCO	—	a1	a2	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
1	—	CC1	a1	a2	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
2	a1	a2	CC2	—	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
3	a1	a2	—	CC3	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
4	a1	a2	b	c	CC4	—	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
5	a1	a2	b	c	—	CC5	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
6	a1	a2	b	c	d1	d2	CC6	—	e	f	g1	g2	h	i	j	k	l	m	dp
7	a1	a2	b	c	d1	d2	—	CC7	e	f	g1	g2	h	i	j	k	l	m	dp

Table 3. Connection Scheme for Eight 14-Segment Digits

DIGIT	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0	CCO	—	a	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
1	—	CC1	a	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
2	a	—	CC2	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
3	a	—	—	CC3	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
4	a	—	b	c	CC4	—	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
5	a	—	b	c	—	CC5	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
6	a	—	b	c	d	—	CC6	—	e	f	g1	g2	h	i	j	k	l	m	dp
7	a	—	b	c	d	—	—	CC7	e	f	g1	g2	h	i	j	k	l	m	dp

Table 4. Connection Scheme for Sixteen 7-Segment Digits

DIGIT	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0, 0a	CC0	—	1a	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
1, 1a	—	CC1	1a	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
2, 2a	1a	—	CC2	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
3, 3a	1a	—	—	CC3	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
4, 4a	1a	—	1b	1c	CC4	—	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
5, 5a	1a	—	1b	1c	—	CC5	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
6, 6a	1a	—	1b	1c	1d	1dp	CC6	—	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
7, 7a	1a	—	1b	1c	1d	1dp	—	CC7	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp

Message Format for Writing

A write to the MAX6955 comprises the transmission of the MAX6955's slave address with the $R/\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte, which determines which register of the MAX6955 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX6955 takes no further action (Figure 7) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6955 selected by the command byte (Figure 8).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6955 internal registers because the command byte address generally autoincrements (Table 6) (Figure 9).

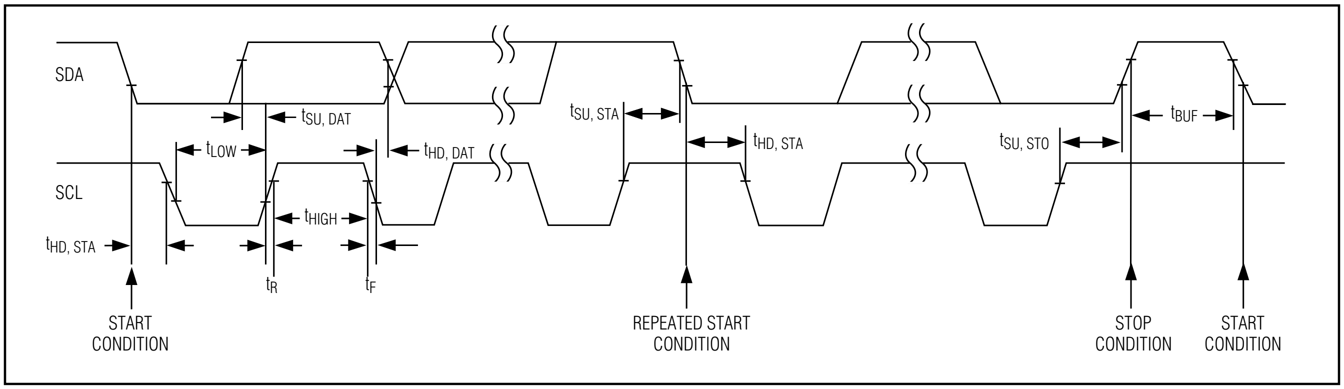


Figure 2. 2-Wire Serial Interface Timing Details

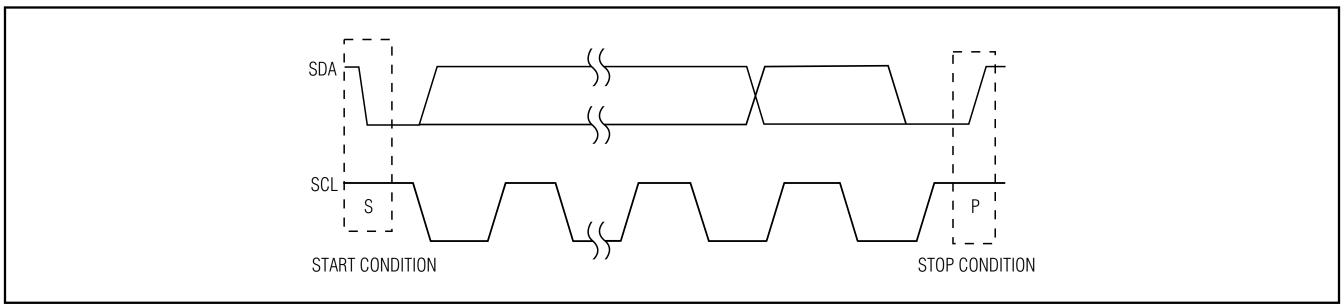


Figure 3. Start and Stop Conditions

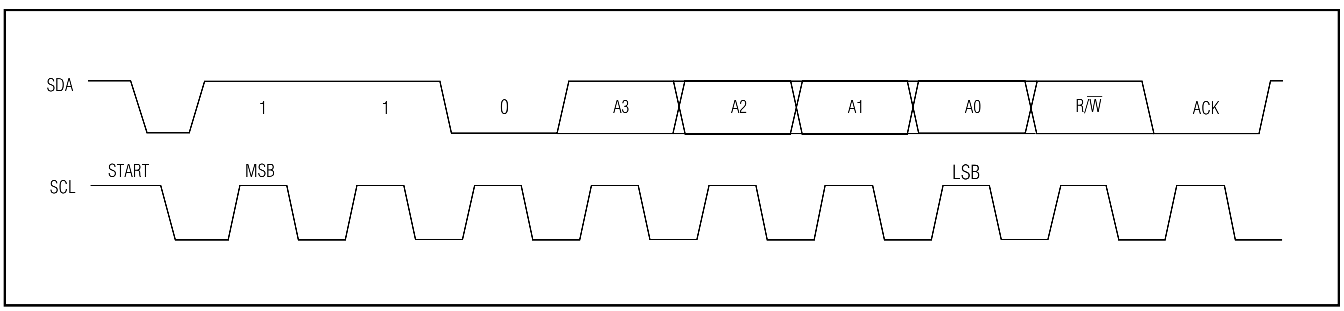


Figure 4. Slave Address

Table 5. MAX6955 Address Map

PIN CONNECTION		DEVICE ADDRESS						
AD1	AD0	A6	A5	A4	A3	A2	A1	A0
GND	GND	1	1	0	0	0	0	0
GND	V+	1	1	0	0	0	0	1
GND	SDA	1	1	0	0	0	1	0
GND	SCL	1	1	0	0	0	1	1
V+	GND	1	1	0	0	1	0	0
V+	V+	1	1	0	0	1	0	1
V+	SDA	1	1	0	0	1	1	0
V+	SCL	1	1	0	0	1	1	1
SDA	GND	1	1	0	1	0	0	0
SDA	V+	1	1	0	1	0	0	1
SDA	SDA	1	1	0	1	0	1	0
SDA	SCL	1	1	0	1	0	1	1
SCL	GND	1	1	0	1	1	0	0
SCL	V+	1	1	0	1	1	0	1
SCL	SDA	1	1	0	1	1	1	0
SCL	SCL	1	1	0	1	1	1	1

Message Format for Reading

The MAX6955 is read using the MAX6955's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 6). Thus, a read is initiated by first configuring the MAX6955's command byte by performing a write (Figure 7). The master can now read n consecutive bytes from the MAX6955, with the first data byte being read from the register addressed by the initialized command byte (Figure 9). When performing read-after-write verification, reset the command byte's address because the stored byte address generally is autoincremented after the write (Table 6).

Operation with Multiple Masters

If the MAX6955 is operated on a 2-wire interface with multiple masters, a master reading the MAX6955 should use a repeated start between the write, which sets the MAX6955's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX6955's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX6955's address pointer, then master 1's delayed read may be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the MAX6955 to be configured with the shortest number of transmissions by minimizing the number of times the command byte needs to be sent. The command address or the font pointer address stored in the MAX6955 generally increments after each data byte is written or read (Table 6). To utilize the autoincrement read cycle feature, the master clocks SCL after the first data byte is read, and the MAX6955 continues sending data, incrementing the pointer after each byte is sent. A not-acknowledge or stop condition halts autoincrement.

Digit Type Registers

The MAX6955 uses 32 digit registers to store the characters that the user wishes to display. These digit registers are implemented with two planes, P0 and P1. Each digit is represented by 2 bytes of memory, 1 byte in plane P0 and the other in plane P1. The digit registers are mapped so that a digit's data can be updated in plane P0, plane P1, or both planes at the same time (Table 7).

If the blink function is disabled through the Blink Enable Bit E (Table 20) in the configuration register, then the digit register data in plane P0 is used to multiplex the display. The digit register data in P1 is not used. If the blink function is enabled, then the digit register data in both plane P0 and plane P1 are alternately used to multiplex the display. Blinking is achieved by multiplexing the LED display using data plane P0 and plane P1 on alternate phases of the blink clock (Table 21).

Table 6. Command Address Autoincrement Rules

COMMAND BYTE ADDRESS RANGE	AUTOINCREMENT BEHAVIOR
x0000000 to x0001100	Command byte address autoincrements after byte read or written.
x0001101	Factory reserved; do not write this register.
x0001111 to x1111110	Command byte address autoincrements after byte read or written.
x1111111	Command byte address remains at x1111111 after byte read or written.

The data in the digit registers does not control the digit segments directly for 14- and 16-segment displays. Instead, the register data is used to address a character generator that stores the data for the 14- and 16-segment fonts (Tables 8 and 9). The lower 7 bits of the digit data (D6 to D0) select the character from the font. The most significant bit of the register data (D7) controls the DP segment of the digits; it is set to 1 to light DP, and to zero to leave DP unlit (Table 10).

For 7-segment displays, the digit plane data register can be used to address a character generator, which contains the data of a 16-character font containing the hexadecimal font. The decode mode register can be used to disable the character generator and allow the segments to be controlled directly. Table 11 shows the one-to-one pairing of each data bit to the appropriate segment line in the digit plane data registers. The hexadecimal font is decoded according to Table 12.

The digit-type register configures the display driver for various combinations of 14-segment digits, 16-segment digits, and/or pairs, or 7-segment digits. The function of this register is to select the appropriate font for each digit and route the output of the font to the appropriate MAX6955 driver output pins. The MAX6955 has four digit drive slots. A slot can be filled with various combinations of monocolor and bicolor 16-segment displays, 14-segment displays, or two 7-segment displays. Each pair of bits in the register corresponds to one of the four digit drive slots, as shown in Table 13. Each bit also corresponds to one of the eight common-cathode digit drive outputs, CC0 to CC7. When using bicolor digits, the anode connections for the two digits within a slot are always the same. This means that a slot correctly drives two monocolor or one bicolor 14- or 16-segment digit. The digit type register can be written, but cannot be read. Examples of configuration settings required for some display digit combinations are shown in Table 14.

7-Segment Decode-Mode Register

In 7-segment mode, the hexadecimal font can be disabled (Table 15). The decode-mode register selects between hexadecimal code or direct control for each of eight possible pairs of 7-segment digits. Each bit in the register corresponds to one pair of digits. The digit pairs are {digit 0, digit 0a} through {digit 7, digit 7a}. Disabling decode mode allows direct control of the 16 LEDs of a dual 7-segment display. Direct control mode can also be used to drive a matrix of 128 discrete LEDs.

A logic high selects hexadecimal decoding, while a logic low bypasses the decoder. When direct control is selected, the data bits D7 to D0 correspond to the segment lines of the MAX6955. Write x0010000 to blank all segments in hexadecimal decode mode.

Display Blink Mode

The display blinking facility, when enabled, makes the driver flip automatically between displaying the digit register data in planes P0 and P1. If the digit register data for any digit is different in the two planes, then that digit appears to flip between two characters. To make a character appear to blink on or off, write the character to one plane, and use the blank character (0x20) for the other plane. Once blinking has been configured, it continues automatically without further intervention.

Blink Speed

The blink speed is determined by the frequency of the multiplex clock, OSC, and by the setting of the Blink Rate Selection Bit B (Table 19) in the configuration register. The Blink Rate Selection Bit B sets either fast or slow blink speed for the whole display.

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, intensities are set to minimum, and shutdown is enabled (Table 16).

Configuration Register

The configuration register is used to enter and exit shutdown, select the blink rate, globally enable and disable the blink function, globally clear the digit data, select between global or digit-by-digit control of intensity, and reset the blink timing (Tables 17–20 and 22–25).

The configuration register contains 7 bits:

- S bit selects shutdown or normal operation (read/write).
- B bit selects the blink rate (read/write).
- E bit globally enables or disables the blink function (read/write).
- T bit resets the blink timing (data is not stored—transient bit).
- R bit globally clears the digit data for both planes P0 and P1 for ALL digits (data is not stored—transient bit).
- I bit selects between global or digit-by-digit control of intensity (read/write).
- P bit returns the current phase of the blink timing (read only—a write to this bit is ignored).

Character Generator Font Mapping

The font is composed of 104 characters in ROM. The lower 7 bits of the 8-bit digit register represent the character selection. The most significant bit, shown as x in the ROM map of Tables 8 and 9, is 1 to light the DP segment and zero to leave the DP segment unlit.

The character map follows the standard ASCII font for 96 characters in the x0101000 through x1111111 range. The first 16 characters of the 16-segment ROM map cover 7-segment displays. These 16 characters are numeric 0 to 9 and characters A to F (i.e., the hexadecimal set).

Multiplex Clock and Blink Timing

The OSC pin can be fitted with capacitor C_{SET} to GND to use the internal RC multiplex oscillator, or driven by an external clock to set the multiplex clock frequency and blink rate. The multiplex clock frequency determines the frequency that the complete display is updated. With OSC at 4MHz, each display digit is enabled for 200µs.

The internal RC oscillator uses an external resistor, R_{SET}, and an external capacitor, C_{SET}, to set the oscillator frequency. The suggested values of R_{SET} (56kΩ) and C_{SET} (22pF) set the oscillator at 4MHz, which makes the blink frequency 0.5Hz or 1Hz.

The external clock is not required to have a 50:50 duty cycle, but the minimum time between transitions must be 50ns or greater and the maximum time between transitions must be 750ns.

The on-chip oscillator may be accurate enough for applications using a single device. If an exact blink rate is required, use an external clock ranging between 1MHz and 8MHz to drive OSC. The OSC inputs of multiple MAX6955s can be connected to a common external clock to make the devices blink at the same rate. The relative blink phasing of multiple MAX6955s can be synchronized by setting the T bit in the control register for all the devices in quick succession. If the serial interfaces of multiple MAX6955s are daisy-chained by connecting the DOUT of one device to the DIN of the next, then synchronization is achieved automatically by updating the configuration register for all devices simultaneously. Figure 10 is the multiplex timing diagram.

OSC_OUT Output

The OSC_OUT output is a buffered copy of either the internal oscillator clock or the clock driven into the OSC pin if the external clock has been selected. The feature is useful if the internal oscillator is used, and the user wishes to synchronize other MAX6955s to the same blink frequency. The oscillator is disabled while the MAX6955 is in shutdown.

Scan-Limit Register

The scan-limit register sets how many 14-segment digits or 16-segment digits or pairs of 7-segment digits are displayed, from 1 to 8. A bicolor digit is connected as two monocolor digits. The scan register also limits the number of keys that can be scanned.

Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading-zero suppression). Table 26 shows the scan-limit register format.

Intensity Registers

Digital control of display brightness is provided and can be managed in one of two ways: globally or individually. Global control adjusts all digits together. Individual control adjusts the digits separately.

The default method is global brightness control, which is selected by clearing the global intensity bit (I data bit D6) in the configuration register. This brightness setting applies to all display digits. The pulse-width modulator is then set by the lower nibble of the global intensity register, address 0x02. The modulator scales the average segment current in 16 steps from a maximum of 15/16 down to 1/16 of the peak current. The minimum interdigit blanking time is set to 1/16 of a cycle. When using bicolor digits, 256 color/brightness combinations are available.

Individual brightness control is selected by setting the global intensity bit (I data bit D6) in the configuration register. The pulse-width modulator is now no longer set by the lower nibble of the global intensity register, address 0x02, and the data is ignored. Individual digital control of display brightness is now provided by a separate pulse-width modulator setting for each digit. Each digit is controlled by a nibble of one of the four intensity registers: intensity10, intensity32, intensity54, and intensity76 for all display types, plus intensity10a, intensity32a, intensity54a, and intensity76a for the extra eight digits possible when 7-segment displays are used. The data from the relevant register is used for each digit as it is multiplexed. The modulator scales the average segment current in 16 steps in exactly the same way as global intensity adjustment.

Table 27 shows the global intensity register format. Table 28 shows individual segment intensity registers. Table 29 shows the even individual segment intensity format. Table 30 shows the odd individual segment intensity format.

GPIO and Key Scanning

The MAX6955 features five general-purpose input/output (GPIO) ports: P0 to P4. These ports can be individually enabled as logic inputs or open-drain logic outputs. The GPIO ports are not debounced when configured as inputs. The ports can be read and the outputs set using the 2-wire interface.

Some or all of the five ports can be configured to perform key scanning of up to 32 keys. Ports P0 to P4 are renamed Key_A, Key_B, Key_C, Key_D, and IRQ, respectively, when used for key scanning. The full key-scanning configuration is shown in Figure 11. Table 31 is the GPIO data register.

Table 7. Register Address Map

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	0	0	0	0x00
Decode Mode	X	0	0	0	0	0	0	1	0x01
Global Intensity	X	0	0	0	0	0	1	0	0x02
Scan Limit	X	0	0	0	0	0	1	1	0x03
Configuration	X	0	0	0	0	1	0	0	0x04
GPIO Data	X	0	0	0	0	1	0	1	0x05
Port Configuration	X	0	0	0	0	1	1	0	0x06
Display Test	X	0	0	0	0	1	1	1	0x07
Write KEY_A Mask Read KEY_A Debounce	X	0	0	0	1	0	0	0	0x08
Write KEY_B Mask Read KEY_B Debounce	X	0	0	0	1	0	0	1	0x09
Write KEY_C Mask Read KEY_C Debounce	X	0	0	0	1	0	1	0	0x0A
Write KEY_D Mask Read KEY_D Debounce	X	0	0	0	1	0	1	1	0x0B
Write Digit Type Read KEY_A Pressed	X	0	0	0	1	1	0	0	0x0C
Read KEY_B Pressed*	X	0	0	0	1	1	0	1	0x0D
Read KEY_C Pressed*	X	0	0	0	1	1	1	0	0x0E
Read KEY_D Pressed*	X	0	0	0	1	1	1	1	0x0F
Intensity 10	X	0	0	1	0	0	0	0	0x10
Intensity 32	X	0	0	1	0	0	0	1	0x11
Intensity 54	X	0	0	1	0	0	1	0	0x12
Intensity 76	X	0	0	1	0	0	1	1	0x13
Intensity 10a (7 Segment Only)	X	0	0	1	0	1	0	0	0x14
Intensity 32a (7 Segment Only)	X	0	0	1	0	1	0	1	0x15
Intensity 54a (7 Segment Only)	X	0	0	1	0	1	1	0	0x16
Intensity 76a (7 Segment Only)	X	0	0	1	0	1	1	1	0x17
Digit 0 Plane P0	X	0	1	0	0	0	0	0	0x20
Digit 1 Plane P0	X	0	1	0	0	0	0	1	0x21
Digit 2 Plane P0	X	0	1	0	0	0	1	0	0x22
Digit 3 Plane P0	X	0	1	0	0	0	1	1	0x23
Digit 4 Plane P0	X	0	1	0	0	1	0	0	0x24
Digit 5 Plane P0	X	0	1	0	0	1	0	1	0x25
Digit 6 Plane P0	X	0	1	0	0	1	1	0	0x26
Digit 7 Plane P0	X	0	1	0	0	1	1	1	0x27
Digit 0a Plane P0 (7 Segment Only)	X	0	1	0	1	0	0	0	0x28
Digit 1a Plane P0 (7 Segment Only)	X	0	1	0	1	0	0	1	0x29
Digit 2a Plane P0 (7 Segment Only)	X	0	1	0	1	0	1	0	0x2A
Digit 3a Plane P0 (7 Segment Only)	X	0	1	0	1	0	1	1	0x2B

**Do NOT write to register.*

Table 7. Register Address Map (continued)

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Digit 4a Plane P0 (7 Segment Only)	X	0	1	0	1	1	0	0	0x2C
Digit 5a Plane P0 (7 Segment Only)	X	0	1	0	1	1	0	1	0x2D
Digit 6a Plane P0 (7 Segment Only)	X	0	1	0	1	1	1	0	0x2E
Digit 7a Plane P0 (7 Segment Only)	X	0	1	0	1	1	1	1	0x2F
Digit 0 Plane P1	X	1	0	0	0	0	0	0	0x40
Digit 1 Plane P1	X	1	0	0	0	0	0	1	0x41
Digit 2 Plane P1	X	1	0	0	0	0	1	0	0x42
Digit 3 Plane P1	X	1	0	0	0	0	1	1	0x43
Digit 4 Plane P1	X	1	0	0	0	1	0	0	0x44
Digit 5 Plane P1	X	1	0	0	0	1	0	1	0x45
Digit 6 Plane P1	X	1	0	0	0	1	1	0	0x46
Digit 7 Plane P1	X	1	0	0	0	1	1	1	0x47
Digit 0a Plane P1 (7 Segment Only)	X	1	0	0	1	0	0	0	0x48
Digit 1a Plane P1 (7 Segment Only)	X	1	0	0	1	0	0	1	0x49
Digit 2a Plane P1 (7 Segment Only)	X	1	0	0	1	0	1	0	0x4A
Digit 3a Plane P1 (7 Segment Only)	X	1	0	0	1	0	1	1	0x4B
Digit 4a Plane P1 (7 Segment Only)	X	1	0	0	1	1	0	0	0x4C
Digit 5a Plane P1 (7 Segment Only)	X	1	0	0	1	1	0	1	0x4D
Digit 6a Plane P1 (7 Segment Only)	X	1	0	0	1	1	1	0	0x4E
Digit 7a Plane P1 (7 Segment Only)	X	1	0	0	1	1	1	1	0x4F
Write Digit 0 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	0	0	0	0x60
Write Digit 1 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	0	0	1	0x61
Write Digit 2 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	0	1	0	0x62
Write Digit 3 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	0	1	1	0x63
Write Digit 4 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	1	0	0	0x64
Write Digit 5 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	1	0	1	0x65
Write Digit 6 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	1	1	0	0x66
Write Digit 7 Planes P0 and P1 with Same Data, Reads as 0x00	X	1	1	0	0	1	1	1	0x67
Write Digit 0a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	0	0	0	0x68
Write Digit 1a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	0	0	1	0x69

Table 7. Register Address Map (continued)

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Write Digit 2a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	0	1	0	0x6A
Write Digit 3a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	0	1	1	0x6B
Write Digit 4a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	1	0	0	0x6C
Write Digit 5a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	1	0	1	0x6D
Write Digit 6a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	1	1	0	0x6E
Write Digit 7a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	X	1	1	0	1	1	1	1	0x6F

Note: *Unused register bits read as zero.*

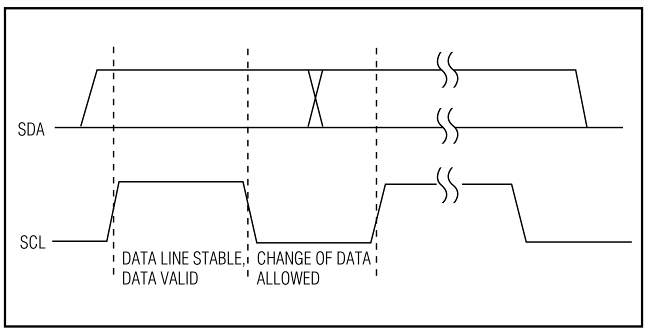


Figure 5. Bit Transfer

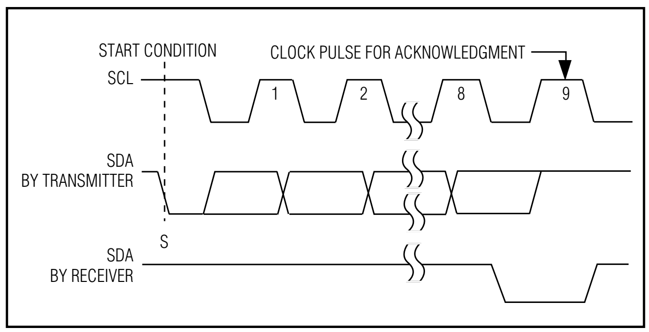


Figure 6. Acknowledge

One diode is required per key switch. Note that the forward voltages of the diode and LED must exceed V_{IH} of P0–P3. If this condition is not met, the voltage input to the port might be lower than the logic threshold and keys will not be detected properly.

The MAX6955 can only scan the maximum 32 keys if the scan-limit register is set to scan the maximum eight digits. If the MAX6955 is driving fewer digits, then a maximum of (4 x n) switches can be scanned, where n is the number of digits set in the scan-limit register. For example, if the MAX6955 is driving four 14-segment digits, cathode drivers O0 to O3 are used. Only 16 keys can be scanned in this configuration; the switches shown connected to O4 through O7 are not read.

If the user wishes to scan fewer than 32 keys, then fewer scan lines can be configured for key scanning. The unused Key_x ports are released back to their original GPIO functionality. If key scanning is enabled, regardless of the number of keys being scanned, P4/$\overline{IRQ}$ is always configured as IRQ (Table 32).

The key-scanning circuit utilizes the LEDs' common-cathode driver outputs as the key-scan drivers. O0 to O7 go low for nominally 200µs (with OSC = 4MHz) in turn as the displays are multiplexed. By varying the oscillator frequency, the debounce time changes, though key scanning still functions. Key_x inputs have internal pullup resistors that allow the key condition to be tested. The Key_x input is low during the appropriate digit multiplex period when the key is pressed. The timing diagram of Figure 12 shows the normal situation where all eight LED cathode drivers are used.

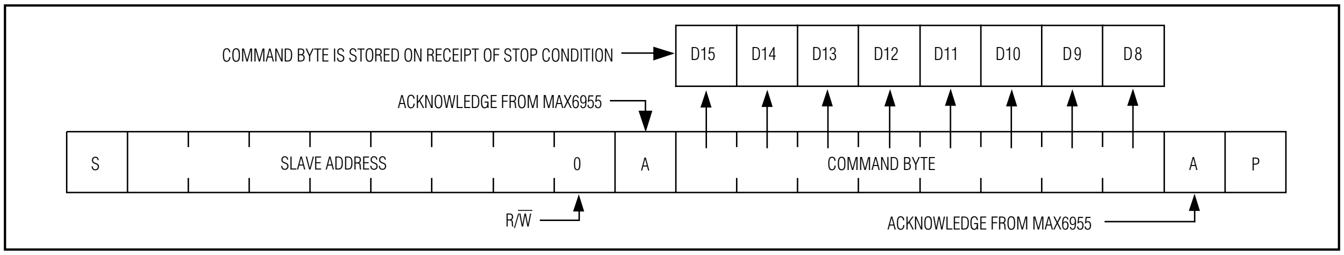


Figure 7. Command Byte Received

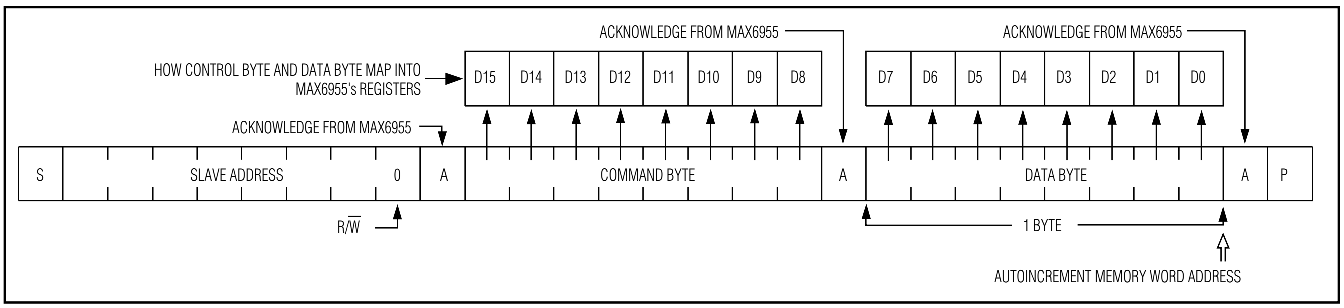


Figure 8. Command and Single Data Byte Received

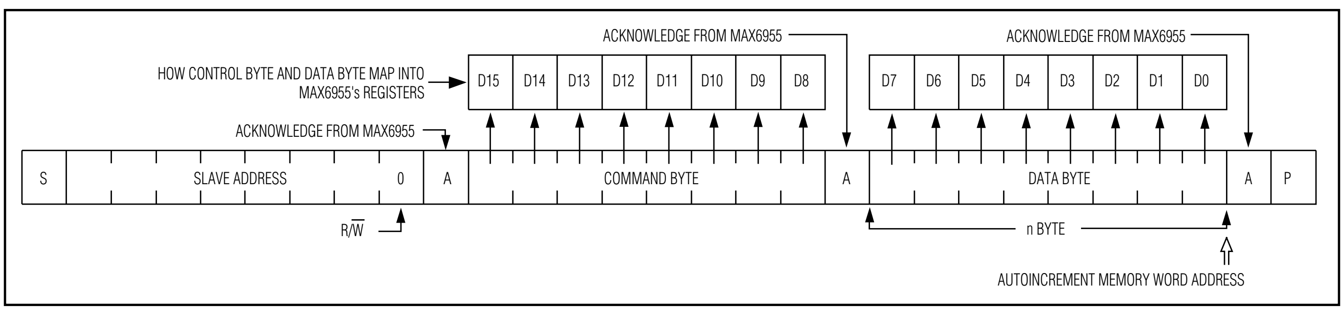


Figure 9. n Data Bytes Received

Each key press is scanned twice in a 25.6ms time period with a nominal oscillator frequency of 4MHz, as shown in Figure 12. In the first key test period of 1.6ms, input level at ports P0–P3 (Key_A, Key_B, Key_C, and Key_D) are examined in conjunction with the signal-low period of ports O0–O7 to see if any key is pressed. If pressed, the corresponding key pressed register bit is set. In the second key test period of 1.6ms, input level at ports P0–P3 are examined again (debounce) to see if the key is still pressed. If still pressed, the corresponding debounce register bit is set. The debounce time between key tests is 12.8ms.

Port Configuration Register

The port configuration register selects how the five port pins are used. The port configuration register format is described in Table 33.

Key Mask Registers

The Key_A Mask, Key_B Mask, Key_C Mask, and Key_D Mask write-only registers (Table 34) configure the key-scanning circuit to cause an interrupt only when selected (masked) keys have been debounced. Each bit in the register corresponds to one key switch. The bit is clear to disable interrupt for the switch, and set to enable interrupt. Keys are always scanned (if enabled through the port configuration register), regardless of the setting of these interrupt bits, and the key status is stored in the appropriate Key_x pressed register.

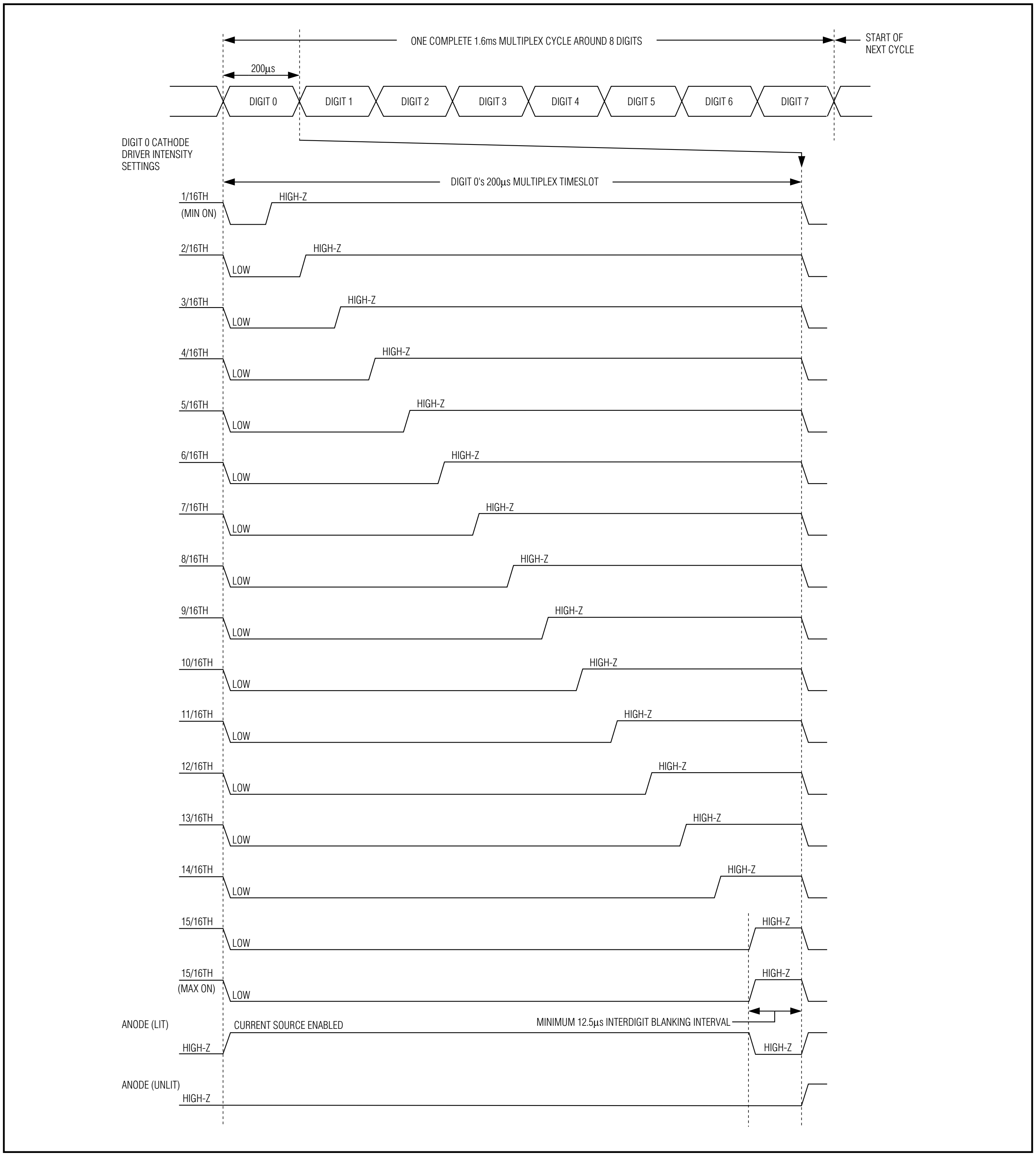


Figure 10. Multiplex Timing Diagram (OSC = 4MHz)

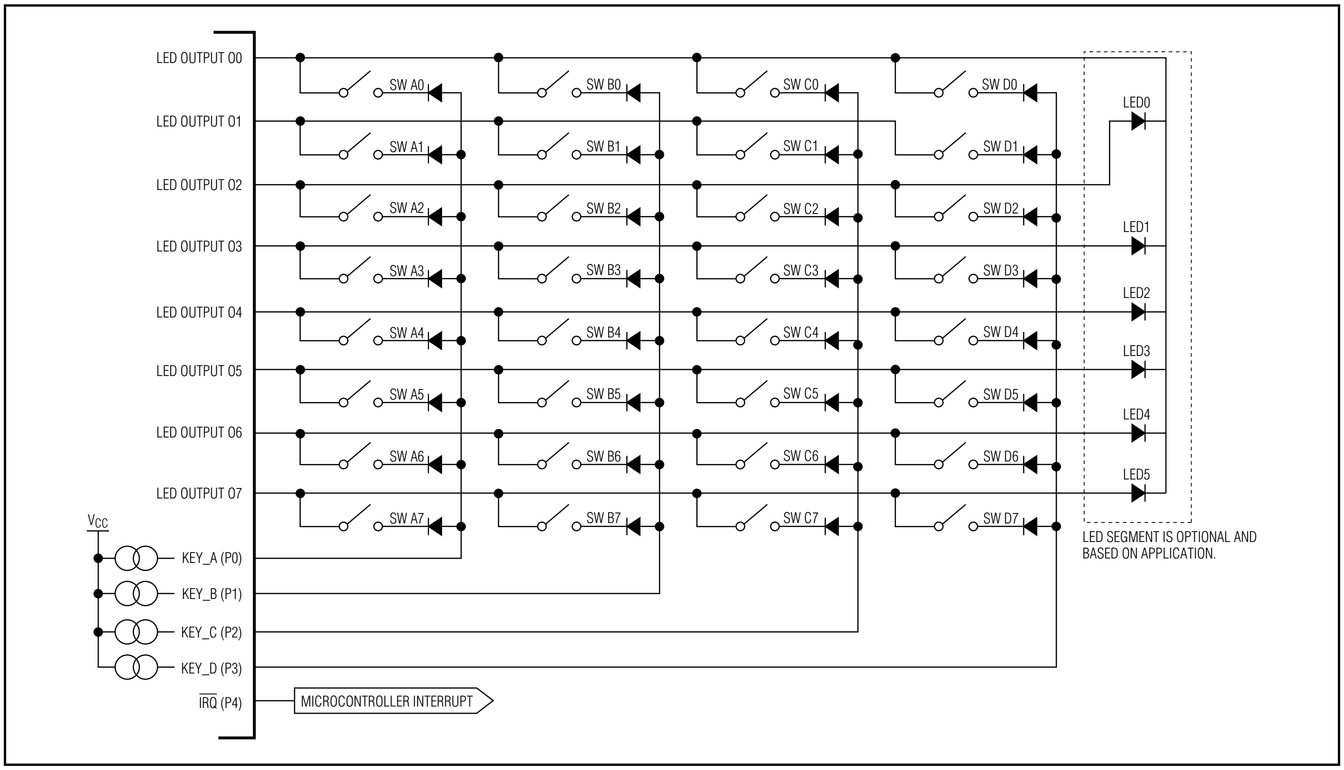


Figure 11. Key-Scanning Configuration

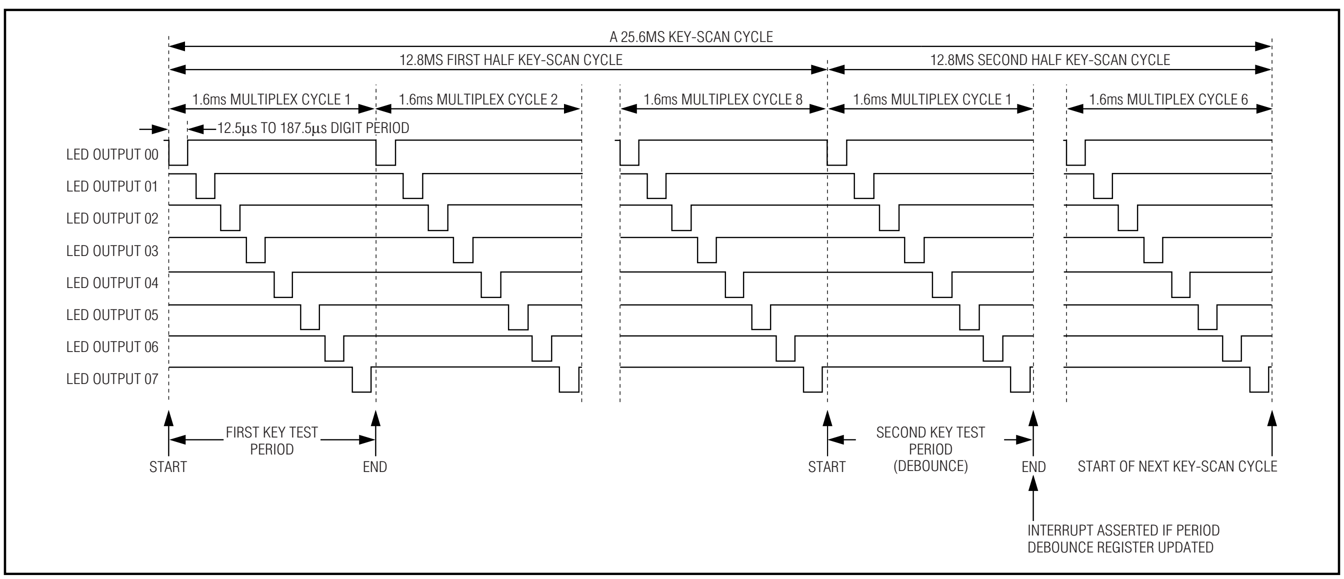


Figure 12. Key-Scan Timing Diagram

Key Debounced Registers

The Key_A debounced, Key_B debounced, Key_C debounced, and Key_D debounced read-only registers (Table 35) show which keys have been detected as debounced by the key-scanning circuit.

Each bit in the register corresponds to one key switch. The bit is set if the switch has been correctly debounced since the register was read last. Reading a debounced register clears that register (after the data has been read) so that future keys pressed can be identified. If the debounced registers are not read, the key-scan data accumulates. However, as there is no FIFO in the MAX6955, the user is not able to determine key order, or whether a key has been pressed more than once, unless the debounced key status registers are read after each interrupt, and before the next key-scan cycle.

Reading any of the four debounced registers clears the P4/$\overline{IRQ}$ output. If a key is pressed and held down, the key is reported as debounced (and IRQ issued) only once. The key must be detected as released by the key-scanning circuit, before it debounces again. If the debounced registers are being read in response to the P4/$\overline{IRQ}$ being asserted, then the user should generally read all four registers to ensure that all the keys that were detected by the key-scanning circuit are discovered.

Key Pressed Registers

The Key_A pressed, Key_B pressed, Key_C pressed, and Key_D pressed read-only registers (Table 36) show which keys have been detected as pressed by the key-scanning circuit during the last test.

Each bit in the register corresponds to one key switch. The bit is set if the switch has been detected as pressed by the key-scanning circuit during the last test. The bit is cleared if the switch has not been detected as pressed by the key-scanning circuit during the last test. Reading a pressed register does not clear that register or clear the P4/$\overline{IRQ}$ output.

Display Test Register

The display test register (Table 37) operates in two modes: normal and display test. Display test mode turns all LEDs on (including DPs) by overriding, but not altering, all controls and digit registers (including the shutdown register), except for the digit-type register and the GPIO configuration register. The duty cycle, while in display test mode, is 7/16 (see the *Choosing Supply Voltage to Minimize Power Dissipation* section).

Selecting External Components R_{SET} and C_{SET} to Set Oscillator Frequency and Peak Segment Current

The RC oscillator uses an external resistor, R_{SET}, and an external capacitor, C_{SET}, to set the frequency, f_{OSC}. The allowed range of f_{OSC} is 1MHz to 8MHz. R_{SET} also sets the peak segment current. The recommended values of R_{SET} and C_{SET} set the oscillator to 4MHz, which makes the blink frequencies selectable between 0.5Hz and 1Hz. The recommended value of R_{SET} also sets the peak current to 40mA, which makes the segment current adjustable from 2.5mA to 37.5mA in 2.5mA steps.

$$I_{SEG} = K_L/R_{SET} \text{ mA}$$

$$f_{OSC} = K_F/(R_{SET} \times C_{SET}) \text{ MHz}$$

where:

$K_L = 2240$

$K_F = 10K$ (typ)

R_{SET} = external resistor in kΩ

C_{SET} = external capacitor in pF

C_{STRAY} = stray capacitance from OSC pin to GND in pF

The recommended value of R_{SET} is 56kΩ and the recommended value of C_{SET} is 22pF.

The recommended value of R_{SET} is the minimum allowed value, since it sets the display driver to the maximum allowed peak segment current. R_{SET} can be set to a higher value to set the segment current to a lower peak value where desired. The user must also ensure that the peak current specifications of the LEDs connected to the driver are not exceeded.

The effective value of C_{SET} includes not only the actual external capacitor used, but also the stray capacitance from OSC to GND. This capacitance is usually in the 1pF to 30pF range, depending on the layout used.

Applications Information

Driving Bicolor LEDs

Bicolor digits group a red and a green die together for each display element, so that the element can be lit red or green (or orange), depending on which die (or both) is lit. The MAX6955 allows each segment's current to be set individually from the 1/16th (minimum current and LED intensity) to 15/16th (maximum current and LED intensity), as well as off (zero current). Thus, a bicolor (red-green) segment pair can be set to 256 color/intensity combinations.

Choosing Supply Voltage to Minimize Power Dissipation

The MAX6955 drives a peak current of 40mA into LEDs with a 2.2V forward-voltage drop when operated from a supply voltage of at least 3.0V. The minimum voltage drop across the internal LED drivers is therefore (3.0V - 2.2V) = 0.8V. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward-voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.6V of headroom.

The voltage drop across the drivers with a nominal 5V supply (5.0V - 2.2V) = 2.8V is nearly 3 times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V) = 1.1V. In most systems, consumption is an important design criterion, and the MAX6955 should be operated from the system's 3.3V nominal supply. In other designs, the lowest supply voltage may be 5V. The issue now is to ensure the dissipation limit for the MAX6955 is not exceeded. This can be achieved by inserting a series resistor in the supply to the MAX6955, ensuring that the supply decoupling capacitors are still on the MAX6955 side of the resistor. For example, consider the requirement that the minimum supply voltage to a MAX6955 must be 3.0V, and the input supply range is 5V ±5%. Maximum supply current is 35mA + (40mA x 17) = 715mA. Minimum input supply voltage is 4.75V. Maximum series resistor value is (4.75V - 3.0V)/0.715A = 2.44Ω. We choose 2.2Ω ±5%. Worst-case resistor dissipation is at maximum toleranced resistance, i.e., (0.715A) 2 x (2.2Ω x 1.05) = 1.18W. The maximum MAX6955 supply voltage is at maximum input supply voltage and minimum toleranced resistance, i.e., 5.25V - (0.715A x 2.2Ω x 0.95) = 3.76V.

Low-Voltage Operation

The MAX6955 works over the 2.7V to 5.5V supply range. The minimum useful supply voltage is determined by the forward-voltage drop of the LEDs at the peak current I_{SEG}, plus the 0.8V headroom required by the driver output stages. The MAX6955 correctly regulates I_{SEG} with a supply voltage above this minimum voltage. If the supply drops below this minimum voltage, the driver output stages can brown out, and be unable to regulate the current correctly. As the supply voltage drops further, the LED segment drive current becomes effectively limited by the output driver's on-resistance, and the LED drive current drops. The characteristics of each individual LED in a display digit are well matched, so the result is that the display intensity dims uniformly as supply voltage drops out of regulation and beyond.

Computing Power Dissipation

The upper limit for power dissipation (P_D) for the MAX6955 is determined from the following equation:

$$P_D = (V+ \times 35mA) + (V+ - V_{LED}) (DUTY \times I_{SEG} \times N)$$

where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 17)

V_{LED} = LED forward voltage at I_{SEG}

I_{SEG} = segment current set by R_{SET}

P_D = Power dissipation, in mW if currents are in mA

Dissipation example:

$$I_{SEG} = 30mA, N = 17, DUTY = 15/16,$$
$$V_{LED} = 2.4V \text{ at } 30mA, V+ = 3.6V$$
$$P_D = 3.6V (35mA) + (3.6V - 2.4V)(15/16 \times 30mA \times 17) = 0.700W$$

Thus, for a 36-pin SSOP package (T_{JA} = 1/0.0118 = +85°C/W from Operating Ratings), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + (P_D \times T_{JA}) = +150°C$$
$$= T_A + (0.700 \times +85°C/W)$$

So T_A = +90.5°C. Thus, the part can be operated safely at a maximum package temperature of +85°C.

Power Supplies

The MAX6955 operates from a single 2.7V to 5.5V power supply. Bypass the power supply to GND with a 0.1µF capacitor as close to the device as possible. Add a 47µF capacitor if the MAX6955 is not close to the board's input bulk decoupling capacitor.

Table 8. 16-Segment Display Font Map

LSB \ MSB	x000	x001	x010	x011	x100	x101	x110	x111
0000								
0001								
0010								
0011								
0100								
0101								
0110								
0111								
1000								
1001								
1010								
1011								
1100								
1101								
1110								
1111								

Table 9. 14-Segment Display Font Map

LSB \ MSB	x000	x001	x010	x011	x100	x101	x110	x111
0000								
0001								
0010								
0011								
0100								
0101								
0110								
0111								
1000								
1001								
1010								
1011								
1100								
1101								
1110								
1111								

Table 10. Digit Plane Data Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
14-segment or 16-segment mode, writing digit data to use font map data with decimal place unlit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	0	Bits D6 to D0 select font characters 0 to 127						
14-segment or 16-segment mode, writing digit data to use font map data with decimal place lit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	1	Bits D6 to D0 select font characters 0 to 127						
7-segment decode mode, DP unlit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	0	0	0	0	D3 to D0			
7-segment decode mode, DP lit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	1	0	0	0	D3 to D0			
7-segment no-decode mode	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	Direct control of 8 segments							

Table 11. Segment Decoding for 7-Segment Displays

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Segment Line	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	dp	a	b	c	d	e	f	g

Table 12. 7-Segment Segment Mapping Decoder for Hexadecimal Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6, D5, D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0	—	X	0	0	0	0	—	1	1	1	1	1	1	0
1	—	X	0	0	0	1	—	0	1	1	0	0	0	0
2	—	X	0	0	1	0	—	1	1	0	1	1	0	1
3	—	X	0	0	1	1	—	1	1	1	1	0	0	1
4	—	X	0	1	0	0	—	0	1	1	0	0	1	1
5	—	X	0	1	0	1	—	1	0	1	1	0	1	1
6	—	X	0	1	1	0	—	1	0	1	1	1	1	1
7	—	X	0	1	1	1	—	1	1	1	0	0	0	0
8	—	X	1	0	0	0	—	1	1	1	1	1	1	1
9	—	X	1	0	0	1	—	1	1	1	1	0	1	1
A	—	X	1	0	1	0	—	1	1	1	0	1	1	1
B	—	X	1	0	1	1	—	0	0	1	1	1	1	1
C	—	X	1	1	0	0	—	1	0	0	1	1	1	0
D	—	X	1	1	0	1	—	0	1	1	1	1	0	1
E	—	X	1	1	1	0	—	1	0	0	1	1	1	1
F	—	X	1	1	1	1	—	1	0	0	0	1	1	1

**The decimal point is set by bit D7 = 1.*

Table 13. Digit-Type Register

DIGIT-TYPE REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Output Drive Line	0x0C	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Slot Identification		Slot 4		Slot 3		Slot 2		Slot 1	

Table 14. Example Configurations for Display Digit Combinations

DIGIT-TYPE REGISTER SETTING	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Digits 7 to 0 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	0	0	0
Digit 0 is a 14-segment digit, digits 7 to 1 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	0	0	1
Digits 2 to 0 are 14-segment digits, digits 7 to 3 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	1	1	1
Digits 7 to 0 are 14-segment digits.	0x0C	1	1	1	1	1	1	1	1

Table 15. Decode-Mode Register Examples

DECODE MODE	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digit pairs 7 to 0.	0x01	0	0	0	0	0	0	0	0	0x00
Hexadecimal decode for digit pair 0, no decode for digit pairs 7 to 1.	0x01	0	0	0	0	0	0	0	1	0x01
Hexadecimal decode for digit pairs 2 to 0, no decode for digit pairs 7 to 3.	0x01	0	0	0	0	0	1	1	1	0x07
Hexadecimal decode for digit pairs 7 to 0.	0x01	1	1	1	1	1	1	1	1	0xFF

Table 16. Initial Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Decode Mode	Decode mode enabled	0x01	1	1	1	1	1	1	1	1
Global Intensity	1/16 (min on)	0x02	X	X	X	X	0	0	0	0
Scan Limit	Display 8 digits: 0, 1, 2, 3, 4, 5, 6, 7	0x03	X	X	X	X	X	1	1	1
Control Register	Shutdown enabled, blink speed is slow, blink disabled	0x04	0	0	X	X	0	0	0	0
GPIO Data	Outputs are low	0x05	X	X	X	0	0	0	0	0
Port Configuration	No key scanning, P0 to P4 are all inputs	0x06	0	0	0	1	1	1	1	1
Display Test	Normal operation	0x07	X	X	X	X	X	X	X	0
Key_A Mask	None of the keys cause interrupt	0x08	0	0	0	0	0	0	0	0
Key_B Mask	None of the keys cause interrupt	0x09	0	0	0	0	0	0	0	0
Key_C Mask	None of the keys cause interrupt	0x0A	0	0	0	0	0	0	0	0
Key_D Mask	None of the keys cause interrupt	0x0B	0	0	0	0	0	0	0	0
Digit Type	All are 16 segment or 7 segment	0x0C	0	0	0	0	0	0	0	0
Intensity10	1/16 (min on)	0x10	0	0	0	0	0	0	0	0
Intensity32	1/16 (min on)	0x11	0	0	0	0	0	0	0	0
Intensity54	1/16 (min on)	0x12	0	0	0	0	0	0	0	0
Intensity76	1/16 (min on)	0x13	0	0	0	0	0	0	0	0
Intensity10a	1/16 (min on)	0x14	0	0	0	0	0	0	0	0
Intensity32a	1/16 (min on)	0x15	0	0	0	0	0	0	0	0
Intensity54a	1/16 (min on)	0x16	0	0	0	0	0	0	0	0
Intensity76a	1/16 (min on)	0x17	0	0	0	0	0	0	0	0
Digit 0	Blank digit, both planes	0x60	0	0	1	0	0	0	0	0
Digit 1	Blank digit, both planes	0x61	0	0	1	0	0	0	0	0
Digit 2	Blank digit, both planes	0x62	0	0	1	0	0	0	0	0
Digit 3	Blank digit, both planes	0x63	0	0	1	0	0	0	0	0
Digit 4	Blank digit, both planes	0x64	0	0	1	0	0	0	0	0
Digit 5	Blank digit, both planes	0x65	0	0	1	0	0	0	0	0
Digit 6	Blank digit, both planes	0x66	0	0	1	0	0	0	0	0
Digit 7	Blank digit, both planes	0x67	0	0	1	0	0	0	0	0
Digit 0a	Blank digit, both planes	0x68	0	0	0	0	0	0	0	0
Digit 1a	Blank digit, both planes	0x69	0	0	0	0	0	0	0	0
Digit 2a	Blank digit, both planes	0x6A	0	0	0	0	0	0	0	0
Digit 3a	Blank digit, both planes	0x6B	0	0	0	0	0	0	0	0
Digit 4a	Blank digit, both planes	0x6C	0	0	0	0	0	0	0	0
Digit 5a	Blank digit, both planes	0x6D	0	0	0	0	0	0	0	0
Digit 6a	Blank digit, both planes	0x6E	0	0	0	0	0	0	0	0
Digit 7a	Blank digit, both planes	0x6F	0	0	0	0	0	0	0	0
Key_A Debounced	No key presses have been detected	0x08	0	0	0	0	0	0	0	0
Key_B Debounced	No key presses have been detected	0x09	0	0	0	0	0	0	0	0
Key_C Debounced	No key presses have been detected	0x0A	0	0	0	0	0	0	0	0
Key_D Debounced	No key presses have been detected	0x0B	0	0	0	0	0	0	0	0
Key_A Pressed	Keys are not pressed	0x0C	0	0	0	0	0	0	0	0
Key_B Pressed	Keys are not pressed	0x0D	0	0	0	0	0	0	0	0
Key_C Pressed	Keys are not pressed	0x0E	0	0	0	0	0	0	0	0
Key_D Pressed	Keys are not pressed	0x0F	0	0	0	0	0	0	0	0