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General Description

The MAX7037 is an ultra-low-power, high-performance quad-band multichannel transceiver with integrated 8051 microcontroller, flash memory, and sensor interface. The MAX7037 runs from a minimum supply voltage of only 2.1V, extending battery life and enabling it to cope with different sources of energy, like solar cells, electromechanical or thermoelectrical energy. Hardware-implemented transmit-and-receive routines, in combination with a microcontroller, enable a high-efficiency transceiver system for wireless fail-safe multiband/multichannel communication with advanced FSK and ASK protocol features. Sleep modes allow easy implementation of low-power applications with fast reaction times.

Applications

- Ultra-Low-Power Sensor Networks
- Smart Metering
- Building Automation
- Short-Range Communication

Ordering Information **appears at end of data sheet.**

Benefits and Features

- Ultra-Low-Power Consumption for Battery-Based Operation
  - Current Consumption TX (P_{OUT} = +6dBm, FSK): 16mA
  - Current Consumption RX (FSK): 22mA
  - Current Consumption Deep Sleep Mode (Watchdog Timer and PRAM Active): 100nA
  - Supply Voltage Range: 2.1V to 5.5V
  - Integrated Ultra-Low-Power On/Off Voltage Threshold Detectors
- Worldwide Usable Frequency Band Coverage
  - ISM Band Frequency Coverage: 315/433/868/915~930MHz
- Fractional-N LO Generation For Multichannel Operation
  - RF Synthesizer Resolution: 244Hz/488Hz
- FFSK/FMSK/ASK Modulation for Optimum Compatibility with Various Communication Standards
  - Gross Data Rates: Up To 125Kbit/s
  - ASK with Programmable Transition Shape for Spectral Tuning
- Fully Integrated RF, TX, and RX Front-End for Minimum External Components
  - Maximum TX Output Power (R_{LOAD} = 400Ω): +10dBm
  - RX Sensitivity (FFSK, BW = 150kHz): -100dBm
- Mixed-Signal Sensor Interface with Analog I/O Through ADC/DAC and On-Chip Buffers (Contact Factory for Future Support)
  - Integrated 9-Bit Sigma Delta ADC for Applications
  - Integrated 8-Bit DAC
  - 8 Mixed-Signal I/Os with Versatile Switching Matrix; Up to 18 Digital I/Os
- Wristwatch Crystal-Based Real-Time Clock (Contact Factory for Future Support)
  - Wristwatch Crystal Oscillator Integrated: 32768Hz

maxim integrated™

Absolute Maximum Ratings

Continuous Current In/Out of Pins ....±100mA
Duration of Pin Short Circuit to Ground or Supply ....Continuous
Duration of Short-Circuit Between Pins....................Continuous
Continuous Power Dissipation (T_A = +70°C)
    Package 1 Multilayer Board
    (derate 37mW/°C above +70°C) 2600mW
Junction Temperature..+150°C
Operating Temperature Range........................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Supply Voltage at High-Voltage Supply Pins
    V_{DD} and V_{DDLIM} ....-0.5V to +6.0V
Supply Voltage for Mixed-Signal Sensor Interface
    (GPIO1) and Extended Serial Interface 0 Pins
    (GPIO0) ....-0.5V to +6.0V
Voltage at GPIO1 Port Pins (ADIO0~7) and GPIO2 Port Pins
    (WXIDIO, WXODIO) in Analog Mode.................-0.5V to 2.0V

Voltage at Digital Input Pins
    WAKE0, WAKE1, RESET GND.........................-0.5V to 3.6V
Voltage at GPIO2 Port Pins
    (WXIDIO, WXODIO) in digital mode...................-0.5V to 2.0V
Voltage at GPIO0 Port Pins
    (BIST_DONE, TEST1, TEST3, SCSEDIO0,
    SCLKDIO1, WSDADIO2, RSDADIO3, BIST_PASS) and
    GPIO1 Port Pins (ADIO0~7) in Digital Mode .....-0.5V to 6.0V
Maximum Permanent Elimination Current at the Parallel
    Regulator (Generally Limited by Max (V_{DD}) and PTOT)
    ....50mA
Input Current Into Any Pin Except Supply Pins
    .... -50mA to +50mA
Electrostatic Discharge Sensible Pins, as are:
    RFP, RFN, XTIN, XTOT, V_{DD}, V_{DDLIM}, UVDD, WAKE0,
    WAKE1, RESET 2kV
Electrostatic Discharge Normal Pins.....................................2kV
Power Dissipation..300 mW

Note 1: ESD Test according to AEC-Q100-002 (JESD22-A114): HBM: R = 1.5kΩ, C = 100pF. ESD protected to 2kV Human Body Model.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

40-Pin QFN (6mm x 6mm)
    Junction-to-Ambient Thermal Resistance (θ_{JA}) ....27°C/W
    Junction-to-Case Thermal Resistance (θ_{JC})............16.5°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Voltage	V_{DD}	At input pins V_{DD} and V_{DDLIM}	Min (V_{OFF})	3.3	5.5	V
Tolerated Supply Voltage Slope for Ambient Supply	V_{DDSLP}	Valid for rising and falling slope.	0	3	5	V/ms
Positive Supply Voltage at Shutdown	V_{DDS}	At input pins V_{DD} and V_{DDLIM}. No normal performance required.	Min (V_{OFF}) – 0.025			V
Supply Voltage for Mixed-Signal Sensor Interface and Extended Serial Interface 0 Pins	V_{IOVDD}	GPIO0/1	1.7	DVDD	5.5	V
Ground	GND			0		V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Operating Conditions (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Levels on Digital I/O Pins of GPIO0/1 Ports	V_L	All pins which are or can be configured as digital I/O.	Min (VIOVDD)		Max (VIOVDD)	
Tolerated Ripple on V_{DD}	V_{DDR}	100Hz ripple from full wave rectifier on V_{DD} whereas Min(V_{DD}) > V_{ON}			50	mV_{P-P}
ADC Measurement Input Common Mode Range		The sigma-delta ADCs have a differential input. The ADC input CMR is provided by the R2R buffer.	0		RVDD	V
ADC Measurement Input Amplitude for Single-Ended or Differential Measurements	VIN_MEAS	Measurement possible only via R2R input buffer. Possible selectable internal references: GND, RVDD, VADCCMR (~0.8V), VBG	0		±RVDD	Vd
Analog Input Range (GPIO1 Port, ADIO0~7)		Single-ended	0		VRVDD	V
Nominal Differential Load Resistance	R_{LOAD} (Note 3)	Resonance resistance R_{LOAD} at fCTX of the load resonance circuit with the impedance Z_{LOAD}. Smaller R_{LOAD} values will lead to increased current consumption for equal POUT		400	900	Ω
RF Port DC Supply Voltage		RF_N, RF_P pins	Min (RVDD)	RVDD	Max (RVDD)	V
Differential Voltage Swing Between RF Pins	V_{TX}	Absolute Maximum Rating. Must be respected even if different load impedances are used			6.0	V_{P-P}
Required Relative 16M XTAL Frequency Tolerance for WB/ DWB Operation	d_{fXO}	~315MHz band: ~433MHz band: ~868MHz band: ~915MHz band:			55 40 20 19	ppm ppm ppm ppm
TX-RX Carrier Frequency Deviation	d_{fTRD}	Application design requirement. Given by SAW based ASK transmitters			100	kHz
Ambient Operating Temperature	T_A		-40°C		+85°C	°C

Note 3: Maximum differential R_{LOAD} for +6dBm output power (based on P = V^2/R formula and considering $RVDD_{MIN}$ and V_{DSAT} of output stage MOS).

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Current Consumption

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption in RESET *(Off Mode)*	I_{DD_RESET}	Current into V_{DD} pin. RESET active.		15		nA
Current Consumption *Deep Sleep Mode*	I_{DD_DS}	On/Off threshold detectors, UVDD regulator and watchdog timer running.		100		nA
Current Consumption *Flywheel Sleep Mode*	I_{DD_FS}	On/Off threshold detectors, UVDD regulator, watchdog timer, wristwatch crystal and flywheel timer running.		700		nA
Current Consumption *Short-Term Sleep Mode*	I_{DD_SS}	On/Off threshold detectors, UVDD regulator, watchdog timer, short-term RCO and timer running.		3.4		μA
Current Consumption *CPUSTOP* Mode	$I_{DD\_CPUSTOP}$			1		mA
Current Consumption *CPUIDLE* Mode	$I_{DD\_CPUIDLE}$			1.3		mA
Current Consumption *CPU Mode – CRCO*	I_{DD_CRCO}	R/S/DVDD regulators, CPU RCO, and CPU 8051 at ~16MHz.		3.3		mA
Current Consumption *CPU Mode – XTAL*	I_{DD_XTAL}	R/S/DVDD regulators, XTAL 16M, and CPU 8051 at 16MHz.		3.9		mA
FLASH Program/Page Erase/Mass Erase Current		This current is additional to normal CPU Mode operating current.		< 7		mA
Current Consumption *TX Mode* ASK	I_{TX9A10_MO}	At ~868MHz and +10dBm available TX power during transmitting a PRBS sequence. CPU 8051 stopped.		23		mA
Current Consumption *TX Mode* ASK	I_{TX9A6_MO}	At ~868MHz and +6dBm available TX power during transmitting a PRBS sequence. CPU 8051 stopped.		16		mA
Current Consumption *RX Mode*	$I_{RX9\_ASK/FSK}$	At ~868MHz: ASK or FSK, at maximum sensitivity. CPU 8051 stopped.		22		mA
Current Consumption *TX Mode* ASK	I_{TX3A10_MO}	At ~315MHz and +10dBm available TX power during transmitting a PRBS sequence. CPU 8051 stopped.		26		mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Current Consumption (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption *TX Mode* ASK	I_{TX3A6_MO}	At ~315MHz and +6dBm available TX power during transmitting a PRBS sequence. CPU 8051 stopped.		20		mA
Current Consumption *RX Mode*	$I_{RX3\_ASK/FSK}$	At ~315MHz: ASK or FSK, at maximum sensitivity. CPU 8051 stopped.		22		mA

Ambient Power Management and Voltage Regulators

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC BANDGAP						
Sigma-Delta ADC/Mixed-Signal I/O Bandgap Reference	V_{BGADC}		1.10	1.21	1.30	V
Bandgap Voltage Tolerance Magnitude	d_{VBG}	Overtemperature and process variations		< 4		%
Bandgap Voltage Tolerance Magnitude Over Temperature	d_{VBGT}	Overtemperature per device, related to room temperature		< ±2		%
VOLTAGE LIMITER (SHUNT REGULATOR)						
Limitation Voltage of Shunt Regulator	V_{LIM_50mA}	At 50mA current sink	3.9	4.8	5.5	V_{DC}
Current Consumption Voltage Limiter Only	I_{LIM_3V5}	Current into V_{DDLIM} pin. V_{DD} = 3.5 V.		15		nA
Maximum Permanent Elimination Current of Limiter	I_{LIM}			50		mA
ON/OFF THRESHOLD DETECTION						
Turn-On Threshold Voltage	V_{ON}		2.3	2.45	2.6	V_{DC}
Shutdown Threshold Voltage	V_{OFF}	Automatic shutdown when not in sleep mode if V_{DD} drops below this level	1.82	1.92	2.10	V_{DC}

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Frequency Generation

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
XTAL OSCILLATOR						
XTAL Oscillator frequency	f_{XO}			16.000		MHz
TX – RX Frequency Difference at Wideband Operation	d_{fTR_WB}	Within all frequency bands assuming equal XO tolerances in TX and RX		35		kHz
Crystal Oscillator Startup Time	t_{XOON}	Crystal ESR maximum 300Ω		0.7	1.2	ms
WRISTWATCH XTAL OSCILLATOR						
Wristwatch XTAL Oscillator Frequency	f_{WXO}	2 (Note 15)		32.768		kHz
Wristwatch Crystal Oscillator Tolerance	df_{WXO}	Depends on application and used crystal tolerance. Oscillator circuit will add ~30% typ to crystal tolerance. Typical crystal tolerance assumed here: 30ppm		40		ppm
Wristwatch Crystal Oscillator Startup Time	t_{WXOON}	Crystal ESR maximum 50kΩ		1		s
RF SYNTHESIZER						
RF Synthesizer Type				Fractional N with three configurable ranges (B3, B4, B9).		–
RF Synthesizer Reference Frequency	f_{REF_RF}		–	f_{XO}	–	MHz
Low-Frequency Band Coverage	f_{RF_B3}		312		320	MHz
Mid-Frequency Band Coverage	f_{RF_B4}		431		465	MHz
High-Frequency Band Coverage	f_{RF_B9}		862		930	MHz
Low-Frequency Step Size	d_{fLO}	B3/B4 band: B9 band:		~244 ~488		Hz
RF Synthesizer Switching Speed	$t_{SYNTH\_SW3/4/9}$	Settling to a frequency error of ±10kHz from steady-state value		<50		µs
RF Synthesizer Turn-On Time	$t_{SYNTH\_ON3/4/9}$	At turning on at available reference frequency settling to a frequency error of ±10kHz from steady-state value			75	µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Frequency Generation (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL CLOCK SYNTHESIZER						
Digital Clock Synthesizer Type				Integer N		–
Digital Clock Synthesizer Reference Frequency	f_{REFDC}		–	f_{XO}	–	MHz
Primary Digital Clock Frequency	f_{S0}	Synthesized by digital clock synthesizer		32.000		MHz
Digital Clock Synthesizer Turn-On Speed	tf_{S0_ON}	At turning on at available reference frequency to a frequency error of ±1kHz from steady-state value		< 75		µs
CPU RCO (CRCO)						
Nominal CRCO Frequency		Free-running frequency	11.7	16	20.0	MHz
CRCO Startup Time		From start of RCO to usable clock		4		Cycles

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Transmit Operation

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ASK TRANSMISSION						
Nominal ASK Transmit Data Rate	RTXA (Note 4)		31.25		125	kBit/s
ASK TX Data Rate Tolerance	d_{RTXA}			< d_{fXO}		ppm
ASK Transmit Filter Order			–	4	–	–
ASK Transmit Filter Type				Bessel		–
ASK Transmit Filter Bandwidth	BTXA	-3dB bandwidth		1.5/2 RTXA		kHz
Transmit DAC Resolution				6		Bit
Over Sampling of ASK TX Waveform				16		–
ASK Anti-Aliasing Filter Bandwidth	BAAA	-3dB bandwidth		1.5 RTXA		kHz
FSK TRANSMISSION						
ASK Carrier Leakage		Transmitting a long "L" sequence at POUT = 10dBm. Related to power high.		< -40		dB
Nominal FSK Transmit Data Rate	RTXF (Note 4)	Digital NCO based (derived from 16MHz XTAL)	31.25		125	kBit/s
FSK TX Data Rate Tolerance	d_{RTXF}			<d_{fXO}		ppm
FSK Transmit Filter Order			–	2	–	–
FSK Transmit Filter Type				Bessel		–
FSK Transmit Filter Bandwidth	BTXF	-3dB bandwidth		1.5/2 RTXF		kHz
Magnitude of FSK Frequency Deviation	d_{fTXF} (Note 4)	Digital NCO based (derived from 16MHz XTAL)	4	RTXF/4 (for MSK)	60	kHz
ASK AND FSK TRANSMISSION						
TX power steps	NPTX			7		–
Maximum Available TX Output Power, Into Resonant Circuit with R_{LOAD} (Differential)	PTX (Note 1)	For ASK: TX power during physical 'H'		-2 to +10		dBm
TX Output Power Variation Over Temperature	PTX_T (Note 1)	T_A = -40°C to +85°C		< ±1.5		dB

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Transmit Operation (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious Emission Power Transmitting At ~315Mhz At P_{OUT+10} Into Resonant Circuit With R_{LOAD} (Differential)	POUT_SP3 (Notes 2, 3)	≈2 x 315MHz: ≈3 x 315MHz: ≥≈4 x 315MHz: (harmonics of US band)		< -29 < -29 < -21		dBm dBm dBm
Spurious Emission Power Transmitting At ~433Mhz At P_{OUT+10} Into Resonant Circuit With R_{LOAD} (Differential)	POUT_SP4 (Notes 2, 3)	≈2 x 433MHz: ≥≈3 x 433MHz: (harmonics of EU band)		< -16 < -10		dBm dBm
Spurious Emission Power Transmitting At ~868Mhz At P_{OUT+10} Into Resonant Circuit With R_{LOAD} (Differential)	POUT_SP8 (Notes 2, 3)	≈2 x 868MHz: ≥≈3 x 868MHz: (harmonics of EU band)		< -10 < -10		dBm dBm
Spurious Emission Power Transmitting At ~915Mhz At P_{OUT+10} Into Resonant Circuit With R_{LOAD} (Differential)	POUT_SP9 (Notes 2, 3)	≈2 x 915MHz: ≥ ≈3 x 915MHz: (harmonics of US band)		< -16 < -10		dBm dBm

Note 1: Available TX power from the MAX7037 in reactive load with R_{LOAD} while transmitting at the transmit frequency f_{TX}. The TX power is measured by a matching network and a measurement balun single-ended on 50Ω level. The measurement result is backwards projected to the MAX7037 port by the known transfer function of the measurement balun and the matching network. Additionally, the radiated TX power is dependent on the (optional) RF-filter, antenna selectivity, and loss. Therefore, it will NOT be production tested.

Note 2: Spurious power generated by the MAX7037 in reactive load with R_{LOAD} while transmitting at the transmit frequency f_{TX}. Spurious emission values are measured by a matching network and a measurement balun single-ended on 50Ω level with a RBW of 100kHz being a replacement for the matching network and the differential antenna. The measurement result is backwards projected to the MAX7037 port by the known transfer function of the measurement balun and the matching net-work. Additionally, the radiated spurious emissions are dependent on the (optional) RF-filter, antenna-selectivity, and loss. Therefore, it will NOT production tested. Spurious emission suppression at carrier harmonics is also a part of filter and antenna design.

Note 3: Antenna and matching network loss and attenuation by antenna selectivity for spurious assumed to be at least 20dB. The (optional) RF filter is not taken into account.

Note 4: Digital implementation parameter, not parametrically tested (covered by ATPG testing).

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Receive Operation

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Input Impedance (Differential)	RIN (Note 5)	For all frequency bands B3/B4/B9. LNACONF = "001001"		288~526 Typ: 400		Ω
Receiver Source Impedance (Differential)	RSOURCE	(Antenna impedance)		400		Ω
Receiving Protocol				SSB reception LSB or USB selectable		-
Receiving Mode				SSB reception LSB or USB selectable		-
Received Modulation Method				ASK or FSK		–
LNA Gain	GLNA	Switchable in NLNA steps		0/20		dB$_{V/V}$
LNA Gain Steps	NLNA			2		–
VGA Gain	G_IVGA G_QVGA	Switchable in NVGA steps		0/3/6/9/12/15/18/21		dB$_{V/V}$
VGA Gain Steps	NVGA			8		–
1dB Input Compression Point (In-Band)	ICP1	At highest sensitivity (LNA and VGA maximum gain)		-43		dBm
Dynamic Range Of Sigma-Delta ADC	DYNADC	Sinusoidal signal at 125kHz in 200kHz output bandwidth		78		dB
Data Oversampling Factor	OV	Different logical treatment in compatible asynchronous SOF	–	8	–	–
ASK/FSK RX Data Rate	RRX (Note 7)	ASK or FSK tested at maximum data rate. ASK: FSK:	min RTXA min RTXF	RTXA RTXF	max RTXA max RTXF	kBit/s
Acceptable Advanced TX-RX Data Rate Deviation	d$_{RTRXA}$	Tolerance of nominal FSK data rate between TX and RX.		< 2 df$_{XO}$		ppm
IF Magnitude Word Width				16		Bits
RSS Word Width				16		Bits
LTRSS Word Width				16		Bits
DOUBLE WIDEBAND OPERATION						
Nominal Intermediate Frequency Wideband Operation	f$_{IFD}$			250		kHz
Effective Receiver Bandwidth	BRXD	-3dB, defined by integrated digital IF filter	-	300	-	kHz
Magnitude Of FSK Frequency Deviation	df$_{RXD}$ (Note 5)		15	dfTX	60	kHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Receive Operation (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal ASK Receiver Sensitivity At MAX7037 Input	S0RX3_D_A S0RX4_D_A S0RX9_D_A (Notes 1, 3)	At max RTXA, high LNA gain and max IF gain for SRQ (Note 2) at -10°C < T_A < +70°C		-95		dBm
Normal FSK Receiver Sensitivity At MAX7037 Input	S0RX3_D_F S0RX4_D_F S0RX9_D_F (Notes 1, 3)	At MSK with max RTXF, high LNA gain and max IF gain for SRQ (Note 2) at -10°C < T_A < +70°C		-95		dBm
Temperature Sensitivity Reduction	d_{S0D_T}	-40°C < T_A <-10°C or +70°C < T_A <+85°C.		<3		dB
Receiver Sensitivity Reduction Caused By TX-RX Frequency Offset	d_{S0D_F}	For SRQ (Note 2) at maximum df_{TRW}		<4		dB
Receiver Sensitivity Reduction Caused By Data Rate Deviation	d_{S0D_R}	For SRQ (Note 2) at maximum d_{RTRXC}		<3		dB
Reduced FSK Receiver Sensitivity	S1RX3/4/9_D_F (Notes 1, 3)	At low LNA gain, for SRQ (Note 2) at -10°C < T_A < +70°C		-84		dBm
Maximum ASK Target Signal Input Level	PMAX_D_A (Note 1)	At max RTXA, high LNA gain and max IF gain for SRQ (Note 2) at -10°C < T_A < +70°C		-20		dBm
Target Blocking Mask	(Note 4)	Covered by digital tests		Figure 3		dBc
Equivalent IF Magnitude Bandwidth	BIFMAG_D			150		kHz
RSS Bandwidth	BRSS_D			10		kHz
RSS Settling Time	t_{RSS0_D} (Note 7)	Dominated by BRSS_D kHz RSS measurement bandwidth		150	250	µs
LTRSS Bandwidth	BLTRSS_D			1		kHz
LTRSS Settling Time	t_{RSS1_D} (Note 7)	Given by BLTRSS_D kHz measurement bandwidth		1.5	2.0	ms
Gain Control Switching Time	t_{GCD} (Note 7)	One cycle from highest gain to lower gain		typ (t_{RSS0_D})	max (t_{RSS0_D})	µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Receive Operation (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WIDEBAND OPERATION						
Nominal Intermediate Frequency Wideband Operation	f_{IFW}			125		kHz
Effective Receiver Bandwidth	BRXW	-3dB, defined by integrated digital IF filter	–	150	–	kHz
Magnitude Of FSK Frequency Deviation	df_{RXW} (Note 7)		15	dfTX	60	kHz
Normal ASK Receiver Sensitivity At MAX7037 Input	S0RX3_W_A S0RX4_W_A S0RX9_W_A (Notes 1, 3)	At max RTXA, high LNA gain and max IF gain for SRQ (Note 2) at 10°C < T_A < +70 C		-100		dBm
Normal FSK Receiver Sensitivity At MAX7037 Input	S0RX3_W_F S0RX4_W_F S0RX9_W_F (Notes 1, 3)	At MSK with max RTX_F, high LNA gain and max IF gain for SRQ (Note 2) at 10°C < T_A < +70°C		-100		dBm
Temperature Sensitivity Reduction	d_{S0W_T}	-40°C < T_A < -10°C or +70°C < T_A < +85°C		<3		dB
Receiver Sensitivity Reduction Caused By TX-RX Frequency Offset	d_{S0W_F}	For SRQ (Note 2) at maximum df_{TRW}		<4		dB
Receiver Sensitivity Reduction Caused By Data Rate Deviation	d_{S0W_R}	For SRQ (Note 2) at maximum d_{RTRXC}		<3		dB
Reduced FSK Receiver Sensitivity.	S1RX3/4/9_W_F (Notes 1, 3)	At low LNA gain, for SRQ (Note 2) at -10°C < T_A < +70°C		-88		dBm
Maximum ASK Target Signal Input Level	PMAX_W_A (Notes 1, 3)	At max RTX_A, high LNA gain, and max IF gain for SRQ (Note 2) at -10°C < T_A < +70°C		-20		dBm
Target Blocking Mask	(Note 4)	Covered by digital tests		Figure 4		dBc
Equivalent IF Magnitude Bandwidth	BIFMAG_W			75		kHz
RSS Bandwidth	BRSS_W			5		kHz
RSS Settling Time	t_{RSS0_W} (Note 7)	Dominated by BRSS_W kHz RSS measurement bandwidth		300	500	µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Receive Operation (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LTRSS Bandwidth	BLTRSS_W (Note 7)			500		Hz
LTRSS Settling Time	t_{RSS1_W} (Note 7)	Given by BLTRSS_W kHz measurement bandwidth		3	4	ms
Gain Control Switching Time	t_{GCW} (Note 7)	One cycle from highest gain to lower gain		Typ (t_{RSS0_W})	Max (t_{RSS0_W})	µs
GENERAL						
Image Rejection Untrimmed	XRX3_IRJ XRX4_IRJ XRX9_IRJ	Untrimmed, at maximum RX sensitivity setting. Image signal in-band at LSB RX +2 f_{IF} above band center. Image signal in-band at USB RX -2 f_{IF} below band center		24		dB
Image Rejection Trimmed		Trimmed, at maximum RX sensitivity setting. Image signal in-band at LSB RX +2 f_{IF} above band center. Image signal in-band at USB RX -2 f_{IF} below band center See receive section for image rejection tuning and Figure 4.		34		dB
Available RX Low Power Leakage at $f_{LORX,X}$	PLOLeak (Note 6)	Low power in a differentially matching source resistor as load with LNA in high or low gain mode		< -50		dBm

Note 5: The RX sensitivity is measured close to the application by a single-ended on 50Ω source through a balun and a matching network. The measurement result is forward projected to the MAX7037 port by the known transfer function of the balun and the matching network.

Note 6: Standard Receive Quality (SRQ) is a bit error probability (without error correcting coding) of 10^{-3}.

Note 7: The radiated sensitivity of the whole RX is dependent of the (optional) RF filter- and antenna- selectivity and loss is therefore NOT production tested.

Note 8: SRQ fulfilled with: Useful signal applied 3dB above the measured sensitivity limit, however not below maximum of $S0_X$ + 3dB. Blocking signal un-modulated CW. This measurement method is slightly more restrictive than the EN300 220-1V 1.3.1 (2000) section 9.3.2 for class 2 receivers due to they are related to the nominal received carrier position instead of the band edges. Blocking is not production tested.

Note 9: Values from simulation. Actual obtained RIN is also dependent on the LNACONF configuration setting.

Note 10: Carrier generated by the MAX7037 in reactive load with R_{LOAD} while receiving at the frequency fTRX. The leakage power is measured by a matching network and a measurement balun single-ended on 50Ω level being a replacement for the matching network and the differential antenna. The measurement result is backwards projected to the MAX7037 port by the known transfer function of the measurement balun and the matching network. The radiated leakage is furthermore dependent on the (optional) RF-filter- and antenna- loss and, therefore, NOT production tested. Spurious emission suppression at carrier harmonics is also a part of filter and antenna design.

Note 11: Digital implementation parameter, not parametrically tested (covered by ATPG testing).

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

TX and RX Timing Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STARTING AND RE-STARTING TX AND RX						
TX Starting Time	t_{0CT} (Notes 1, 2)	Time for starting transmitting a packet from turned off synthesizer. Dominated by synthesizer startup.		$<t_{SYNTH\_ON}$		µs
TX Restarting Time	t_{CT} (Notes 1, 2)	Time for starting transmitting a packet at running synthesizer. Dominated by synthesizer switching.		$<t_{SYNTH\_SW}$		µs
TX Continuing Time	t_T (Notes 1, 2)	Time for starting transmitting a packet at synthesizer running on correct channel.		$<t_{SYNTH\_SW}$		µs
RX Starting Time	t_{0CR} (Notes 1, 2)	Time for starting receiving from turned off synthesizer. Dominated by synthesizer startup. LTRSS is forced		$<t_{SYNTH\_ON}$ $+t_{RSS1x}$		µs
RX Restarting Time	t_{CR} (Notes 1, 2)	Time for starting receiving running synthesizer. Dominated by synthesizer switching. LTRSS is forced		$<t_{SYNTH\_SW}$ $+t_{RSS1x}$		µs
RX Continuing Time	t_R (Notes 1, 2)	Time for starting receiving at synthesizer running on correct channel		$t_{RSS0x}\sim$ t_{RSS1x}		µs
SINGLE CHANNEL (BAND) OPERATION						
TX->TX Switching Time Same RF Channel (Band)	t_{TT} (Notes 1, 2)	Time between transmitting two packets. Estimation, given by CPU 8051.		10		µs
TX->RX Switching Time Same RF Channel (Band)	t_{TR0} (Notes 1, 2)	At constant LTRSS, until packet start possible (for receiving at SRQ)		$<t_{RSS0x}$		µs
TX->RX Switching Time Same RF Channel (Band)	t_{TR1} (Notes 1, 2)	At totally different RSS where the LTRSS has to be adapted until packet start possible (for receiving at SRQ).		$<t_{RSS1x}$		µs
RX->TX Switching Time Same RF Channel (Band)	t_{RT} (Notes 1, 2)	Time between end receiving and start transmitting a packet. Estimation, given by CPU 8051.		10		µs
RX->RX Switching Time Same RF Channel (Band)	t_{RR0} (Notes 1, 2)	At constant LTRSS, until packet start possible (for receiving at SRQ).		$<t_{RSS0x}$		µs
RX->RX Switching Time Same RF Channel (Band)	t_{RR1} (Notes 1, 2)	At totally different RSS where the LTRSS has to be adapted until packet start possible (for receiving at SRQ).		$<t_{RSS1x}$		µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = 85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

TX and RX Timing Parameters (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTI CHANNEL (BAND) OPERATION						
TX->TX Channel (Band) Switching Time	t_{TCT} (Notes 1, 2)	Time between transmitting two packets. Dominated by synthesizer switching.		$< t_{SYNTH\_SW}$		µs
TX->RX Switching Time Other RF Channel (Band)	t_{TCR0} (Notes 1, 2)	At constant LTRSS, until packet start possible (for receiving at SRQ).		$< t_{SYNTH\_SW} + t_{RSS0x}$		µs
TX->RX Switching Time Other RF Channel (Band)	t_{TCR1} (Notes 1, 2)	At totally different RSS where the LTRSS has to be adapted until packet start possible (for receiving at SRQ).		$< t_{SYNTH\_SW} + t_{RSS1x}$		µs
RX->TX Switching Time Other RF Channel (Band)	t_{RCT} (Notes 1, 2)	Time between end receiving and start transmitting a packet. Dominated by synthesizer switching.		$< t_{SYNTH\_SW}$		µs
RX->RX Switching Time Other RF Channel (Band)	t_{RCR0} (Notes 1, 2)	At constant LTRSS, until packet start possible (for receiving at SRQ).		$< t_{SYNTH\_SW} + t_{RSS0x}$		µs
RX->RX Switching Time Other RF Channel (Band)	t_{RCR1} (Notes 1, 2)	At totally different RSS where the LTRSS has to be adapted until packet start possible (for receiving at SRQ).		$< t_{SYNTH\_SW} + t_{RSS1x}$		µs

Note 1: SRQ fulfilled with: Useful signal applied 3dB above the measured sensitivity limit, however not below maximum of $S0_X$ + 3dB.

Note 2: Timings are a composite of tested subtimings therefore laboratory evaluation only, not directly production tested.

Pin Configuration

TOP VIEW

MAX7037

QFN40
(6mm x 6mm)
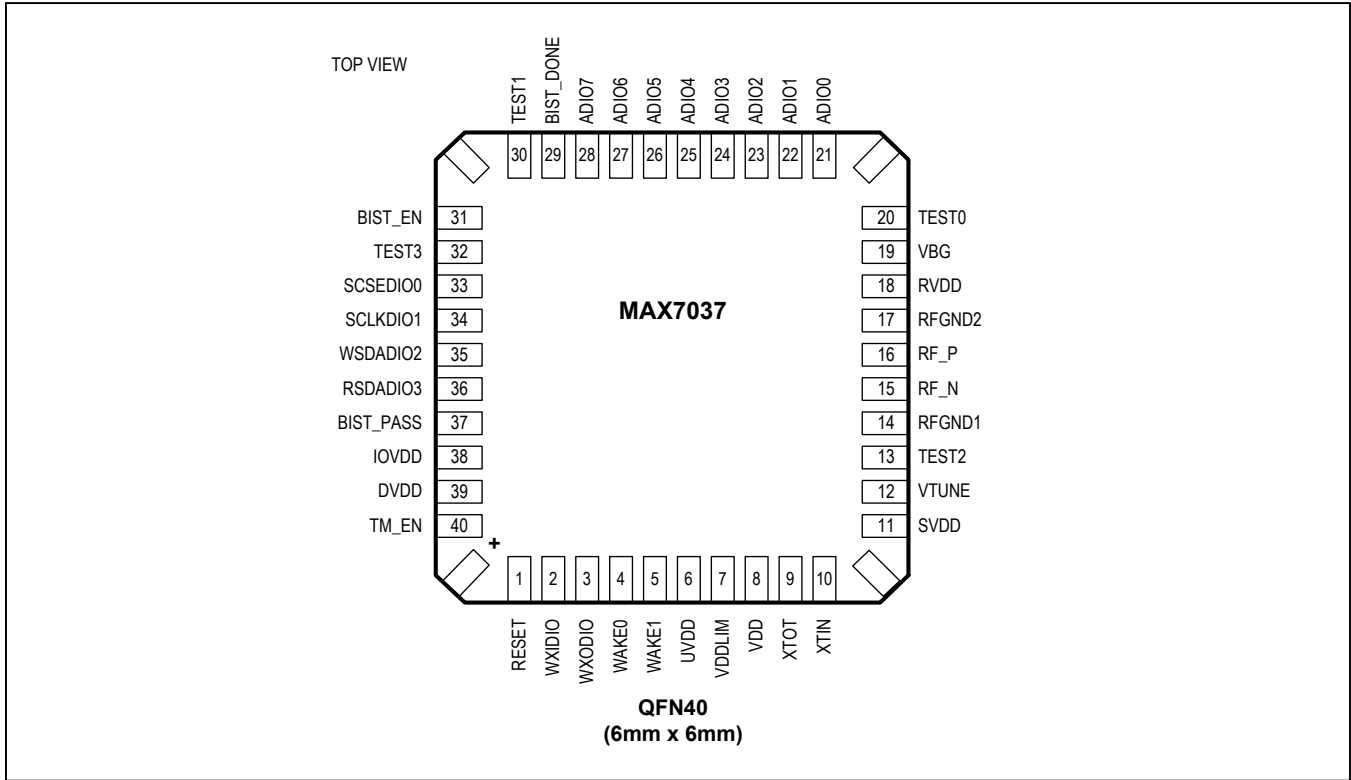
Pin Description

PIN	PIN NAME	DIRECTION	PAD TYPE	DESCRIPTION	SUPPLY/ IO VOLTAGE DOMAIN
1	RESET	DI	PD	External Reset Input. High active.	1.8
2	WXIDIO	ADIO	SPUPD	GPIO2 Group: Analog/Slow Digital I/O – 32kHz Oscillator XTAL Input	1.8
3	WXODIO	ADIO	SPUPD	GPIO2 Group: Analog/Slow Digital I/O – 32kHz Oscillator XTAL Output.	1.8
4	WAKE0	DI	S	Wake 0 Input.	1.8
5	WAKE1	DI	S	Wake 1 Input.	1.8
6	UVDD	AP		UVDD Regulator Output.	1.8
7	VDDLIM	A_HV		V_{DD} Limiter.	5
8	V_{DD}	A_HV		Main V_{DD} – Input for DVDD/SVDD/RVDD/UVDD regulators	5
9	XTOT	AO		16MHz XTAL Output	1.8
10	XTIN	AI		16MHz XTAL Input	1.8

Pin Description (continued)

PIN	PIN NAME	DIRECTION	PAD TYPE	DESCRIPTION	SUPPLY/ IO VOLTAGE DOMAIN
11	SVDD	AP		SVDD Regulator Output.	1.8
12	VTUNE	AIO		RF PLL Vtune Debug I/O.	1.8
13	TEST2	DI	PD	Test2	1.8
14	RFGND1	AG		RF GND	1.8
15	RF_N	AIO		RF I/O (n)	1.8
16	RF_P	AIO		RF I/O (p)	1.8
17	RFGND2	AG		RF GND	1.8
18	RVDD	AP		RVDD Regulator Output.	1.8
19	VBG	AIO		SD-ADC Bandgap Reference Buffered Output. Decoupling capacitor needed.	1.8
20	TEST0	DI	PD	Test0	3.3
21	ADIO0	ADIO	SPUPD	GPIO1 Group: Analog/Digital I/O.	3.3
22	ADIO1	ADIO	SPUPD	GPIO1 Group: Analog/Digital I/O.	3.3
23	ADIO2	ADIO	SPUPD	GPIO1 Group: Analog/Digital I/O.	3.3
24	ADIO3	ADIO	SPUPD	GPIO1 Group: Analog/Digital I/O.	3.3
25	ADIO4	ADIO	PUPD	GPIO1 Group: Analog/Digital I/O.	3.3
26	ADIO5	ADIO	PUPD	GPIO1 Group: Analog/Digital I/O.	3.3
27	ADIO6	ADIO	PUPD	GPIO1 Group: Analog/Digital I/O.	3.3
28	ADIO7	ADIO	PUPD	GPIO1 Group: Analog/Digital I/O.	3.3
29	BIST_DONE	ADIO	PD	GPIO0 Group: DIO5. BIST done output (BIST_EN = 1). Analog functionality only in test mode.	3.3
30	TEST1	DIO	PD	GPIO0 Group: DIO6. Test1 in test mode.	3.3
31	BIST_EN	DI	PD	BIST Enable.	3.3
32	TEST3	DIO	PD	GPIO0 Group: DIO7. Test3 in test mode.	3.3
33	SCSEDIO0	DIO	PUPD	GPIO0 Group: DIO0 – SPI Chip Select.	3.3
34	SCLKDIO1	DIO	PUPD	GPIO0 Group: DIO1 - SPI Clock.	3.3
35	WSDADIO2	DIO	PUPD	GPIO0 Group: DIO2 - SPI Data In.	3.3
36	RSDADIO3	DIO	PUPD	GPIO0 Group: DIO3 - SPI Data Out.	3.3
37	BIST_PASS	DIO	PD	GPIO0 Group: DIO4. BIST pass/fail output (BIST_EN=1).	3.3
38	IOVDD	DP		I/O V_{DD}.	3.3
39	DVDD	DP		Digital V_{DD}.	1.8
40	TM_EN	DI	PD	Test mode enable	1.8
41	GND	ADG		Exposed Pad. Connect to ground.	

Functional (or Block) Diagram
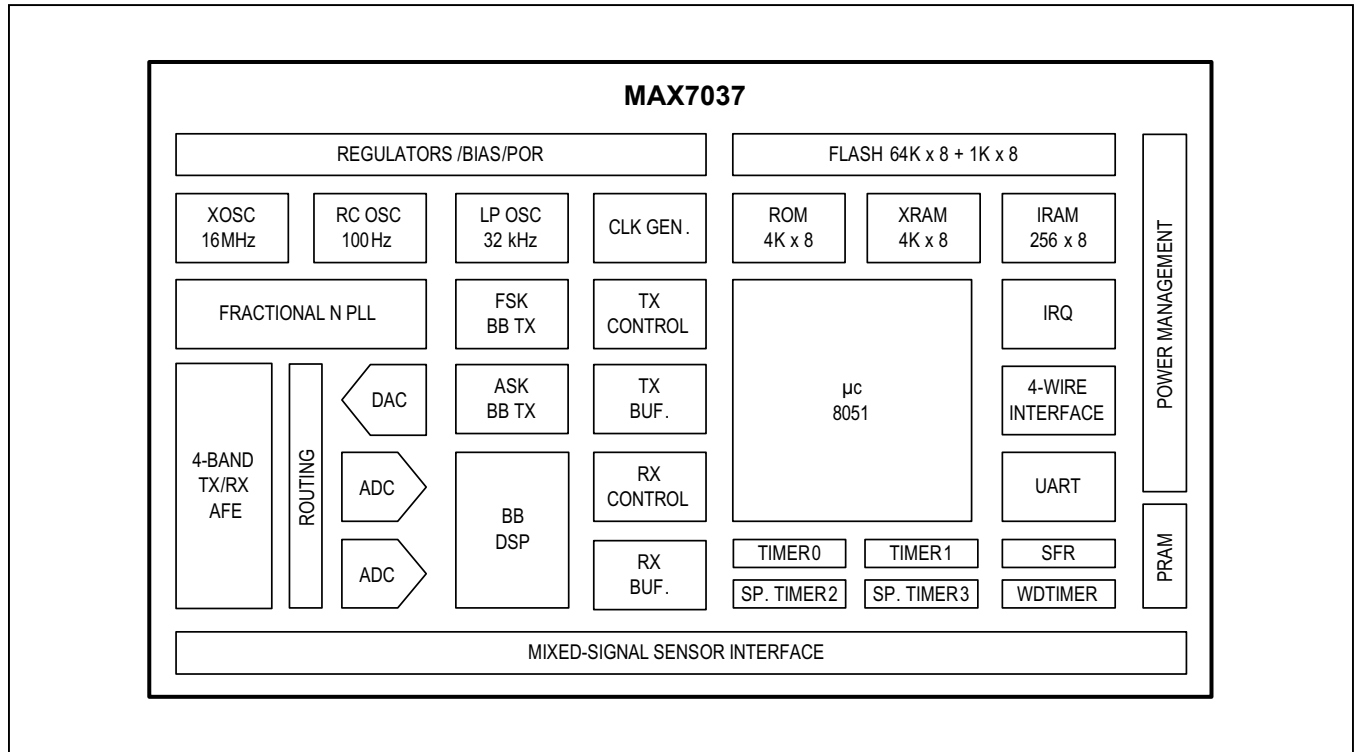
Detailed Description

Operation Modes

Overview

The MAX7037 provides three active modes, a deep sleep mode, and an off mode. The three active modes are:

- CPU Active mode
- RF Transmit mode
- RF Receive mode

CPU Active Mode

In CPU Active mode, the CPU is running normally[1], and executing application firmware from FLASH. This is the default mode after power-up.

This mode is typically used for TX/RX configuration, system management tasks, or mixed-signal sensor interface activity.

In order to switch to TX or RX activity, certain UART commands should be sent. See below section on *Communication*.

RF Transmit Mode

The RF Transmit mode is a fully autonomous process controlled by the internal TX state machine (TX FSM), as well as the internal firmware. It requires the CPU to run on a stabilized XTO clock, an RF configuration, and the desired data to be written into the shared RX/TX data buffer. RF Transmit mode is controlled through the firmware and is described in detail in the *Communication* section below.

The following sequence will configure the MAX7037 for RF Transmit mode and transmit a packet of data. Strings that are sent to the MAX7037 are enclosed in double quotes in the description, but the quotes should not be included in the string.

1) Host sends the string "config_tx_radio N" through the UART to MAX7037 firmware. The value N is 1 through 6 inclusive and corresponds to the specific radio mode.

2) Host sends the string "write_tx_pkt 4 Byte1 Byte 2 … Byte N" through the UART to MAX7037 firmware. Byte1, Byte2 etc. are replaced by the actual values of the bytes. For example, to send a packet containing byte values 14 58 34 137 216, one would send the string "write_tx_pkt 4 14 58 34 137 216". The maximum number of data byte values that can be included in the string is 59.

3) Host sends the string "send_pkt 1" through the UART to the MAX7037 firmware.

4) To send another different packet, without changing radio mode, go back to Step 2. Repeat steps 2 and 3 for every packet to be sent.

RF Receive Mode

Similar to the RF Transmit, the RF Receive mode is a fully autonomous process controlled by the internal RX state machine (RX FSM), as well as the internal firmware. It requires the CPU to run on a stabilized XTO clock and an RF configuration. RF Receive mode is controlled through the firmware, and is described in detail in the *Communication* section below.

The following sequence will configure the MAX7037 for RF Receive mode. Once in receive mode, the host can read out the received data. Strings that are sent to the

MAX7037 are enclosed in double quotes in the description, but the quotes should not be included in the string.

1) Host sends the string "config_rx_radio N" through the UART to MAX7037 firmware. The value N is 1 through 6 inclusive and corresponds to the specific radio mode.

2) Host sends the string "rx_pkt_start v" through the UART to MAX7037 firmware.

3) Host reads the characters received from the MAX7037 UART. Discard all characters until the string "Byte 1 = X\n" where X is the value of the byte and \n is the newline character. The remaining bytes of the packet will be received in the following characters of the string. For example, using the byte values given in the RF Transmit step-by-step instructions, the following will be received: "Byte 1 = 14\nByte 2 = 58\nByte 3 = 34\nByte 4 = 137\nByte 5 = 216\n". Host extracts the values for the data bytes and discards all other characters.

4) The MAX7037 will remain in receive mode, printing out all received packets to the UART until taken out of receive mode by receiving the command string "rx_pkt_stop" from the host. To demarc the end of one packet and the start of the next packet, host must scan for the string: "Byte 0 = X\n". This string will always be sent before the actual user data values of the packet. For example, if the string contains "Byte 1 = 14\nByte 2 = 58\nByte 3 = 34\nByte 4 = 137\nByte 5 = 216\nByte 0 = 15\nByte 1 = 35\n" then the host knows that the data bytes of one packet are 14, 58, 34, 137, 216, and the first byte of the next packet is 35.

5) Host sends the string "rx_pkt_stop" to terminate reception. To resume receive mode, without changing radio mode, go back to step 2.
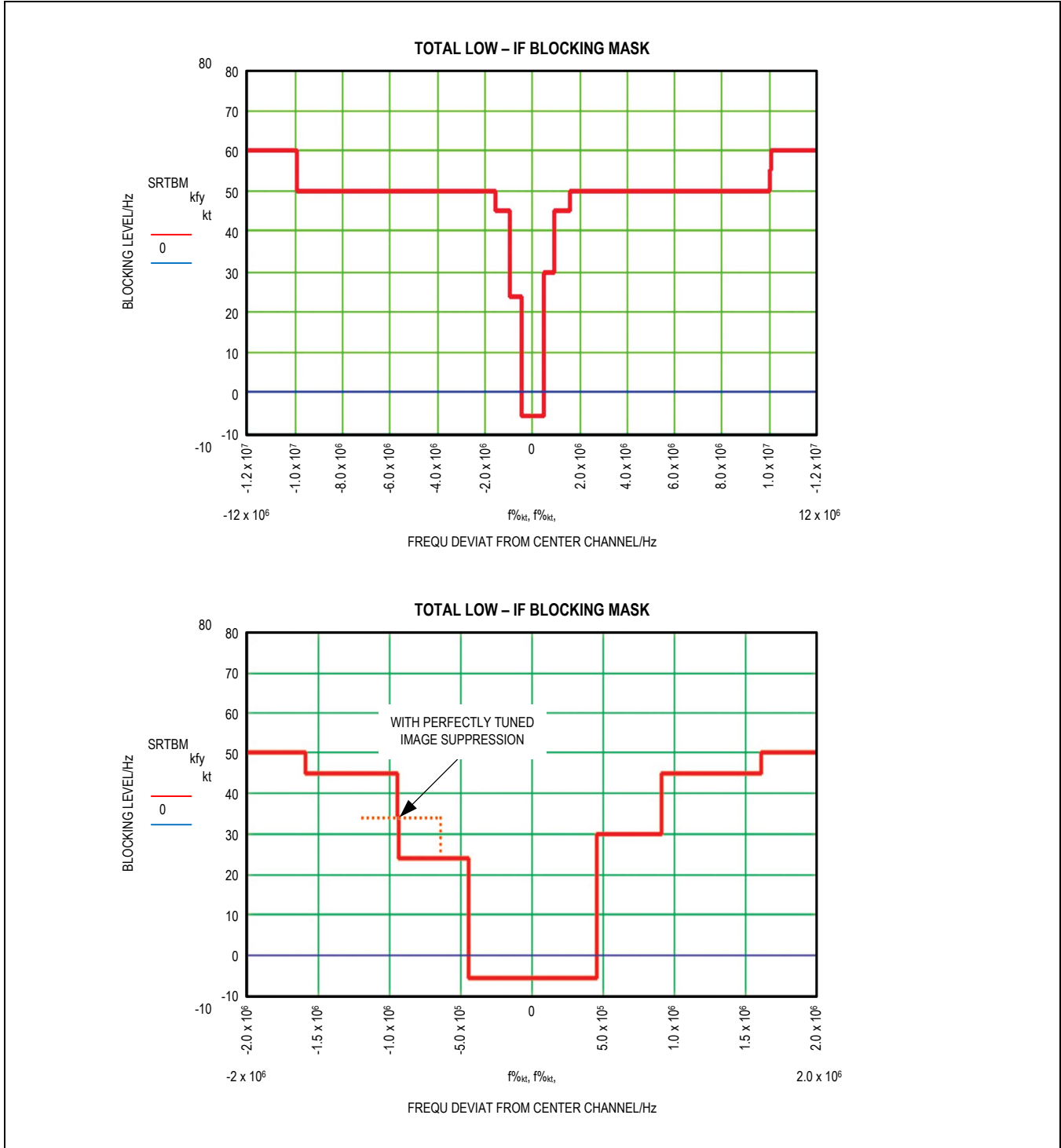
Figure 1. Blocking Mask of the Receiver at Double Wideband Operation. (Dotted line with perfect image rejection tuning. The image position may be swapped to upper side too. SRQ fulfilled with: Useful signal applied 3dB above the measured sensitivity limit. However, not below maximum of $S0_X$ + 3dB. Blocking signal unmodulated CW.)
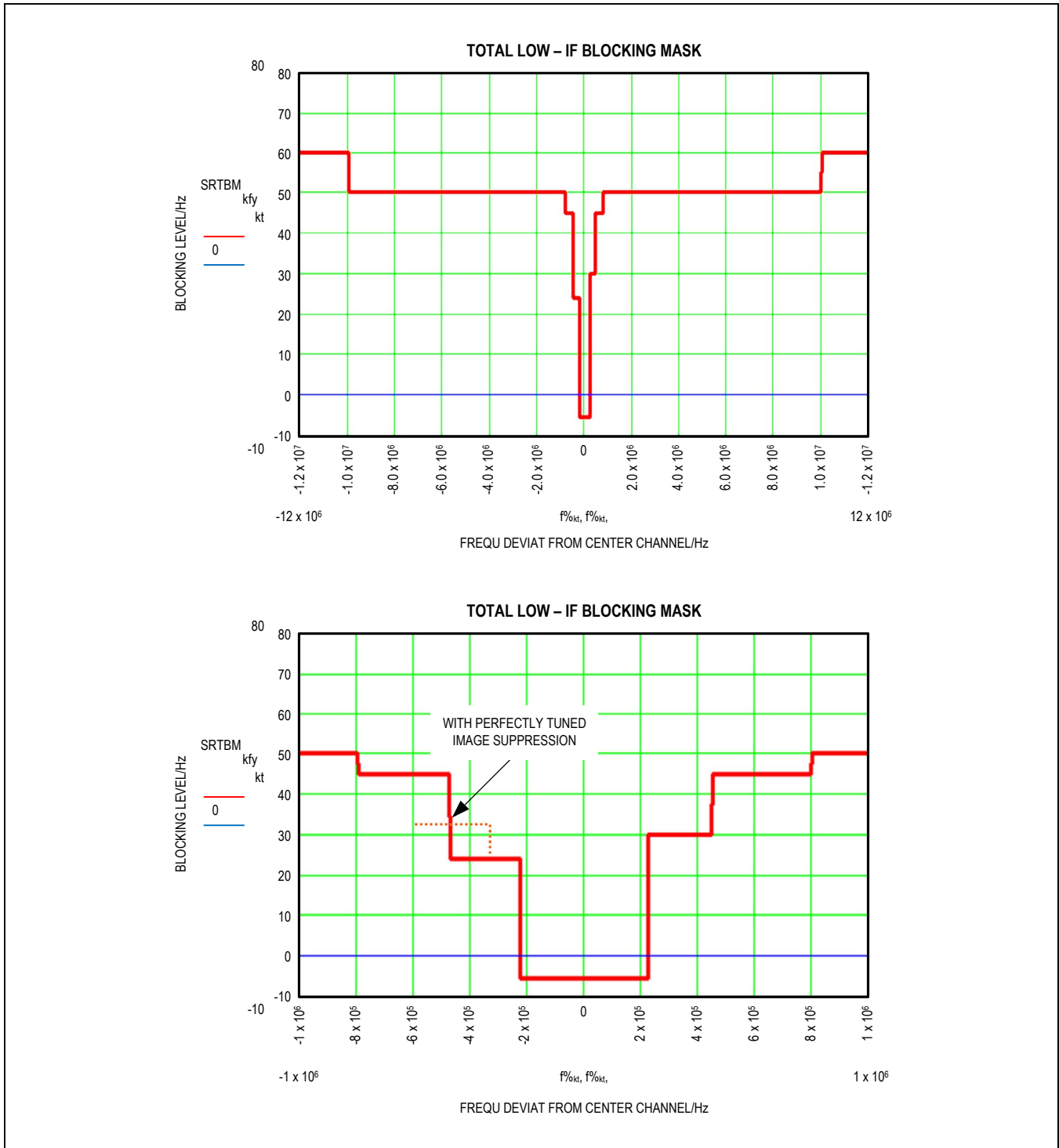
TOTAL LOW – IF BLOCKING MASK

TOTAL LOW – IF BLOCKING MASK

Figure 2. Blocking Mask of the Receiver at Wideband Operation. (Dotted line with perfect image rejection tuning. The image position may be swapped to upper-side too. SRQ fulfilled with: Useful signal applied 3dB above the measured sensitivity limit. However, not below maximum of $S0_X$ + 3dB. Blocking signal unmodulated CW.)

Deep Sleep Mode

Deep Sleep mode is used for weak, ambient energy-powered, event-triggered TX applications, where ultra-low power consumption is a must. In Deep Sleep mode, only the ultra-low power blocks, excluding WXTO, flywheel timer and short-term timer, are active. Deep Sleep mode is interrupted periodically by an RCO-based, ultra-low-power watchdog timer to allow system polling. A change on the WAKE pins can also be used to exit Deep Sleep mode.

After wakeup from Deep Sleep mode, all configurations have to be re-established.

The system will transition directly from CPU STOP to Deep Sleep mode if there is no TX/RX Activity, and no other destination state is specified.

Off Mode

The MAX7037 is in Off mode when insufficient supply is available. There is no MAX7037 activity and the MAX7037 will not drain current from potentially weak energy sources.

The system will transition from Off mode to CPU Active mode when sufficient supply becomes available (i.e., V_{DD} > V_{ON}), as defined in the *Ambient Power Management and Voltage Regulators* section.

The MAX7037 will transition from any mode to Off mode, in a controlled manner, if the supply voltage (V_{DD}) falls below the off threshold (V_{OFF}) and enough battery charge is available to finish this operation. Further details can be found in the *Ambient Power Management and Voltage Regulators* section.

It is recommended that, prior to performing the flash write/erase operation, the supply voltage is measured to ensure that that sufficient energy exists to complete the operation. This ensures that the MAX7037 does not transition to Off mode during write/erase of the flash, leading to possible corruption.

Communication

Overview

This section deals with host CPU communication with the MAX7037. There are two topics discussed:

1) Configuration of IC through UART.

2) Download of firmware to flash memory through SPI.

UART Communications

The host CPU configures the MAX7037 through a set of defined commands. These are sent to the MAX7037 through the UART interface. The firmware, which is in flash memory and is executed by the 8051 microcontroller, implements a command handler routine. The firmware waits for a command to be received from the host. Once a command is received, it parses it, checks for validity of the command and any input arguments, then executes the command. Any command will cause some characters to be output to the host through the UART. For example, if an invalid command is sent, the firmware will respond with a text string indicating the non-validity of the command and prompting for a new command.

Host UART Settings

The configuration of the host UART must be as follows:

Baud Rate = 38400 bps
Data = 8 bits
Parity = None
One stop bit
No Flow Control

UART Pins and Timing

The Tx pin is ADIO7 (pin 28) and the Rx pin is ADIO6 (pin 27). The timing is the standard serial interface timing. A single start bit which is always 0 is followed by the 8 data bits, least significant bit first. The final 10th bit is a stop bit which is always 1. The bits are shifted into the Rx pin or out of the Tx pin at the baud rate of 38400 bits/sec so the duration of each bit is the reciprocal of the baud rate. Refer to the timing diagram in Figure 3.
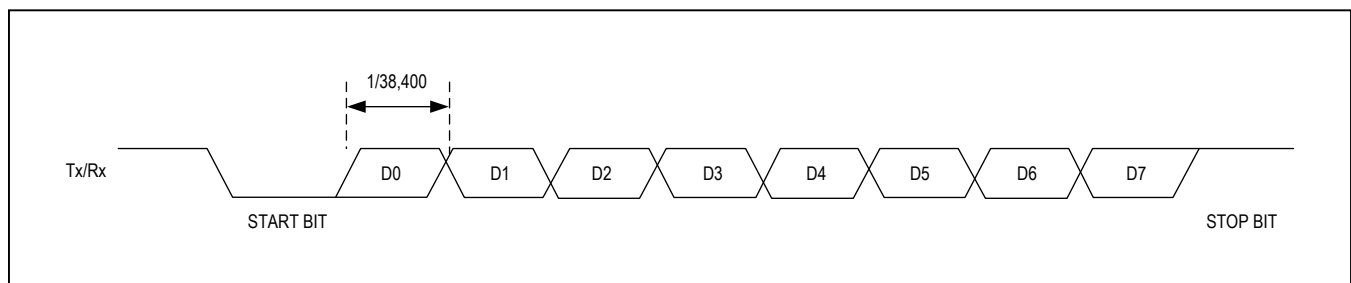

Figure 3. UART Timing Diagram

Commands

There are a set of commands available for configuring the MAX7037. The whole set can be seen by simply sending the string "help". The result is shown in Figure 4. If an invalid command is received, the firmware returns a string indicating the command is invalid. To get help for each command, send "help cmd" where cmd is replaced by the command string. For example, "help rssi" will cause the help text for the rssi command to be returned.

The detailed syntax of each command is provided in the following sections. Optional input parameters are enclosed in square parentheses. All input parameters must be separated by one or more space characters. A command is terminated with a newline character.

help [cmd]

The help command will cause a brief description of the command to be returned. The syntax is

>> help cmd

Where cmd is replaced by the actual command. If just help is input, then the set of commands is returned.

write_tx_pkt pkt_index [Byte1, Byte2, …, ByteN]

The write_tx_pkt command is used to load the contents of a transmit packet into the data buffer. Either a predefined packet can be loaded or a user-defined packet.

pkt_index

The pkt_index input parameter is an integer with range [0:3] which is used to select one of four pre-defined packets. All four pre-defined packets have a fixed 2-byte preamble and 2-byte packet synchronization bit sequence comprising the packet header. The packet payload depends on the input parameters. The packet corresponding to pkt_index = 0 consists of 24 bytes of incrementing values with the exception of the first byte which specifies the length of the payload in bytes for all packets. The packet payload corresponding to pkt_index = 1 consists of 24 random byte values, again with the exception of the first byte which has a value of 24. The packet payload corresponding to pkt_index = 2 is 60 bytes of incrementing values, and the packet payload corresponding to pkt_index = 3 consists of 60 random byte values. If pkt_index is any value other > 3, then it is ignored and the user-specified payload defined by the optional Byte1, …, ByteN input parameters are used instead. If a value of pkt_index > 3 is specified and there are no user-defined input parameters, then the firmware will return an error message without taking further action.

Figure 4: List of Available Commands

The four predefined packets have the following contents:

PACKET #0	PACKET #1	PACKET #2	PACKET #3	PACKET #0	PACKET #1	PACKET #2	PACKET #3
24	24	60	60			30	43
1	231	1	208			31	180
2	32	2	231			32	8
3	233	3	32			33	70
4	161	4	233			34	11
5	24	5	161			35	24
6	71	6	24			36	210
7	140	7	71			37	177
8	245	8	140			38	81
9	247	9	245			39	243
10	40	10	247			40	8
11	248	11	40			41	112
12	245	12	248			42	97
13	124	13	245			43	195
14	204	14	124			44	203
15	36	15	204			45	47
16	107	16	36			46	125
17	234	17	107			47	114
18	202	18	234			48	165
19	245	19	202			49	181
20	167	20	245			50	193
21	9	21	167			51	70
22	217	22	9			52	174
23	239	23	217			53	167
		24	239			54	41
		25	173			55	30
		26	193			56	127
		27	190			57	245
		28	100			58	87
		29	167			59	149

Byte1, Byte2, …, ByteN

The user can define their own packet payload through the optional Byte1, …, ByteN input parameters. Each parameter must be a value between 0 and 255 inclusive. If any value is outside of this range, it is replaced with 0 by the firmware. The firmware will count the number of bytes entered and automatically set the first byte of the payload to the length of the payload. Hence inputting N bytes results in a payload of N + 1 bytes, and a total packet length including the header of N + 5 bytes. The maximum payload length supported by MAX7037 is 60 bytes, so if more than 59 byte values are input, any byte values after the 59th one are ignored.

write_rx_pkt pkt_index [Byte1, Byte2, …, ByteN]

The write_rx_pkt command is used to load the expected contents of a received packet into RAM inside the MAX7037. This is required for BER testing. The syntax and usage of the write_rx_pkt command are identical to that of the write_tx_pkt command.

send_pkt numTimes [contTx]

The send_pkt command causes the firmware to initiate transmission of the packet specified by the write_tx_pkt command. The same packet will be transmitted the number of times defined by the input parameter numTimes. One can specify continuous back-to-back transmission of the packet with the contTx input parameter.

numTimes

If numTimes = 0, then the the packet will be continuously transmitted until stopped by reception of a "q" character. If numTimes is any value between 1 and 65535, the packet will be transmitted numTimes number of times, then transmission will stop automatically. The only legal values are 0 to 65535 inclusive. Between successive packet transmissions, the MAX7037 will ramp down the PA output power, pause, then proceed with the next packet transmission, ramping up the PA output power. For BER testing, this does not cause issues, and represents the normal operation of the device where it is sending or receiving one packet at a time. However, for testing of Tx spectral mask compliance, it is preferable to avoid having the PA keep turning off and on. To support this, the optional contTx input parameter is provided.

contTx

If the user provides a contTx input parameter, then it is read by the firmware. If the value is 0, then it is ignored. If non-zero, then the firmware ignores the numTimes parameter and instead just configures the MAX7037 to repeatedly loop through the data buffer causing the same packet to be transmitted continuously. This will continue until reception of a "q" character. This mode differs from setting numTimes = 0 in that the transmitter circuitry does not power down between each packet transmission. This mode is provided to support transmit mask compliance testing.

tx_interval period

The tx_interval command is used to set the interval between successive packet transmissions.

period

The period input parameter is the interval in 10 millisecond units. The legal range of values is 2 through 255 inclusive. The default value is 100 resulting in one second between successive packet transmissions.

rx_pkt_start [verbose]

The rx_pkt_start command causes the firmware to configure the MAX7037 to receive packets. The MAX7037 remains in this state until the stop_pkt_rx command is received. If the optional input parameter, verbose, is sent, and has a value of "v", then the contents of each received packet will be output to the terminal. If no input parameter is provided, then nothing is returned. Each time a packet is received, the MAX7037 will toggle the state of the GPIO output pin GPIO1.0 (pin 21). On the MAX7037 EV kit, this pin can be connected to an LED (through appropriate setting of a DIP switch), which will toggle on and off to give a visual indication of packet reception.

Once the rx_pkt_start command has been issued, there are only four commands that can be sent: reset_ber, read_ber, rssi and rx_pkt_stop. Once the rx_pkt_stop command is received by the firmware, it will return full control to the user so that the whole set of commands are available.

rx_pkt_stop

The rx_pkt_stop command causes the firmware to configure the MAX7037 to stop reception of packets. Any reception of any packet that is being received when the command is issued will be completed, after which the reception will be stopped gracefully.

ber_enable

The ber_enable command is used to enable bit error rate measurements. This command would be issued to a MAX7037 configured as a receiver prior to starting packet transmission at a MAX7037 configured as a transmitter. The data field of all packets received will be compared against the expected pattern (programmed with the write_rx_pkt command). Any bit mismatches are counted and the BER is reported as the ratio of errored bits to total bits.