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# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### General Description

The MAX7456 single-channel monochrome on-screen display (OSD) generator lowers system cost by eliminating the need for an external video driver, sync separator, video switch, and EEPROM. The MAX7456 serves all national and international markets with 256 user-programmable characters in NTSC and PAL standards. The MAX7456 easily displays information such as company logo, custom graphics, time, and date with arbitrary characters and sizes. The MAX7456 is preloaded with 256 characters and pictographs and can be reprogrammed in-circuit using the SPI™ port.

The MAX7456 is available in a 28-pin TSSOP package and is fully specified over the extended (-40°C to +85°C) temperature range.

### Applications

Security Switching Systems  
 Security Cameras  
 Industrial Applications  
 In-Cabin Entertainment  
 Consumer Electronics

**Pin Configuration appears at end of data sheet.**

*SPI is a trademark of Motorola, Inc.*

### Features

- ◆ 256 User-Defined Characters or Pictographs in Integrated EEPROM
- ◆ 12 x 18 Pixel Character Size
- ◆ Blinking, Inverse, and Background Control Character Attributes
- ◆ Selectable Brightness by Row
- ◆ Displays Up to 16 Rows x 30 Characters
- ◆ Sag Compensation On Video-Driver Output
- ◆ LOS, VSYNC, HSYNC, and Clock Outputs
- ◆ Internal Sync Generator
- ◆ NTSC and PAL Compatible
- ◆ SPI-Compatible Serial Interface
- ◆ Delivered with Preprogrammed Character Set

### Ordering Information

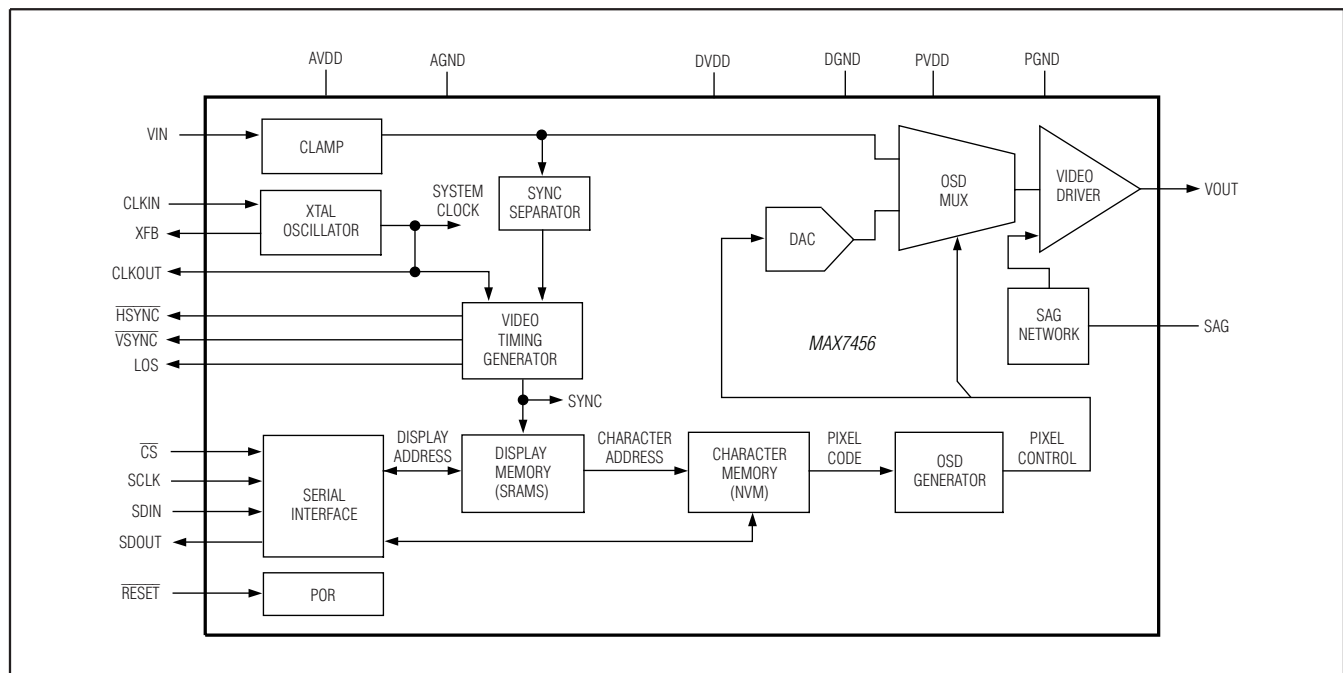
PART	PIN-PACKAGE	LANGUAGE
MAX7456EUI+	28 TSSOP-EP*	English/ Japanese

\*EP = Exposed pad.

+ Denotes a lead-free/RoHS-compliant package.

**Note:** This device is specified over the -40°C to +85°C operating temperature range.

### Simplified Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at [www.maximintegrated.com](http://www.maximintegrated.com).

# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....	-0.3V to +6V	CLKIN, CLKOUT, XFB to DGND .....	-0.3V to (V <sub>DVDD</sub> + 0.3V)
DVDD to DGND .....	-0.3V to +6V	SDIN, SCLK, $\overline{\text{CS}}$ , SDOOUT to DGND.....	-0.3V to (V <sub>DVDD</sub> + 0.3V)
PVDD to PGND.....	-0.3V to +6V	Maximum Continuous Current into V <sub>OUT</sub> .....	±100mA
AGND to DGND.....	-0.3V to +0.3V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
AGND to PGND .....	-0.3V to +0.3V	28-Pin TSSOP (derate 27mW/°C above +70°C).....	2162mW*
DGND to PGND .....	-0.3V to +0.3V	Operating Temperature Range .....	-40°C to +85°C
VIN, VOUT, SAG to AGND.....	-0.3V to (V <sub>AVDD</sub> + 0.3V)	Junction Temperature .....	+150°C
HSYNC, VSYNC, LOS to AGND .....	-0.3V to +6V	Storage Temperature Range .....	-60°C to +150°C
RESET to AGND .....	-0.3V to (V <sub>AVDD</sub> + 0.3V)	Lead Temperature (soldering, 10s) .....	+300°C

\* As per JEDEC51 Standard (Multilayer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>AVDD</sub> = +4.75V to +5.25V, V<sub>DVDD</sub> = +4.75V to +5.25V, V<sub>PVDD</sub> = +4.75V to +5.25V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>. Typical values are at V<sub>AVDD</sub> = V<sub>DVDD</sub> = V<sub>PVDD</sub> = +5V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES</b>						
Analog Supply Voltage	V <sub>AVDD</sub>		4.75	5	5.25	V
Digital Supply Voltage	V <sub>DVDD</sub>		4.75	5	5.25	V
Driver Supply Voltage	V <sub>PVDD</sub>		4.75	5	5.25	V
Analog Supply Current	I <sub>AVDD</sub>	V <sub>IN</sub> = 1V <sub>P-P</sub> (100% white flat field signal), V <sub>OUT</sub> load, R <sub>L</sub> = 150Ω		24	35	mA
Digital Supply Current	I <sub>DVDD</sub>	V <sub>IN</sub> = 1V <sub>P-P</sub> (100% white flat field signal), V <sub>OUT</sub> load, R <sub>L</sub> = 150Ω		25	30	mA
Driver Supply Current	I <sub>PVDD</sub>	V <sub>IN</sub> = 1V <sub>P-P</sub> (100% white flat field signal), V <sub>OUT</sub> load, R <sub>L</sub> = 150Ω		58	80	mA
<b>NONVOLATILE MEMORY</b>						
Data Retention		T <sub>A</sub> = +25°C		100		Years
Endurance		T <sub>A</sub> = +25°C		100,000		Stores
<b>DIGITAL INPUTS (<math>\overline{\text{CS}}</math>, SDIN, <math>\overline{\text{RESET}}</math>, SCLK)</b>						
Input High Voltage	V <sub>IH</sub>		2.0			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input Hysteresis	V <sub>HYS</sub>			50		mV
Input Leakage Current		V <sub>IN</sub> = 0 or V <sub>DVDD</sub>			±10	μA
Input Capacitance	C <sub>IN</sub>			5		pF
<b>DIGITAL OUTPUTS (SDOUT, CLKOUT, VSYNC, HSYNC, LOS)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 4mA (SDOUT, CLKOUT)	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 4mA			0.45	V
Tri-State Leakage Current		SDOUT, $\overline{\text{CS}}$ = V <sub>DVDD</sub>			±10	μA

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{AVDD} = +4.75V$  to  $+5.25V$ ,  $V_{DVDD} = +4.75V$  to  $+5.25V$ ,  $V_{PVDD} = +4.75V$  to  $+5.25V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CLOCK INPUT (CLKIN)</b>						
Clock Frequency				27		MHz
Clock-Pulse High			14			ns
Clock-Pulse Low			14			ns
Input High Voltage			0.7 x $V_{DVDD}$			V
Input Low Voltage					0.3 x $V_{DVDD}$	V
Input Leakage Current		$V_{IN} = 0V$ or $V_{DVDD}$			$\pm 50$	$\mu A$
<b>CLOCK OUTPUT (CLKOUT)</b>						
Duty Cycle		5pF and 10k $\Omega$ to DGND	40	50	60	%
Rise Time		5pF and 10k $\Omega$ to DGND		3		ns
Fall Time		5pF and 10k $\Omega$ to DGND		3		ns
<b>VIDEO CHARACTERISTICS</b>						
DC Power-Supply Rejection		$V_{AVDD} = V_{DVDD} = V_{PVDD} = 5V$ ; $V_{IN} = 1V_{P-P}$ , measured at VOUT		40		dB
AC Power-Supply Rejection		$V_{AVDD} = V_{DVDD} = V_{PVDD} = 5V$ ; $V_{IN} = 1V_{P-P}$ , measured at VOUT; $f = 5MHz$ ; power-supply ripple = 0.2V $_{P-P}$		30		dB
Short-Circuit Current		VOUT to PGND			230	mA
Line-Time Distortion	LTD	Figures 1a, 1b			0.5	%
Output Impedance	ZOUT	Figures 1a, 1b		0.2		$\Omega$
Gain		Figures 1a, 1b	1.89	2.0	2.11	V/V
Black Level		At VOUT, Figures 1a, 1b			AGND + 1.5	V
Input-Voltage Operating Range	$V_{IN}$	Figures 1a, 3 (Note 2)	0.5		1.2	V $_{P-P}$
Input-Voltage Sync Detection Range	$V_{INSD}$	Figures 1a, 3 (Note 3)	0.5		2.0	V $_{P-P}$
Maximum Output-Voltage Swing	VOUT	Figures 1a, 1b	2.4			V $_{P-P}$
Output-Voltage Sync Tip Level				0.7		V
Large Signal Bandwidth (0.2dB)	BW	$V_{OUT} = 2V_{P-P}$ , Figures 1a, 1b		6		MHz
VIN to VOUT Delay				30		ns
Differential Gain	DG			0.5		%
Differential Phase	DP			0.5		Degrees
OSD White Level		VOUT 100% white level with respect to black level	1.25	1.33	1.45	V
Horizontal Pixel Jitter		Between consecutive horizontal lines		24		ns
Video Clamp Settling Time				32		Lines

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{AVDD} = +4.75V$  to  $+5.25V$ ,  $V_{DVDD} = +4.75V$  to  $+5.25V$ ,  $V_{PVDD} = +4.75V$  to  $+5.25V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OSD CHARACTERISTICS</b>						
OSD Rise Time		OSD insertion mux register OSDM[5,4,3] = 011b		60		ns
OSD Fall Time		OSD insertion mux register OSDM[5,4,3] = 011b		60		ns
OSD Insertion Mux Switch Time		OSD insertion mux register OSDM[2,1,0] = 011b		75		ns

### TIMING CHARACTERISTICS

( $V_{AVDD} = +4.75V$  to  $+5.25V$ ,  $V_{DVDD} = +4.75V$  to  $+5.25V$ ,  $V_{PVDD} = +4.75V$  to  $+5.25V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SPI TIMING</b>						
SCLK Period	$t_{CP}$		100			ns
SCLK Pulse-Width High	$t_{CH}$		40			ns
SCLK Pulse-Width Low	$t_{CL}$		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup	$t_{CSS0}$		30			ns
$\overline{CS}$ Fall After SCLK Rise Hold	$t_{CSH0}$		0			ns
$\overline{CS}$ Rise to SCLK Setup	$t_{CSS1}$		30			ns
$\overline{CS}$ Rise After SCLK Hold	$t_{CSH1}$		0			ns
$\overline{CS}$ Pulse-Width High	$t_{CSW}$		100			ns
SDIN to SCLK Setup	$t_{DS}$		30			ns
SDIN to SCLK Hold	$t_{DH}$		0			ns
SDOUT Valid Before SCLK	$t_{DO1}$	20pF to ground	25			ns
SDOUT Valid After SCLK	$t_{DO2}$	20pF to ground	0			ns
$\overline{CS}$ High to SDOUT High Impedance	$t_{DO3}$	20pF to ground	300			ns
$\overline{CS}$ Low to SDOUT Logic Level	$t_{DO4}$	20pF to ground	20			ns
<b>HSYNC, VSYNC, AND LOS TIMING</b>						
LOS, $\overline{VSYNC}$ , and $\overline{HSYNC}$ Valid before CLKOUT Rising Edge	$t_{DOV}$	20pF to ground		30		ns
VOUT Sync to $\overline{VSYNC}$ Falling Edge Delay	$t_{VOUT-VSF}$	NTSC external sync mode, Figure 4		375		ns
		PAL external sync mode, Figure 6		400		

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### TIMING CHARACTERISTICS (continued)

( $V_{AVDD} = +4.75V$  to  $+5.25V$ ,  $V_{DVDD} = +4.75V$  to  $+5.25V$ ,  $V_{PVDD} = +4.75V$  to  $+5.25V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{AVDD} = V_{DVDD} = V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOUT Sync to $\overline{VSYN}$ Rising Edge Delay	$t_{VOUT-VSR}$	NTSC external sync mode, Figure 4		400		ns
		PAL external sync mode, Figure 6		425		
$\overline{VSYN}$ Falling Edge to VOUT Sync Delay	$t_{VSF-VOUT}$	NTSC internal sync mode, Figure 5		40		ns
		PAL internal sync mode, Figure 7		45		
$\overline{VSYN}$ Rising Edge to VOUT Sync Delay	$t_{VSR-VOUT}$	NTSC internal sync mode, Figure 5		32		ns
		PAL internal sync mode, Figure 7		30		
VOUT Sync to $\overline{HSYN}$ Falling Edge Delay	$t_{VOUT-HSF}$	NTSC and PAL external sync mode, Figure 8		310		ns
VOUT Sync to $\overline{HSYN}$ Rising Edge Delay	$t_{VOUT-HSR}$	NTSC and PAL external sync mode, Figure 8		325		ns
$\overline{HSYN}$ Falling Edge to VOUT Sync Delay	$t_{HSF-VOUT}$	NTSC and PAL internal sync mode, Figure 9		115		ns
$\overline{HSYN}$ Rising Edge to VOUT Sync Delay	$t_{HSR-VOUT}$	NTSC and PAL internal sync mode, Figure 9		115		ns
All Supplies High to $\overline{CS}$ Low	$t_{PUD}$	Power-up delay		50		ms
NVM Write Busy	$t_{NVW}$			12		ms

**Note 1:** See the standard test circuits of Figure 1.  $R_L = 75\Omega$ , unless otherwise specified. All digital input signals are timed from a voltage level of  $(V_{IH} + V_{IL}) / 2$ . All parameters are tested at  $T_A = +85^\circ C$  and values through temperature range are guaranteed by design.

**Note 2:** The input-voltage operating range is the input range over which the output signal parameters are guaranteed (Figure 3).

**Note 3:** The input-voltage sync detection range is the input composite video range over which an input sync signal is properly detected and the OSD signal appears at VOUT. However, the output voltage specifications are not guaranteed for input signals exceeding the maximum specified in the input operating voltage range (Figure 3).

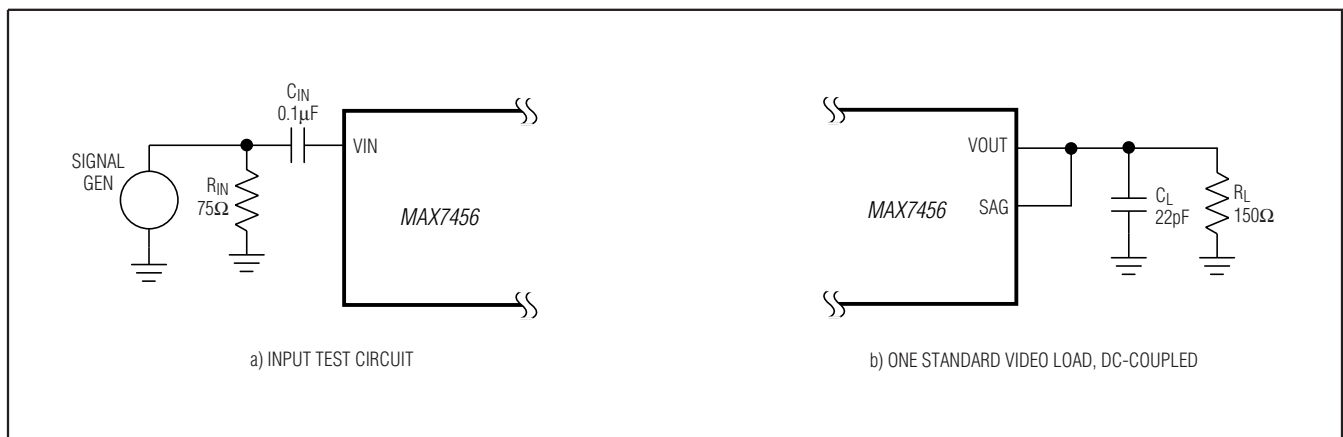


Figure 1. Standard Test Circuits

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

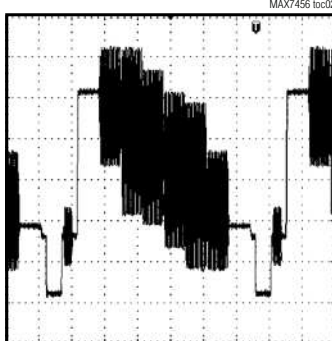
### Typical Operating Characteristics

( $V_{AVDD} = +5V$ ,  $V_{DVDD} = +5V$ ,  $V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

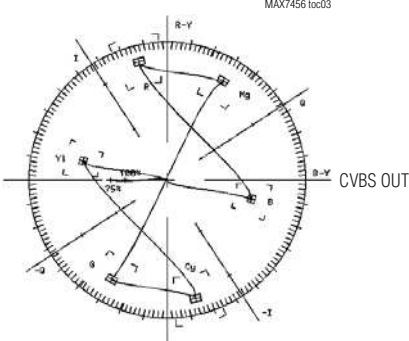
IMAGE WITH ON-SCREEN GRAPHICS



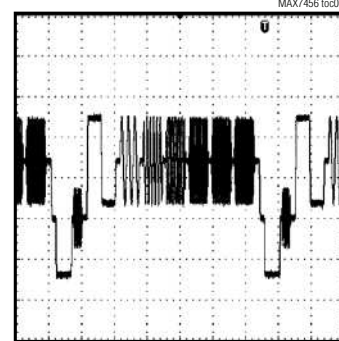
100% COLOR BARS RESPONSE



75% COLOR BARS VECTOR DIAGRAM



60% MULTIBURST RESPONSE



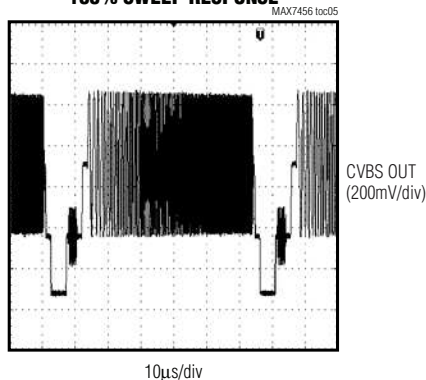
# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

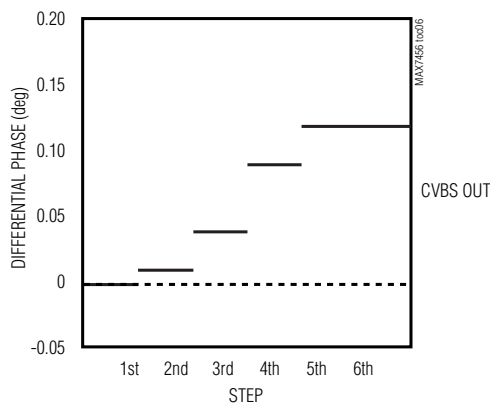
### Typical Operating Characteristics (continued)

( $V_{AVDD} = +5V$ ,  $V_{DVDD} = +5V$ ,  $V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

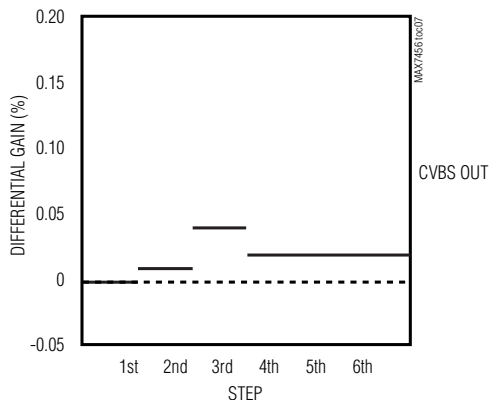
100% SWEEP RESPONSE



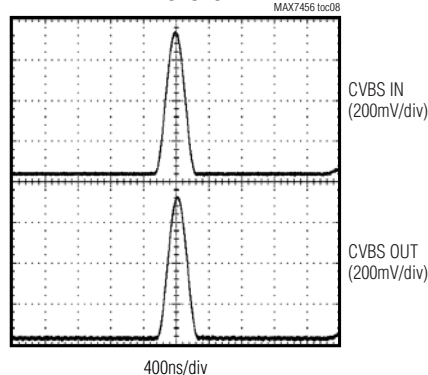
DIFFERENTIAL PHASE



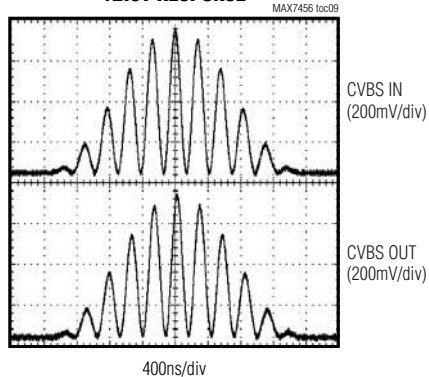
DIFFERENTIAL GAIN



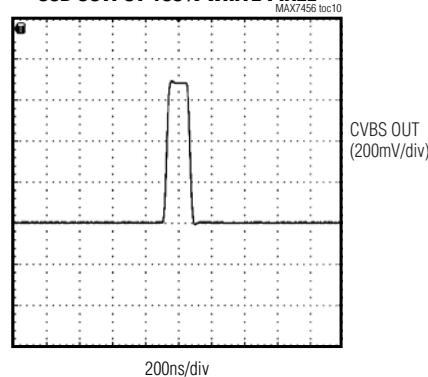
2T RESPONSE



12.5T RESPONSE



OSD OUTPUT 100% WHITE PIXEL





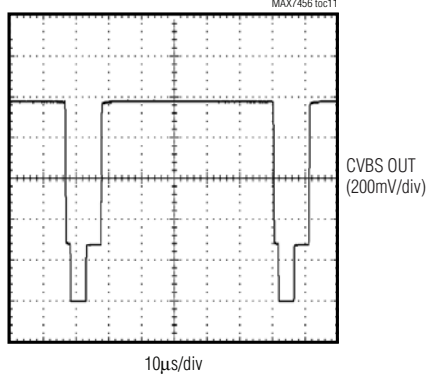
# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

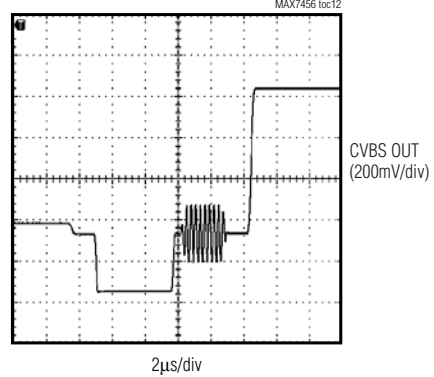
### Typical Operating Characteristics (continued)

( $V_{AVDD} = +5V$ ,  $V_{DVDD} = +5V$ ,  $V_{PVDD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. See the *Typical Operating Circuit* of Figure 2, if applicable.)

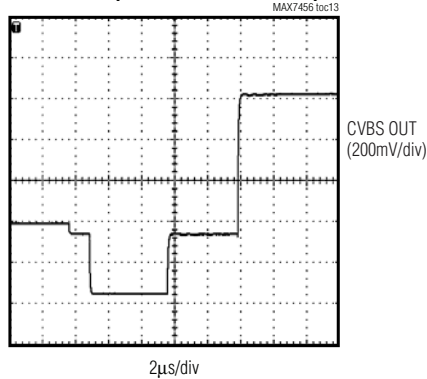
**LINE-TIME DISTORTION**



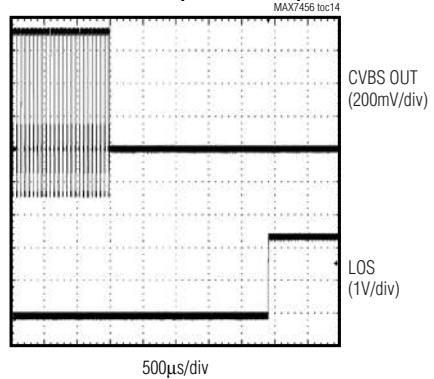
**H TIMING (EXTERNAL-SYNC MODE)**



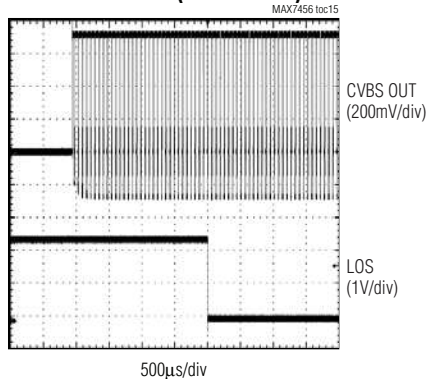
**H TIMING (INTERNAL-SYNC MODE)**



**LOSS-OF-SYNC (LOW TO HIGH)**



**LOSS-OF-SYNC (HIGH TO LOW)**



# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### Pin Description

PIN	NAME	FUNCTION
1, 2, 13–16, 27, 28	N.C.	No Connection. Not internally connected.
3	DVDD	Digital Power-Supply Input. Bypass to DGND with a 0.1µF capacitor.
4	DGND	Digital Ground
5	CLKIN	Crystal Connection 1. Connect a parallel resonant, fundamental mode crystal between CLKIN and XFB for use as a crystal oscillator, or drive CLKIN directly with a 27MHz system reference clock.
6	XFB	Crystal Connection 2. Connect a parallel resonant, fundamental mode crystal between CLKIN and XFB for use as a crystal oscillator, or leave XFB unconnected when driving CLKIN with a 27MHz system reference clock.
7	CLKOUT	Clock Output. 27MHz logic-level output system clock.
8	$\overline{CS}$	Active-Low Chip-Select Input. SDOUT goes high impedance when $\overline{CS}$ is high.
9	SDIN	Serial Data Input. Data is clocked in at rising edge of SCLK.
10	SCLK	Serial Clock Input. Clocks data into SDIN and out of SDOUT. Duty cycle must be between 40% and 60%.
11	SDOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
12	LOS	Loss-of-Sync Output (Open-Drain). LOS goes high when the VIN sync pulse is lost for 32 consecutive lines. LOS goes low when 32 consecutive valid sync pulses are received. Connect to a 1kΩ pullup resistor to DVDD or another positive supply voltage suitable for the receiving device.
17	$\overline{VSYN}$	Vertical Sync Output (Open-Drain). $\overline{VSYN}$ goes low following the video input's vertical sync interval. $\overline{VSYN}$ is either recovered from VIN or internally generated when in internal sync mode. Connect to a 1kΩ pullup resistor to DVDD or another positive supply voltage suitable for the receiving device.
18	$\overline{HSYN}$	Horizontal Sync Output (Open-Drain). $\overline{HSYN}$ goes low following the video input's horizontal sync interval. $\overline{HSYN}$ is either recovered from VIN or internally generated when in internal sync mode. Connect to a 1kΩ pullup resistor to DVDD or another positive supply voltage suitable for the receiving device.
19	$\overline{RESET}$	System Reset Input. The minimum $\overline{RESET}$ pulse width is 50ms. All SPI registers are reset to their default values after 100µs following the rising edge of $\overline{RESET}$ . These registers are not accessible for reading or writing during that time. The display memory is reset to its default value of 00H in all locations after 20µs following the rising edge of $\overline{RESET}$ .
20	AGND	Analog Ground
21	AVDD	Analog Power-Supply Input. Bypass to AGND with a 0.1µF capacitor.
22	VIN	PAL or NTSC CVBS Video Input
23	PGND	Driver Ground. Connect to AGND at a single point.
24	PVDD	Driver Power-Supply Input. Bypass to PGND with a 0.1µF capacitor.
25	SAG	Sag Correction Input. Connect to VOUT if not used. See Figure 1b.
26	VOUT	Video Output
—	EP	Exposed Pad. Internally connected to AGND. Connect EP to the AGND plane for improved heat dissipation. Do not use EP as the only ground connection.

# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

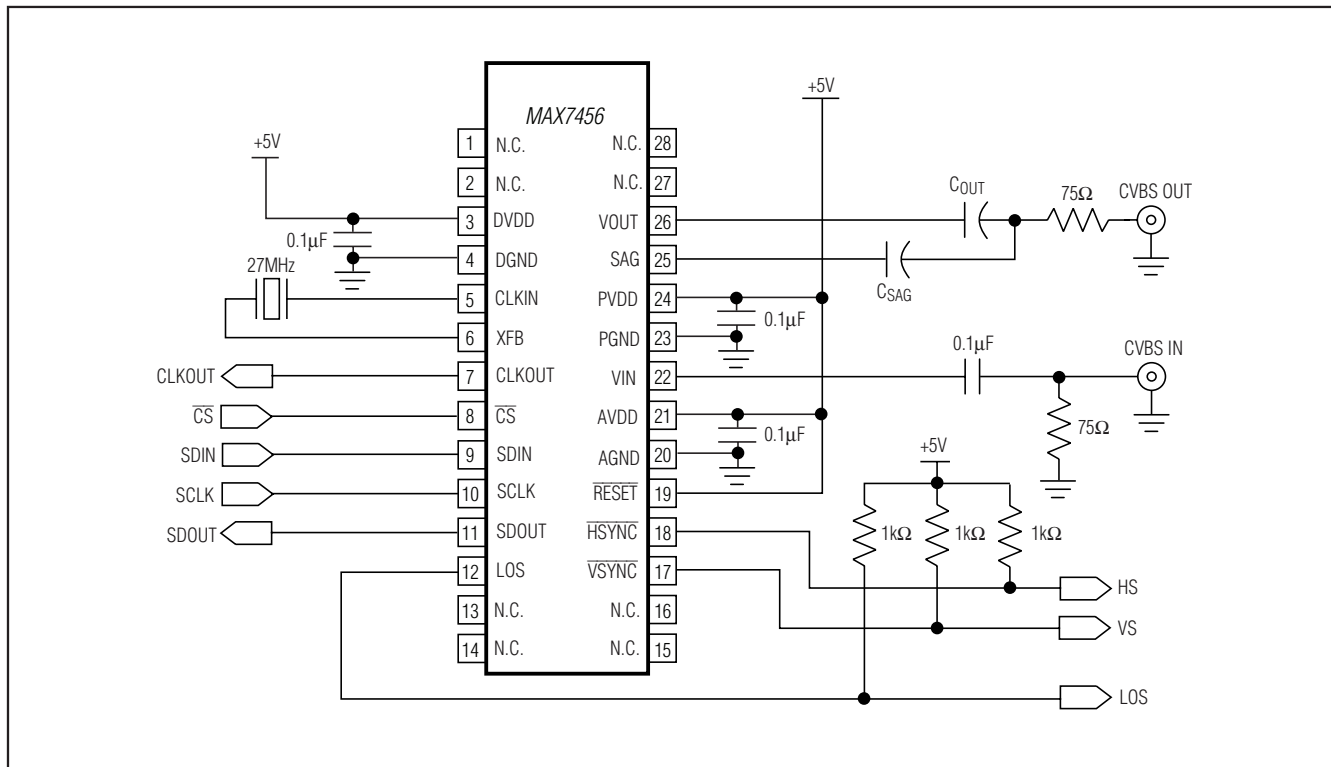


Figure 2. Typical Operating Circuit

### Detailed Description

The MAX7456 single-channel monochrome on-screen display (OSD) generator integrates all the functions needed to generate a user-defined OSD and insert it into the output signal. The MAX7456 accepts a composite NTSC or PAL video signal. The device includes an input clamp, sync separator, video timing generator, OSD insertion mux, nonvolatile character memory, display memory, OSD generator, crystal oscillator, an SPI-compatible interface to read/write the OSD data, and a video driver (see the *Simplified Functional Diagram*). Additionally, the MAX7456 provides vertical sync ( $\overline{\text{VSYNC}}$ ), horizontal sync (HSYNC), and loss-of sync (LOS) outputs for system synchronization. A clock output signal (CLKOUT) allows daisy-chaining of multiple devices.

See the *MAX7456 Register Description* section for an explanation of register notation use in this data sheet.

The 256 user-defined 12 x 18 pixel character set comes preloaded and is combined with the input video stream to generate a CVBS signal with OSD video output. A maximum of 256 12 x 18 pixel characters can be reprogrammed in the NVM. In NTSC mode, 13 rows x 30 characters are displayed. In PAL mode, 16 rows x 30 characters are displayed. When the input video signal is absent, the OSD image can still be displayed by using the MAX7456's internal video timing generator.

### Video Input

The MAX7456 accepts standard NTSC or PAL CVBS signals at VIN. The video signal input must be AC-coupled with a 0.1µF capacitor and is internally clamped. An input coupling capacitance of 0.1µF is required to guarantee the specified line-time distortion (LTD) and video clamp settling time. The video clamp settling time changes proportionally to the input coupling capacitance, and LTD changes inversely proportional to the capacitance.

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

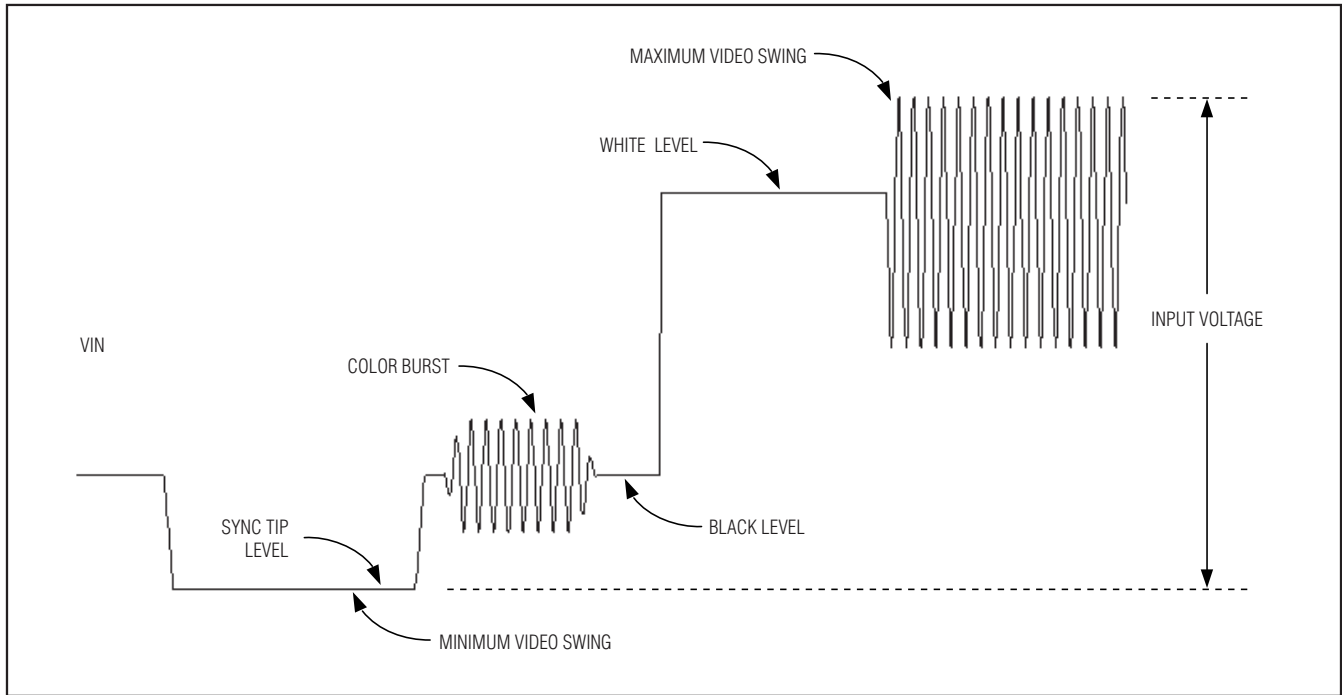


Figure 3. Definition of Terms

### Input Clamp

The MAX7456's clamp is a DC-restore circuit that uses the input coupling capacitor to correct any DC shift of the input signal, on a line-by-line basis, such that the sync tip at VIN is approximately 550mV. This establishes a DC level at VIN suitable for the on-chip sync detection and video processing functions. This circuitry also removes low-frequency noise such as 60Hz hum or other additive low-frequency noise.

### Sync Separator

The sync separator detects the composite sync pulses on the video input and extracts the timing information to generate  $\overline{\text{HSYNC}}$  and  $\overline{\text{VSYNC}}$ . It is also used for internal OSD synchronization and loss-of-sync (LOS) detection. LOS goes high if no sync signal is detected at VIN for 32 consecutive lines, and goes low if 32 consecutive horizontal sync signals are detected. During a LOS condition, when VM0[5] = 0 (Video Mode 0 register, bit 5), only the OSD appears at the VOUT. At this time, the input image is set to a gray level at VOUT as determined by VM1[6:4]. The behavior of all sync modes is shown in Table 1.

Table 1. Video Sync Modes

VIDEO MODE	VIN	$\overline{\text{VSYNC}}$	$\overline{\text{HSYNC}}$	LOS	VOUT
Auto Sync Select Mode VM0[5, 4] = 0x	Video	Active	Active	Low	VIN + OSD
	No input	Active	Active	High	OSD only
External Sync Select VM0[5, 4] = 10	Video	Active	Active	Low	VIN + OSD
	No input	Inactive (high)	Inactive (high)	High	DC
Internal Sync Select VM0[5, 4] = 11	Video	Active	Active	High	OSD only
	No input	Active	Active	High	OSD only

X = Don't care.

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### Video Timing Generator

The video timing generator is a digital circuit generating all internal and external ( $\overline{\text{VSYNC}}$  and  $\overline{\text{HSYNC}}$ ) timing signals.  $\overline{\text{VSYNC}}$  and  $\overline{\text{HSYNC}}$  can be synchronized to VIN, or run independently of any input when in internal sync mode. The video timing generator can generate NTSC or PAL timing using the same 27MHz crystal (see Figures 4–9).

### Crystal Oscillator

The internal crystal oscillator generates the system clock used by the video timing generator. The oscillator uses a 27MHz crystal or can be driven by an external 27MHz TTL clock at CLKIN. For external clock mode, connect the 27MHz TTL input clock to CLKIN and leave XFB unconnected.

### Display Memory (SRAM)

The display memory stores 480 character addresses that point to the characters stored in the NVM character memory. The content of the display memory is user-programmable through the SPI-compatible serial interface. The display-memory address corresponds to a fixed location on a monitor (see Figure 10). Momentary breakup of the OSD image can be prevented by writing to the display memory during the vertical blanking interval. This can be achieved by using  $\overline{\text{VSYNC}}$  as an interrupt to the host processor to initiate writing to the display memory.

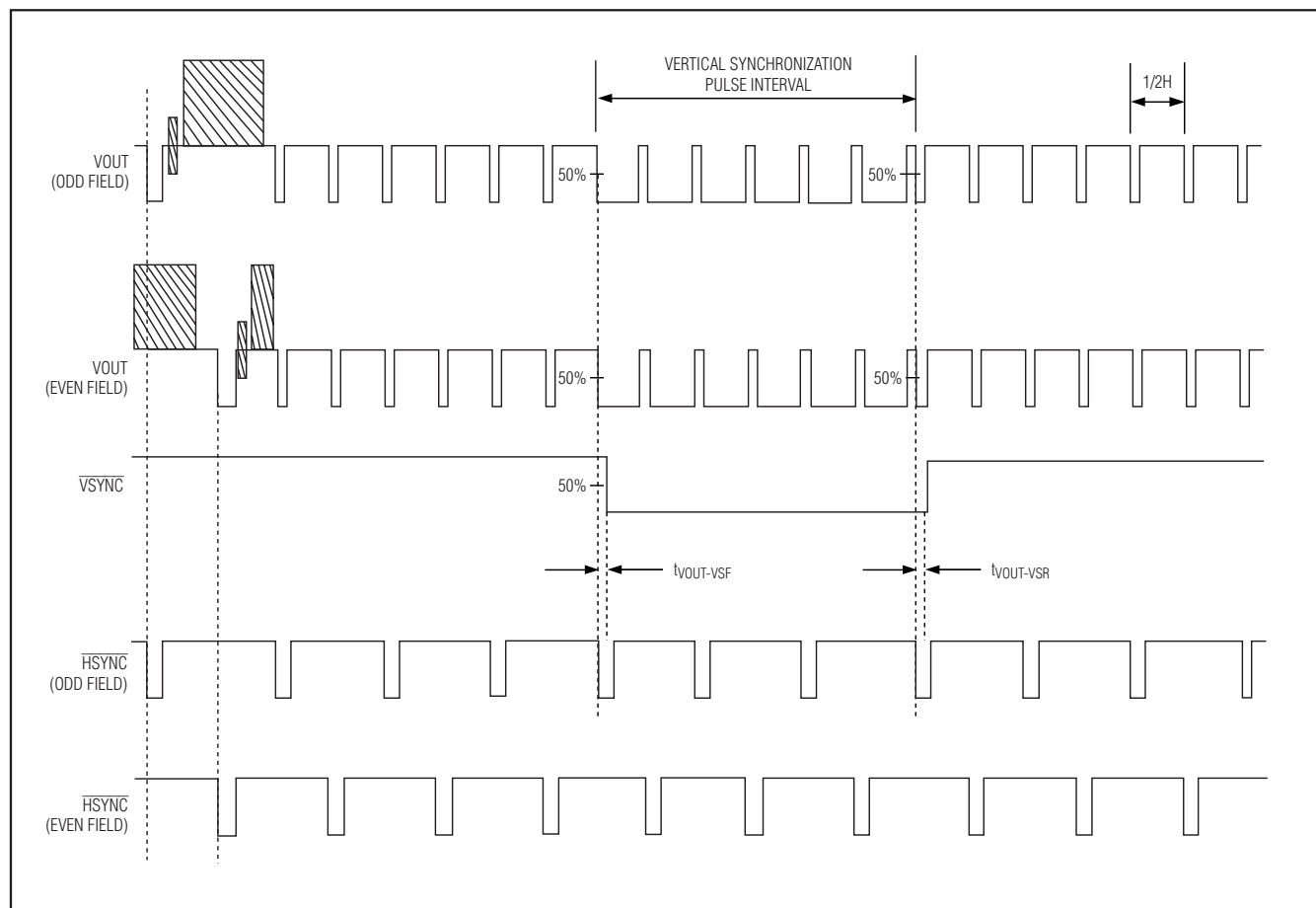


Figure 4. VOUT,  $\overline{\text{VSYNC}}$ , and  $\overline{\text{HSYNC}}$  Timing (NTSC, External Sync Mode)

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

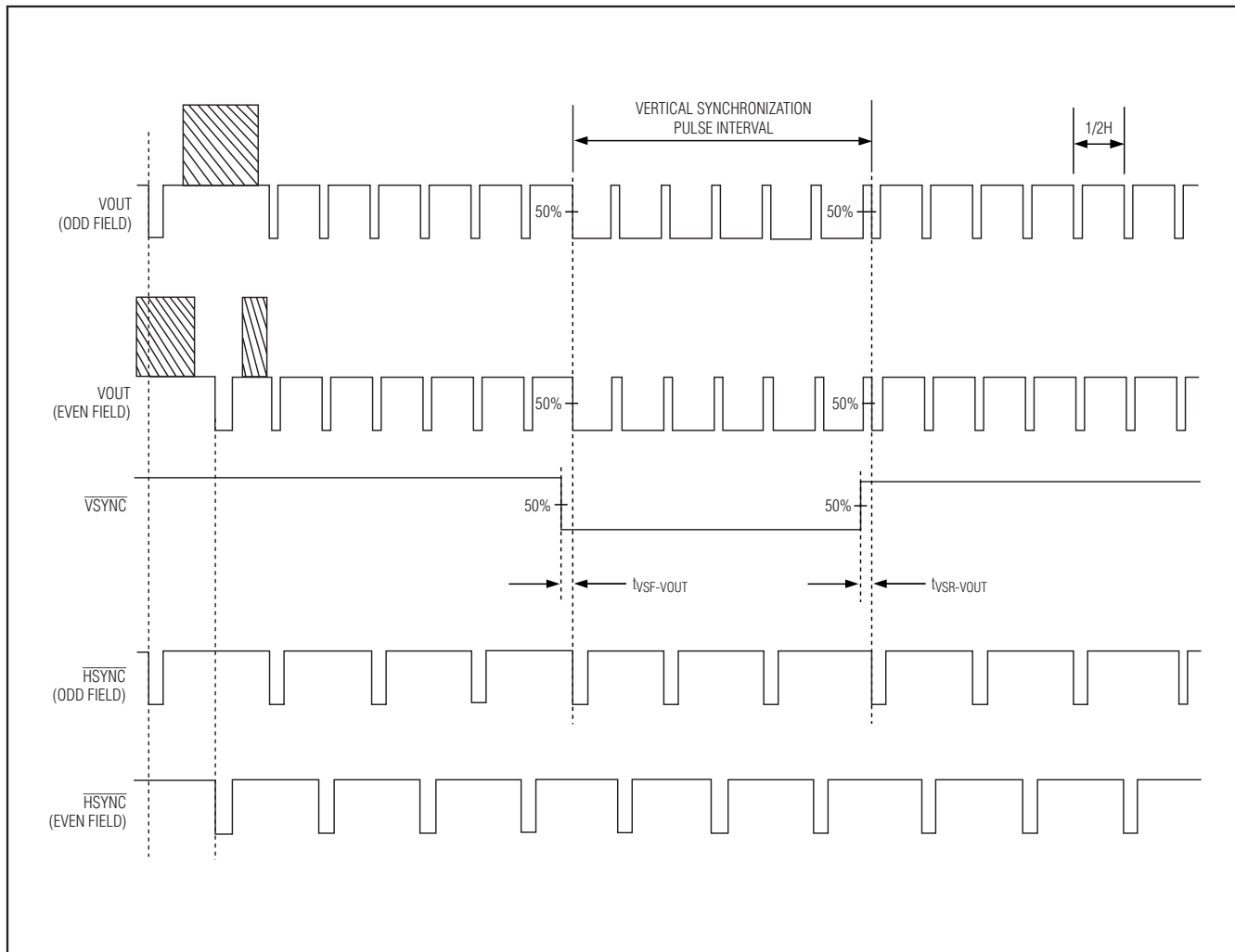


Figure 5. VOUT, VSYNC, and HSYNC Timing (NTSC, Internal Sync Mode)

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

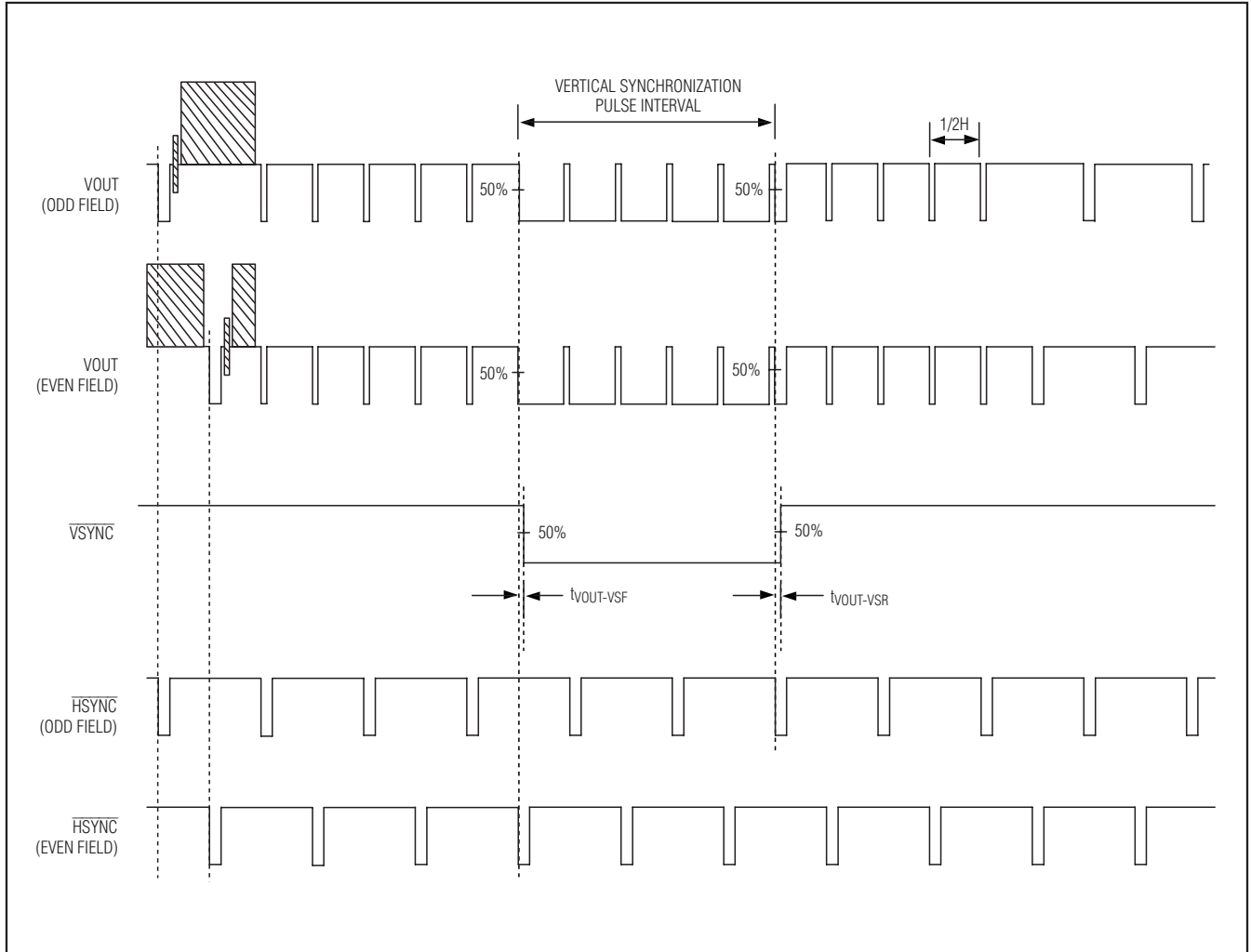


Figure 6. VOUT, VSYNC, and HSYNC Timing (PAL, External Sync Mode)

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

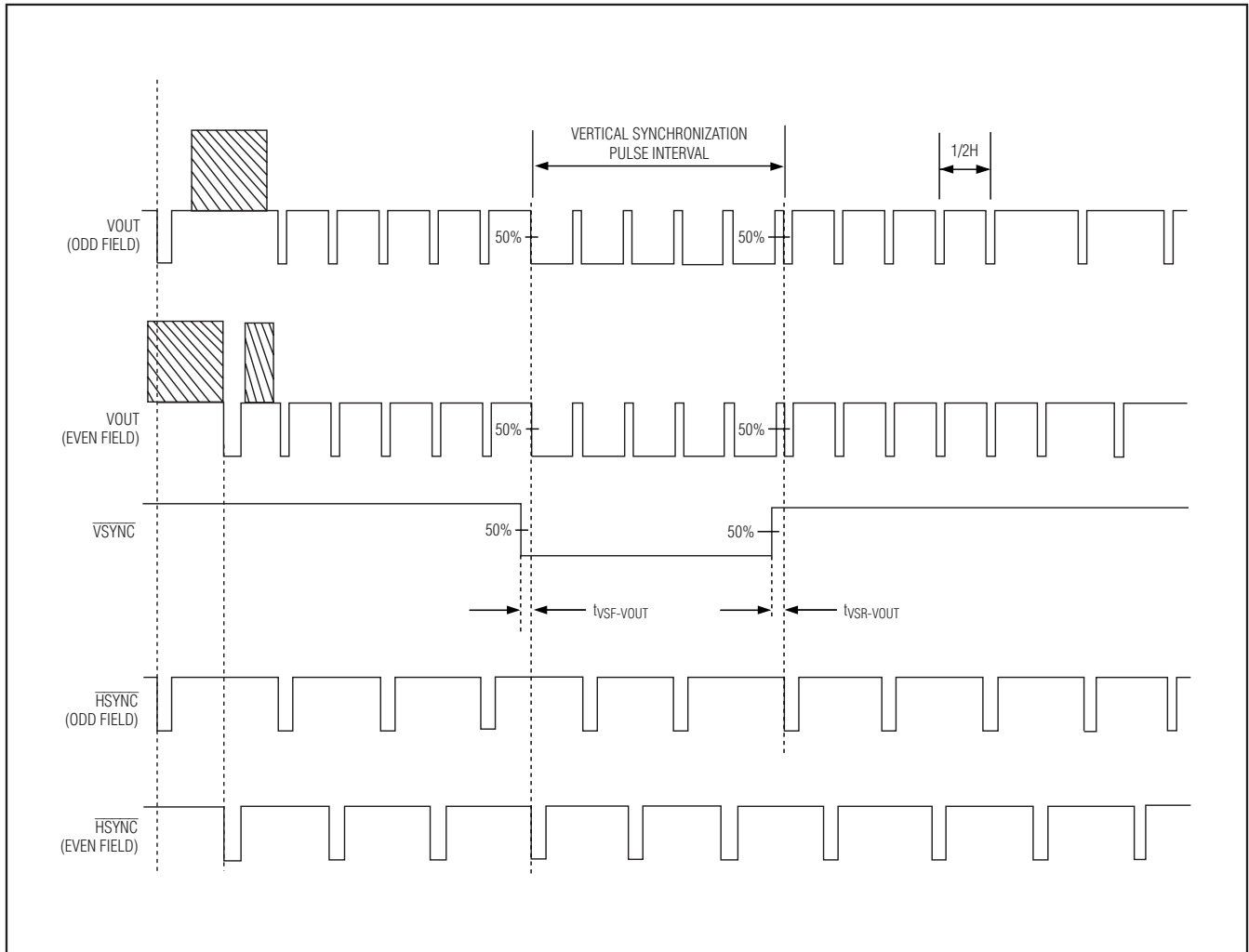


Figure 7. VOUT, VSYNC, and HSYNC Timing (PAL, Internal Sync Mode)



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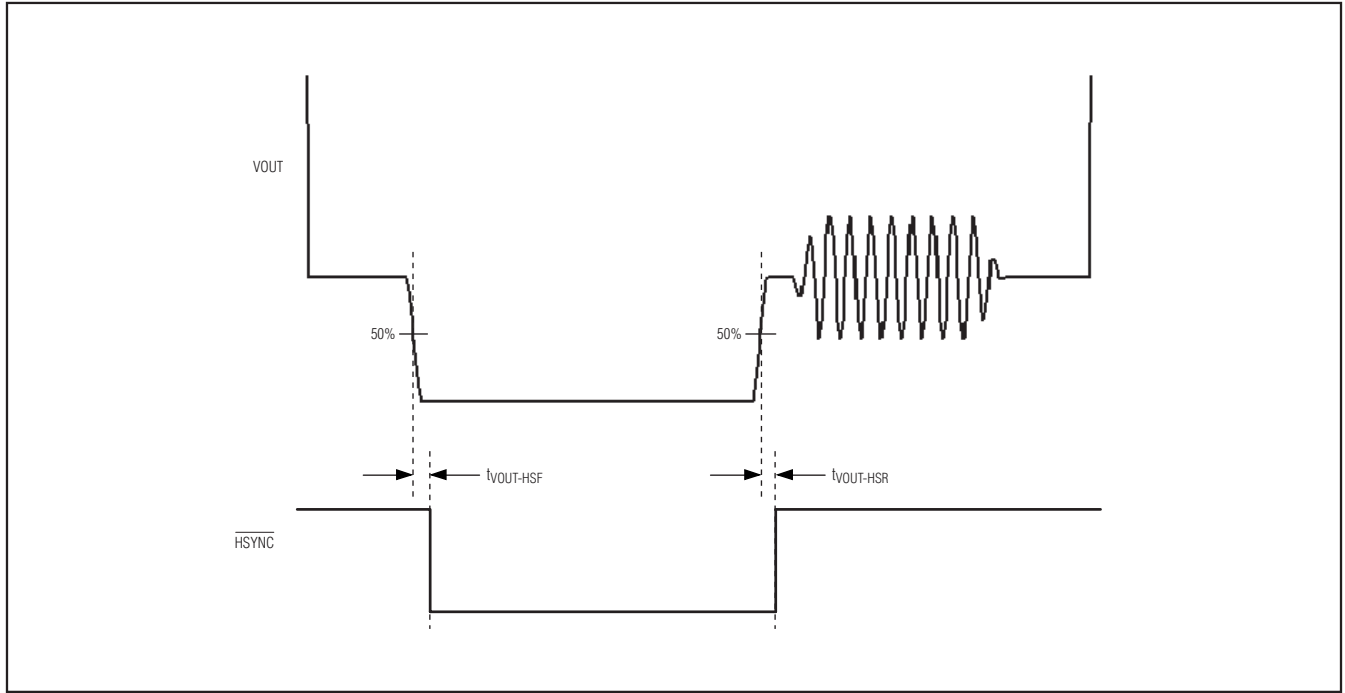


Figure 8. VOUT, and  $\overline{HSYNC}$  Horizontal Sync Timing (NTSC and PAL, External Sync Mode)

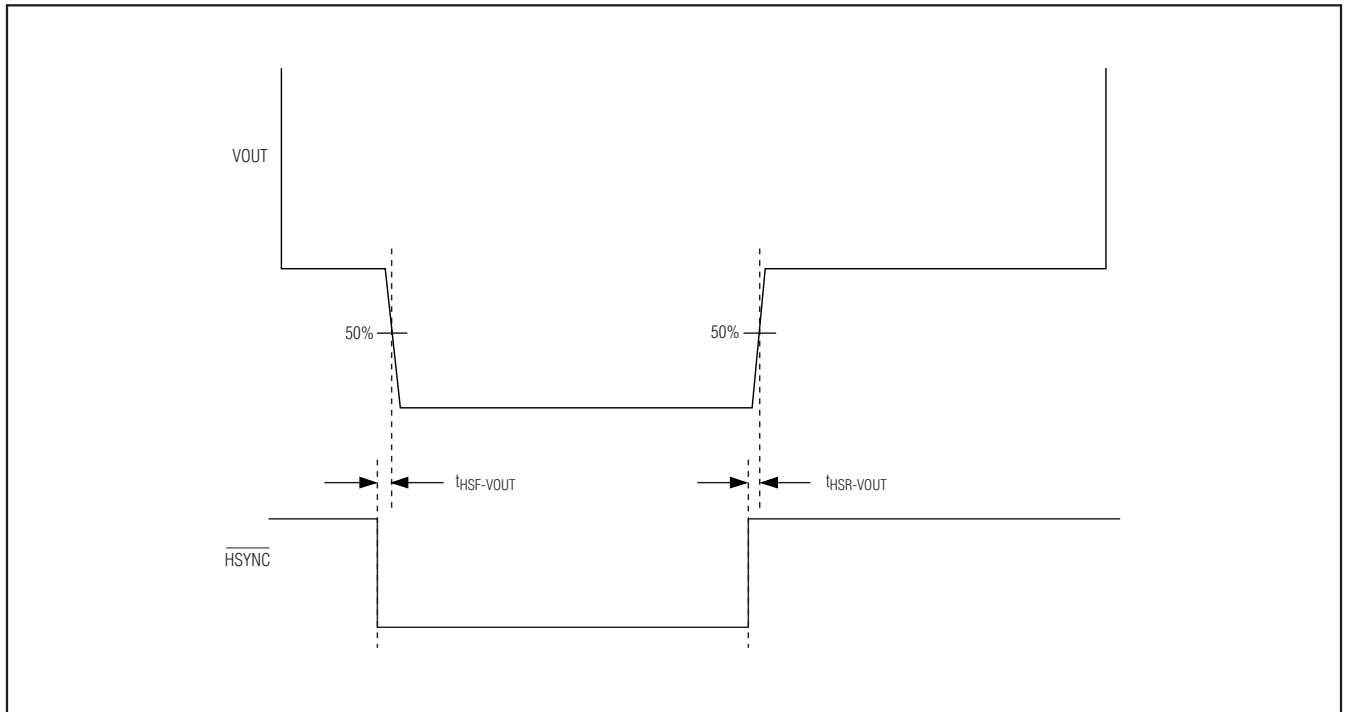


Figure 9. VOUT and  $\overline{HSYNC}$  Horizontal Sync Timing (NTSC and PAL, Internal Sync Mode)

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### Character Memory (NVM)

The character memory is a 256-row x 64-byte wide nonvolatile memory (NVM) that stores the characters or graphic images, and is factory preloaded with the characters shown in Figure 12. The content of the character memory is user-programmable through the SPI-compatible serial interface. Each row contains the description of a single OSD character. Each character consists of 12 horizontal x 18 vertical pixels where each pixel is represented by 2 bits of data having three states: white, black, or transparent. Thus, each character requires 54 bytes of pixel data (Figure 11).

The NVM requires reading and writing a whole character (64 bytes) at a time. This is enabled by an additional

row of memory called the shadow RAM. The 64-byte temporary shadow RAM contains all the pixel data of a selected character (CMAH[7:0]) and is used as a buffer for read and write operations to the NVM (Figure 13). Accessing the NVM is always through the shadow RAM, and is thus a two-step process. To write a character to the NVM, the user first fills the shadow RAM using 54 8-bit SPI write operations, and then executes a single shadow RAM write command. Similarly, reading a character's pixel values requires first reading a character's pixel data into the shadow RAM, and then reading the desired pixel data from the shadow RAM to the SPI port.

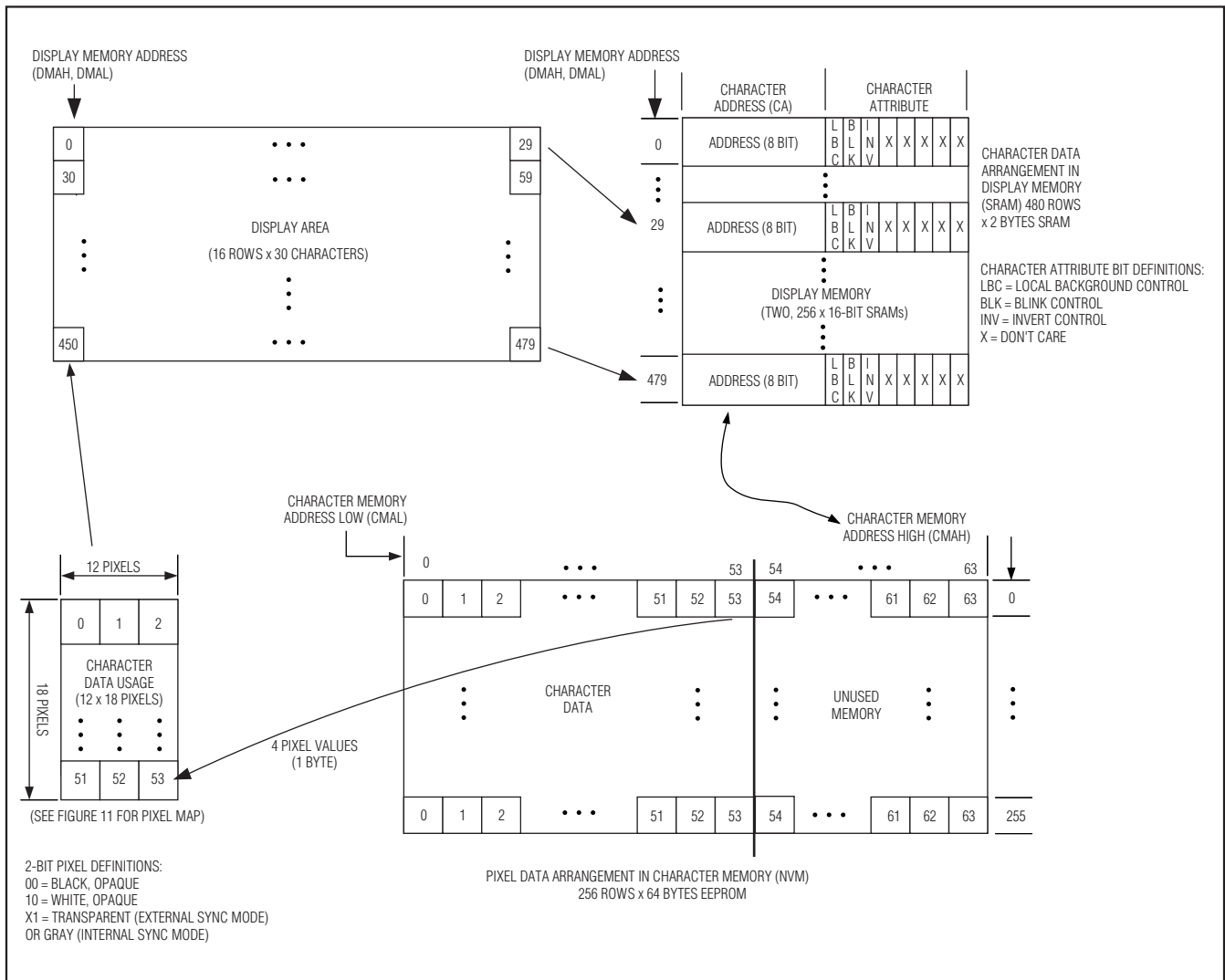


Figure 10. Definitions of Various Parameters

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

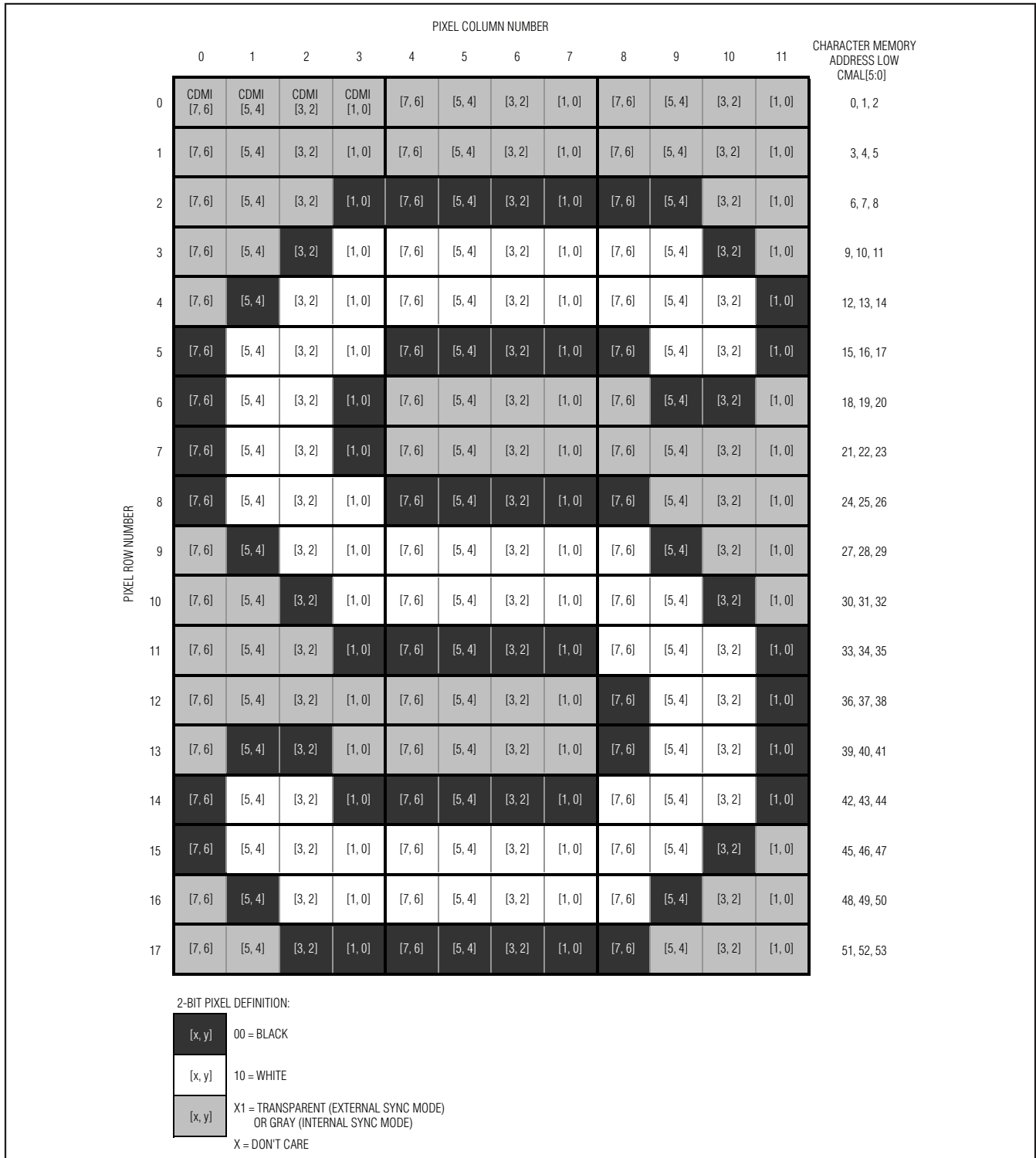


Figure 11. Character Data Usage (Pixel Map)

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

		CA[3:0], CMAH[3:0]															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
CA[7:4], CMAH[7:4]	0	█	1	2	3	4	5	6	7	8	9	0	A	B	C	D	E
	1	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U
	2	U	W	X	Y	Z	a	b	c	d	e	f	g	h	i	j	k
	3	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z	(
	4	)	.	?	;	:	,	'	/	"	-	<	>	@	ア	イ	ウ
	5	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ	タ	チ	ツ	テ
	6	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ	マ	ミ	ム	メ	モ
	7	ヤ	ユ	ヨ	ラ	リ	ル	ロ	ワ	ン	ビ	ブ	ポ	ピ	ボ	グ	
	8	ズ	ダ	デ	ト	ャ	ュ	ョ	ッ	ぁ	ぃ	ぅ	え	お	が	き	く
	9	け	こ	さ	し	す	せ	そ	た	ち	つ	て	と	な	に	ぬ	ね
	A	の	は	ひ	ふ	へ	ほ	ま	み	む	め	も	や	ゆ	よ	ら	り
	B	る	れ	ろ	わ	を	ん	が	ご	だ	づ	ぞ	ど	や	ゆ	よ	っ
	C	再	生	早	巻	戻	年	月	日	火	水	木	金	土	主	副	声
	D	音	色	濃	淡	開	始	終	了	時	刻	確	認	計	押	停	止
	E	入	力	出	質	操	作	方	法	使	用	曜	量	■	[	■	■
	F	■	■	■	]	■	☼	☼	☾	☾	☼	☼	☼	☼	☼	☼	☼

Figure 12. Character Address Map (Default Character Set)

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## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

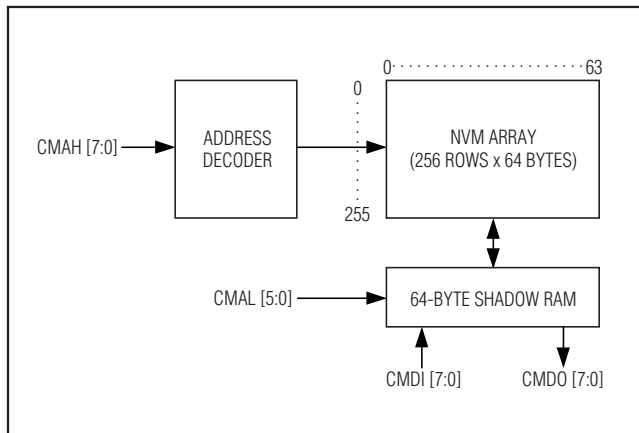


Figure 13. NVM Structure

### On-Screen Display (OSD) Generator

The OSD generator sets each pixel amplitude based on the content of the character memory and Row Brightness registers (RB0–RB15).

### OSD Insertion Mux

The OSD insertion mux selects between an OSD pixel and the input video signal. The OSD image sharpness is controlled by the OSD Rise and Fall Time bits, and the OSD Insertion Mux Switching Time bits, found in the OSD Insertion Mux (OSDM) register. This register controls the trade-off between OSD image sharpness and crosscolor/crossluma artifacts. Lower time settings produce sharper pixels, but potentially greater crosscolor/crossluma artifacts. The optimum setting depends on the requirements of the application and, therefore, can be set by the user.

### Video-Driver Output

The MAX7456 includes a video-driver output with a gain of 2. The driver has a maximum of 2.4V<sub>P-P</sub> output swing and a 6MHz large signal bandwidth ( $\leq 0.2$ dB attenuation). The driver output is capable of driving two 150 $\Omega$  standard video loads.

### Sag Correction

Sag correction is a means of reducing the electrical and physical size of the output coupling capacitor while achieving acceptable line-time distortion. Sag correction refers to the low frequency compensation of the highpass filter formed by the 150 $\Omega$  load of a back-terminated coaxial cable and the output coupling capacitor. This breakpoint must be low enough in frequency to pass the vertical sync interval ( $< 25$ Hz for PAL and  $< 30$ Hz for NTSC) to avoid field tilt. Traditionally, the breakpoint is made  $< 5$ Hz, and the coupling capacitor

must be very large, typically  $> 330\mu\text{F}$ . The MAX7456 reduces the value of this capacitor, replacing it with two smaller capacitors ( $C_{\text{OUT}}$  and  $C_{\text{SAG}}$ ), substantially reducing the size and cost of the coupling capacitors while achieving acceptable line-time distortion (Table 2). Connect SAG to VOUT if not used.

Table 2. SAG-Correction Capacitor Values

$C_{\text{OUT}}$ ( $\mu\text{F}$ )	$C_{\text{SAG}}$ ( $\mu\text{F}$ )	LINE-TIME DISTORTION (% typ)
470	—	0.2
100	—	0.4
100	22	0.3
47	47	0.3
22	22	0.4
10	10	0.6

### Serial Interface

The SPI-compatible serial interface programs the operating modes and OSD data. Read capability permits write verification and reading the Status (STAT), Display Memory Data Out (DMDO), and Character Memory Data Out (CMDO) registers.

### Read and Write Operations

The MAX7456 supports interface clocks (SCLK) up to 10MHz. Figure 15 illustrates writing data and Figure 16 illustrates reading data from the MAX7456. Bring  $\overline{\text{CS}}$  low to enable the serial interface. Data is clocked in at SDIN on the rising edge of SCLK. When  $\overline{\text{CS}}$  transitions high, data is latched into the input register. If  $\overline{\text{CS}}$  goes high in the middle of a transmission, the sequence is aborted (i.e., data does not get written into the registers). After  $\overline{\text{CS}}$  is brought low, the device waits for the first byte to be clocked into SDIN to identify the type of data transfer being executed.

The SPI commands are 16 bits long with the 8 most significant bits (MSBs) representing the register address and the 8 least significant bits (LSBs) representing the data (Figures 15 and 16). There are two exceptions to this arrangement:

- 1) Auto-increment write mode used for display memory access is a single 8-bit operation (Figure 21). When performing the auto-increment write for the display memory, the 8-bit address is internally generated, and only 8-bit data is required at the serial interface.
- 2) Reading character data from the display memory, when in 16-bit operation mode, is a 24-bit operation (8-bit address plus 16-bit data). See Figure 20.

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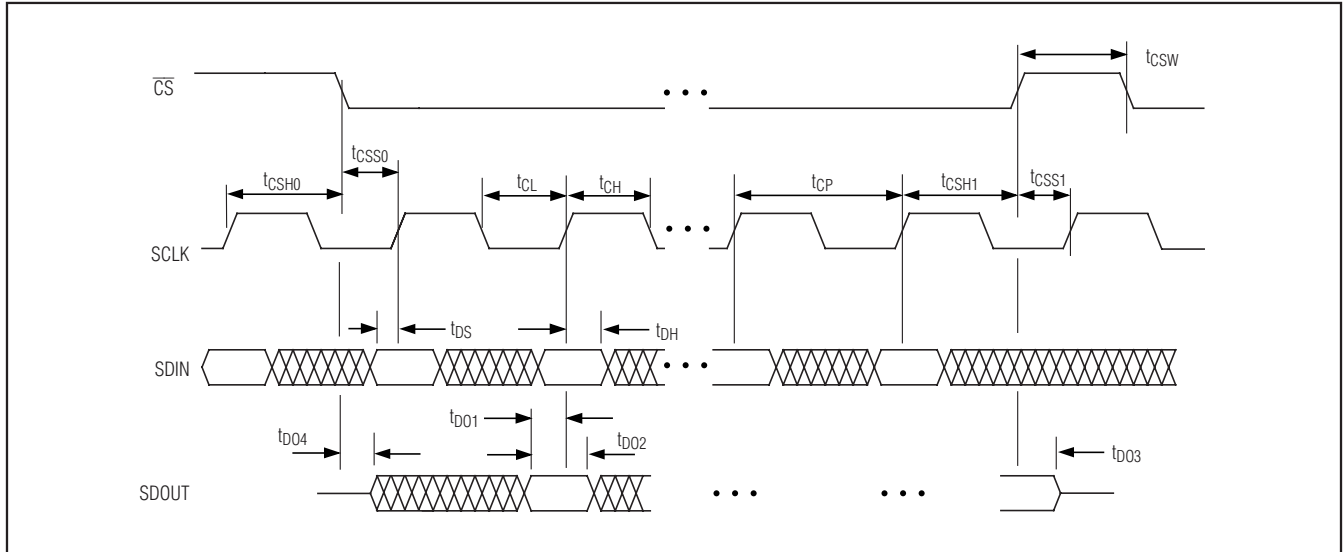


Figure 14. Detailed Serial-Interface Timing

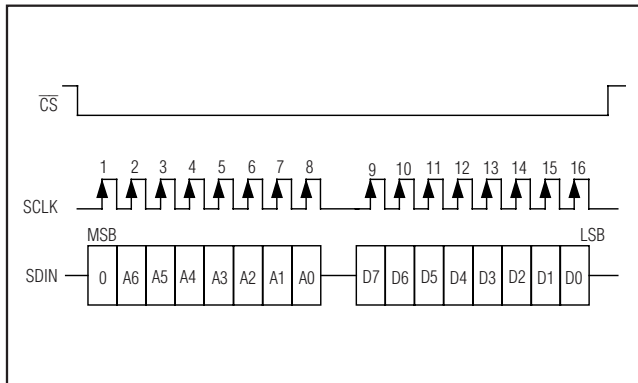


Figure 15. Write Operation

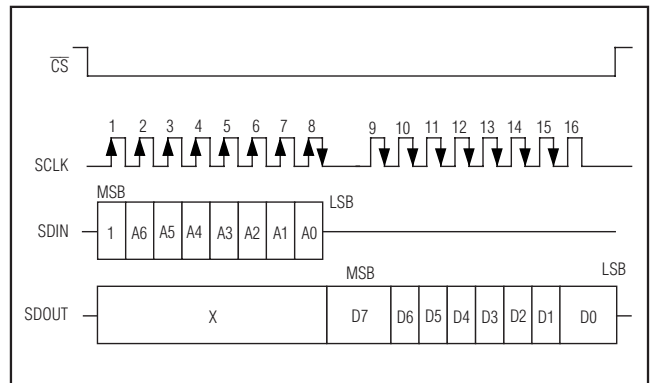


Figure 16. Read Operation

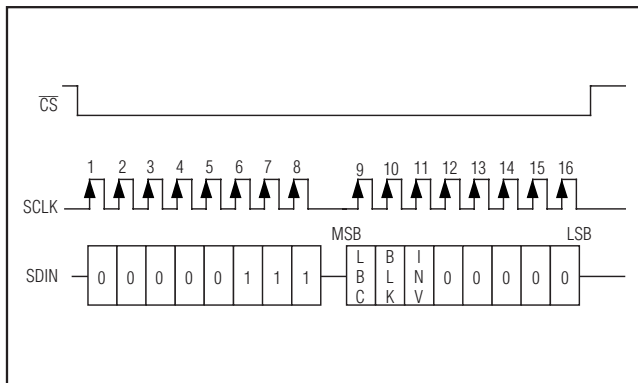


Figure 17. Writing Character Attribute Byte in 8-Bit Operation Mode

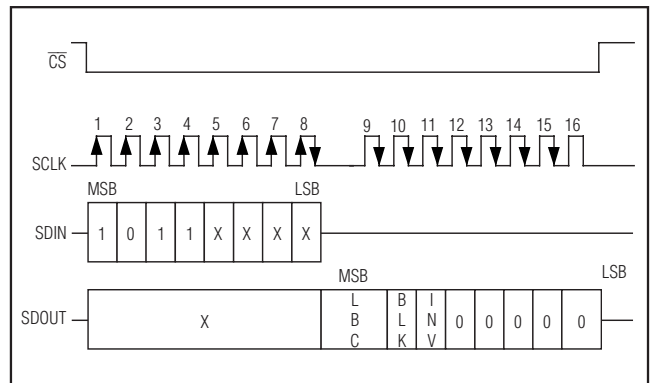


Figure 18. Reading Character Attribute Byte in 8-Bit Operation Mode

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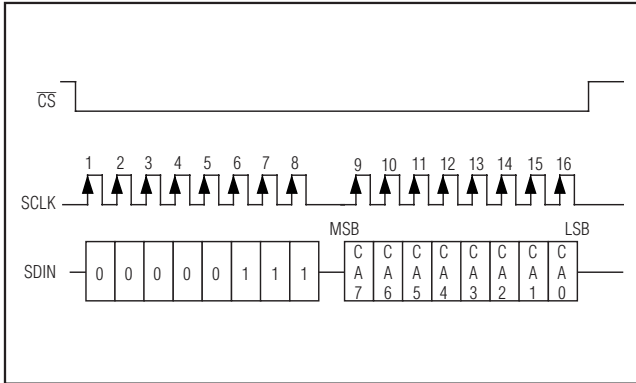


Figure 19. Writing Character Address Byte in 8-Bit and 16-Bit Operation Modes

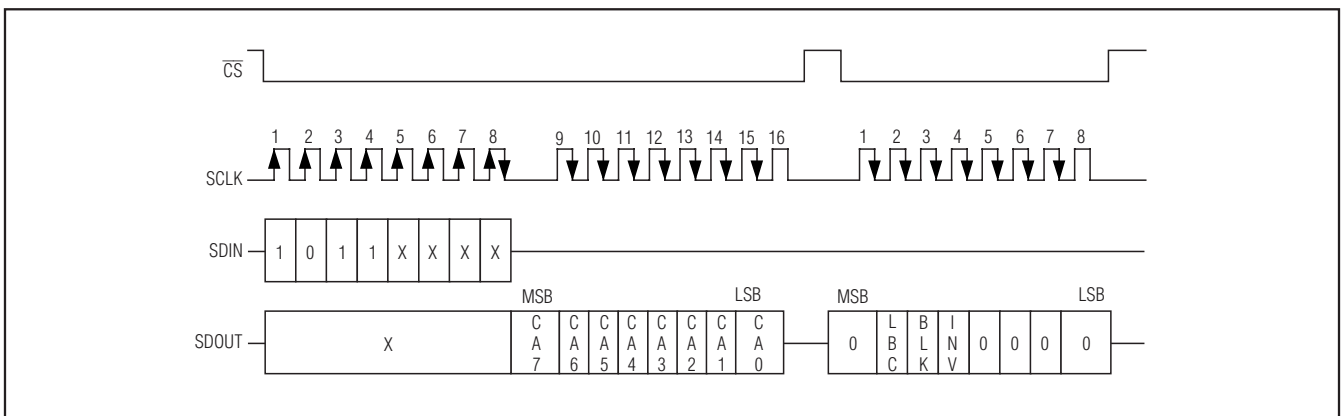


Figure 20. Reading Character Address and Character Attribute Bytes in 16-Bit Operation Mode

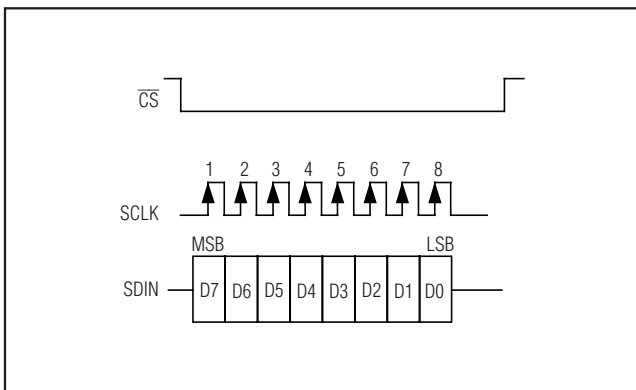


Figure 21. Write Operation in Auto-Increment Mode

### Resets

#### Power-On Reset

The MAX7456's power-on reset circuitry (POR) provides an internal reset signal that is active after the supply voltage has stabilized. The internal reset signal resets all registers to their default values and clears the display memory. The register reset process requires 100µs, and to avoid unexpected results, read/write activity is not allowed during this interval. The display memory is reset, and the OSD is enabled typically 50ms after the supply voltage has stabilized and a stable 27MHz clock is available. The user should avoid SPI operations during this time to avoid unexpected results. After 50ms (typical), STAT[6] can be polled to verify that the reset sequence is complete (Figure 22).

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

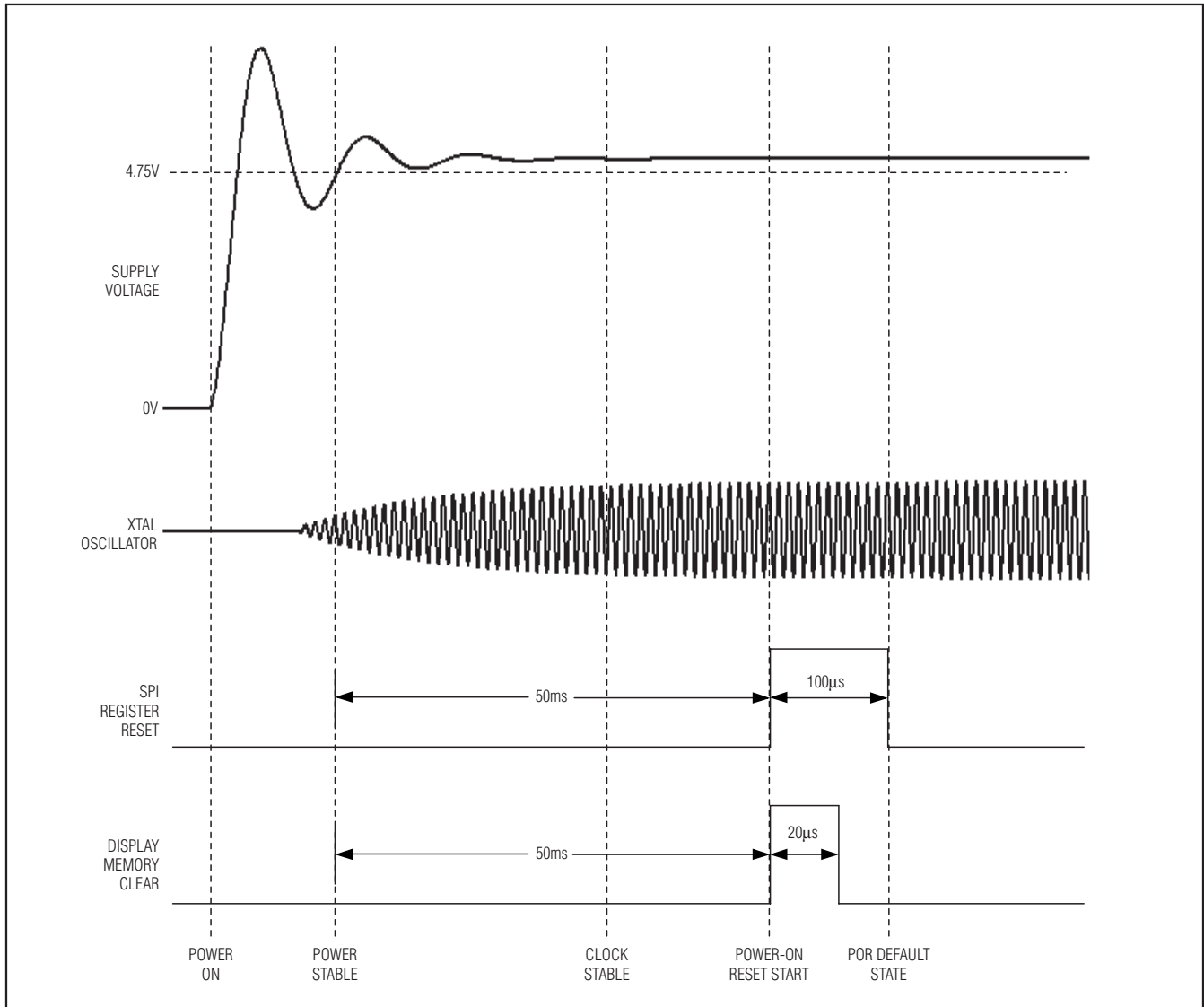


Figure 22. Power-On Reset Sequence

### Software Reset

The MAX7456 features a Software Reset bit (VM0[1]) that, when set high, clears the display memory and resets all registers to their default values except the OSD Black Level register (OSDBL). After 100µs (typical), STAT[6] can be polled to verify that the reset process is complete.

### Hardware Reset

The MAX7456 provides a hardware reset input ( $\overline{\text{RESET}}$ ) that functions the same as the POR. All registers are

reset to their default values and are not accessible for reading/writing when  $\overline{\text{RESET}}$  is driven low. The resetting process requires a  $\geq 50\text{ms}$  wide  $\overline{\text{RESET}}$  pulse, and no other activities are allowed during this interval. All SPI registers are reset to their default values 100µs after the rising edge of  $\overline{\text{RESET}}$ . The display memory is reset to its default value of 00H in all locations 20µs after the rising edge of  $\overline{\text{RESET}}$ .  $\overline{\text{RESET}}$  takes precedence over the Software Reset bit. After  $\overline{\text{RESET}}$  has been deasserted, STAT[6] can be polled to verify that the reset sequence is complete.



# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### MAX7456 Register Description

Access to all MAX7456 operations, including display-memory and character-memory access, are through the SPI registers listed in Table 3. There is no direct access to the display and character memories through the SPI port. See the *Applications Information* section

for step-by-step descriptions of the SPI operations needed to access the memories.

The register format used in this data sheet is REGISTER\_NAME [BIT\_NUMBERS]. For example, bit 1 in Video Mode 0 register is written as VM0[1].

**Table 3. Register Map**

WRITE ADDRESS	READ ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
00H	80H	VM0	Video Mode 0
01H	81H	VM1	Video Mode 1
02H	82H	HOS	Horizontal Offset
03H	83H	VOS	Vertical Offset
04H	84H	DMM	Display Memory Mode
05H	85H	DMAH	Display Memory Address High
06H	86H	DMAL	Display Memory Address Low
07H	87H	DMDI	Display Memory Data In
08H	88H	CMM	Character Memory Mode
09H	89H	CMAH	Character Memory Address High
0AH	8AH	CMAL	Character Memory Address Low
0BH	8BH	CMDI	Character Memory Data In
0CH	8CH	OSDM	OSD Insertion Mux
10H	90H	RB0	Row 0 Brightness
11H	91H	RB1	Row 1 Brightness
12H	92H	RB2	Row 2 Brightness
13H	93H	RB3	Row 3 Brightness
14H	94H	RB4	Row 4 Brightness
15H	95H	RB5	Row 5 Brightness
16H	96H	RB6	Row 6 Brightness
17H	97H	RB7	Row 7 Brightness
18H	98H	RB8	Row 8 Brightness
19H	99H	RB9	Row 9 Brightness
1AH	9AH	RB10	Row 10 Brightness
1BH	9BH	RB11	Row 11 Brightness
1CH	9CH	RB12	Row 12 Brightness
1DH	9DH	RB13	Row 13 Brightness
1EH	9EH	RB14	Row 14 Brightness
1FH	9FH	RB15	Row 15 Brightness
6CH	ECH	OSDBL	OSD Black Level
—	AxH	STAT	Status
—	BxH	DMDO	Display Memory Data Out
—	CxH	CMDO	Character Memory Data Out

X = Don't care.

# MAX7456

## Single-Channel Monochrome On-Screen Display with Integrated EEPROM

### Video Mode 0 Register (VM0)

Write address = 00H, read address = 80H.

Read/write access: unrestricted.

To write to this register, the following conditions must be met:

- 1) STAT[5] = 0, the character memory (NVM) is not busy.
- 2) DMM[2] = 0, the display memory (SRAM) is not in the process of being cleared.

BIT	DEFAULT	FUNCTION
7	0	Don't Care
6	0	Video Standard Select 0 = NTSC 1 = PAL
5, 4	00	Sync Select Mode (Table 1) 0x = Autosync select (external sync when LOS = 0 and internal sync when LOS = 1) 10 = External 11 = Internal
3	0	Enable Display of OSD Image 0 = Off 1 = On
2	0	Vertical Synchronization of On-Screen Data 0 = Enable on-screen display immediately 1 = Enable on-screen display at the next VSYNC
1	0	Software Reset Bit When this bit is set, all registers are set to their default values and the display memory is cleared. When a stable 27MHz clock is present, this bit is automatically cleared internally after typically 100µs. The user does not need to write a 0 afterwards. SPI operations should not be performed during this time or unpredictable results may occur. The status of the bit can be checked by reading this register after typically 100µs. This register is not accessible for writing until the display memory clear operation is finished (typically 20µs).
0	0	Video Buffer Enable 0 = Enable 1 = Disable (VOUT is high impedance)

X = Don't care.