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MAX77278

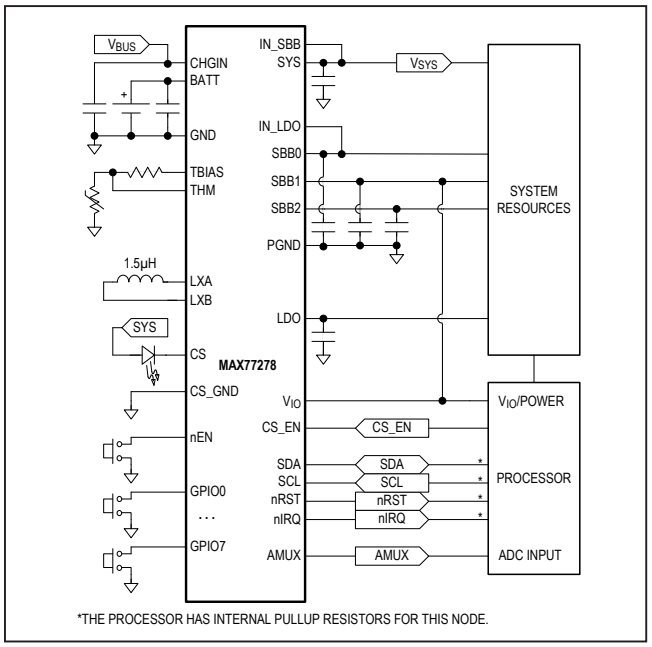
Ultra-Low Power PMIC with 3-Output SIMO, Power Path Charger Optimized for Small Li+, 425mA Current Sink, and 8 GPIO

General Description

The MAX77278 provides highly-integrated battery charging and power supply solutions for low-power applications where size and efficiency are critical. The device features a single-inductor multiple-output (SIMO) buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. A 50mA LDO provides ripple rejection for audio and other noise-sensitive applications. A highly-configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA).

The device includes other features such as a programmable current sink that can be used to drive an IR-LED, 8 general-purpose input/output (GPIO) control pins, and an analog multiplex (AMUX) output that provides access to useful battery charging signals. A bidirectional I²C interface allows for configuring and checking the status of the device. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality when the device is on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Simplified Application Circuit



Benefits and Features

- Highly Integrated
  - Smart Power Selector™ Li+/Li-Poly Charger
  - Three Output, SIMO Buck-Boost Regulator
  - 50mA LDO
  - Programmable 250mA to 425mA Current Sink Driver
  - Analog MUX Output for Power Monitoring
  - Eight GPIOs (Configured for One-Button Wake-Up and Two-Button Shutdown)
- Low Power
  - 0.3µA Standby Current
  - 16µA Operating Current
- Charger Optimized for Small Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Flexible and Configurable
  - I²C-Compatible Interface
  - Eight GPIOs
  - Factory OTP Options Available
- Small Size
  - 3.15mm x 2.15mm x 0.7mm
  - 35-Bump, 0.4mm-Pitch, 7x5 Ball Array, WLP
  - Small Total Solution Size (24mm²)

Applications

- Remote Controls
- Wearables
- Internet of Things (IoT)

Ordering Information appears at end of data sheet.

19-100167; Rev 2; 7/18

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Absolute Maximum Ratings

CHGIN to AGND ..... -0.3V to +30.0V
SCL, SDA to AGND ..... -0.3V to V_{IO} + 0.3V
SYS, BATT to AGND ..... -0.3V to +6.0V
IN_SBB, GPIO0-7 to AGND ..... -0.3V to V_{SYS} + 0.3V
CS_EN, nEN, nRST, nIRQ, to AGND ..... -0.3V to V_{SYS} + 0.3V
THM, TBIAS, V_L to AGND ..... -0.3V to +6.0V
LDO to AGND (Note 1) ..... -0.3V to V_{IN_LDO} + 0.3V
CS to CS_GND ..... -0.3V to +6.0V
IN_SBB to PGND ..... -0.3V to +6.0V
BST to LXB ..... -0.3V to +6.0V
CS_GND, PGND to AGND ..... -0.3V to +0.3V
V_{IO} to AGND ..... -0.3V to V_{SYS} + 0.3V
BST to IN_SBB ..... -0.3V to +6.0V
SBB0, SBB1, SBB2 to PGND (Note 1) ..... -0.3V to +6.0V
IN_LDO to AGND ..... -0.3V to +6.0V
nEN, nIRQ, nRST, SDA, SCL, GPIO0-7 Continuous Current ..... ±20mA
CHGIN Continuous Current ..... $1.2A_{RMS}$
SYS Continuous Current ..... $1.2A_{RMS}$
BATT Continuous Current (Note 2) ..... $1.2A_{RMS}$
LXA Continuous Current (Note 3) ..... $1.2A_{RMS}$
LXB Continuous Current (Note 4) ..... $1.2A_{RMS}$
SBB0, SBB1, SBB2 Short-Circuit Duration ..... Continuous
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 20.4mW/°C above +70°C) 1632mW

Note 1: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.

Note 2: Do not repeatedly hot-plug a source to the BATT terminal at a rate greater than 10Hz. Hot plugging low-impedance sources results in an ~8A momentary (~2µs) current spike.

Note 3: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.

Note 4: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} +0.3V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

35 WLP 0.4mm Pitch

PACKAGE CODE	W352C3+1
Outline Number	21-100152
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics—Global Resources

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into BATT, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, CS), T_A = +25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3		µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1		
		Current measured into BATT, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, CS), T_A = +25°C	Main bias is on in normal mode (SBIA_EN = 1, SBIA_LPM = 0)		28		
Quiesent Supply Current	I_Q	Current measured into BATT, IN_SBB, and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. CS is disabled.	Main bias is in low-power mode (SBIA_LPM = 1)		13		µA
			Main bias is in normal mode (SBIA_LPM = 0)		48		
Main Bias Enable Time	t_{SBIAS_EN}				0.5		ms
VOLTAGE MONITORS/POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.65	1.9	2.15	V
POR Threshold Hysteresis					100		mV
VOLTAGE MONITORS/UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.4	2.6	2.8	V
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
VOLTAGE MONITORS/OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.65	5.85	6.05	V
THERMAL MONITORS							
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN Falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_R}$	nEN Rising			V_{SYS} - 0.9	V_{SYS} - 0.6	V
Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
Manual Reset Time	t_{MRST}			14	16	20	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	C_{nIRQ} = 25pF			2		ns
Leakage Current	I_{nIRQ_LKG}	V_{SYS} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
		V_{SYS} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 and Figure 7 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{SYS} = 3.8V				0.3 X V_{SYS}	V
Input Voltage High	V_{IH}	V_{SYS} = 3.8V		0.7 x V_{SYS}			V
Input Leakage Current	I_{GPI_LKG}	DIRx = 1, V_{SYS} = 5.5V, V_{GPIOx} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 8mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 8mA		0.8 x V_{SYS}			V
Input Debounce Time	t_{DBNC_GPI}	DB_CNFG[1:0] = 0b00			1.25		ms
		DB_CNFG[1:0] = 0b01			2.5		
		DB_CNFG[1:0] = 0b10			5		
		DB_CNFG[1:0] = 0b11			10		
GPIO Manual Reset Time	t_{MRST_GPIO}	GPIO_MRT[1:0] = 0b00			10		s
		GPIO_MRT[1:0] = 0b01			5		
		GPIO_MRT[1:0] = 0b10			2.5		
		GPIO_MRT[1:0] = 0b11			1.25		
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6			2.56		ms

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER/DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC Rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage-Lockout Hysteresis				500		mV
Input Current-Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA
Input Current-Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0]	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms
CHARGER/SUPPLY AND QUIESCENT CURRENTS						
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		5		µA
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0A			50	µA
CHGIN Suspend Supply Current	$I_{CHGIN-SUS}$	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)			50	µA
CHARGER/PREQUALIFICATION						
Charge and Input Current-Limit Soft-Start Slew Time		Zero to full scale		1		ms

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prequalification Voltage Threshold Range	V_{PQ}	Charger is in prequalification mode when V_{BATT} < V_{PQ}, this threshold has 100mV of hysteresis, programmable in 100mV steps with CHG_PQ[2:0]	2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V	-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 0		10		%
		V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V	27	30	33	minutes
CHARGER/FAST-CHARGE						
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]	3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]	7.5		300	mA
Fast-Charge Current Accuracy		T_A= +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV, $I_{FAST-CHG}$ = 15mA	-1.5		+1.5	%
		T_A= +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV, $I_{FAST-CHG}$ = 300mA	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV T_A = 0°C to +85°C	-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], from prequal done to timerfault	3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours	-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, loading conditions and/or a weak charging source caused charge current to drop below this threshold, expressed as a percentage of $I_{FAST-CHG}$		20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG_SET[2:0]	60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise		-5.4		%/°C

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER/TERMINATION AND TOP-OFF						
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)		5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)		7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		10		
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)		15		
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C	1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C	27	30	33	
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]	0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes	-10		+10	%
CHARGER/DEVICE ON-RESISTANCE AND LEAKAGE						
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS		100		mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = +25°C, charger disabled		0.1	1.0	µA
		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = +85°C, charger disabled		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V, I_{CHGIN} = $I_{CHGIN-LIM}$ = 450mA		600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +25°C, body-switched diode is reverse biased		0.1	1.0	µA
		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +85°C, body-switched diode is reverse biased		1		
CHARGER/SYSTEM NODE						
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]	4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = +25°C	4.41	4.50	4.59	V
		$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = -40°C to +85°C	4.365	4.500	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, V_{SYS} < $V_{SYS-REG}$ due to I_{CHGIN} = $I_{CHGIN-LIM}$ (input in current limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)	4.34	4.40	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA		V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS}= 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5°C increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5°C increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5°C increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5°C increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTCβ = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTCβ = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs						
Full-Scale Voltage	V_{FS}			1.25		V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting		0.26		V/V
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/CHGIN POWER						
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting		2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}		0.167		V/V

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/BATT MONITOR							
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CHG_CC[5:0])			12.5		mV/%
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA	T_A = 0°C to +85°C	-0.5		+0.8	mA
			T_A = -40°C	-1.1		+1.4	
Battery-Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/ANALOG MULTIPLEXER							
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/THM AND TBIAS							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.8V, V_{IN_SBB} = 3.8V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_SBB}			2.8	3.8	5.5	V
Shutdown Current (Note 5)		SBB0, SBB1, SBB2 are disabled, V_{SYS} = V_{IN_SBB} = 5.5V, V_{LXA} = 0V	T_A = +25°C		0.05	1	µA
			T_A = 0°C to +85°C		0.25		
SIMO Quiescent Supply Current (Note 5)	I_{Q_SBB0}	No load	SBB0 set to 5.3V		5.0		µA
	I_{Q_SBB1}		SBB1 set to 1.9V		3.0		
	I_{Q_SBB2}		SBB2 set to 3.2V		4.5		
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB0)							
Minimum Output Voltage				2.35			V
Maximum Output Voltage						5.5	V
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage				1.412			V
Maximum Output Voltage						2.2	V
Output DAC Bits					6		bits
Output DAC LSB Size					12.5		mV
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage				0.85			V
Maximum Output Voltage						4	V
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
STATIC OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		T_A = 0°C to +85°C (Note 6)		-4		+4	%
TIMING CHARACTERISTICS							
Soft-Start Ramp Rate	dV/dt_{SS}			2	5.0	8	mV/µs

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.8V, V_{IN_SBB} = 3.8V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	µA
			T_A = +85°C		+0.1		
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	µA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 7)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 5: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the quiescent supply current specification.

Note 6: Measured as the falling threshold of the output voltage where LXA switches high.

Note 7: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms for more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.8V, V_{IN_LDO} = 5.3V, V_{LDO} = 5.14V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	Note 8		3.733		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 9)			0.1	1	µA
LDO Quiescent Supply Current (Note 9)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO} = 0mA, LDO output enabled and in regulation, V_{IN_LDO} = 5.5V, V_{LDO} = 5.1375V			1.1	3.1	µA
Fixed Headroom Control Quiescent Current	I_{Q_FHC}	Additional current into SYS due to fixed headroom controller, V_{LDO} = 5.1375V, EN_FHC = 1			1.8	3.0	µA
Maximum Output Current	I_{OUT}			50			mA
Current Limit		V_{LDO} programmed to 5.1375V, V_{LDO} externally forced to 4.6375V			322		mA
Output Capacitance	C_{OUT}	Effective, derated capacitance. ESR must be less than 10mΩ, ESL must be less than 200pH		4	10	13	µF
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		3.7125		5.3000	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Output Voltage Accuracy		V_{LDO} programmed from 4V to 5.1375V, V_{IN_LDO} = 5.3V,LDO not in dropout, I_{LDO} = 0mA to 20mA, T_A = 0°C to +85°C		-2		+2	%
FHC Headroom Voltage	V_{HDRM}	V_{LDO} = 5.175V, I_{LDO} = 20mA, EN_FHC = 1	V_HDRM[1:0] = 0b00		150		mV
			V_HDRM[1:0] = 0b01		175		
			V_HDRM[1:0] = 0b10		200		
			V_HDRM[1:0] = 0b11		225		

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.8V, V_{IN_LDO} = 5.3V, V_{LDO} = 5.14V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.32		ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value, T_A = +25°C			1.6		V/ms
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	5.1375V programmed output voltage (TV_LDO[6:0] = 0x72), V_{IN_LDO} = 5V, I_{LDO} = 20mA (Note 10)			4.6	20	mV
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C		+0.1	+1.0	µA
			T_A = 0°C to +85°C		+1.0		

Note 8: When the input voltage is within the specified range, the LDO headroom is being regulated by the fixed-headroom-control loop and the LDO output voltage is regulated by the LDO. However, the regulator can be in dropout. For example, if the output voltage is fixed at 5.14V and a 5V input is provided, the output is 5.14V minus the dropout voltage (V_{LDO} = V_{IN_LDO} - V_{LDO_DO}). To achieve the specified output voltage, the input voltage must be the output voltage plus the dropout voltage ($V_{IN\_LDO} \geq V_{LDO} + V_{LDO\_DO\_MAX}$).

Note 9: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the Shutdown Supply Current and Quiescent Supply Current specification in the Electrical Characteristics—Global Resources table.

Note 10: The dropout voltage is the difference between the input voltage and the output voltage when the input voltage is within the valid input voltage range, but below the output voltage setpoint. For example, if the output voltage setpoint is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{LDO_DO} = V_{IN_LDO} - V_{LDO}).

Electrical Characteristics—Current Sink

(V_{SYS}= 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Supply Voltage		Supply voltage range for current sink V_{CS} = 400mV, I_{CS} = 350mA		3	3.8	5	V
Input Voltage for LED Termination				3	3.8	5.5	V
Current Sink Quiescent Current	I_Q	Change in supply current at SYS when current sink is enabled			400	550	µA
Current Sink Leakage		CS_PRE_EN = 0, V_{CS} = 4.2V			+0.1	+1.0	µA
CS_EN Input Voltage Low	$V_{CS\_EN\_IL}$	V_{SYS} = 3.8V			0.4		V
CS_EN Input Voltage High	$V_{CS\_EN\_IH}$	V_{SYS} = 3.8V			V_{IO}-0.4		V
CURRENT SINK RANGE							
Minimum Sink Current		CS_CURR[2:0] = 0b000			250		mA
Maximum Sink Current		CS_CURR[2:0] = 0b111			425		mA
Current Sink Accuracy		CS_CURR[2:0] = 0b100, V_{SYS} = 3.8V	T_A = +25°C	-3%	350	+3%	mA
			T_A = 0°C to +85°C	-5%	350	+5%	
Headroom Voltage	V_{CS_HDRM}	CS_CURR[2:0] = 0b100, I_{CS} = 350mA; minimum headroom is defined where current drops 3% from nominal value		400			mV
TIMING CHARACTERISTICS							
Frequency Range	F_{EN}	V_{SYS} = 3.8V,CS_CURR[2:0] = 0b100		10		500	KHz
Preenable Set-Up Time	t_{SU}	Minimum time to operate current sink after current sink preenable (CS_PRE_EN = 1)			10		µs
Watchdog Timer	t_{WD}	Time out after last CS_EN falling edge resulting in an IRQ. Reset after each rising edge of CS_EN			12.8		ms
TIMING CHARACTERISTICS/PULSE PERIOD SETTINGS							
Duty Cycle						50	%
Rise Time	t_{rCS}	V_{SYS} = 3.8V, CS_CURR[2:0] = 0b100, V_{CS_HDRM} = 600mV, T_A = 0°C to +85°C	Time from CS_EN rising edge to 90% of final DC current value.		100	500	ns
Overshoot	I_{CS_OS}	V_{SYS} = 3.8V, CS_CURR[2:0] = 0b100, V_{CS_HDRM} = 600mV, T_A = 0°C to +85°C	Percent overshoot above final DC current value		25%		%

Electrical Characteristics—I²C

(V_{SYS}= 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA and SCL I/O Stage						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 11)	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 11)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (Note 11)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns

Electrical Characteristics—I²C (continued)

(V_{SYS}= 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

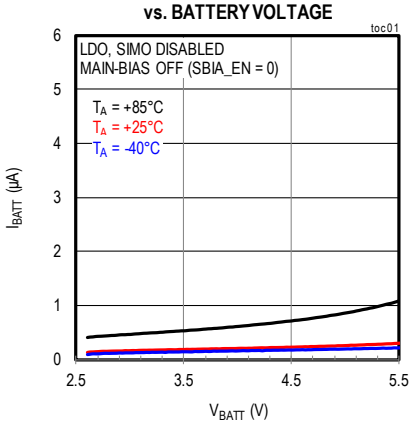
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (Note 11)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 11: Design guidance only. Not production tested.

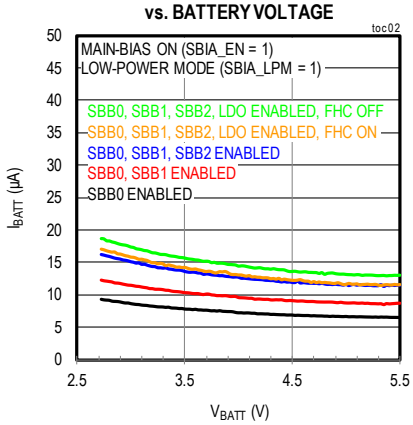
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

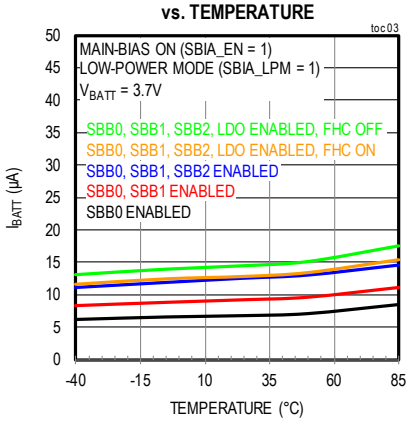
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



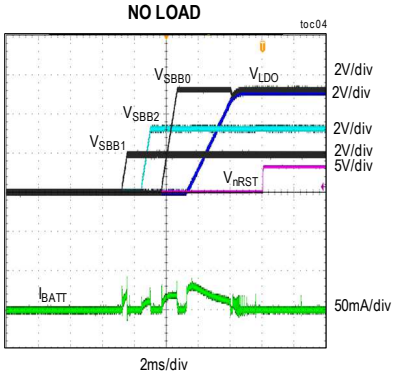
QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



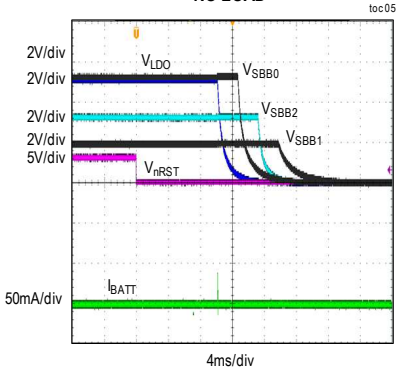
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



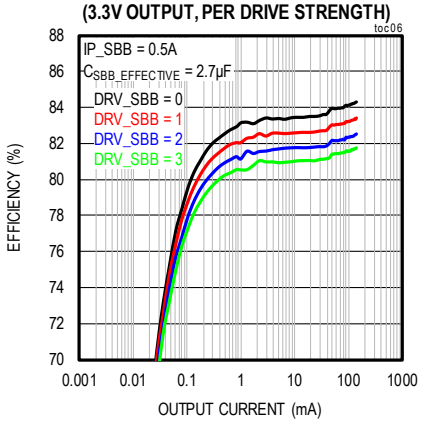
POWER-UP NO LOAD



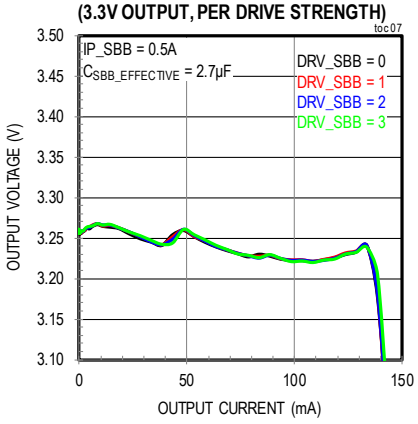
POWER-DOWN NO LOAD



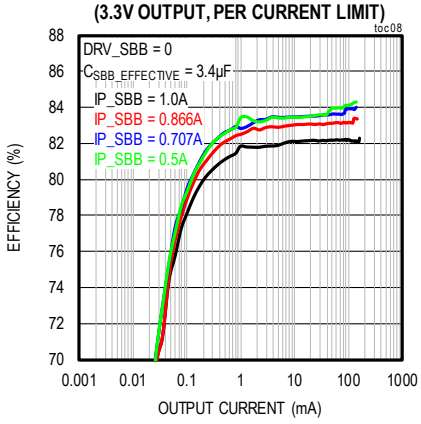
SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER DRIVE STRENGTH)



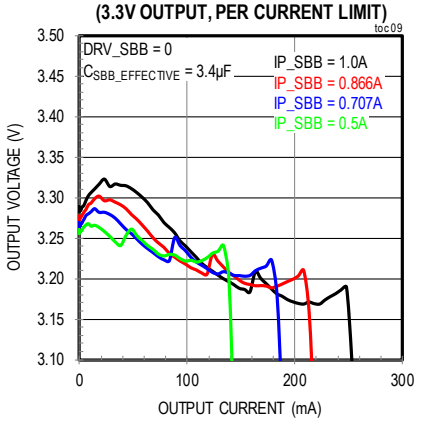
SIMO LOAD REGULATION (3.3V OUTPUT, PER DRIVE STRENGTH)



SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER CURRENT LIMIT)



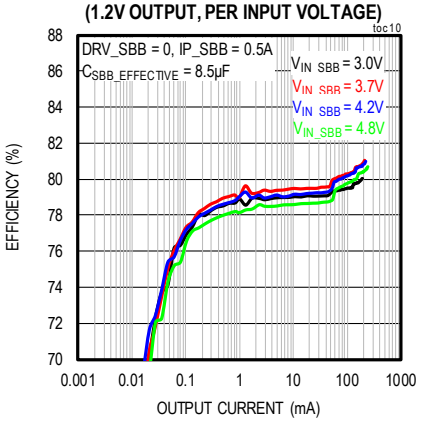
SIMO LOAD REGULATION (3.3V OUTPUT, PER CURRENT LIMIT)



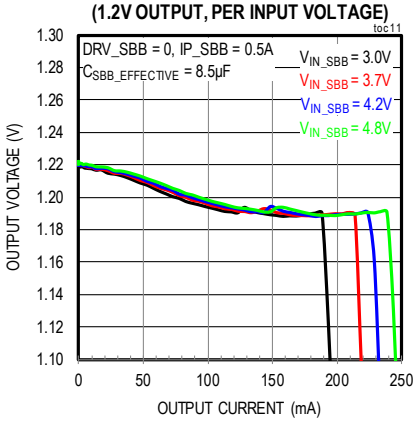
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

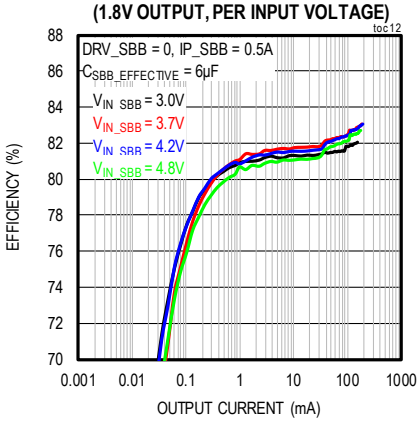
SIMO EFFICIENCY vs. OUTPUT CURRENT (1.2V OUTPUT, PER INPUT VOLTAGE)



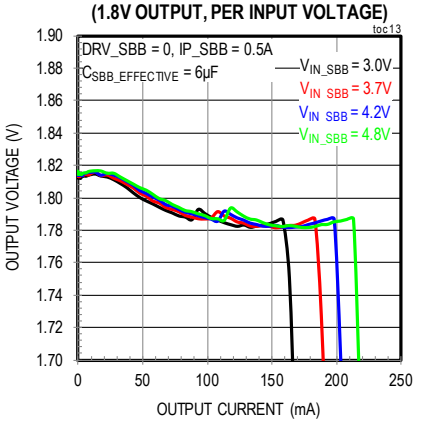
SIMO LOAD REGULATION (1.2V OUTPUT, PER INPUT VOLTAGE)



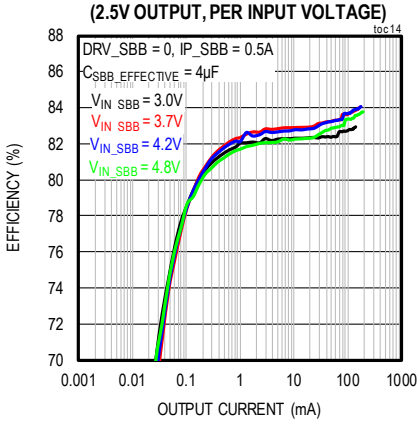
SIMO EFFICIENCY vs. OUTPUT CURRENT (1.8V OUTPUT, PER INPUT VOLTAGE)



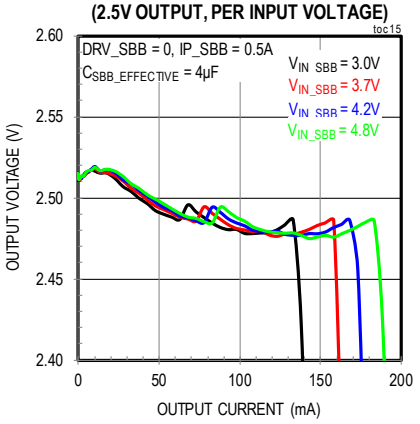
SIMO LOAD REGULATION (1.8V OUTPUT, PER INPUT VOLTAGE)



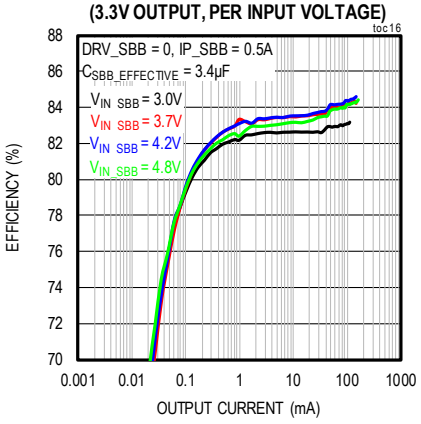
SIMO EFFICIENCY vs. OUTPUT CURRENT (2.5V OUTPUT, PER INPUT VOLTAGE)



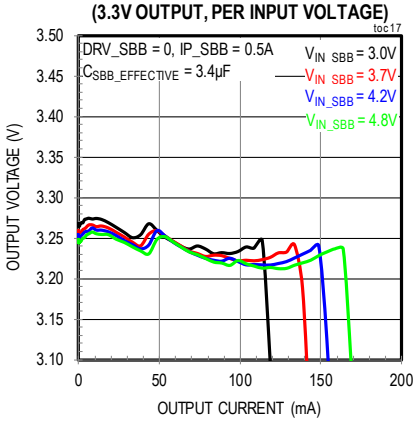
SIMO LOAD REGULATION (2.5V OUTPUT, PER INPUT VOLTAGE)



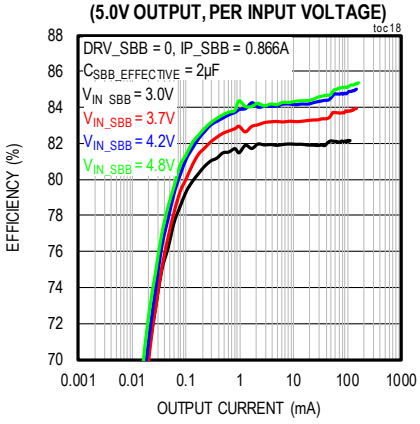
SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER INPUT VOLTAGE)



SIMO LOAD REGULATION (3.3V OUTPUT, PER INPUT VOLTAGE)



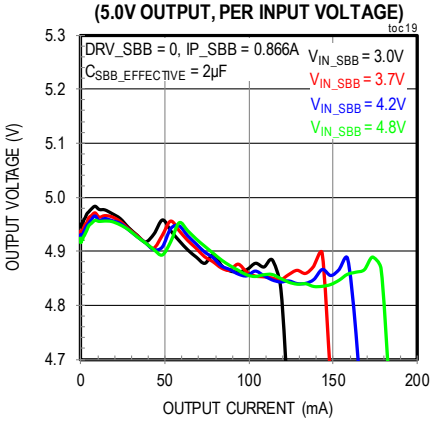
SIMO EFFICIENCY vs. OUTPUT CURRENT (5.0V OUTPUT, PER INPUT VOLTAGE)



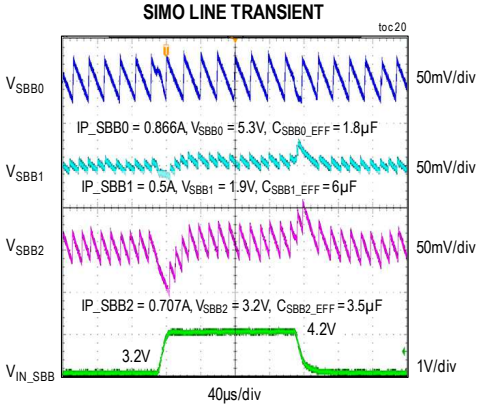
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

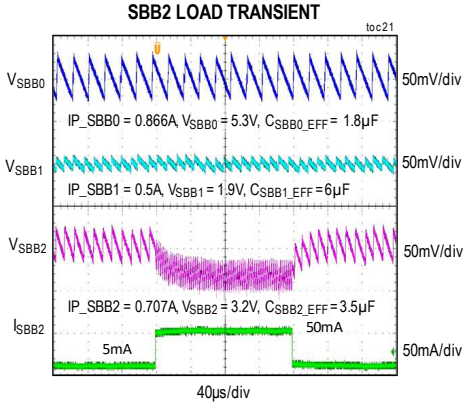
SIMO LOAD REGULATION (5.0V OUTPUT, PER INPUT VOLTAGE)



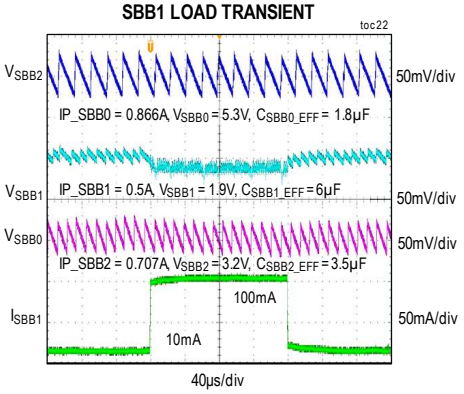
SIMO LINE TRANSIENT



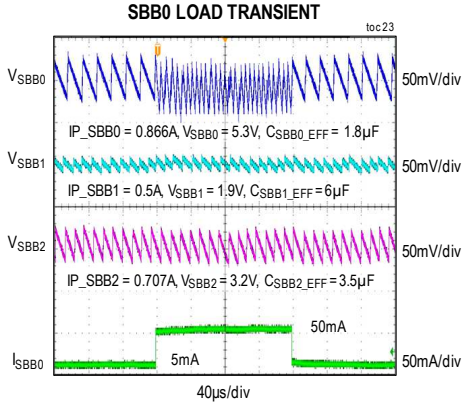
SBB2 LOAD TRANSIENT



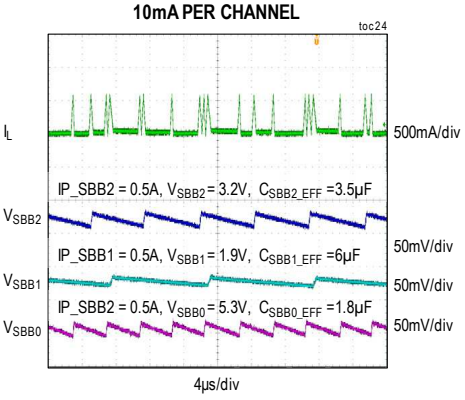
SBB1 LOAD TRANSIENT



SBB0 LOAD TRANSIENT



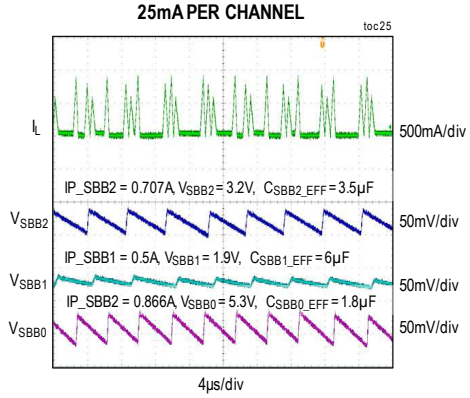
SIMO SWITCHING WAVEFORMS LIGHT UTILIZATION 10mA PER CHANNEL



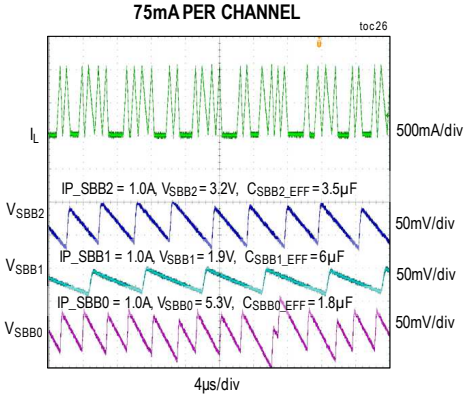
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

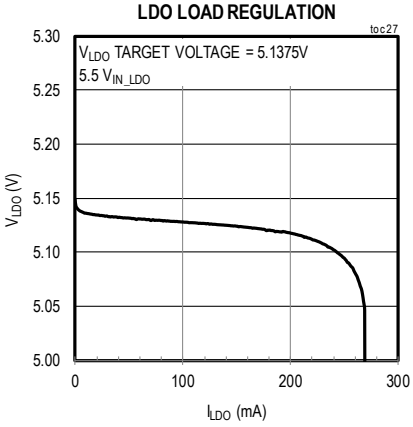
**SIMO SWITCHING WAVEFORMS
MEDIUM UTILIZATION
25mA PER CHANNEL**



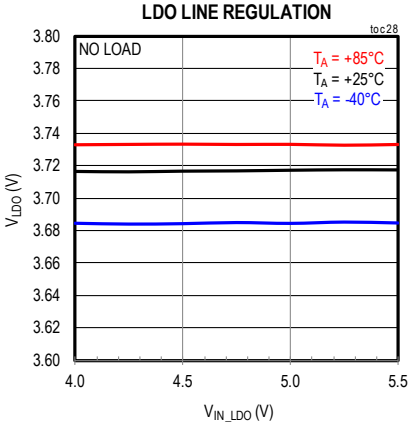
**SIMO SWITCHING WAVEFORMS
HEAVY UTILIZATION
75mA PER CHANNEL**



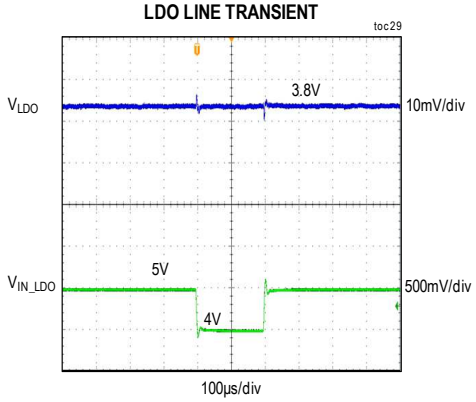
LDO LOAD REGULATION



LDO LINE REGULATION



LDO LINE TRANSIENT



LDO LOAD TRANSIENT