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EVALUATION KIT AVAILABLE

MAX77301

JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

General Description

The MAX77301 is a JEITA-compliant* lithium-ion linear battery charger that operates from a USB port, a dedicated charger, or universal adapter. The IC provides automatic adapter-type detection and enumeration with a USB host or hub. The IC integrates independent battery charge switch, current sense circuit, MOSFET pass elements, thermal regulation circuitry, and eliminates the external reverse-blocking Schottky diode to create the simplest and smallest USB-compliant charging solution.

The IC includes automated detection of charge adapter type, making it possible to distinguish USB 2.0 device, USB charger, dedicated charger devices as well as standard input adapters. See Table 2. When enumeration is enabled, the IC automatically negotiates with a USB host, making it possible to achieve the highest-charging current available from a USB 2.0 device or USB charger without processor intervention. The adapter type detection is compliant with USB 2.0 as well as battery charging Specification Revision 1.1.

The IC controls the charging sequence for single-cell Li+ batteries from battery detection, prequalification, fast charge, top-off, and charge termination. Charging is controlled using constant current, constant voltage and constant die-temperature (CCCVCTj) regulation for safe operation under all conditions. The IC is also compliant with JEITA battery charging requirements.

The Smart Power Selector feature makes the best use of limited USB or adapter power. Battery charge current is set independent of the input current limit. Power not used by the system charges the battery. The battery assists the input source when needed. System voltage is maintained by allowing the application to operate without a battery, a discharged battery, or a dead battery. Automatic input selection switches the system from battery to external power.

The I²C interface provides full programmability of battery charge characteristics, input current limit, and protection features. This provides flexibility for use with a wide range of adapter and battery sizes.

Other features include undervoltage lockout (UVLO), overvoltage protection (OVP), charge status flag, charge fault flag, input power-OK monitor, battery detection, JEITA-compliant charging, charge timer, 3.3V/10mA auxiliary output, and an external power-on switch.

Benefits and Features

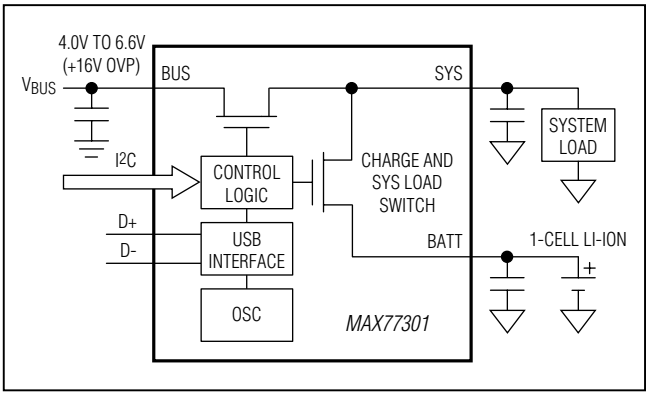
- **Enables Charging from a USB Port**
- **Automatic Detection of Adapter Type**
- **Input Current Up to 1500mA and Charging Current Up to 900mA**
- **Enumeration Without Processor Intervention**
- **Supports USB Low-Speed and Full-Speed**
- **Compliant with USB 2.0 Specification and Battery Charging Specification (Revision 1.1)**
- **Compliant with Next Generation Low-Voltage Li-Ion Battery Profiles**
- **Input Overvoltage Protection Up to 16V**
- **Smart Power Selector™ Allows Power Path Operation with Discharged or No Battery**
- **Battery Detection Including Packs with Open Protectors**
- **Thermal Regulation Prevents Overheating**
- **LED Indicator for Charge Done, Precharge, and Time/Temperature Error**
- **Serial (400kHz) I²C-Compatible Interface**
- **6µA (typ) Shutdown Current**
- **2.44mm x 2.44mm, 25-Bump WLP Package**

Applications

Bluetooth Headsets, PDAs, and MP3 Players

Other Portable Devices

Simplified Operating Circuit



***Ordering Information* appears at end of data sheet.**

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

**U.S. Patent # 6,507,172.*

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX77301.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6556; Rev 0; 1/13

MAX77301

JEITA-Compliant, Li+ Charger with Smart Power Selector, Automatic Detection, and USB Enumeration

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ABSOLUTE MAXIMUM RATINGS

BUS_ to AGND ..... -0.3V to +16.0V
INT_3V3 to AGND ..... -0.3V to +6V
CHG_TYPE, IBUS_DEF, $\overline{ENU\_EN\_HW}$, $\overline{IRQ}$, D+, D-, $\overline{UOK}$, $\overline{CHG\_STAT}$, BAT_, SYS_, CEN, $\overline{STDB\_EN\_HW}$ to AGND ..... -0.3V to +6.0V
XIN, THM, XOUT, to AGND ..... -0.3V to (V_{INT_3V3} + 0.3V)
$\overline{EXT\_PWRON}$, SDA, SCL to AGND ..... -0.3V to (V_{SYS} + 0.3V)
DGND to AGND ..... -0.3V to +0.3V
I_{BUS} and I_{SYS} Continuous Current (Note 1) ..... $2200mA_{RMS}$
I_{BAT} Continuous Current (Note 1) ..... $1800mA_{RMS}$
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 19.2mW/°C above +70°C) 1538mW
Operating Temperature ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: $I_{BUS} = I_{BUS\_A} + I_{BUS\_B}$; $I_{SYS} = I_{SYS\_A} + I_{SYS\_B}$; $I_{BAT} = I_{BAT\_A} + I_{BAT\_B}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 52°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
USB-TO-SYS PREREGULATOR							
USB Operating Range	V_{BUS}	Initial V_{BUS} voltage before enabling charger		4.0		6.6	V
USB Standoff Voltage		V_{BAT} = V_{SYS} = 0V, I_{BUS} < 800µA				14	V
USB_OK Debounce Timer	t_{USB_DB}	Time from BUS within valid range until $\overline{UOK}$ goes high impedance			30	50	ms
USB Undervoltage Lockout Threshold		$\overline{UOK}$ logic-low, V_{BUS} rising, 100mV hysteresis	Before initial detection of external device	3.85	4.0	4.15	V
		$\overline{UOK}$ logic-low, V_{BUS} falling, customer UVLO	For > 500mA adapter and except for ILIM [2:0] = 000, 111	3.40	3.55	3.70	
		$\overline{UOK}$ logic-low, V_{BUS} falling	USB 2.0 low-power device	3.75	3.9	4.05	
		$\overline{UOK}$ logic-low, V_{BUS} falling	USB 2.0 high-power device	3.95	4.1	4.25	
USB Overvoltage Protection Threshold		$\overline{UOK}$ logic-low, V_{BUS} rising, 100mV hysteresis		6.7	6.9	7.1	V

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
USB Input Supply Current (Notes 3, 4)	I_{DETECT}	Charge type detection, I_{SYS} = I_{BAT} = 0mA				0.5	mA
	$I_{ENUMERATE}$	USB 2.0 enumeration in progress, I_{SYS} = I_{BAT} = 0mA				100	
	$I_{SUSPEND}$	Suspended mode, I_{SYS} = I_{BAT} = 0mA, $V_{\overline{STDB\_EN\_HW}}$ = 0V				0.5	
	I_{USB_100mA}	USB 2.0 low-power device detected	T_A = 0°C to +85°C			100	
			T_A = -40°C to +85°C			102.5	
	I_{USB_500mA}	USB 2.0 high-power device detected				500	
USB Input Current Limit	I_{SUS}	During suspend			0		mA
	I_{ENU}	During USB enumeration, T_A = +25°C		80	90	98	
	I_{USB_LP}	USB 2.0 low-power device detected, T_A = +25°C		80	90	98	
	I_{USB_HP}	USB 2.0 high-power device detected		460	475	490	
	I_{LIMIT}	ILIM = 000, T_A = +25°C		80	90	98	
		ILIM = 001 (default)		460	475	490	
		ILIM = 010			600		
		ILIM = 011			700		
		ILIM = 100			900		
		ILIM = 101			1000		
		ILIM = 110, T_A = +25°C (Note 3)		1344	1500	1650	
		ILIM = 110, T_A = -40°C to +85°C		1324	1500	1700	
$V_{BUS\_}$ to $V_{SYS\_}$ On-Resistance		V_{BUS} = 5V, I_{SYS} = 400mA			200	320	mΩ
$V_{SYS\_}$ to $V_{BAT\_}$ Reverse Regulation		When SYS is in regulation and charging stops, $V_{SYS\_}$ falling, 50mV typical hysteresis		V_{BAT} - 80mV	V_{BAT} - 50mV	V_{BAT} - 20mV	
Input Limiter Soft-Start Time		Input current ramp time			50	100	µs
Thermal-Limit Start Temperature	T_{DIE_LIM}	THERM_REG = 00			90		°C
		THERM _REG = 01			100		
		THERM _REG = 10			110		
		THERM _REG = 11			120		
Thermal-Limit Triggers $\overline{IRQ}$					T_{DIE_LIM} + 10°C		°C
Thermal-Limit Gain		I_{SYS} reduction/die temperature			5		%/°C
SYS Regulation Voltage		V_{BAT} > 3.45V, I_{SYS} = 1mA to 1.6A			140mV + V_{BAT}	210mV + V_{BAT}	V

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Minimum SYS Regulation Voltage	V_{SYS_MIN}	V_{BUS} = 6V, I_{SYS} = 1mA to 1.6A	V_SYS = 00			3.4		V
			V_SYS = 01	T_A = 25°C	4.2	4.35	4.524	
				T_A = -40°C to +85°C	4.185	4.35	4.524	
			V_SYS = 10			4.4		
			V_SYS = 11			4.5		
Undervoltage Lockout	V_{SYS_UVLO}	$V_{BUS\_}$ = 5.5V rising				3.0		V
		$V_{BUS\_}$ = 5.5V falling			2.6	2.85	3.1	
CHARGER								
BAT-to-SYS On-Resistance		V_{BAT} = 4.2V, I_{SYS} = 200mA				55	80	mΩ
BAT Undervoltage Lockout (Register 0x10h, Bit 7 = 0)	$V_{BAT\_UVLO\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 1 (Register 0x10h)		2.15	2.40	2.65	V
	$V_{BAT\_UVLO\_R}$	V_{BAT} rising			2.45	2.70	2.95	
	$V_{BAT\_UVLO\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 0 (default, Register 0x10h)		1.60	1.85	2.10	
	$V_{BAT\_UVLO\_R}$	V_{BAT} rising			1.85	2.10	2.35	
Charger Soft-Start Time						1		ms
BAT Leakage Current		V_{BAT} = 4.2V	V_{BUS} not connected			2	6	µA
			V_{BUS} connected, V_{CEN} = 0V			6	15	
PRECHARGE MODE								
BAT Precharge Current	I_{PCHG}	V_{BAT} > 1.4V (Note 5)				50*		mA
BAT Prequalification Threshold	$V_{BAT\_PCHG\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 1 (Register 0x10h)		2.60	2.70	2.80	V
	$V_{BAT\_PCHG\_R}$	V_{BAT} rising			2.70	2.80	2.95	
	$V_{BAT\_PCHG\_F}$	V_{BAT} falling	BAT_UVLO_VPREQ = 0 (default, Register 0x10h)		2.05	2.15	2.25	
	$V_{BAT\_PCHG\_R}$	V_{BAT} rising			2.15	2.25	2.40	
FAST-CHARGE MODE								
BAT Charge-Current Set Range	I_{FCHG}	I_{FCHG} = 000				100		mA
		I_{FCHG} = 010 (default)				200		
		I_{FCHG} = 001				300		
		I_{FCHG} = 110				370		
		I_{FCHG} = 111				450		
		I_{FCHG} = 011				600		
		I_{FCHG} = 100				800		
		I_{FCHG} = 101				900		

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
BAT Fast-Charge Threshold	$V_{BAT\_FCHG\_R}$	V_{BAT} rising threshold, where charging current I_{FCHG} is reduced to I_{TCHG}	BAT_FCHG = 00			3.8		V
			BAT_FCHG = 01			3.9		
			BAT_FCHG = 10 (default)		3.88	4	4.12	
			BAT_FCHG = 11			4.1		
	$V_{BAT\_FCHG\_HYS}$	V_{BAT} hysteresis, the falling threshold where charging current is increased to I_{FCHG} is: $V_{BAT\_FCHG\_HYS} = V_{BAT\_FCHG\_R} - V_{BAT\_FCHG\_F}$	BAT_FCHG_HYS = 00			150		mV
			BAT_FCHG_HYS = 01 default			200		
			BAT_FCHG_HYS = 10			250		
			BAT_FCHG_HYS = 11			300		
TOP-OFF CHARGE MODE								
Top-Off Charge Current	I_{TCHG}	V_{BAT} > 1.4V (Note 5)	TCHG = 00			0.4 x I_{FCHG}		mA
			TCHG = 01			0.6 x I_{FCHG}		
			TCHG = 10			0.8 x I_{FCHG}		
			TCHG = 11 (default)			1.0 x I_{FCHG}		
Charge DONE Qualification (Note 3)	I_{CHG_DONE}	CHG_DONE = 000				10		mA
		CHG_DONE = 001				20		
		CHG_DONE = 010			30	40	50	
		CHG_DONE = 011			37.5	50	62.5	
		CHG_DONE = 100 (default)			45	60	75	
		CHG_DONE = 101				80		
		CHG_DONE = 110				100		
		CHG_DONE = 111				120		
BAT Regulation Voltage	V_{BAT_REG}	$I_{BAT\_}$ = 0mA	BAT_REG = 00			4.05		V
			BAT_REG = 01			4.10		
			BAT_REG = 10			4.15		
			BAT_REG = 11 (default)	T_A = +25°C	4.179	4.200	4.221	
				T_A = 0°C to +85°C	4.158	4.200	4.242	

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT Recharge Threshold	V_{BAT_RECHG}	With respect to V_{BAT_REG}	BAT_RECHG = 00 (default)		-350		mV
			BAT_RECHG = 10		-300		
			BAT_RECHG = 01		-250		
			BAT_RECHG = 11		-200		
CHARGE TIMER							
Prequalification Timer	t_{PCHG}	From start of precharge until end of prequalification charge model (Figure 10)	PCHG_TMR = 00		30		Minutes
			PCHG_TMR = 01		60		
			PCHG_TMR = 10 (default)		120		
			PCHG_TMR = 11		240		
Fast-Charge Timer	t_{FCHG}	From start of fast charge until maintains charge (Figure 10)	FCHG_TMR = 00		75		Minutes
			FCHG_TMR = 01		150		
			FCHG_TMR = 10		300		
			FCHG_TMR = 11 Default		600		
Maintain-Charge Timer	t_{MTCHG}	(Figure 11)	MTCHG_TMR = 10 (default)		0		Minutes
			MTCHG_TMR = 01		15		
			MTCHG_TMR = 00		30		
			MTCHG_TMR = 11		60		
Timer Accuracy				-30		+30	%
Timer Extend Threshold		Percentage of charge current below which timer clock operates at half speed			50		%
Timer Suspend Threshold		Percentage of charge current below which timer clock pauses			20		%
INSERTION AND REMOVAL DETECTION							
BAT Discharge Current	I_{DIS}	1V ≤ V_{BAT} ≤ 4.2V, C_{BAT} ≤ 10µF		0.375		1.125	mA
BAT Discharge Time	t_{DIS}	Discharge timer expires if V_{BAT} drop > V_{BAT_UVLO} threshold, battery cap ≤ 10µF			150		ms
Charge Debounce Timer	t_{DB}	Delay before checking charge done		100	150	200	ms
Battery Detecting Current	I_{BAT_DET}	Charging in prograss (precharge, fast-charge or maintain charge); if I_{BAT} < I_{BAT_DET} = battery absence		1	3	5	mA
ADAPTER TYPE DETECTION							
D- Current Sink	I_{DM_SINK}			50	100	150	µA
D+ Current source	I_{DP_SRC}			7		13	µA

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D- Weak Current Sink	$I_{DM\_CD\_PD}$				0.1	µA
D+ Source Voltage	V_{DP_SRC}	I_{DP_SRC} = 200µA	0.5	0.6	0.7	V
D+ Detection Threshold	V_{DAT_REF}		0.25	0.32	0.40	V
D- Logic-High Threshold	V_{DM_IH}		0.8		2.0	V
D+ Logic-High Threshold	V_{DP_IH}		0.8		2.0	V
D+/D- Detection Threshold	DP_25% DM_25%	Detection threshold for custom chargers as % of V_{BUS}	23.75	25.0	26.25	%
	DM_34%		32.3	34	35.7	
	DP_47% DM_47%		44.65	47.00	49.4	
	DP_60% DM_60%		57	60	63	
D- Pulldown Resistor	R_{DM_DWN}		14.25		24.8	kΩ
D- Pullup Resistor	R_{DM_PU}	External resistor = 33Ω, low speed only	1.425	1.500	1.575	kΩ
D+ Pullup Resistor	R_{DP_PU}	External resistor = 33Ω, full speed only	1.425	1.500	1.575	kΩ
D+ Charger Detection Pullup Resistor	$R_{DP\_CD\_PU}$	$R_{DP\_CD\_PU}$ connected to INT_3V3	200	330	600	kΩ
Data Contact Detection Debounce Timer	t_{DCD_DBNC}			30		ms
D+ Source On Time	$t_{DP\_SRC\_ON}$		100			ms
D+ Source to High-Current Time	$t_{DP\_SRC\_HC}$		40			ms
Enumeration Time Limit	t_{ENUM}	Time from start of enumeration process until enumeration		10		s
Reenumeration Timer	t_{RE_ENUM}	Time from suspend mode until it re-enumerates, RWU_EN = 1		100		ms
Reconnect Timer	t_{FAULT}	Time from failed enumeration to adapter type detection reenabled, nENU_EN = 0		3		s
Detecting Time		D+/D- open power source nENU_EN = 1		100		ms
Enumeration Fail to Reconnect Timer	t_{ENU_FAULT}	Time from enumeration fail at 500mA until enumeration is retried at 100mA or time from enumeration fail at 100mA until reconnect timer is started		87		ms
XIN, XOUT PINS						
Oscillator Frequency Accuracy		Internal oscillator (low speed), T_A = +25°C	5.91	6.00	6.09	MHz
XIN, XOUT Input Capacitance		With external crystal (full speed)		3		pF

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
XIN Input Current		With external crystal (full speed)				10	µA
XIN Logic-High Input Voltage				0.667 x V_{INT_3V3}		V_{INT_3V3}	V
XIN Logic-Low Input Voltage						0.4	V
THERMISTOR MONITOR (THM)							
THM Hot Threshold	T_4	V_{THM} raising, 2% hysteresis			32.2		% of V_{INT_3V3}
THM Warm Threshold	T_3	V_{THM} raising, 2% hysteresis			46.5		
THM Cool Threshold	T_2	V_{THM} falling, 2% hysteresis			81.9		
THM Cold Threshold	T_1	V_{THM} falling, 2% hysteresis			88.7		
THM Disable Threshold		V_{THM} falling, 2% hysteresis			3.4		
THM Input Impedance	THM_{ZIN}	High impedance when no BUS or THM is disabled		500			kΩ
THM Input Leakage		THM = AGND THERM_EN = 0	T_A = +25°C	-1	0.001	+1	µA
			T_A = +85°C		0.01		
$\overline{EXT\_PWRON}$							
Logic-Low Output Voltage		Sinking 10mA			35	100	mV
High-Impedance Time	$t_{EXT\_PWR\_RESET}$	Time where $\overline{EXT\_PWRON}$ is high-impedance during transition between two $\overline{EXT\_PWRON}$ low states			63		ms
CHARGER STATUS ($\overline{CHG\_STAT}$)							
Logic-Low Output Voltage		Sinking 10mA			35	100	mV
Blink Period for Temperature Suspend Mode		50% duty cycle, battery present			1.5		s
Blink Period for Timeout Mode		50% duty cycle, battery present			0.15		s
LOGIC I/O: $\overline{UOK}$, CEN, $\overline{ENU\_EN\_HW}$, CHG_TYPE, IBUS_DEF, $\overline{IRQ}$, SDA, SCL, $\overline{STDB\_EN\_HW}$							
Logic Input Voltage		High level		1.3			V
		High level for SDA and SCL		1.4			
		Low level				0.4	
Logic Input-Leakage Current		V_{BUS} = 0V to 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
Logic-Low Output Voltage (CHG_TYPE, $\overline{IRQ}$, $\overline{UOK}$, Only)		Sinking 10mA			35	100	mV

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic-High Output-Leakage Current (CHG_TYPE, $\overline{IRQ}$, $\overline{UOK}$, Only)		V_{SYS} = 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
$\overline{UOK}$ Blink Period During USB Suspend		Only for USB automatically entering suspend mode, 50% duty cycle			1.5		s
$\overline{UOK}$ Blink Period with Open D+/D- Detected		50% duty cycle			0.15		s
I²C INTERFACE (See Figure 19) (Note 3)							
Clock Frequency						400	kHz
Bus-Free Time Between START and STOP	t_{BUF}			1.3			µs
Hold Time Repeated START Condition				0.6			µs
SCL Low Period	t_{LOW}			1.3			µs
SCL High Period	t_{HIGH}			0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}			0.6			µs
SDA Hold Time	t_{HD_DAT}			0			µs
SDA Setup Time	t_{SU_DAT}			100			ns
Maximum Suppressed Pulse Width		Width of spikes that must be suppressed by the input filter of both SDA and SCL signals			50		ns
Setup Time for STOP Condition	t_{SU_STO}			0.6			µs
USB DATA INTERFACE							
Differential-Receiver Input Sensitivity	$\lvert V_{D+} - V_{D-} \rvert$			0.2			V
Differential-Receiver Common-Mode Voltage				0.8		2.5	V
D+, D- Input Impedance				300			kΩ
D+, D- Output Low Voltage	V_{OL}	R_{LOAD} = 1.5kΩ from V_{D-} to 3.6V				0.3	V
D+, D- Output High Voltage	V_{OH}	R_{LOAD} = 15kΩ from D+ and D- to AGND		2.8		3.6	V
Driver Output Impedance		Excludes external resistor		2	7	11	Ω
BUS Idle Time	t_{IDLE}	Only valid when an adapter type is detected as a USB 2.0 device; time BUS is inactive until charging current is reduced to $I_{SUSPEND}$			3		ms

ELECTRICAL CHARACTERISTICS (continued)

(THM = AGND, CEN = INT_3V3, V_{BAT} = 4.2V, $V_{BUS\_}$, $\overline{EXT\_PWRON}$, $\overline{UOK}$, $\overline{IRQ}$, CHG_TYPE, and $\overline{CHG\_STAT}$ are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Host Remote Wake-Up Timer	t_{RWU}	Time delay from suspend mode until it requests the host for a remote wake-up		100		ms
D+, D- Rise Time (Note 3)	t_{RISE}	C_L = 50pF to 600pF, low speed only	75		250	ns
		C_L = 50pF, full speed only	4		20	
D+, D- Fall Time (Note 3)	t_{FALL}	C_L = 50pF to 600pF, low speed only	75		250	ns
		C_L = 50pF to 600pF, full speed only	4		20	
Rise/Fall-Time Matching (Note 3)		C_L = 50pF to 600pF, low speed only	80		120	%
		C_L = 50pF to 600pF, full speed only	90		110	
Output-Signal Crossover Voltage		C_L = 50pF to 600pF, low speed only	1.3		2.0	V
INT_3V3 REGULATOR						
INT_3V3 Voltage		V_{BUS} = 5V, I_{INT_3V3} = 0 to 10mA	3.0	3.3	3.6	V
ESD PROTECTION (D+, D-, BUS_)						
Human Body Model		BUS bypassed with 1µF to AGND		±8		kV

Note 2: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 3: Guaranteed by design. Limits not production tested.

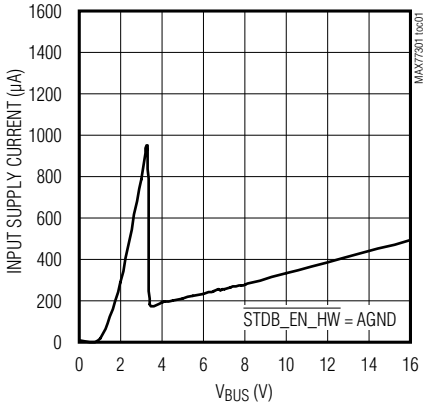
Note 4: Sum of input current limit and current used for INT_3V3.

Note 5: Maximum charging current is adaptively regulated to I_{ILIM} - I_{SYS} though maximum I_{CHG}.

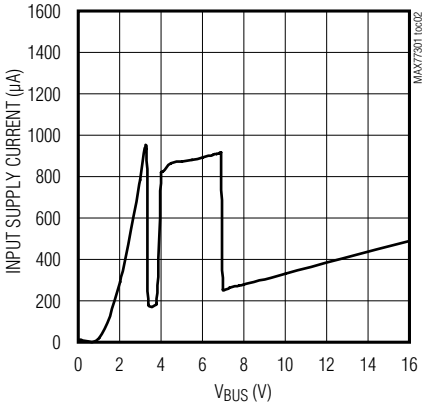
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

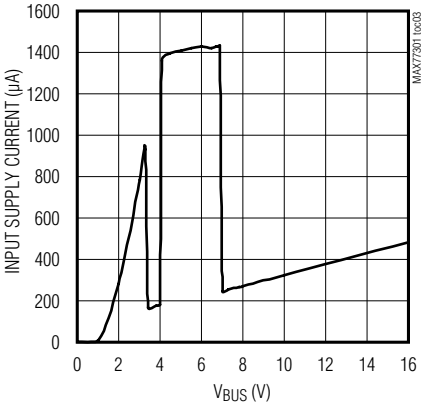
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (SUSPEND MODE)



V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (FULL SPEED)



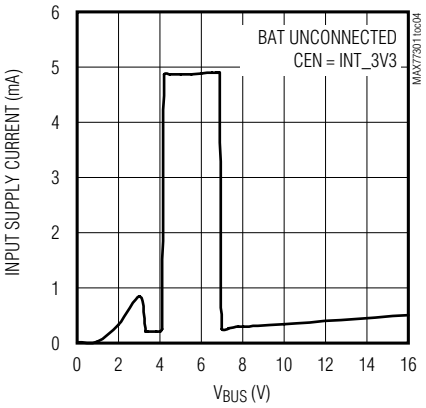
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (LOW SPEED)



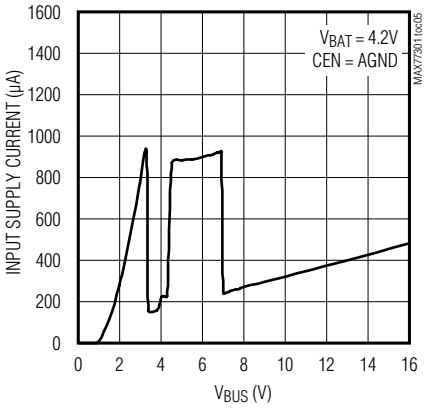
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

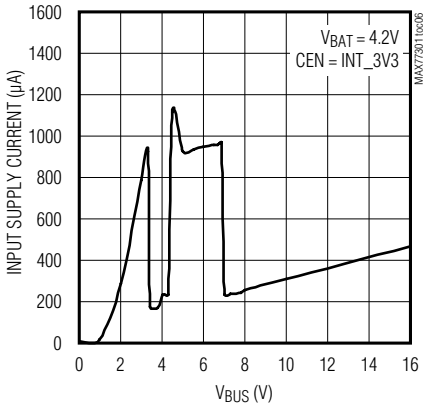
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER ENABLED)



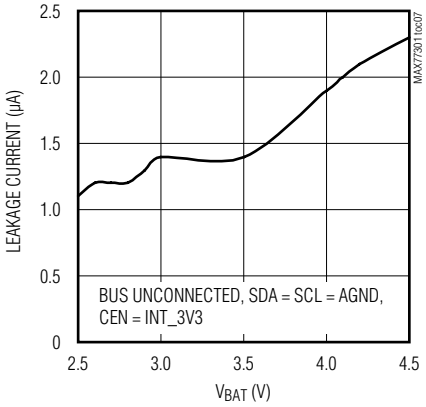
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER DISABLED)



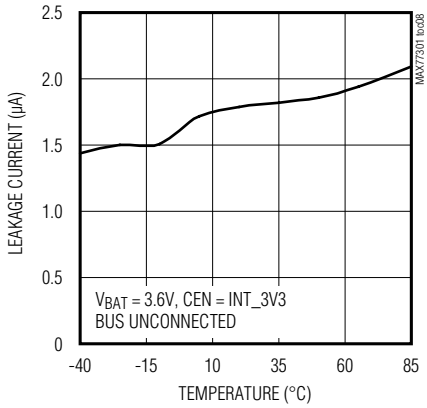
V_{BUS} INPUT SUPPLY CURRENT vs. V_{BUS} (CHARGER DISABLED)



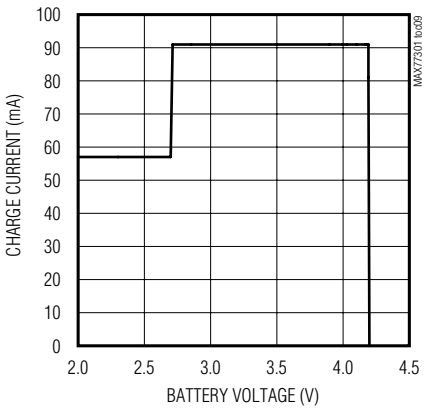
BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE



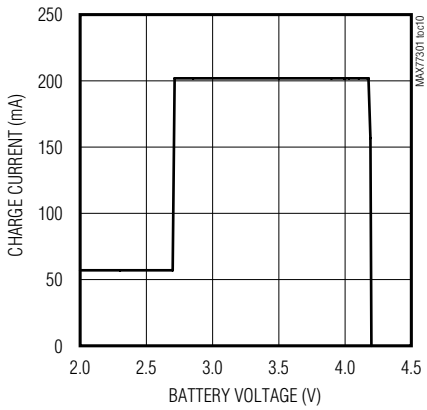
BATTERY LEAKAGE CURRENT vs. TEMPERATURE



CHARGE CURRENT vs. BATTERY VOLTAGE (LOW-POWER MODE)



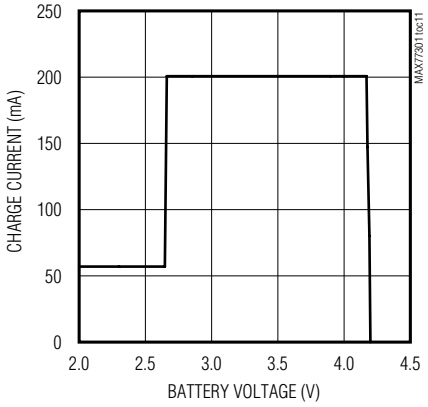
CHARGE CURRENT vs. BATTERY VOLTAGE (HIGH-POWER MODE)



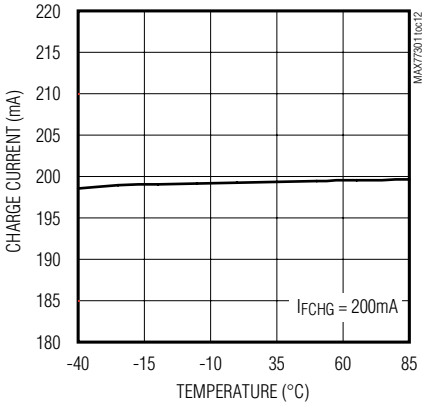
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

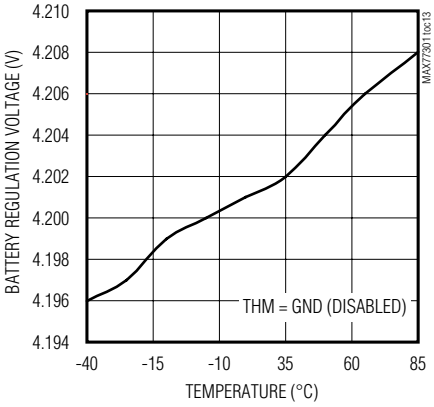
CHARGE CURRENT vs. BATTERY VOLTAGE (1A DEDICATED CHARGER)



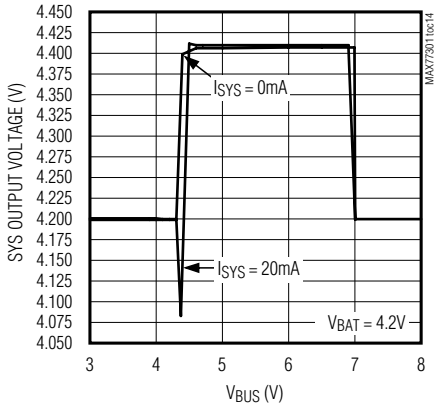
CHARGE CURRENT vs. AMBIENT TEMPERATURE



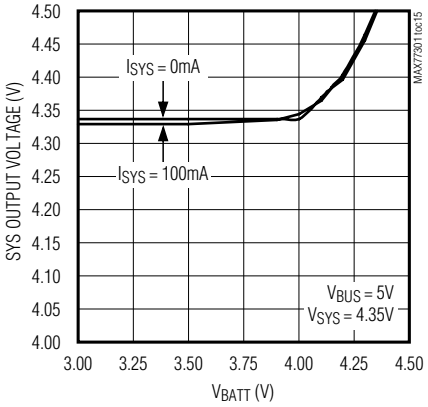
BATTERY REGULATION VOLTAGE vs. AMBIENT TEMPERATURE



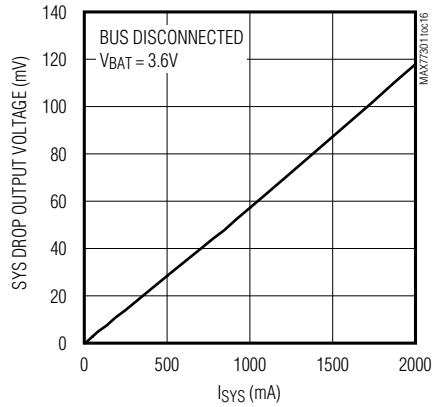
SYS OUTPUT VOLTAGE vs. V_{BUS}



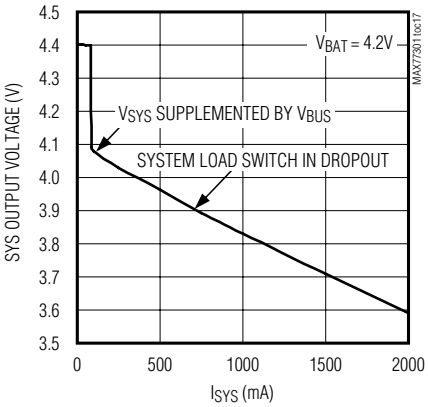
SYS OUTPUT VOLTAGE vs. BATTERY VOLTAGE



BAT-SYS VOLTAGE DROP vs. SYS CURRENT



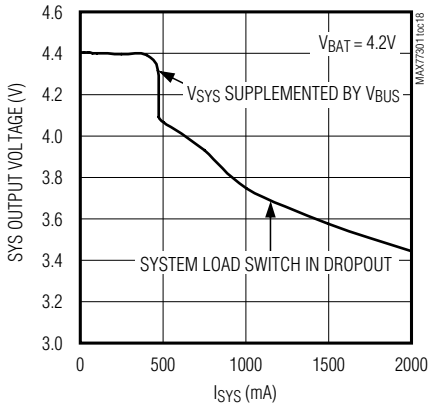
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (USB LOW-POWER MODE)



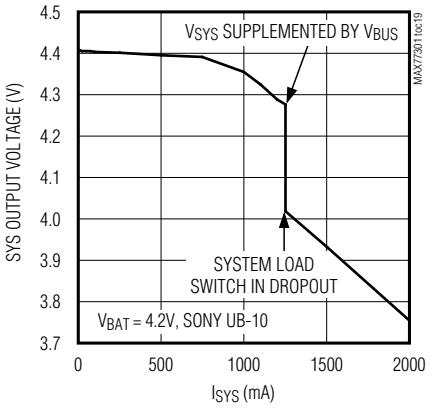
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

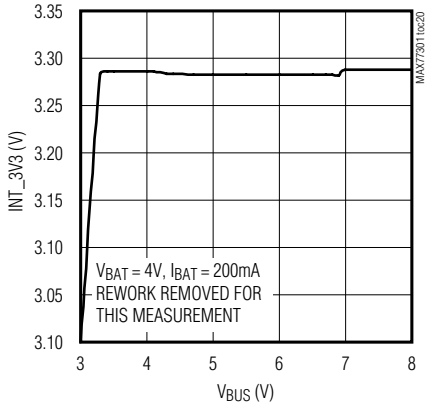
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (USB HIGH-POWER MODE)



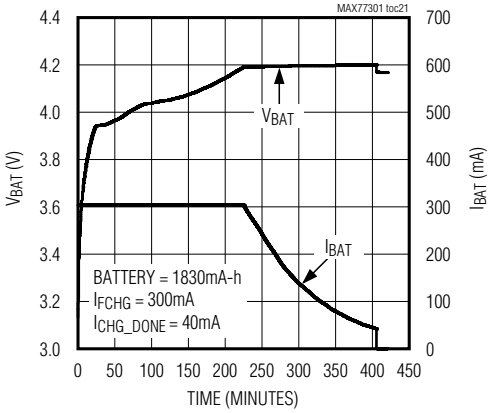
SYS OUTPUT VOLTAGE vs. LOAD CURRENT (DEDICATED CHARGER)



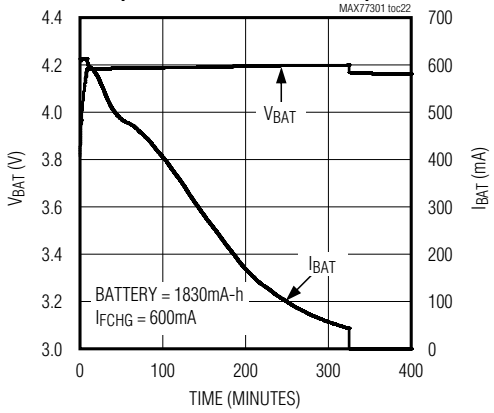
INT_3V3 VOLTAGE vs. BUS VOLTAGE



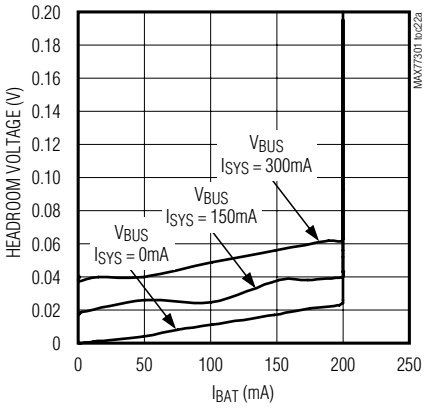
BATTERY CHARGE PROFILE



CHARGE PROFILE (HIGH-POWER USB CHARGER)



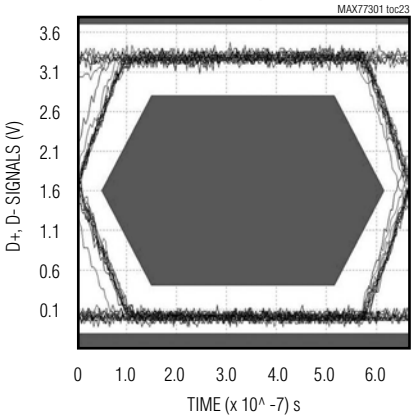
HEADROOM VOLTAGE vs. BATTERY CURRENT SYS VOLTAGE = 4.35V, I_{FCHG} = 200mA



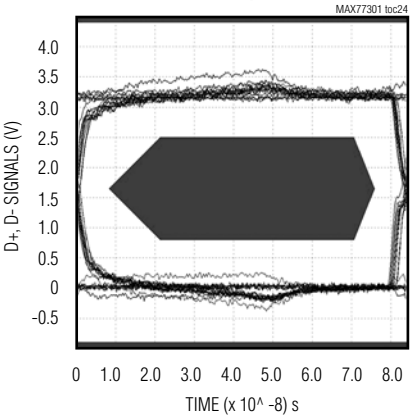
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

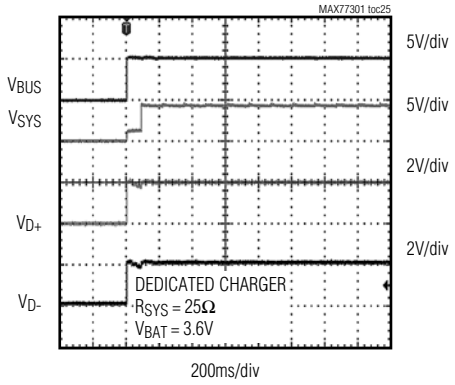
EYE DIAGRAM (LOW SPEED)



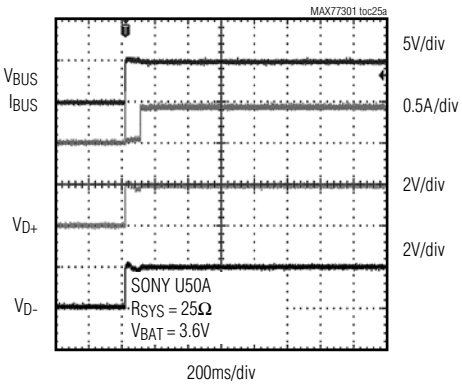
EYE DIAGRAM (FULL SPEED)



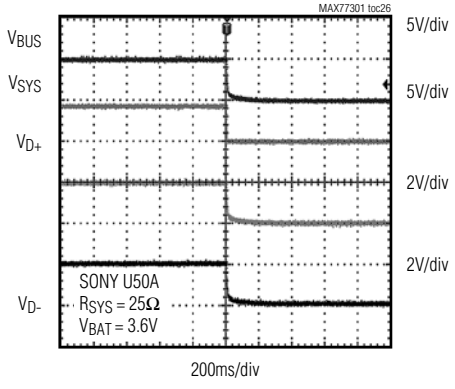
DEDICATED CHARGER CONNECT



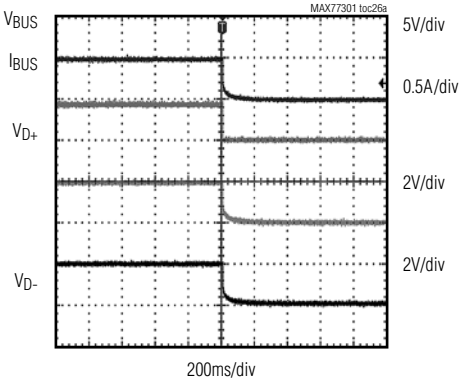
DEDICATED CHARGER CONNECT



DEDICATED CHARGER DISCONNECT



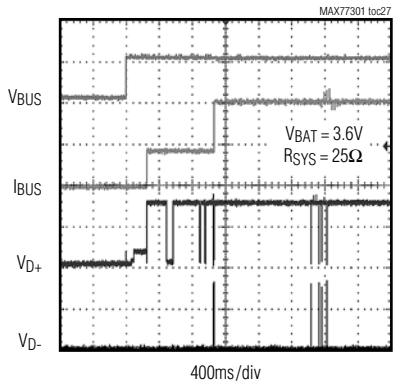
DEDICATED CHARGER DISCONNECT



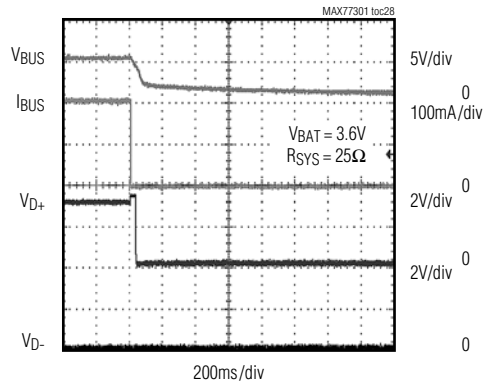
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C unless otherwise noted.)

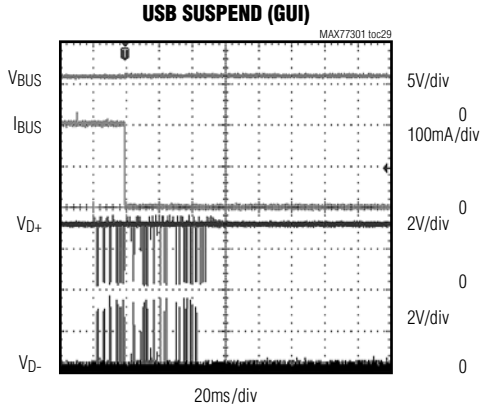
USB HIGH-POWER 2.0 CONNECT



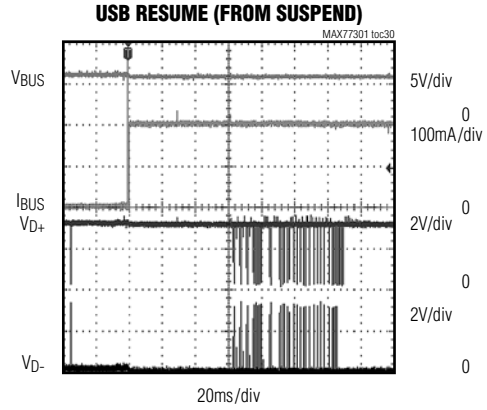
USB HIGH-POWER 2.0 DISCONNECT



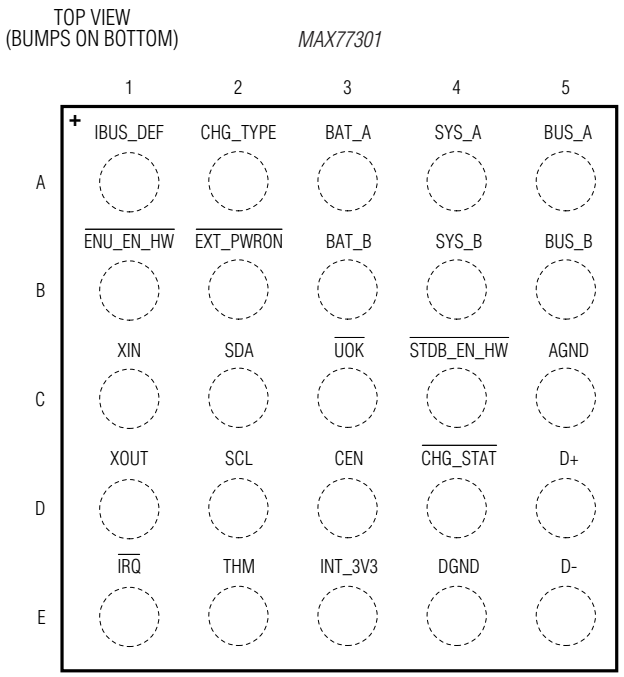
USB SUSPEND (GUI)



USB RESUME (FROM SUSPEND)



Bump Configuration



WLP
(0.4mm PITCH)

Bump Description

BUMP	NAME	FUNCTION	
A1	IBUS_DEF	Logic Input that Sets Input Current Limit. Only valid when enumeration is disabled or D+/D- are open. Logic-high programs the ILIM[2:0] register value. Logic-low sets the input current limit at 100mA.	
		Low	Input current limit = 100mA
		High	Input current limit = ILIM[2:0] (default = 500mA)
A2	CHG_TYPE	Open-drain Output. Used to signal to the processor the current capability of the external adapter. Connect this pin to ground if not used.	
		CHG_TYPE	**ADPATER TYPE**
		Low	USB 2.0 host 100mA or ILIM = 100mA
		High impedance	ILIMIT $\geq$ 500mA
A3, B3	BAT_A BAT_B	Li+ Battery Connection (V_{BAT}). Connect a single-cell Li+ battery from V_{BAT} to ground. Bypass V_{BAT} to DGND with a 10µF X5R or X7R ceramic capacitor. Both BAT_A and BAT_B must be connected together externally.	

Bump Description (continued)

BUMP	NAME	FUNCTION
A4, B4	SYS_A SYS_B	System Supply Output (V_{SYS}). Connect SYS_A and SYS_B to the system load. When a valid voltage is present at V_{BUS}, V_{SYS} is programmed by the greater of register V_SYS[1:0] or V_{BAT} + 0.14V (typ). When V_{BUS} is not present the SYS voltage is set to the battery voltage minus a small voltage drop determined by the system load. Bypass V_{SYS} to DGND with a 10µF X5R or X7R ceramic capacitor. SYS_A and SYS_B must be connected together externally.
A5, B5	BUS_A BUS_B	USB Power Input (V_{BUS}). Connect input power source to BUS_A and BUS_B. Bypass V_{BUS} to DGND with a 10µF X5R or X7R ceramic capacitor. BUS_A and BUS_B must be connected together externally.
B1	$\overline{\text{ENU\_EN\_HW}}$	Automatic Enumeration Enable. $\overline{\text{ENU\_EN\_HW}}$ is a logic-low input used to enable USB enumeration. Connect $\overline{\text{ENU\_EN\_HW}}$ to AGND to allow the IC to automatically perform enumeration. Connect to INT_3V3 or drive logic-high to disable automatic enumeration and enable adapter detection. In case of USB host/hub, do not initiate USB enumeration, but set input current according to IBUS_DEF. The nENU_EN_HW_MASK bit is used to determine if nENU_EN is controlled by $\overline{\text{ENU\_EN\_HW}}$ logic input or if controlled by I²C directly.
B2	$\overline{\text{EXT\_PWRON}}$	Open-Drain Output. Used to enable other parts of the system when valid supply is present. Connect this pin to ground if not used.
C1	XIN	Crystal Oscillator Input. For full-speed operation, connect XIN to one side of a parallel resonant 12MHz ±0.25% crystal and a 33pF capacitor to AGND. XIN can also be driven by an external clock referenced to INT_3V3. For low-speed operation only, a crystal or clock signal is not required. Connect XIN to AGND and connect XOUT to INT_3V3. In this case the internal oscillator is used, and only low-speed operation is supported.
C2	SDA	Data Input for I²C Serial Interface. Connect an external 2.2kΩ pullup resistor from SDA to the logic supply. SDA is high impedance when off.
C3	$\overline{\text{UOK}}$	Active-Low Adapter Type Detection. $\overline{\text{UOK}}$ is an open-drain output that pulls low when adapter detection is successfully completed. In USB suspend mode, $\overline{\text{UOK}}$ flashes with a duty cycle of 50% and a period of 1.5s. When D+/D- open is detected and bit nENU_EN = 1, the $\overline{\text{UOK}}$ pin flashes with a duty cycle of 50% and a period of 0.15s. When no adapter is detected, $\overline{\text{UOK}}$ is high impedance. Connect this pin to ground if not used.
C4	$\overline{\text{STDB\_EN\_HW}}$	Standby Mode Enable. $\overline{\text{STDB\_EN\_HW}}$ is a logic-low input used to force the IC into suspend mode. Connect $\overline{\text{STDB\_EN\_HW}}$ to INT_3V3 or drive logic high for automatic detect mode. In automatic detect mode the IC determines when to enter suspend mode depending on the status of SUS_EN register and USB conditions. The nSTDB_EN_HW_MASK bit determines if nSTDB_EN is controlled by $\overline{\text{STDB\_EN\_HW}}$ logic input or if controlled by I²C directly.
C5	AGND	Analog Ground. Connect AGND to quiet ground, including crystal oscillator and INT_3V3 ground nodes.
D1	XOUT	Crystal Oscillator Output. For full-speed operation, connect XOUT to one side of a parallel resonant 12MHz ±0.25% crystal and a 33pF capacitor to AGND. Connect XOUT unconnected if XIN is driven by an external clock. For low-speed operation only, a crystal or clock signal is not required. Connect XOUT to INT_3V3 and connect XIN to AGND. In this case the internal oscillator is used, and only low-speed operation is supported.

Bump Description (continued)

BUMP	NAME	FUNCTION
D2	SCL	Clock Input for Serial Interface. Connect an external 2.2kΩ pullup resistor from SCL to the logic supply. SCL is high impedance when off.
D3	CEN	Charger Enable Input. Logic-high input used to control charge status. Connect CEN to logic-high to enable battery charging when a valid source is connected at V_{BUS}. Connect to AGND or drive logic-low to disable battery charging. The $\overline{CEN\_MASK}$ bit is used to determine if CHG_EN is controlled by CEN logic input or if controlled by I²C directly.
D4	$\overline{CHG\_STAT}$	Charge Status Output. Logic-low open drain output indicating battery charging. When a temperature fault is detected, the output is pulsed at 50% duty cycle with a period of 1.5s. When a charge timer fault is detected $\overline{CHG\_STAT}$ is pulsed at 50% duty cycle with a period of 0.15s. When no battery is connected, $\overline{CHG\_STAT}$ is pulsed at a 0.1s period and 10%–20% duty cycle. Connect this pin to ground if not used.
D5	D+	USB D+ Signal. Connect a 33Ω resistor between D+ a USB connector to add signal integrity.
E1	$\overline{IRQ}$	Interrupt Request. Logic-low open-drain output that indicates when an interrupt has occurred.
E2	THM	Thermistor Input. Battery temperature detect input. Connect a negative temperature coefficient (NTC) thermistor close to the battery pack. Connect the other thermistor lead to AGND. Connect a pullup resistor from THM to INT_3V3 (47kΩ pullup resistor is recommended with a 100kΩ thermistor). Connect to AGND to disable this feature. Note the thermistor and pullup resistor are required for battery NTC detection mode.
E3	INT_3V3	3.3V Logic Supply Output. Connect a 1µF capacitor from INT_3V3 to AGND. The output is rated for up to a 10mA load. The INT_3V3 output is active whenever a valid voltage is present on BUS_ pins.
E4	DGND	Digital Ground. Connect DGND to power ground, including input capacitor, system capacitor, and battery capacitor ground nodes.
E5	D-	USB D- Signal. Connect a 33Ω resistor between D- a USB connector.

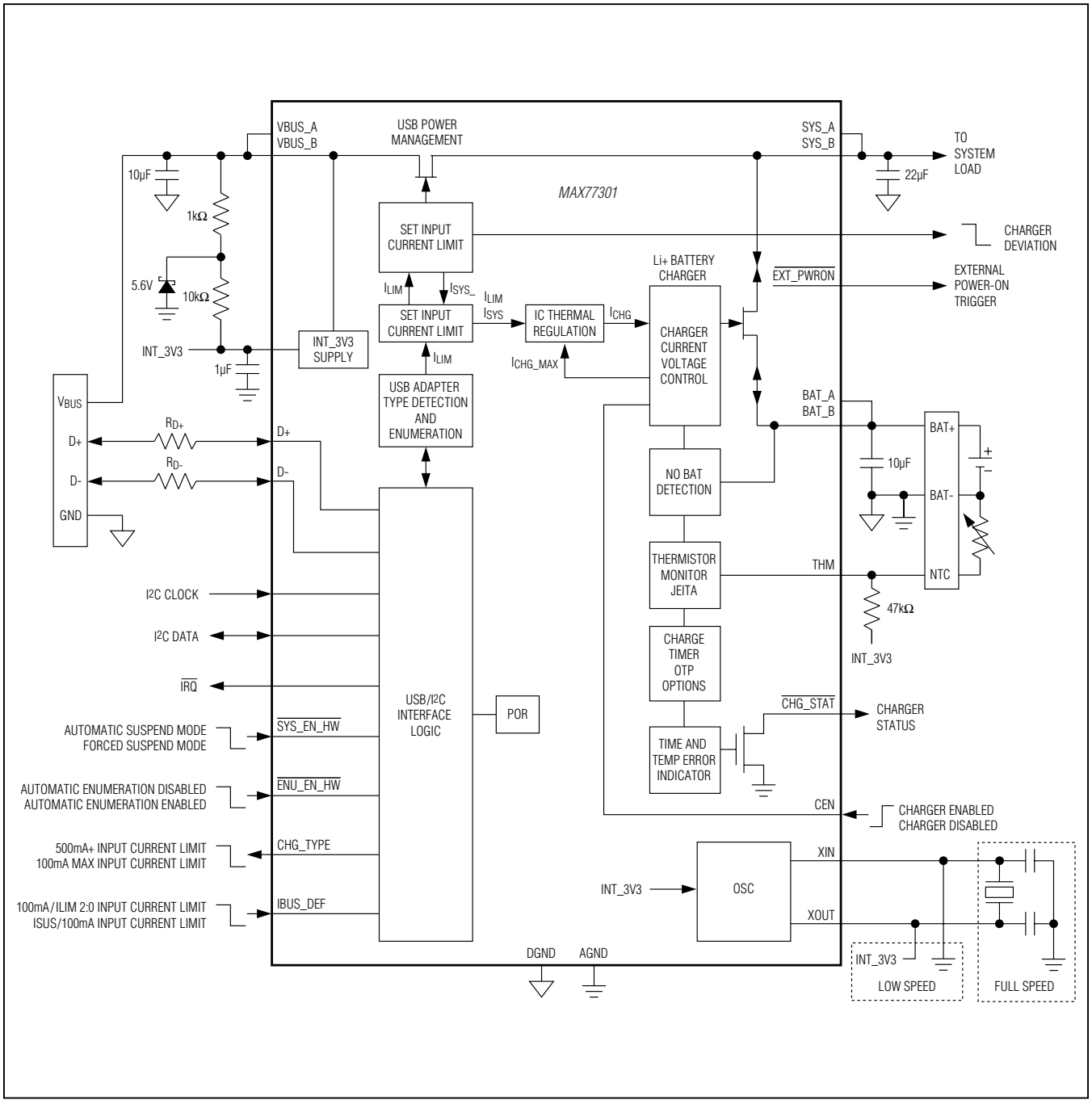


Figure 1. Block Diagram and Typical Application Circuit

Detailed Description

The MAX77301 is a USB-compliant linear battery charger that operates from a USB port, a dedicated charger, or a universal adapter. The IC provides automatic detection of adapter type and enumeration with a USB host. All power switches and charging circuitry is integrated.

The IC is capable of negotiating more than 100mA of charging current from a USB host or hub without processor intervention. Alternatively, the IC automatically detects a dedicated charger and sets the input current limit accordingly. The battery charge current and the input current limit can be set up to 900mA and 1500mA, respectively. If enumeration is disabled or a nonvalid adapter is connected to the IC the current depends on the logic level of IBUS_DEF (IBUS_DEF logic-low sets the current limit to 100mA; logic-high sets the current limit to register value ILIM[2:0] (default = 500mA).

Data Contact Detection

USB plugs are designed so that when the plug is inserted into the receptacle, the power pins make contact before the data pins make contact. This ensures that BUS voltage is applied to data pin contact.

To detect when the data pins have made contact, the data pins are prebiased so at least one of the data pins changes state. When this change is detected, the IC is allowed to check which type of port is attached.

The IC has two different modes of operation during the data contact detection.

The first mode allows up to 3s (see the *Electrical Characteristics* table) for the D+/D- to be connected. If D+/D- are still open after 3s, an interrupt is issued and the IC allows the input current to be user defined. The IC continues to monitor D+ and D- for connection.

The second mode occurs when enumeration is disabled. In this mode, the IC initiates with user defined current limit and then transitions to the ideal charging current determined by the USB enumeration engine.

Power-On Reset

To guarantee the correct startup, the IC triggers power-on reset when a valid adapter or battery is detected. Power-on reset ensures that all I²C registers are set to the default values.

When only a battery is connected to the IC and the battery voltage is above $V_{BAT\_UVLO\_F}$ all internal circuitry is powered down except the internal BAT to SYS switch, UVLO comparator, and I²C. If the battery voltage drops below $V_{BAT\_UVLO\_F}$, the I²C interface and the BAT to SYS switch are disabled.

If a valid power source is present at the BUS input, the mode of operation depends on the battery voltage.

For battery voltage above $V_{BAT\_UVLO\_F}$: The system is supported by battery power when the external adapter current limit is exceeded.

For battery voltage below $V_{BAT\_UVLO\_F}$: The system cannot be supported by an external adapter and battery power. The IC enters fault mode and the charger input current is disabled. This is done to ensure that system does not continuously attempt to start up with an underpowered adapter. Exit this mode by disconnecting the adapter. Use this mode to disconnect the charger.

Interrupt Request ($\overline{IRQ}$)

$\overline{IRQ}$ is an active-low, open-drain output signal that indicates an interrupt event has occurred and status information is available in the EVENT_ and STATUS_ registers. Interrupts indicate temperature and voltages and current fault conditions. Events are triggered by a state change in the associated register. The event registers are reset to default condition when read. When the EVENT_ registers are read in page mode the $\overline{IRQ}$ is not released until the last bit been read. New interrupt events are held until a complete read of all registers has occurred.

USB Interface

An integrated USB peripheral controller provides autoenumeration in full-speed and low-speed modes. The USB controller completes the following tasks:

- Adapter type detection, or
- USB enumeration with USB type inputs

With no crystal oscillator, the IC operates in USB low-speed mode. An external 12MHz crystal oscillator and decouling capacitors are required for USB full-speed mode. This flexibility allows the IC to interface with any USB connector type.

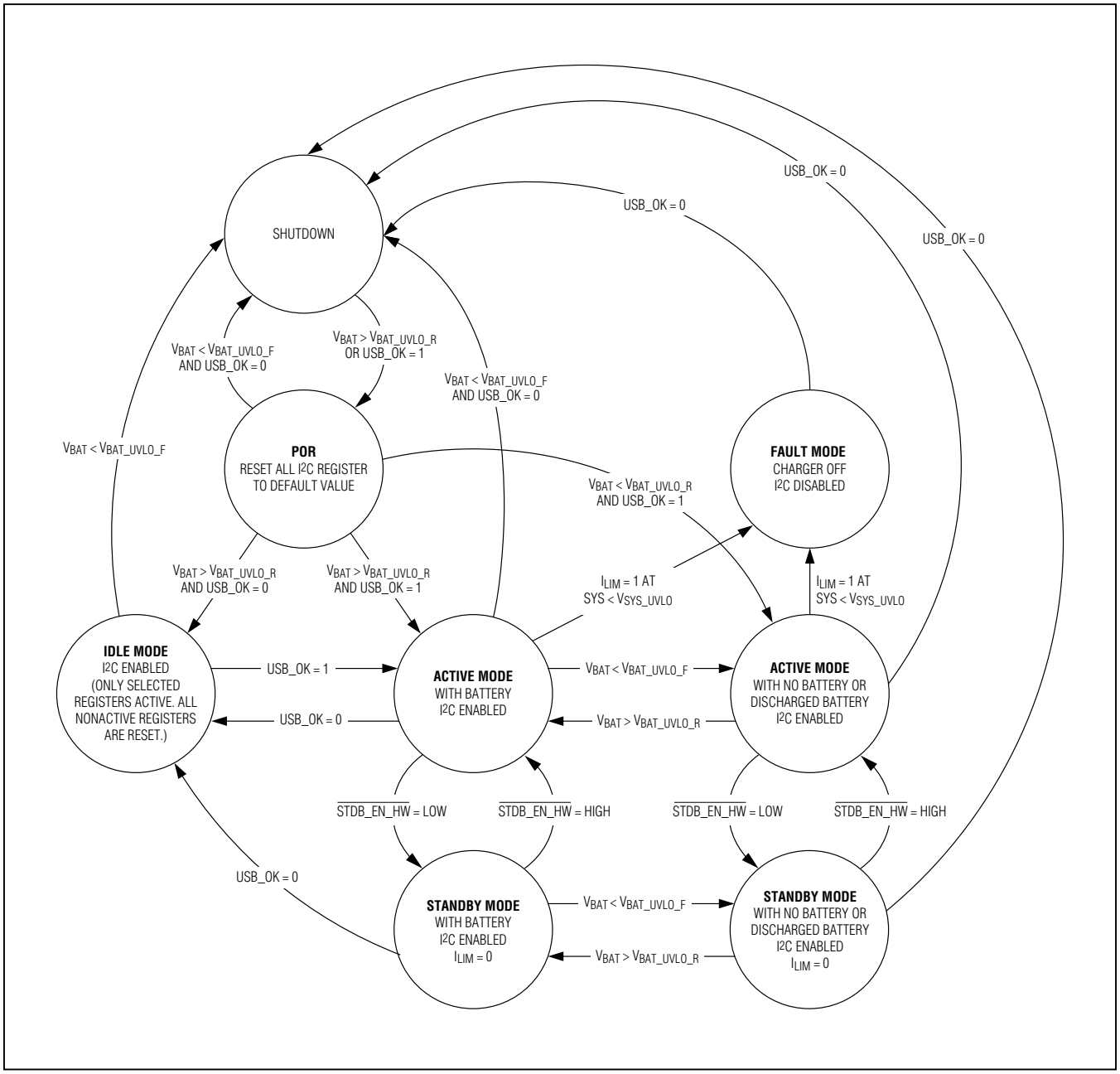


Figure 2. Power-On Reset State Diagram