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MAX77640/MAX77641

Ultra-Low Power PMIC with 3-Output SIMO, 150mA LDO, and Power Sequencer

General Description

The MAX77640/MAX77641 are a low-I_Q power solution for applications where size and efficiency are critical. The device integrates a 3-output single-inductor multiple-output (SIMO) buck-boost regulator, a 150mA LDO, and a 3-channel current-sink driver.

The SIMO operates on an input between 2.7V and 5.5V. The outputs are independently programmable between 0.8V and 5.25V depending on ordering option. Each output is a buck-boost with glitchless transition between buck and boost operation. The SIMO can support >300mA loads ($1.8V_{OUT}$, $3.7V_{IN}$).

The 150mA LDO provides ripple rejection for noise-sensitive applications. The current sinks can be programmed to blink LEDs in custom patterns. The device integrates a power sequencer to control power-up/down order of each output. Default output voltages and sequence order are factory-programmable. An I^2C serial interface further configures the device.

The MAX77640/MAX77641 are available in a 30-bump wafer-level package (WLP). Total solution size is $16mm^2$. For a similar product with a battery charger, refer to the MAX77650.

Applications

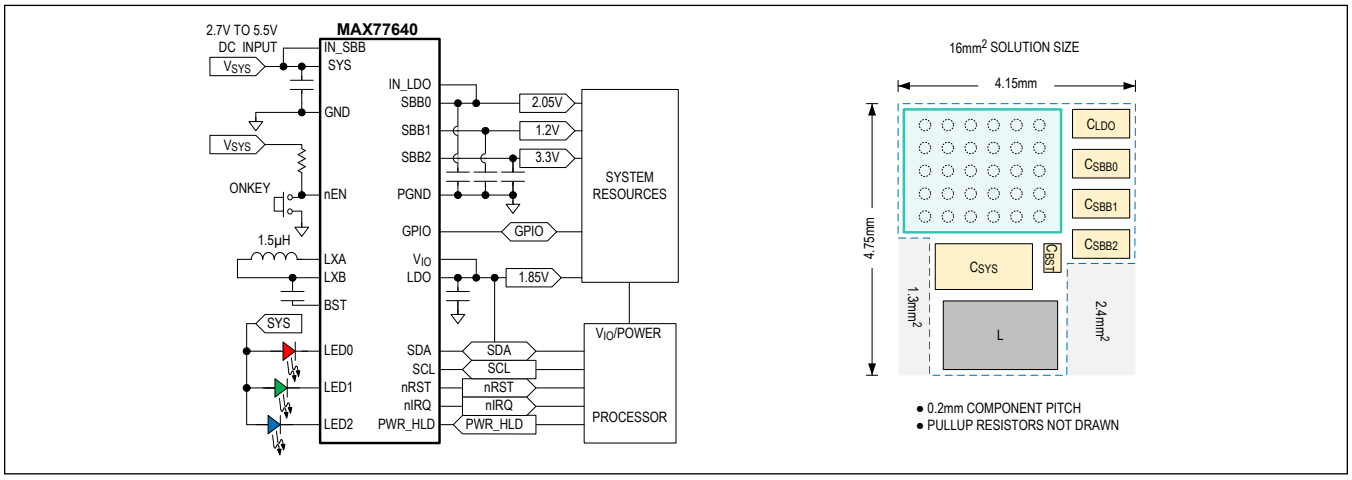
- Hearables: Bluetooth Headphones and Earbuds
- Wearables: Fitness, Health, and Activity Monitors
- Action Cameras, Wearable/Body Cameras
- Internet of Things (IoT) Gadgets

Benefits and Features

- Compact, High-Efficiency Power Solution
  - 3-Output Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
  - 150mA LDO
  - 3-Channel Current-Sink Driver
  - Flexible Power Sequencing
  - GPIO and Reset Output
- 3-Output SIMO Extends Battery Life
  - 2.7V to 5.5V Input Voltage Range from Single Cell Li-Ion
  - 0.8V to 5.25V Output Voltage Range (Table 1)
  - Supports >300mA loads ($1.8V_{OUT}$, $3.7V_{IN}$)
  - Improves Overall System Efficiency while Reducing Size
  - Maintains Regulation without Dropout unlike Traditional Bucks
  - Glitchless Buck-Boost Operation
- Low Quiescent Current
  - 300nA Shutdown Current
  - 5.6µA Operating Current (3 SIMO Channels and LDO On)
- Small Size
  - 2.75mm x 2.15mm (0.7mm max heigh) WLP
  - 30-Bump, 0.4mm Pitch, 6 x 5 Array
  - $16mm^2$ Total Solution Size

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



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Absolute Maximum Ratings

nEN, PWR_HLD, nIRQ, nRST to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, GPIO to GND .....-0.3V to V_{IO} + 0.3V
SYS to GND ..... -0.3V to +6.0V
SYS to IN_SBB ..... -0.3V to +0.3V
nIRQ, nRST, SDA, GPIO Continous Current ..... ±20mA
LDO to GND (Note 1) ..... -0.3V to V_{IN_LDO} + 0.3V
IN_LDO, V_{IO} to GND.....-0.3V to V_{SYS} + 0.3V
LED0, LED1, LED2 to LGND ..... -0.3V to +6.0V
IN_SBB to PGND ..... -0.3V to +6.0V
LXA Continuous Current (Note 1) ..... $1.2A_{RMS}$
LXB Continuous Current (Note 2) ..... $1.2A_{RMS}$
SBB0, SBB1, SBB2 to PGND (Note 3) ..... -0.3V to +6.0V
BST to IN_SBB..... -0.3V to +6.0V
BST to LXB ..... -0.3V to +6.0V
SBB0, SBB1, SBB2 Short-Circuit Duration.....Continuous
PGND to GND..... -0.3V to +0.3V
LGND to GND ..... -0.3V to +0.3V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Continuous Power Dissipation (Multilayer Board)
(T_A = +70°C, derate 20.4mW/°C above +70°C).....1632mW

Note 1: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.

Note 2: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} +0.3V.

Note 3: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

30 WLP 0.4mm Pitch

Package Code	W302H2+1
Outline Number	21-100047
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W (2s2p board)

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics—Top Level

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into SYS, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, LED0, LED1, LED2), T_A = +25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3	1	µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1.0		
			Main bias is on in normal mode (SBIA_EN = 1, SBIA_LPM = 0)		28.0		
Quiescent Supply Current	I_Q	Current measured into SYS, IN_SBB, and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. LED0, LED1, and LED2 are disabled	Main bias is in low-power mode (SBIA_LPM = 1)		5.6	13	µA
			Main bias is normal-power mode (SBIA_LPM = 0)		40	60	
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.6	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.5	2.6	2.7	V
		V_{SYS} falling, UVLO_F[3:0] = 0xF		2.75	2.85	2.95	
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.70	5.85	6.00	V
THERMAL MONITORS							
Overtemperature-Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C

Electrical Characteristics—Top Level (continued)

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
		V_{SYS} = 5.5V, V_{nEN} = 0V and 5.5V	T_A = +85°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_F}$	nEN falling			V_{SYS} - 0.9	V_{SYS} - 0.6	V
nEN Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
nEN Manual Reset Time	t_{MRST}	MRT_OTP = 0		14	16	20	s
		MRT_OTP = 1		7	8	10.5	
POWER HOLD INPUT (PWR_HLD)							
PWR_HLD Input Leakage Current	$I_{PWR\_HLD\_LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PWR_HLD} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
PWR_HLD Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
PWR_HLD Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
PWR_HLD Input Hysteresis	V_{HYS}	V_{IO} = 1.8V			50		mV
PWR_HLD Glitch Filter	$t_{PWR\_HLD\_GF}$	Both rising and falling edges are filtered			100		µs
PWR_HLD Wait Time	$t_{PWR\_HLD\_WAIT}$	Maximum time for PWR_HLD input to assert after nRST deasserts during the power-up sequence		3.5	4.0	5.0	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
nIRQ Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
nIRQ Output Falling Edge Time	t_{f_nIRQ}	$C_{\overline{IRQ}}$ = 25pF			2		ns
nIRQ Output High Leakage Current	I_{nIRQ_LKG}	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
nRST Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V

Electrical Characteristics—Top Level (continued)

(V_{SYS} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
nRST Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
nRST Output High Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
Input Leakage Current	I_{GPI_LKG}	DIR = 1, V_{IO} = 5.5V, V_{GPIO} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DBNC_GPI}	DBEN_GPI = 1			30		ms
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6 for more information			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6 for more information			2.56		ms

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE RANGE (SBB0)						
Minimum Output Voltage				0.8		V
Maximum Output Voltage				2.375		V
Output DAC Bits				6		bits

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output DAC LSB Size					25		mV
OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage		MAX77640			0.8		V
		MAX77641			2.4		
Maximum Output Voltage		MAX77640			1.5875		V
		MAX77641			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size		MAX77640			12.5		mV
		MAX77641			50		
OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage		MAX77640			0.8		V
		MAX77641			2.4		
Maximum Output Voltage		MAX77640			3.95		V
		MAX77641			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
STATIC OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage.	T_A = +25°C	-2.5		+2.5	%
			T_A = -40°C to +85°C	-4.0		+4.0	
TIMING CHARACTERISTICS							
Enable Delay		Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output.			60		µs
Soft-Start Slew Rate	dV/dt_{SS}			3.3	5.0	6.6	mV/µs
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	µA
			T_A = +85°C		+0.1		

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	µA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 5)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 4: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the Shutdown Supply Current and Quiescent Supply Current specification in the *Electrical Characteristics—Top Level* table.

Note 5: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	IN_LDO cannot exceed SYS voltage (Note 6)		1.8		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 4)			0.1	1	µA
LDO Quiescent Supply Current (Note 4)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO}= 0mA	LDO output enabled and in regulation, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V		1.7	5.15	µA
			LDO output enabled and in dropout, V_{IN_LDO} = 1.8V, V_{LDO} target is 1.85V		2.3		
Maximum Output Current	I_{OUT}			150			mA

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit	I_{LIM_LDO}	V_{LDO} externally forced to 1.3V		165	255	375	mA
GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		1.3500		2.9375	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Initial Output Voltage Accuracy		I_{LDO} = 75mA, T_A = +25°C		-2.5		+2.5	%
Output Voltage Accuracy		V_{LDO} programmed from 1.35V to 2.9375V, V_{IN_LDO} = 1.8V to 5.5V, LDO not in dropout, I_{LDO} = 0mA to 150mA, T_A = -5°C to +85°C		-3		+3	%
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 15mA, V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V	Main bias circuits are in normal-power mode (SBIA_LPM = 0)		550		μV_{RMS}
			Main bias circuits are in low-power mode (SBIA_LPM = 1)		800		
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.6	1.25	ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value, T_A = +25°C		0.5	1.25	2.50	mV/µs
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = 150mA (Note 1)			90	180	mV
Dropout On-Resistance	R_{DSON}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = I_{MAX} (Note 1)	T_A = +25°C		0.6	0.9	Ω
		V_{SYS} =3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.7V, I_{LDO} = I_{MAX} (Note 1)	T_A = +85°C			1.2	

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C (Note 7)		+0.1	+1.0	µA
			T_A = +85°C		+1.0		

Note 6: Dropout is the condition where the input voltage is in its valid input range but the output cannot be properly regulated because the input voltage is not sufficiently higher than the output voltage. See the *LDO Dropout* section for more information.

Note 7: Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

Electrical Characteristics—Current Sinks

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Current-Sink Quiescent Current	I_Q	Change in supply current at SYS when one channel is enabled and delivering 12.8mA, V_{LEDx} = 0.2V			6	12	µA
Current-Sink Leakage		All current-sink drivers combined, outputs disabled, V_{LEDx} = 5.5V	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
3.2mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b01, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.1		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			3.2		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.1		mA
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	3.10	3.20	3.25	mA
			T_A = -40ºC to +85ºC	3.03	3.20	3.36	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 2.9mA			35	70	mV
6.4mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b10, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.2		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			6.4		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.2		mA

Electrical Characteristics—Current Sinks (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	6.30	6.40	6.50	mA
			T_A = -40ºC to +85ºC	6.06	6.40	6.72	
Dropout Voltage	V_{DO}	LED_FSx[1:0] = 0b11, BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 5.75mA			35	70	mV
12.8mA CURRENT-SINK RANGE (LED_FSx[1:0] = 0b11, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.4		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			12.8		mA
Current-Sink DAC Bits					5		bits
Current-Sink DAC LSB					0.4		mA
Current-Sink Accuracy		BRT_LEDx[4:0] = 0b11111	T_A = +25ºC	12.6	12.8	13.0	mA
			T_A = -40ºC to +85ºC	12.16	12.80	13.44	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 11.5mA			35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz
TIMING CHARACTERISTICS / BLINK PERIOD SETTINGS							
Minimum Blink Period		P_LEDx[3:0] = 0b0000			0.5		s
					16		clocks
Maximum Blink Period		P_LEDx[3:0] = 0b1111			8		s
					256		clocks
Blink Period LSB					0.5		s
					16		clocks
TIMING CHARACTERISTICS / BLINK DUTY CYCLE							
Minimum Blink Duty Cycle		D_LEDx[3:0] = 0b0000			6.25		%
Maximum Blink Duty Cycle		D_LEDx[3:0] = 0b1111			100		%
Blink Duty Cycle LSB					6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 1)	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (Note 8)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (Note 8)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, Min/Max limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

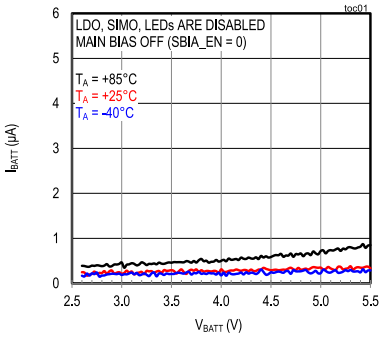
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (Note 8)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 8: Design guidance only. Not production tested.

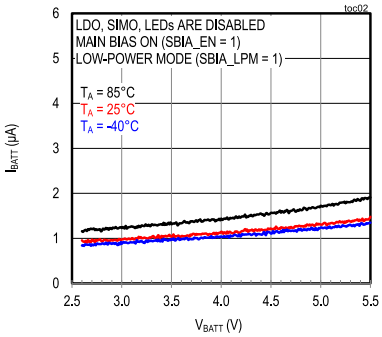
Typical Operating Characteristics

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

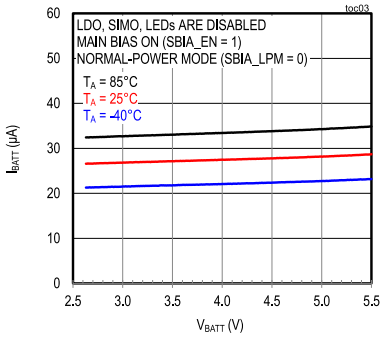
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



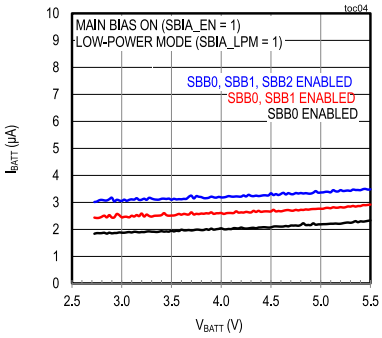
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



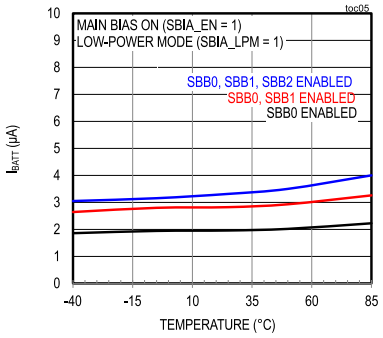
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

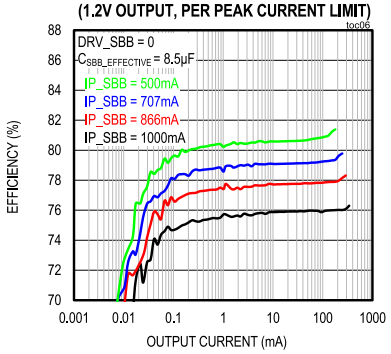


Typical Operating Characteristics (continued)

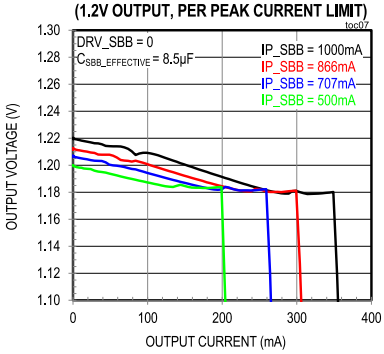
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

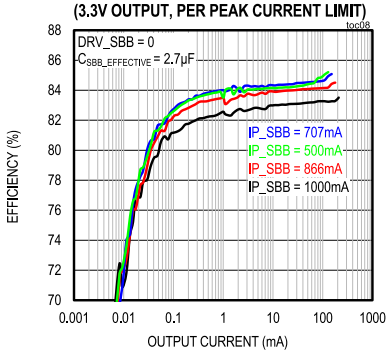
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER PEAK CURRENT LIMIT)



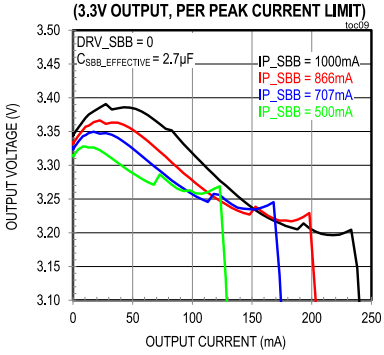
SIMO LOAD REGULATION
(1.2V OUTPUT, PER PEAK CURRENT LIMIT)



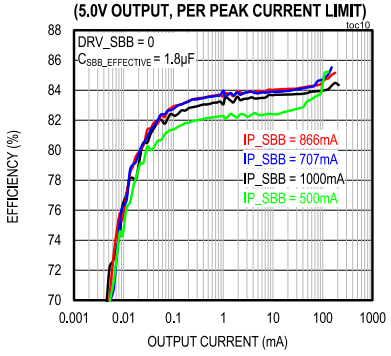
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER PEAK CURRENT LIMIT)



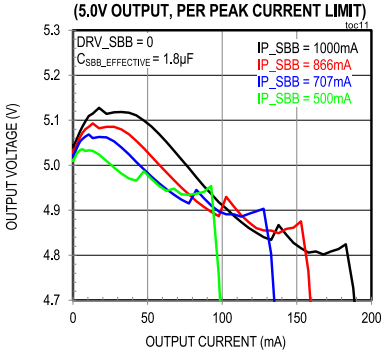
SIMO LOAD REGULATION
(3.3V OUTPUT, PER PEAK CURRENT LIMIT)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER PEAK CURRENT LIMIT)



SIMO LOAD REGULATION
(5.0V OUTPUT, PER PEAK CURRENT LIMIT)

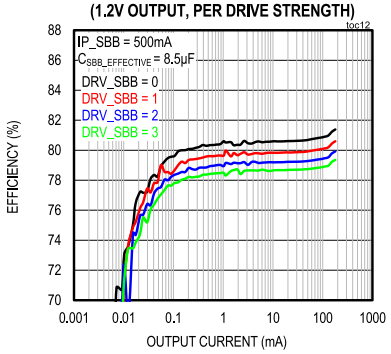


Typical Operating Characteristics (continued)

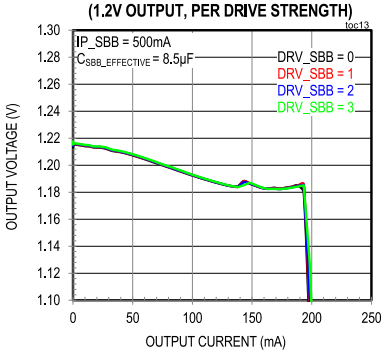
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

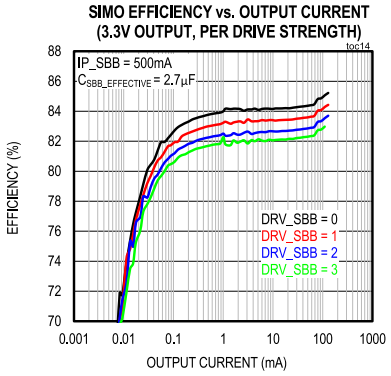
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER DRIVE STRENGTH)



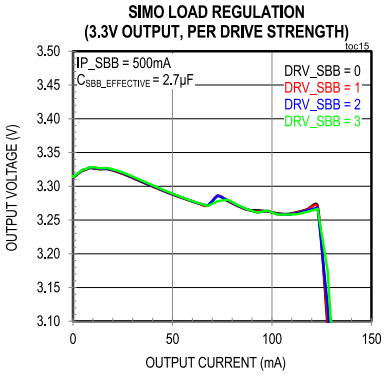
SIMO LOAD REGULATION
(1.2V OUTPUT, PER DRIVE STRENGTH)



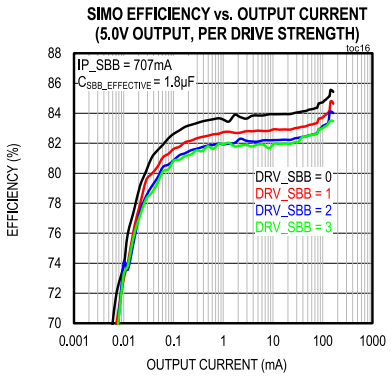
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER DRIVE STRENGTH)



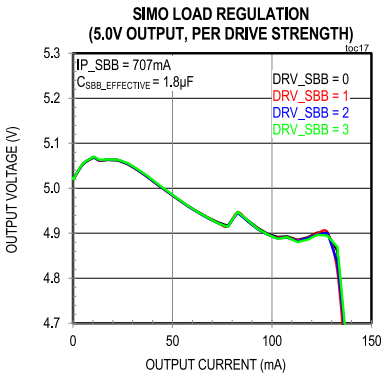
SIMO LOAD REGULATION
(3.3V OUTPUT, PER DRIVE STRENGTH)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER DRIVE STRENGTH)



SIMO LOAD REGULATION
(5.0V OUTPUT, PER DRIVE STRENGTH)

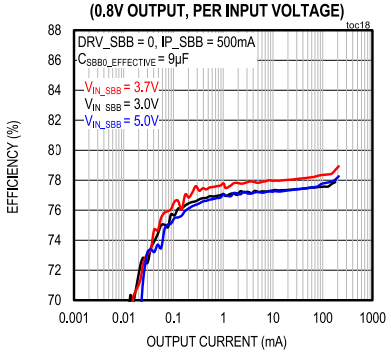


Typical Operating Characteristics (continued)

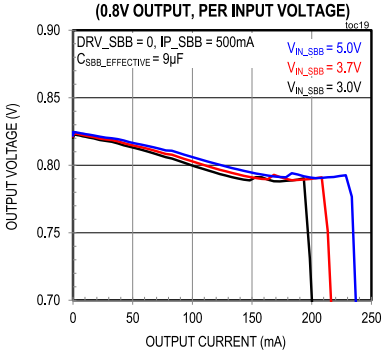
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

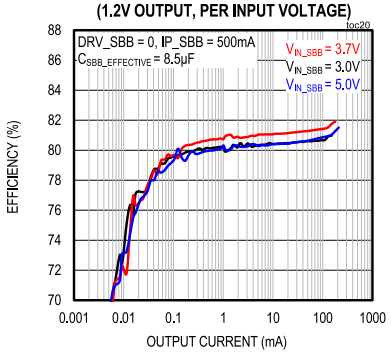
SIMO EFFICIENCY vs. OUTPUT CURRENT
(0.8V OUTPUT, PER INPUT VOLTAGE)



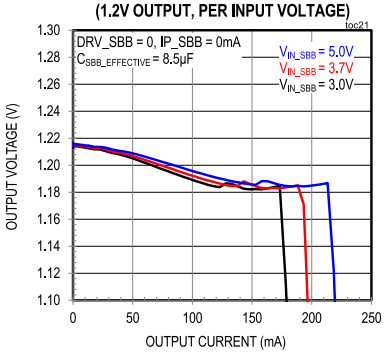
SIMO LOAD REGULATION
(0.8V OUTPUT, PER INPUT VOLTAGE)



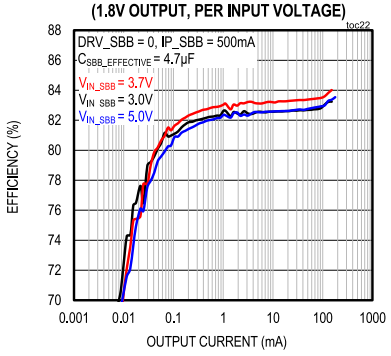
SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.2V OUTPUT, PER INPUT VOLTAGE)



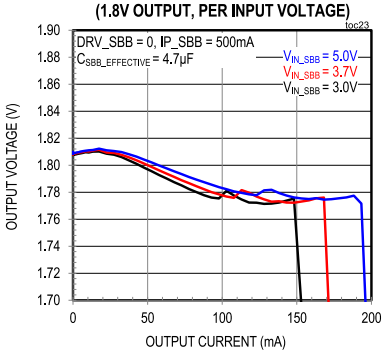
SIMO LOAD REGULATION
(1.2V OUTPUT, PER INPUT VOLTAGE)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(1.8V OUTPUT, PER INPUT VOLTAGE)



SIMO LOAD REGULATION
(1.8V OUTPUT, PER INPUT VOLTAGE)

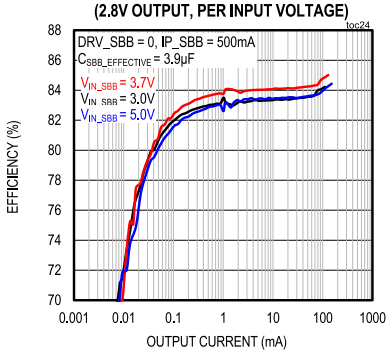


Typical Operating Characteristics (continued)

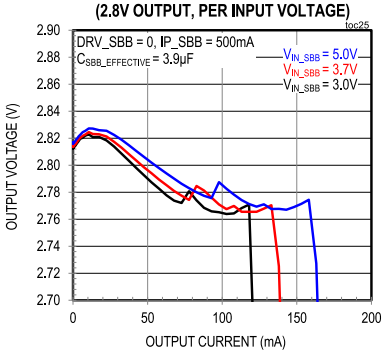
(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

(Inductor = Toko DFE201210S-2R2M, 2.2µH, 127mΩ, ISAT = 1.5A, 2.0x1.2x1.0mm)

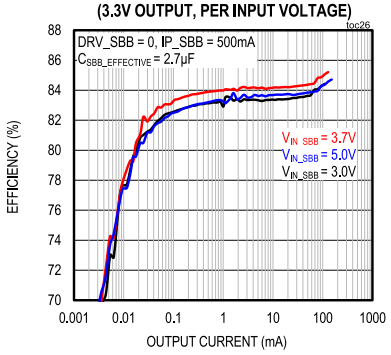
SIMO EFFICIENCY vs. OUTPUT CURRENT
(2.8V OUTPUT, PER INPUT VOLTAGE)



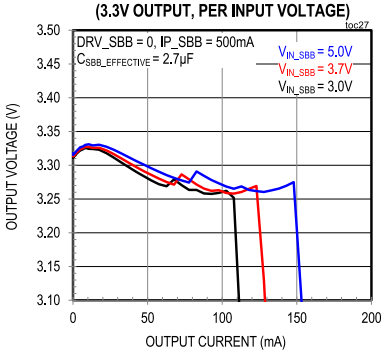
SIMO LOAD REGULATION
(2.8V OUTPUT, PER INPUT VOLTAGE)



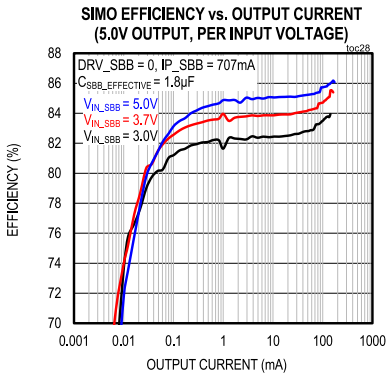
SIMO EFFICIENCY vs. OUTPUT CURRENT
(3.3V OUTPUT, PER INPUT VOLTAGE)



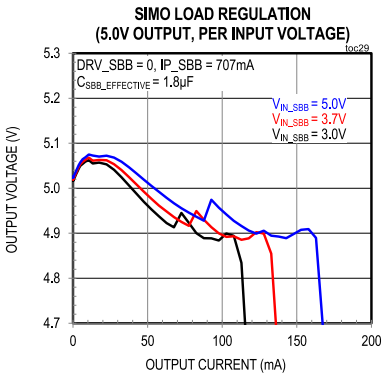
SIMO LOAD REGULATION
(3.3V OUTPUT, PER INPUT VOLTAGE)



SIMO EFFICIENCY vs. OUTPUT CURRENT
(5.0V OUTPUT, PER INPUT VOLTAGE)



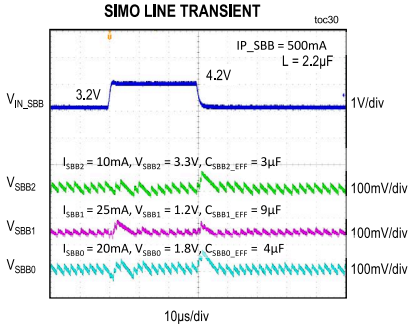
SIMO LOAD REGULATION
(5.0V OUTPUT, PER INPUT VOLTAGE)



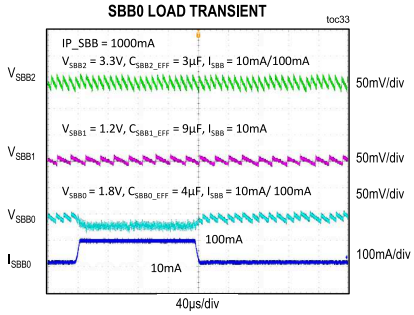
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

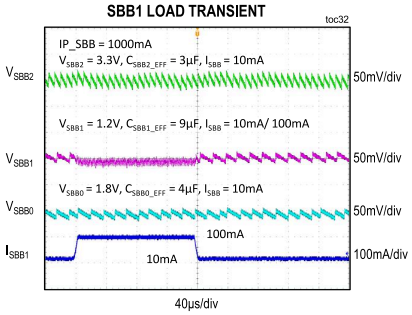
SIMO LINE TRANSIENT



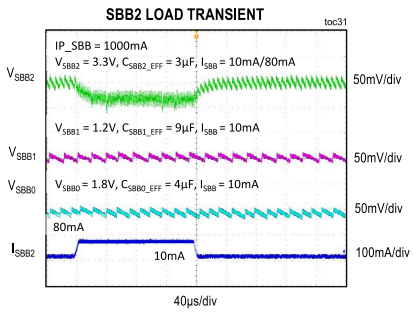
SBB0 LOAD TRANSIENT



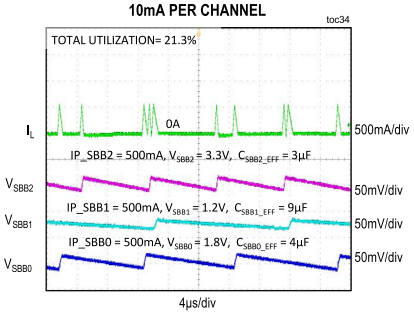
SBB1 LOAD TRANSIENT



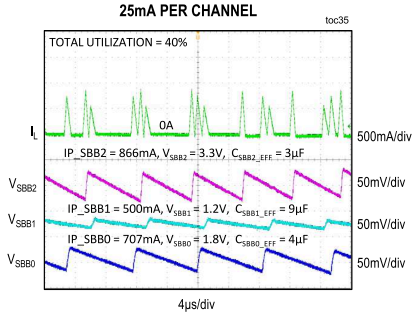
SBB2 LOAD TRANSIENT



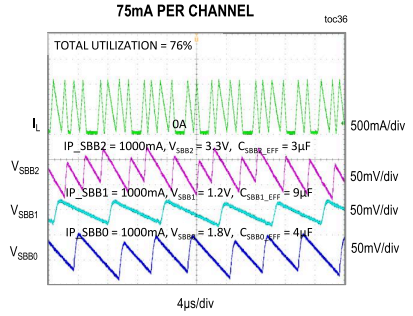
SIMO SWITCHING WAVEFORMS
LIGHT UTILIZATION
10mA PER CHANNEL



SIMO SWITCHING WAVEFORMS
MEDIUM UTILIZATION
25mA PER CHANNEL



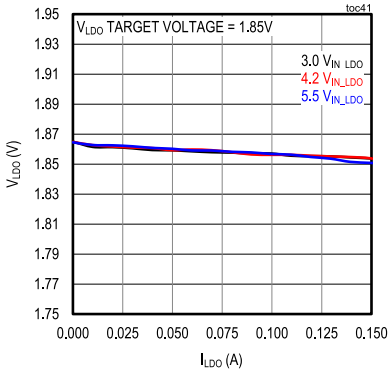
SIMO SWITCHING WAVEFORMS
HEAVY UTILIZATION
75mA PER CHANNEL



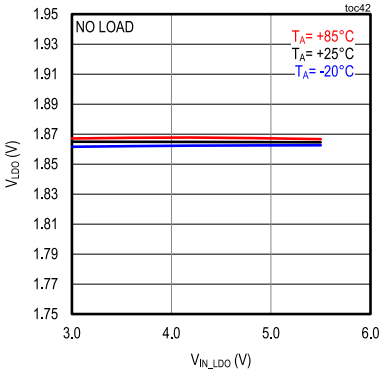
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

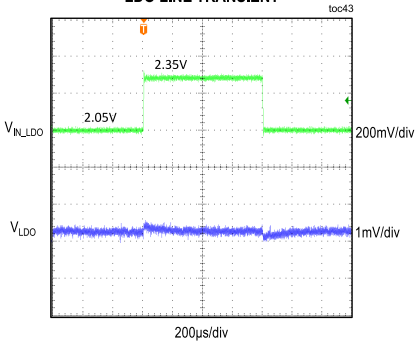
LDO LOAD REGULATION



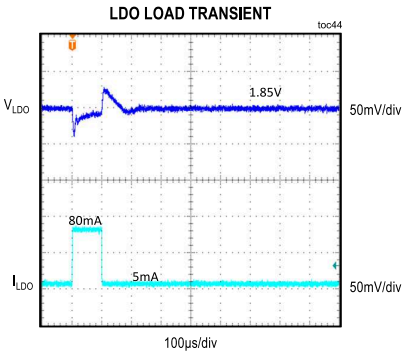
LDO LINE REGULATION



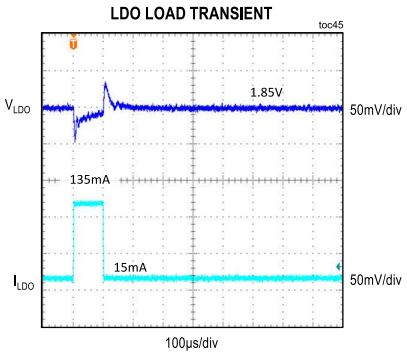
LDO LINE TRANSIENT



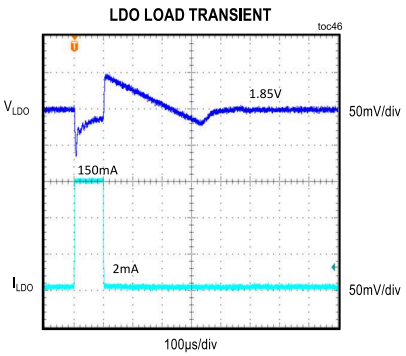
LDO LOAD TRANSIENT



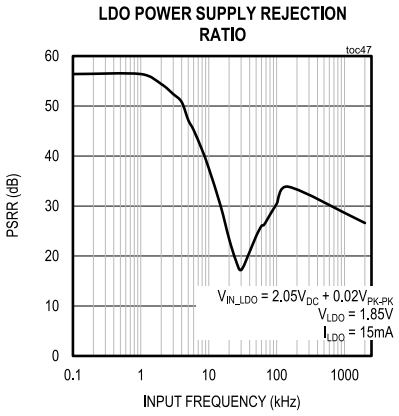
LDO LOAD TRANSIENT



LDO LOAD TRANSIENT



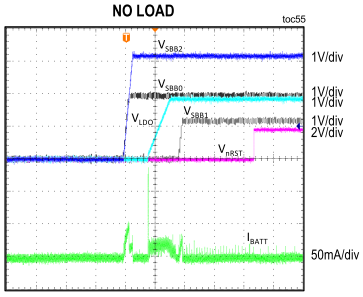
LDO POWER SUPPLY REJECTION RATIO



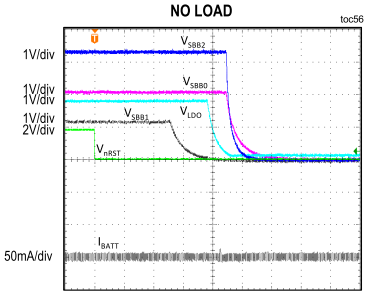
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{SYS} = V_{IN_SBB} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

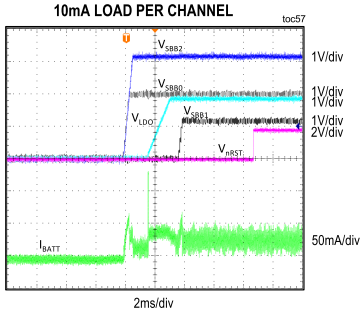
POWER UP
NO LOAD



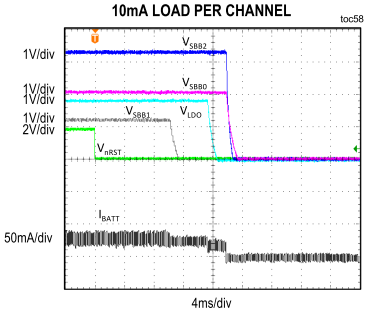
POWER DOWN
NO LOAD



POWER UP
10mA LOAD PER CHANNEL

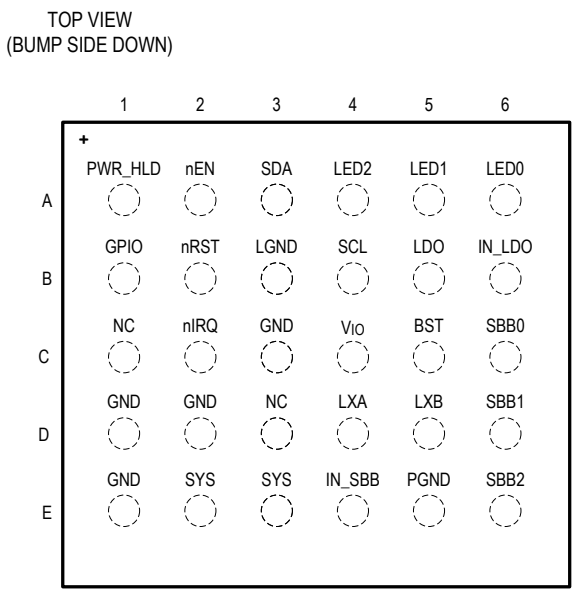


POWER DOWN
10mA LOAD PER CHANNEL



Bump Configuration

MAX77640/MAX77641



WLP
(2.75mm x 2.15mm x 0.7mm)

Bump Descriptions

PIN	NAME	FUNCTION	TYPE
TOP LEVEL			
A1	PWR_HLD	Active-High Power Hold Input. Assert PWR_HLD to keep the on/off controller in its on state. If PWR_HLD is not needed, connect it to SYS and use the SFT_RST bits to power the device down.	digital input
A2	nEN	Active-Low Enable Input. nEN supports push-button or slide-switch configurations. An external pullup resistor (10kΩ to 100kΩ) to SYS is required.	digital input
A3	SDA	I^2C Data	digital i/o
B4	SCL	I^2C Clock	digital input
B1	GPIO	General Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}.	digital i/o
B2	nRST	Active-Low, Open-Drain Reset Output. Connect a 100kΩ pullup resistor between nRST and a voltage equal to or less than V_{SYS}.	digital output
C2	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
E2, E3	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the device. Connect to IN_SBB and bypass to GND with a 22µF ceramic capacitor.	power input
C3, D1, D2, E1	GND	Quiet Ground. Connect GND to PGND, LGND, and the low-impedance ground plane of the PCB.	ground