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MAX77650/MAX77651

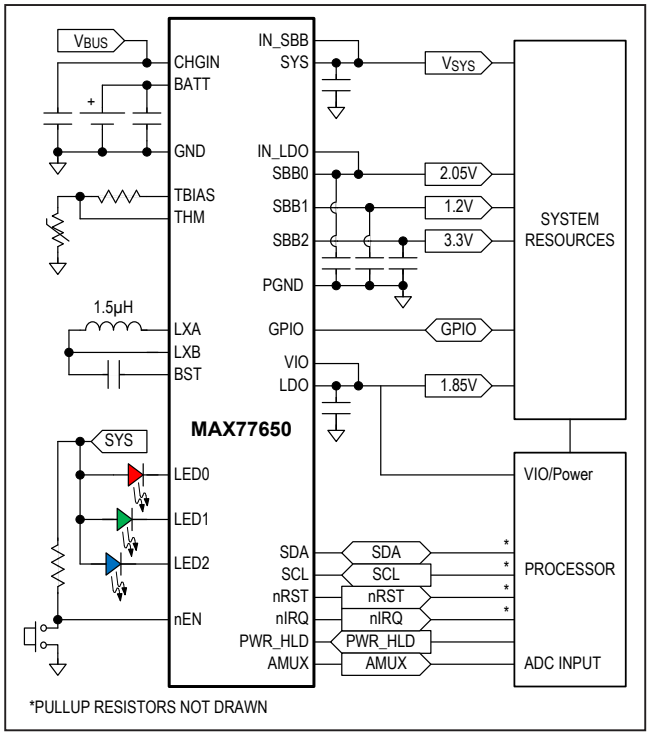
Ultra-Low Power PMIC with 3-Output SIMO and Power Path Charger for Small Li+

General Description

The MAX77650/MAX77651 provide highly-integrated battery charging and power supply solutions for low-power wearable applications where size and efficiency are critical. Both devices feature a SIMO buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. A 150mA LDO provides ripple rejection for audio and other noise-sensitive applications. A highly configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA).

The devices include other features such as current sinks for driving LED indicators and an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I²C interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality when the devices are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Simplified Application Circuit



Benefits and Features

- Highly Integrated
  - Smart Power Selector™ Li+/Li-Poly Charger
  - 3 Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
  - 150mA LDO
  - 3-Channel Current Sink Driver
  - Analog MUX Output for Power Monitoring
- Low Power
  - 0.3µA Shutdown Current
  - 5.6µA Operating Current (3 SIMO Channels + LDO)
- Charger Optimized for Small Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Flexible and Configurable
  - I²C Compatible Interface and GPIO
  - Factory OTP Options Available
- Small Size
  - 2.75mm x 2.15mm x 0.7mm WLP Package
  - 30-Bump, 0.4mm-Pitch WLP, 6x5 Array
  - Small Total Solution Size (19.2mm²)

Applications

- Bluetooth Headphones/Hearables
- Fitness, Health, and Activity Monitors
- Portable Devices
- Internet of Things (IoT)

***Ordering Information* appears at end of data sheet.**

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

19-8550; Rev 6; 7/18

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Absolute Maximum Ratings

nEN, PWR_HLD, nIRQ, nRST to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, GPIO to GND .....-0.3V to V_{IO} + 0.3V
CHGIN to GND .....-0.3V to +30.0V
SYS, BATT to GND .....-0.3V to +6.0V
SYS to IN_SBB .....-0.3V to +0.3V
V_L to GND .....-0.3V to +6.0V
AMUX, THM, TBIAS to GND .....-0.3V to +6.0V
nIRQ, nRST, SDA, AMUX, GPIO Continous Current .....±20mA
CHGIN Continuous Current .....$1.2A_{RMS}$
SYS Continuous Current .....$1.2A_{RMS}$
BATT Continuous Current (Note 1) .....$1.2A_{RMS}$
LDO to GND (Note 2) .....-0.3V to V_{IN_LDO} + 0.3V
IN_LDO, V_{IO} to GND ..... -0.3V to the lower of (V_{SYS} + 0.3V) and +6.0V
LED0, LED1, LED2 to LGND .....-0.3V to +6.0V
IN_SBB to PGND .....-0.3V to +6.0V
LXA Continuous Current (Note 3) .....$1.2A_{RMS}$
LXB Continuous Current (Note 4) .....$1.2A_{RMS}$
SBB0, SBB1, SBB2 to PGND (Note 2) .....-0.3V to +6.0V
BST to IN_SBB .....-0.3V to +6.0V
BST to LXB .....-0.3V to +6.0V
SBB0, SBB1, SBB2 Short-Circuit Duration .....Continuous
PGND to GND .....-0.3V to +0.3V
LGND to GND .....-0.3V to +0.3V
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C
Continuous Power Dissipation (Multilayer Board)
(T_A = +70°C, derate 20.4mW/°C above +70°C) 1632mW

Note 1: Do not repeatedly hot-plug a source to the BATT terminal at a rate greater than 10Hz. Hot plugging low-impedance sources results in an ~8A momentary (~2µs) current spike.
Note 2: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.
Note 3: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.
Note 4: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} + 0.3V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

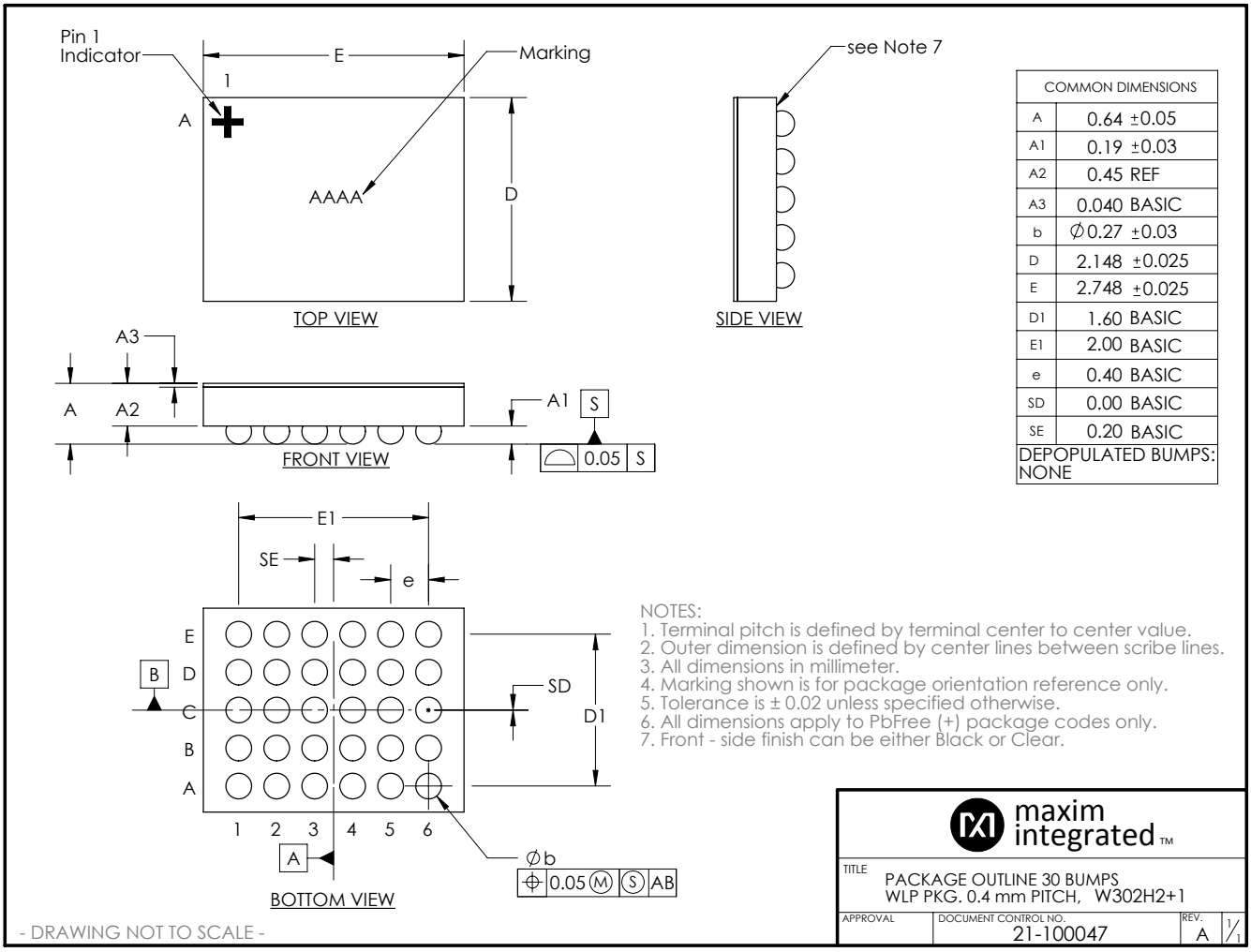
Package Information

PACKAGE CHARACTERISTICS	VALUES
Package Code	W302H2+1
Outline Number	**21-100047**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	49°C/W (2s2p board)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Package Information (continued)



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.040 BASIC
b	∅0.27 ±0.03
D	2.148 ±0.025
E	2.748 ±0.025
D1	1.60 BASIC
E1	2.00 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE		
PACKAGE OUTLINE 30 BUMPS WLP PKG. 0.4 mm PITCH, W302H2+1		
APPROVAL	DOCUMENT CONTROL NO. 21-100047	REV. A

Electrical Characteristics—Top Level

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into BATT and SYS and IN_SBB and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, LED0, LED1, LED2), T_A = 25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3	1	µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1		
			Main bias is on in normal-power mode (SBIA_EN = 1, SBIA_LPM = 0)		28		
Quiescent Supply Current	I_Q	Current measured into BATT and SYS and IN_SBB and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. LED0, LED1, and LED2 are disabled	Main bias is in low-power mode (SBIA_LPM = 1)		5.6	13	µA
			Main bias is in normal-power mode (SBIA_LPM = 0)		40	60	

Electrical Characteristics—Global Resources

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.6	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.5	2.6	2.7	V
		V_{SYS} falling, UVLO_F[3:0] = 0xF		2.75	2.85	2.95	
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.70	5.85	6.00	V
THERMAL MONITORS							
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_F}$	nEN falling			V_{SYS} - 0.9	V_{SYS} - 0.6	V
Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
Manual Reset Time	t_{MRST}	MRT_OTP = 0		14	16	20	s
		MRT_OTP = 1		7	8	10.5	
POWER HOLD INPUT (PWR_HLD)							
PWR_HLD Input Leakage Current	$I_{PWR\_HLD\_LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PWR_HLD} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
PWR_HLD Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
PWR_HLD Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
PWR_HLD Input Hysteresis	V_{HYS}	V_{IO} = 1.8V			50		mV
PWR_HLD Glitch Filter	$t_{PWR\_HLD\_GF}$	Both rising and falling edges are filtered			100		µs
PWR_HLD Wait Time	$t_{PWR\_HLD\_WAIT}$	Maximum time for PWR_HLD input to assert after nRST deasserts during the power-up sequence		3.5	4.0	5.0	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	C_{IRQ} = 25pF			2		ns
Leakage Current	I_{nIRQ_LKG}	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), VnIRQ = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 and Figure 7 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
Input Leakage Current	I_{GPI_LKG}	DIR = 1, V_{IO} = 5.5V, V_{GPIO} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DBNC_GPI}	DBEN_GPI = 1			30		ms
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6			2.56		ms

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage Lockout Hysteresis				500		mV
Input Current Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0].	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms
SUPPLY AND QUIESCENT CURRENTS						
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		5		µA
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), Charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0A			50	µA
CHGIN Suspend Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)			50	µA
PREQUALIFICATIONS						
Charge Current Soft-Start Slew Time		Zero to full scale		1		ms
Input Current Soft-Start Slew Time		Zero to full scale		1		ms
Prequalification Voltage Threshold Range	V_{PQ}	Charger is in prequalification mode when V_{BATT} < V_{PQ}, this threshold has 100mV of hysteresis, programmable in 100mV steps with CHG_PQ[2:0]	2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V	-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 0		10		%
		V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V	27	30	33	minutes

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST CHARGE						
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]	3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]	7.5		300	mA
Fast-Charge Current Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-1.5		+1.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], from prequal done to timer fault	3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours	-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, loading conditions and/or a weak charging source caused charge current to drop below this threshold, expressed as a percentage of $I_{FAST-CHG}$		20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG[2:0]	60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise		-5.4		%/°C
TERMINATION AND TOPOFF						
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)		5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)		7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		10		
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)		15		

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C	1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C	27	30	33	
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]	0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes	-10		+10	%
Charge Restart Threshold	$V_{RESTART}$	CHG = 0 (charging done), charging resumes when V_{BATT} < $V_{FAST-CHG}$ - $V_{RESTART}$	65	150		mV
DEVICE ON-RESISTANCE AND LEAKAGE						
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS		100		mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = 25°C, charger disabled		0.1	1.0	µA
		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = 85°C, charger disabled		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V		600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +25°C, body-switched diode reverse biased		0.1	1.0	µA
		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +85°C, body-switched diode is reverse biased		1		
SYSTEM NODE						
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]	4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = +25°C	4.41	4.50	4.59	V
		$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = -40°C to +85°C	4.365	4.500	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, V_{SYS} < $V_{SYS-REG}$ due to I_{CHGIN} = $I_{CHGIN-LIM}$ (input in current-limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)	4.34	4.4	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA		V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5ºC increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5ºC increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5ºC increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5ºC increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTC β = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTC β = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs						
Full-Scale Voltage	V_{FS}			1.25		V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting		0.26		V/V
CHGIN POWER						
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting		2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}		0.167		V/V
BATT MONITOR						
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CHG_CC[5:0])		12.5		mV/%

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA		-0.5		+0.65	mA
Battery Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V
ANALOG MULTIPLEXER							
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
THM AND TBIAS							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE RANGE (SBB0)							
Minimum Output Voltage					0.8		V
Maximum Output Voltage					2.375		V
Output DAC Bits					6		bits
Output DAC LSB Size					25		mV
OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage		MAX77650			0.8		V
		MAX77651			2.4		
Maximum Output Voltage		MAX77650			1.5875		V
		MAX77651			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size		MAX77650			12.5		mV
		MAX77651			50		
OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage		MAX77650			0.8		V
		MAX77651			2.4		
Maximum Output Voltage		MAX77650			3.95		V
		MAX77651			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage (Note 3)	T_A = +25°C	-2.5		+2.5	%
			T_A = -40°C to +85°C	-4.0		+4.0	
TIMING CHARACTERISTICS							
Enable Delay		Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output.			60		µs
Soft-Start Slew Rate	dV/dt_{SS}			3.3	5.0	6.6	mV/µs

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	µA
			T_A = +85°C		+0.1		
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	µA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 4)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 3: Measured in an open-loop test that determines the output voltage falling threshold where LXA switches high.

Note 4: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	IN_LDO cannot exceed SYS voltage (Note 5)		1.8		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 6)			0.1	1	µA
LDO Quiescent Supply Current (Note 6)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO} = 0mA	LDO output enabled and in regulation, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V		1.7	5.15	µA
			LDO output enabled and in dropout, V_{IN_LDO} = 1.8V, V_{LDO} target is 1.85V		2.3		
Maximum Output Current	I_{OUT}			150			mA
Current Limit		V_{LDO} externally forced to 1.3V		165	255	375	mA
OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		1.3500		2.9375	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Initial Output Voltage Accuracy		I_{LDO} = 75mA, T_A = +25°C		-2.5		+2.5	%
Output Voltage Accuracy		V_{LDO} programmed from 1.35V to 2.9375V, V_{IN_LDO} = 1.8V to 5.5V, LDO not in drop-out, I_{LDO} = 0mA to 150mA, T_A = -5°C to +85°C		-3		+3	%
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 15mA, V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V	Main bias circuits are in normal-power mode (SBIA_LPM = 0)		550		μV_{RMS}
			Main bias circuits are in low-power mode (SBIA_LPM = 1)		800		

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.6	1.25	ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value. T_A = +25°C		0.5	1.25	2.50	mV/µs
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.8V, I_{LDO} = 150mA (Note 5)			90	180	mV
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C (Note 7)		+0.1	+1.0	µA
			T_A = +85°C		+1.0		
Dropout On-Resistance	R_{DSON}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.8V, I_{LDO} = I_{MAX}, (Note 5)	T_A = +25°C		0.6	0.9	Ω
			T_A = +85°C			1.2	

Note 5: Dropout is the condition where the input voltage is in its valid input range but the output cannot be properly regulated because the input voltage is not sufficiently higher than the output voltage. The dropout voltage is the difference between the input voltage and the output voltage when the regulator is in dropout. The dropout on-resistance is the resistance of the power MOSFET between the input and the output when the regulator is in dropout. Generally speaking, applications should avoid dropout by having sufficient input voltage. A dropout detection interrupt is available (DOD_R; see the *Programmer's Guide* for more information). For example, applications with the output voltage target of 1.85V and the maximum load current is 80mA (ILDO_MAX), has a dropout voltage of 96mV (V_{LDO_DO} = ILDO_MAX x RDSON_LDO = 80mA x 1.2Ω = 96mV). To avoid dropout, the input voltage should be 1.95V (V_{IN_LDO} = V_{LDO} + V_{LDO_DO}).

Note 6: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the shutdown supply current and quiescent supply current specification in the *Electrical Characteristics—Top Level* table.

Note 7: Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

Electrical Characteristics—Current Sinks

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Current Sink Quiescent Current	I_Q	Change in supply current at SYS when one channel is enabled and delivering 12.8mA, V_{LEDx} = 0.2V			6	12	µA
Current Sink Leakage		All current sink drivers combined, outputs disabled, V_{LEDx} = 5.5V	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
3.2mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b01, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.1		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			3.2		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.1		mA
Current Sink Accuracy		T_A = +25ºC		3.10	3.20	3.25	mA
		T_A = -40ºC to +85ºC		3.03	3.20	3.36	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 2.9mA			35	70	mV
6.4mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b10, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.2		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			6.4		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.2		mA
Current Sink Accuracy		T_A = +25ºC		6.30	6.40	6.50	mA
		T_A = -40ºC to +85ºC		6.06	6.40	6.72	
Dropout Voltage	V_{DO}	LED_FSx[1:0] = 0b11, BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 5.75mA			35	70	mV
12.8mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b11, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.4		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			12.8		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.4		mA
Current Sink Accuracy		T_A = +25ºC		12.6	12.8	13.0	mA
		T_A = -40ºC to +85ºC		12.16	12.80	13.44	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 11.5mA			35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz

Electrical Characteristics—Current Sinks (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS/BLINK PERIOD SETTINGS						
Minimum Blink Period				0.5		s
				16		clocks
Maximum Blink Period				8		s
				256		clocks
Blink Period LSB				0.5		s
				16		clocks
TIMING CHARACTERISTICS/BLINK DUTY CYCLE						
Minimum Blink Duty Cycle		D_LEDx[3:0] = 0b0000		6.25		%
Maximum Blink Duty Cycle		D_LEDx[3:0] = 0b1111		100		%
Blink Duty Cycle LSB				6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 2)	t_{OF}				120	ns

Electrical Characteristics—I²C (continued)

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST MODE PLUS) (Note 8)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 100pF) (Note 8)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Electrical Characteristics—I²C (continued)

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (Note 8)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 8: Design guidance only. Not production tested.