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MAX77734

Ultra-Low Power Tiny PMIC with Power Path Charger for Small Li+ and 150mA LDO

General Description

The MAX77734 is a tiny PMIC for applications where size and simplicity are critical. The IC integrates a linear-mode Li+ battery charger, low-dropout linear regulator (LDO), analog multiplexer, and dual-channel current sink driver.

The charger is designed for small-battery systems that require accurate termination as low as 0.375mA. The circuit can instantly regulate the system voltage when an input source is connected even if the battery is depleted.

The 150mA LDO's output is programmable between 0.8V and 3.975V with I²C. The analog MUX enables an external ADC to perform conversions on battery V&I signals for power monitoring. The current sinks are capable of sinking 12.8mA each and can be programmed for LEDs to blink in custom patterns.

The MAX77734 is available in a 20-bump, 0.4mm pitch wafer-level package (WLP). For a similar product with additional regulators, see the MAX77650.

Applications

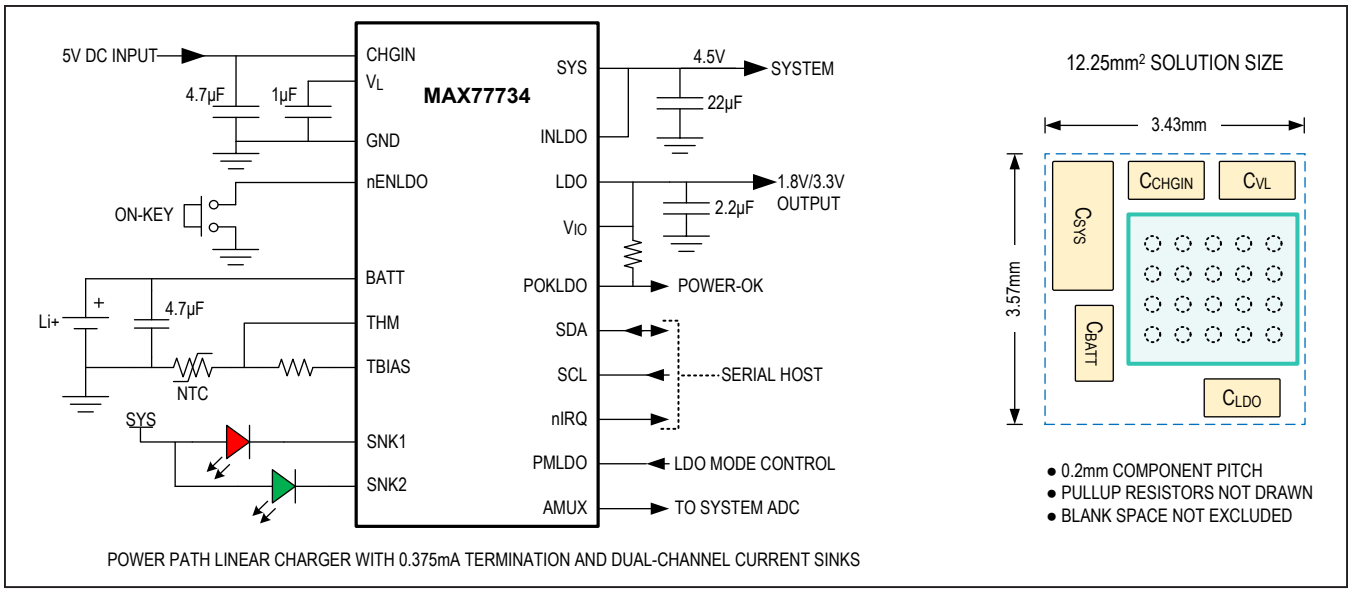
- Hearables: Headsets, Headphones, Earbuds
- Fitness Bands and other Bluetooth Wearables
- Action Cameras, Wearable/Body Cameras
- Low-Power Internet of Things (IoT) Gadgets

Benefits and Features

- Extends Battery Life
  - 200nA Factory-Ship Mode for Long Shelf Life
  - 500nA Shutdown Current
  - 4.5µA Quiescent Current with LDO Enabled
  - Charger Allows Battery to Relax after Charging
- Linear Charger Optimized for Small Battery Size
  - 7.5mA to 300mA Fast-Charge Current
  - Battery Regulation Voltage from 3.6V to 4.6V
  - Accurate Termination Current as low as 0.375mA
  - Instant-On Functionality provided by Maxim's Smart Power Selector™
  - JEITA Battery Temperature Monitors for Safe Charging
- Highly Integrated
  - 150mA LDO with Power-OK Output
  - Dual-Channel Current Sink for LEDs
  - Analog Multiplexer for Power Monitoring
  - Watchdog Timer
  - On-Key Input for LDO Enable and Manual Reset
- Small Size
  - 2.23mm x 1.97mm (0.5mm max height) WLP
  - 20-Bump, 0.4mm Pitch, 4 x 5 Array
  - 12.25mm² Total Solution Size

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



POWER PATH LINEAR CHARGER WITH 0.375mA TERMINATION AND DUAL-CHANNEL CURRENT SINKS

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

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Absolute Maximum Ratings

nIRQ, POKLDO to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, PMLDO to GND .....-0.3V to V_{IO} + 0.3V
nENLDO to GND (Note 1)..... -0.3V to V_{CCINT} + 0.3V
CHGIN to GND.....-0.3V to +30.0V
SYS, BATT to GND .....-0.3V to +6.0V
V_L to GND .....-0.3V to +6.0V
AMUX, THM, TBIAS to GND.....-0.3V to +6.0V
nIRQ, POKLDO Continuous Current.....±3mA
SDA, AMUX Continuous Current .....±20mA
CHGIN, SYS, BATT Continuous Current .....1.2A_{RMS}
LDO to GND..... -0.3V to V_{INLDO} + 0.3V
INLDO, V_{IO} to GND .....-0.3V to V_{SYS} + 0.3V
SNK1, SNK2 to GND .....-0.3V to +6.0V
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C
Continuous Power Dissipation (70°C ambient).....
WLP (derate 18mW/°C above +70°C) 1440mW

Note 1: V_{CCINT} is internally connected to either BATT or V_L. Refer to *nENLDO Pullup Resistors to V_{CCINT} (V_{CC} Internal)* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE CHARACTERISTICS	VALUES
Package Code	N201B2+1
Outline Number	**21-100154**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	55.49 °C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Voltage Range	V_{SYS}			2.7		5.5	V
BATT Factory-Ship Mode Current	$I_{BATT-FSM}$	Factory-ship mode (BATT to SYS switch open), T_A = +25°C, V_{BATT} = 3.7V, V_{SYS} = V_{INLDO} = 0V			0.2	1	µA
BATT Shutdown Current	$I_{BATT-SHDN}$	Shutdown state (all resources and bias off), BATT to SYS switch closed, T_A = +25°C, no load			0.5	1	µA
BATT Standby Current	$I_{BATT-STDBY}$	Standby state (all resources off), BATT to SYS switch closed, no load	Bias enabled in low-power mode (BIAS_REQ = 1, BIAS_LPM = 1)		1.5		µA
			Bias enabled in normal mode (BIAS_REQ = 1, BIAS_LPM = 0)		30		
BATT Quiescent Current	I_{BATT-Q}	Resource on state, BATT to SYS switch closed, current sinks and analog MUX disabled, V_{LDO} = 1.2V, no load	Bias is in low-power mode (BIAS_LPM = 1), LDO enabled in low-power mode		4.5	10	µA
			Bias is in low-power mode (BIAS_LPM = 1), LDO enabled in normal mode		22	40	
			Bias is in normal mode (BIAS_LPM = 0), LDO enabled in normal mode		40	60	
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.5	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling		2.65	2.85	3.05	V
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$				150		mV

Electrical Characteristics (continued)

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.55	5.85	6.15	V
THERMAL MONITORS							
Over-Temperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C
ENABLE INPUT (nENLDO)							
nENLDO Leakage Current	$I_{nENLDO-LKG}$	V_{BATT} = 5.5V, V_{nENLDO} = 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
nENLDO Falling Threshold	$V_{TH\_nENLDO\_F}$	nENLDO Falling		V_{CCINT} - 1.4	V_{CCINT} - 1.0		V
nENLDO Rising Threshold	$V_{TH\_nENLDO\_R}$	nENLDO Rising			V_{CCINT} - 0.9	V_{CCINT} - 0.6	V
V_{CC} Internal	V_{CCINT}	(Note 2)	V_{CHGIN} = 0V, battery is present (V_{BATT} is valid)		V_{BATT}		V
			V_{CHGIN} = 5V, not USB suspended (USBS = 0)		V_L		
nENLDO Pullup	R_{nEN-PU}	Pullup to V_{CCINT}	PU_DIS = 0		200		kΩ
			PU_DIS = 1		10000		
Debounce Time	t_{DBNC_nENLDO}	Rising and falling, not in factory-ship mode	DB_nENLDO = 0 (Note 3)		200		µs
			DB_nENLDO = 1		30		ms
	$t_{FSM-EXDB}$	Falling only, factory-ship mode (Note 4)			250		
Manual Reset Time	t_{MRST}	T_MRST = 0		5	8	10	s
		T_MRST = 1		10	16	20	
Watchdog Timer Period	t_{WD}	WDT_PER[1:0] = 0b11		89	128	154	s

Electrical Characteristics (continued)

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERRUPT OUTPUT (nIRQ)							
nIRQ Output Low Voltage	$V_{nIRQ-LO}$	Sinking 2mA				0.4	V
nIRQ Leakage Current	$I_{nIRQ-LKG}$	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 3.6V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage-Lockout Hysteresis				500		mV
Input Current-Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA
Input Current-Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0]	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND QUIESCENT CURRENTS							
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS[3:0] indicate done), I_{SYS} = 0mA			1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0mA				50	µA
CHGIN Suspend Supply Current	$I_{CHGIN-SUS}$	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)				50	µA
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS[3:0] indicate done), I_{SYS} = 0mA			5		µA
PREQUALIFICATION							
Charge Current Soft-Start Slew Time		Zero to full-scale			1		ms
Prequalification Voltage Threshold Range	V_{PQ}	Programmable in 100mV steps with CHG_PQ[2:0]		2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V		-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$	I_PQ = 0		10		%
			I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V		27	30	33	minutes
FAST-CHARGE							
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]		3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA	$V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
			$V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]		7.5		300	mA

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast-Charge Current Accuracy		T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	$I_{FAST-CHG}$ = 15mA	-1.5		+1.5	%
			$I_{FAST-CHG}$ = 300mA	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV, T_A = -40°C to +85°C		-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], time measured from prequal done to timer fault		3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours		-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, fast-charge safety timer paused when charge current drops below this threshold, expressed as a percentage of $I_{FAST-CHG}$			20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG[2:0]		60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise			-5.4		%/°C
TERMINATION AND TOPOFF							
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)			5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)			7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		8.5	10	11.5	
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)			15		
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]		0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes		-10		+10	%

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Restart Threshold	$V_{RESTART}$	Charging is finished (CHG_DTLS[3:0] indicate done), charging resumes when $V_{BATT} < V_{FAST-CHG} - V_{RESTART}$		65	150		mV
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C		1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C		27	30	33	
End-of-Charge Termination Current Glitch Filter					60		µs
DEVICE ON-RESISTANCE AND LEAKAGE							
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS			100	150	mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, charger disabled	T_A = +25°C		0.1	1.0	µA
			T_A = +85°C		1		
		V_{SYS} = 0V, V_{BATT} = 4.2V, factory-ship mode	T_A = +25°C		0.1	1.0	
			T_A = +85°C		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V, I_{CHGIN} = 400mA			600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, body-switched diode reverse biased	T_A = +25°C		0.1	1.0	µA
			T_A = +85°C		1		
SYSTEM NODE							
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]		4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA	T_A = +25°C	4.41	4.50	4.59	V
		VSYS-REG = 4.5V, ISYS = 1mA	T_A = -40°C to +85°C	4.365	4.5	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, $V_{SYS} < V_{SYS-REG}$ due to $I_{CHGIN} = I_{CHGIN-LIM}$ (input in current limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)		4.34	4.4	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA			V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5ºC increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5ºC increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5ºC increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5ºC increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTC β = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTC β = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER							
Full-Scale Voltage	V_{FS}				1.25		V
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
CHGIN POWER MEASUREMENT							
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting			2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}			0.167		V/V
BATT AND SYS POWER MEASUREMENT							
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CHG_CC[5:0])			12.5		mV/%
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA		-0.5		+0.8	mA
Battery-Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting			0.26		V/V
THM AND TBIAS VOLTAGE MEASUREMENT							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—Linear Regulator

(V_{SYS} = V_{INLDO} = 3.7V, C_{SYS} = 22µF, C_{LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO							
INLDO Voltage Range	V_{INLDO}	INLDO cannot exceed V_{SYS} by 0.3V		1.7		5.5	V
INLDO Supply Current	$I_{INLDO-Q}$	V_{LDO} = 1.2V, no load	Low-power mode		1.5		µA
		V_{LDO} = 1.2V, no load	Normal mode		12		
LDO Output Voltage Range	$V_{LDO-REG}$	Target regulation voltage. Programmable in 25mV steps with LDO_VREG[6:0].		0.8		3.975	V
LDO Output Voltage Accuracy	V_{LDO}	V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings, bias in normal mode	I_{LDO} = 0.1mA to 150mA, T_A = -5°C to +85°C, normal mode	-2		+2	%
			I_{LDO} = 0.1mA to 150mA, T_A = -40°C, normal mode	-3		+3	
			I_{LDO} = 0.1mA to 5mA, low-power mode	-6.5		+6.5	
LDO Maximum Output Current	I_{LDO}	Normal mode (Note 7)		150			mA
		Low-power mode (Note 7)		5			
Load Regulation		V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings	I_{LDO} = 0.1mA to 150mA, normal mode		0.5		%
			I_{LDO} = 0.1mA to 5mA, low-power mode		0.5		
Line Regulation		I_{LDO} = 0.1mA, V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings	Normal mode		0.05		%/V
			Low-power mode		0.05		
Dropout Voltage	V_{DO}	I_{LDO} = 150mA, normal mode (Note 6)	V_{INLDO} = 3.0V, $V_{LDO-REG}$ = 3.3V		60	150	mV
		I_{LDO} = 150mA, Normal Mode (Note 6)	V_{INLDO} = 1.7V, $V_{LDO-REG}$ = 1.85V		100		
LDO Current Limit	$I_{LDO-LIM}$	V_{LDO} = 90% of programmed target	Normal mode	160	300	560	mA
			Low-power mode		40		
LDO Output Capacitance for Stability	C_{LDO}	(Note 5)		1.1	2.2		µF
LDO Startup Ramp Rate	$\Delta V_{LDO}/\Delta t$	10% to 90% of final value			20		mV/µs

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = V_{INLDO} = 3.7V, C_{SYS} = 22µF, C_{LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		LDO and bias in normal mode, f = 10Hz to 100kHz, I_{LDO} = 15mA	V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 0.8V		100		μV_{RMS}
			V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 1.0V		150		
			V_{SYS} = V_{INLDO} = 2.7V, V_{LDO} = 2.0V		200		
			V_{SYS} = V_{INLDO} = 3.7V, V_{LDO} = 3.0V		300		
			V_{SYS} = V_{INLDO} = 5.5V, V_{LDO} = 3.975V		400		
Power-Supply Rejection Ratio	PSRR	LDO in normal-power mode, bias in low-power mode, V_{SYS} =3.6V, V_{INLDO} =2.8V+20mVpp, f = 10Hz to 1kHz, V_{LDO} =1.8V, I_{LDO} =15mA			60		dB
Active Discharge Resistance	R_{AD_LDO}				100		Ω
LDO POWER-OK OUTPUT (POKLDO)							
POKLDO Threshold	V_{POKLDO_R}	V_{LDO} rising, expressed as a percentage of $V_{LDO-REG}$		82.5	87.5	92.5	%
	V_{POKLDO_F}	V_{LDO} falling, expressed as a percentage of $V_{LDO-REG}$		79	84	89	
POKLDO Low Voltage	V_{POKLDO}	POKLDO = low, sinking 2mA				0.4	V
POKLDO Leakage Current	$I_{POKLDO-LKG}$	V_{SYS} = V_{IO} = 5.5V, POKLDO is high-Z, V_{POKLDO} = 0V or 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
LDO POWER-MODE INPUT (PMLDO)							
PMLDO Logic-High Threshold	V_{PMLDO_HI}			0.7 x V_{IO}			V
PMLDO Logic-Low Threshold	V_{PMLDO_LO}					0.3 x V_{IO}	V
PMLDO Debounce Timer	$t_{PMLDO-DB}$	(Note 3)			200		µs
PMLDO Leakage Current	$I_{PMLDO-LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PMLDO} = 0V or 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Dual-Channel Current Sink Driver

(V_{SYS} = 3.7V, V_{SNKx} = 0.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DUAL-CHANNEL CURRENT SINK DRIVER							
Current Sink Quiescent Current	ΔI_{BATT-Q}	Change in supply current when one channel is enabled and delivering 12.8mA, V_{SNKx} = 0.2V			6		µA
Current Sink Leakage		All current sink drivers combined, outputs disabled, V_{SNKx} = 5.5V,	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
Sink Current Range	I_{SNKx}	Programmable with BRT_SNKx[4:0]	SNK_FSx[1:0] = 0b01	0.1		3.2	mA
			SNK_FSx[1:0] = 0b10	0.2		6.4	
			SNK_FSx[1:0] = 0b11	0.4		12.8	
3.2mA CURRENT SINK RANGE (SNK_FSx[1:0]=0b01)							
Current Sink DAC Bits					5		bits
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b01, T_A = +25ºC	3.10	3.20	3.25	mA
			SNK_FSx[1:0] = 0b01, T_A = -40ºC to +85ºC	2.975	3.20	3.425	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b01, I_{SNKx} = 2.9mA		35	70	mV
6.4mA CURRENT SINK RANGE (SNK_FSx[1:0] =0b10)							
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b10, T_A = +25ºC	6.30	6.40	6.50	mA
			SNK_FSx[1:0] = 0b10, T_A = -40ºC to +85ºC	5.95	6.40	6.85	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b10, I_{SNKx} = 5.75mA		35	70	mV
12.8mA CURRENT SINK RANGE (SNK_FSx[1:0]=0b11)							
Current Sink Accuracy		BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b11, T_A = +25ºC	12.6	12.8	13.0	mA
			SNK_FSx[1:0] = 0b11, T_A = -40ºC to +85ºC	11.9	12.8	13.7	
Dropout Voltage	V_{DO}	BRT_SNKx[4:0] = 0b11111	SNK_FSx[1:0] = 0b11, I_{SNKx} = 11.5mA		35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz

Electrical Characteristics—Dual-Channel Current Sink Driver (continued)

(V_{SYS} = 3.7V, V_{SNKx} = 0.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS / BLINK PERIOD SETTINGS						
Minimum Blink Period		P_SNKx[3:0] = 0b0000		0.5		s
				16		clocks
Maximum Blink Period		P_SNKx[3:0] = 0b1111		8		s
				256		clocks
Blink Period LSB				0.5		s
				16		clocks
TIMING CHARACTERISTICS / BLINK DUTY CYCLE						
Minimum Blink Duty Cycle		D_SNKx[3:0] = 0b0000		6.25		%
Maximum Blink Duty Cycle		D_SNKx[3:0] = 0b1111		100		%
Blink Duty Cycle LSB				6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = 3.7V, V_{IO}= 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE/I/O STAGE						
V_{IO} Voltage Range	V_{IO}		1.7		3.6	V
V_{IO} Bias Current		T_A = +25°C	-1	0	+1	µA
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V or 3.6V	-10		10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance		(Note 8)		10		pF
Input Filter Suppressed Spike Maximum Pulse Width	t_{SP}	(Note 8)		50		ns

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = 3.7V, V_{IO}= 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE/TIMING						
Clock Frequency	f_{SCL}				1	MHz
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		260			ns
SCL Low Period	t_{LOW}		500			ns
SCL High Period	t_{HIGH}		260			ns
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns

Note 2: See the *nENLDO Pullup Resistors to V_{CCINT} (V_{CC} Internal)* section of the data sheet.

Note 3: Digitally debounced for two consecutive 100µs clock periods. Typical debounce time is at least 200µs and up to 300µs due to synchronization to the digital clock.

Note 4: This is the amount of additional debounce time required to exit factory-ship mode (250ms, typ additional time).

Note 5: For stability, guaranteed by design and not production tested.

Note 6: The dropout voltage is the difference between the input voltage and the output voltage when the input voltage is within the valid input voltage range, but below the output voltage setpoint. For example, if the output voltage setpoint is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{DO} = V_{INLDO} - V_{LDO}).

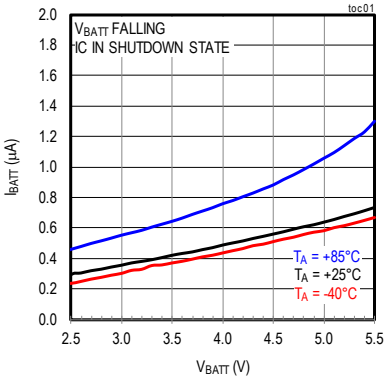
Note 7: The "Maximum Output Current" is guaranteed by the "Output Voltage Accuracy" tests.

Note 8: Design guidance only. Not production tested.

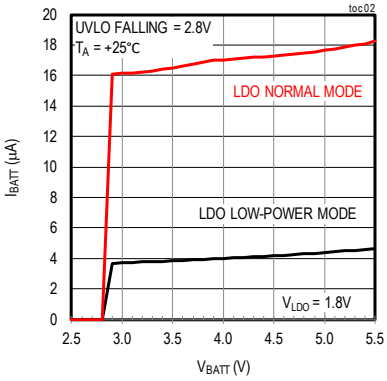
Typical Operating Characteristics

(*Typical Application Circuits*, V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, $V_{SYS-REG}$ = 4.5V, BIAS in low-power mode, LDO in normal mode, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

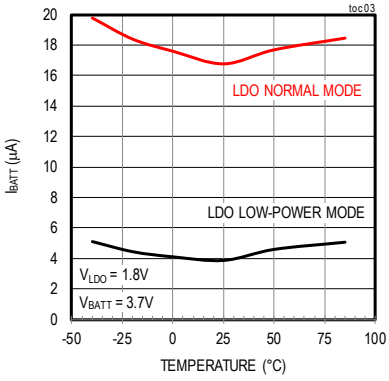
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



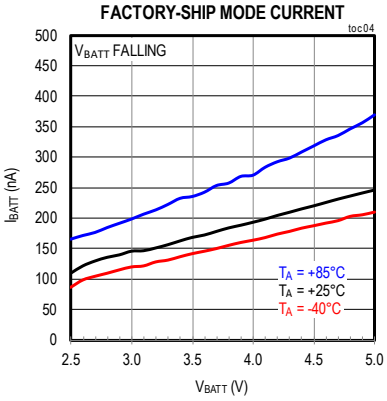
QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



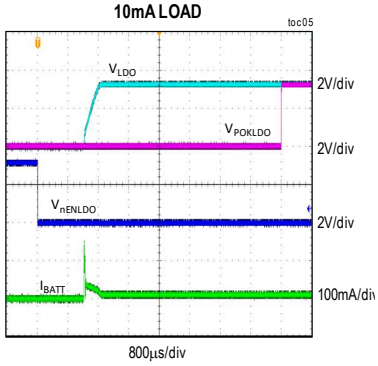
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



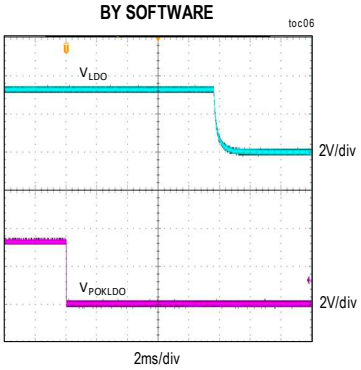
FACTORY-SHIP MODE CURRENT



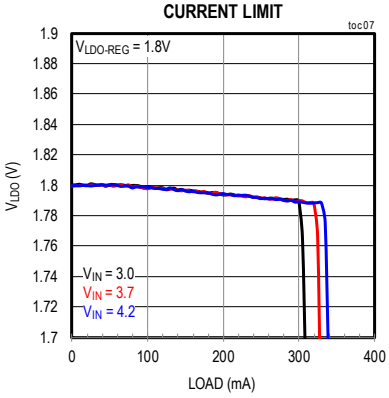
LDO POWER-UP CAUSED BY BUTTON PRESS (LDO_WAKE) 10mA LOAD



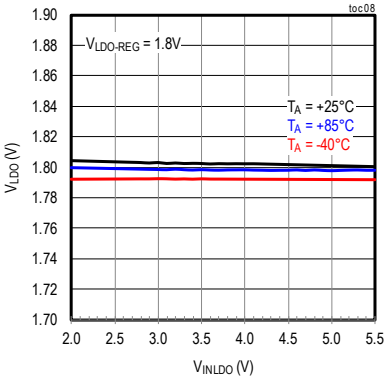
LDO POWER-DOWN CAUSED BY SOFTWARE



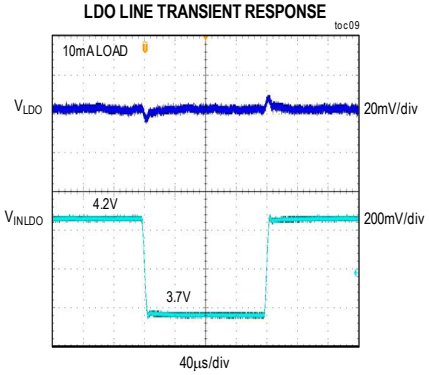
LDO LOAD REGULATION AND CURRENT LIMIT



LDO LINE REGULATION



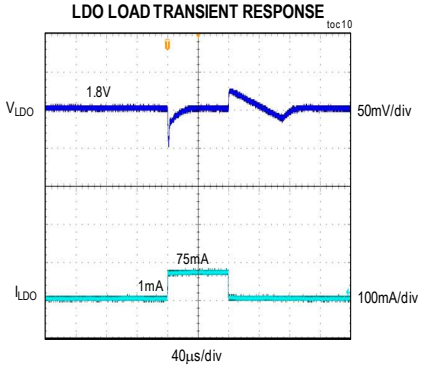
LDO LINE TRANSIENT RESPONSE



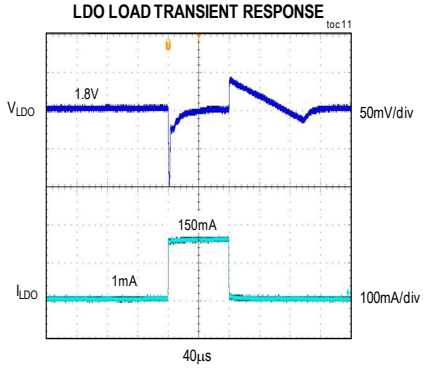
Typical Operating Characteristics (continued)

(*Typical Application Circuits*, V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{INLDO} = 3.7V, V_{IO} = 1.8V, $V_{SYS-REG}$ = 4.5V, BIAS in low-power mode, LDO in normal mode, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

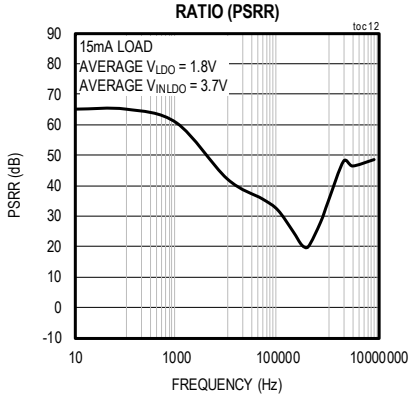
LDO LOAD TRANSIENT RESPONSE



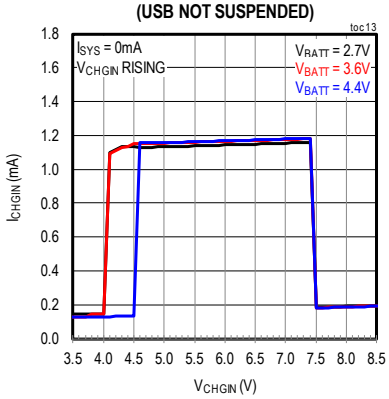
LDO LOAD TRANSIENT RESPONSE



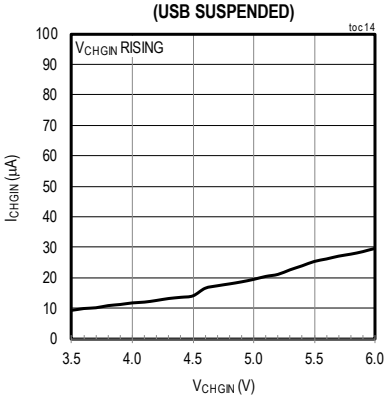
LDO POWER SUPPLY REJECTION RATIO (PSRR)



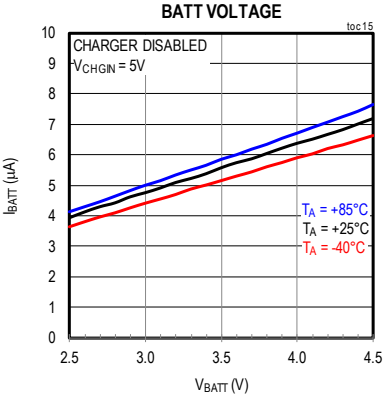
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE (USB NOT SUSPENDED)



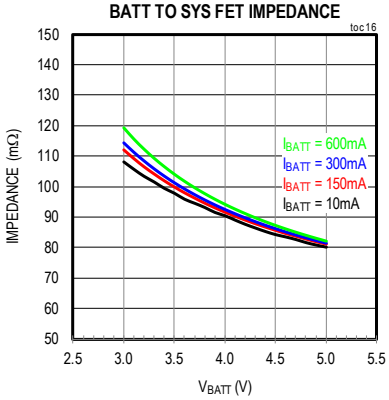
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE (USB SUSPENDED)



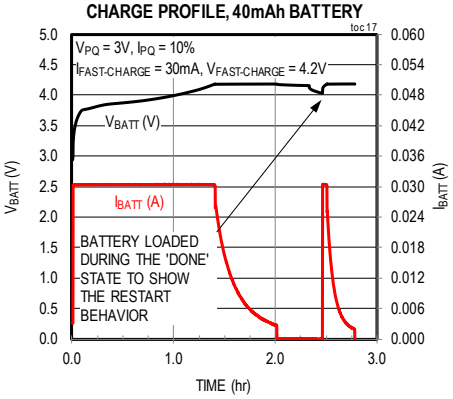
BATT BIAS CURRENT vs. BATT VOLTAGE



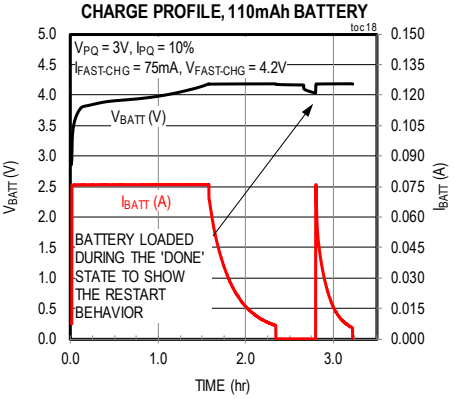
BATT TO SYS FET IMPEDANCE



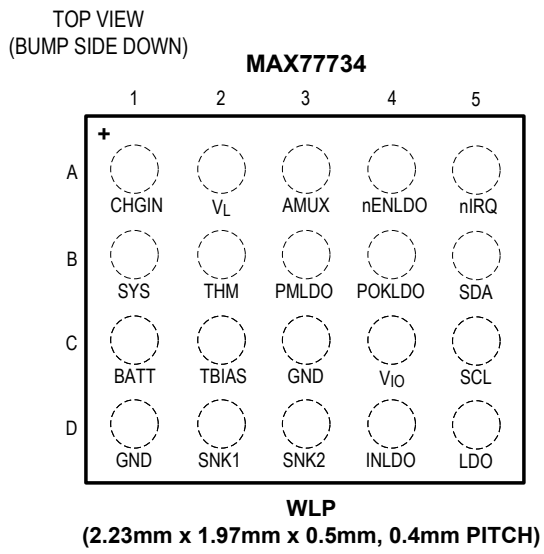
CHARGE PROFILE, 40mAh BATTERY



CHARGE PROFILE, 110mAh BATTERY



Bump Configuration



WLP
(2.23mm x 1.97mm x 0.5mm, 0.4mm PITCH)

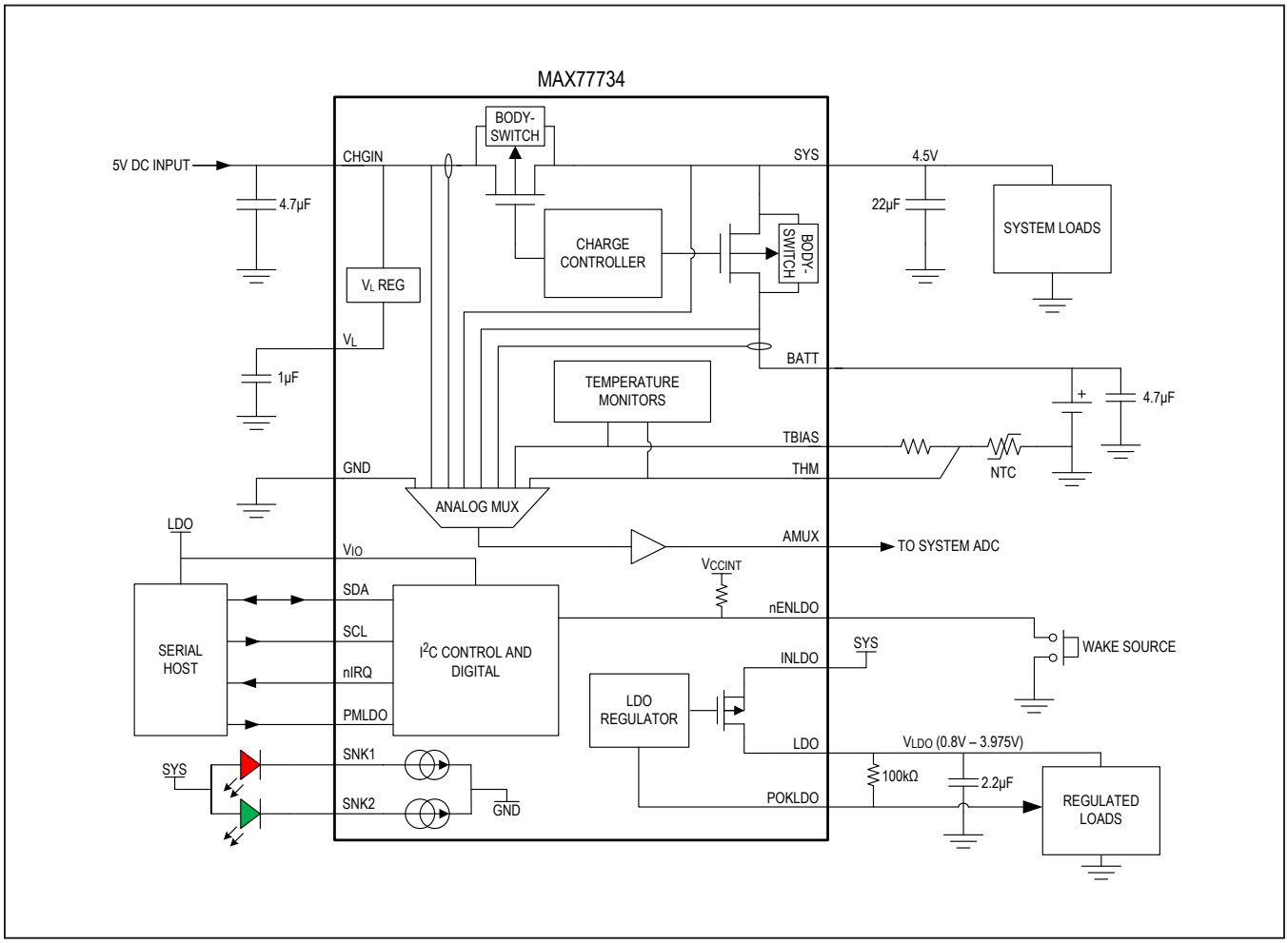
Bump Description

PIN	NAME	FUNCTION	TYPE
CHARGER			
A1	CHGIN	Charger Input. Connect to a 5V DC charging source. Bypass to GND with a 4.7µF ceramic capacitor.	power input
A2	V_L	Internal Charger 3V Logic Supply Powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load V_L externally.	power
A3	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals. Leave this pin unconnected if unused.	analog output
B1	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the IC. Bypass to GND with a 22µF ceramic capacitor.	power output
B2	THM	Thermistor Monitor. Thermally couple an NTC to the battery and connect between THM and GND.	analog input
C1	BATT	Li+ Battery Connection. Connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.	power i/o
C2	TBIAS	Thermistor Bias Supply. Connect a resistor equal to the NTC's room temperature resistance between TBIAS and THM. Do not load TBIAS with other external circuitry.	analog
C3, D1	GND	Ground. Connect to the negative battery terminal and the low-impedance ground plane of the PCB.	ground

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
LINEAR REGULATOR			
A4	nENLDO	Active-Low LDO Enable Input. This digital input also causes the IC to exit factory-ship mode. Pulled up internally to V_{CCINT}. See the *Hardware Enable (nENLDO)* section.	digital input
B3	PMLDO	LDO Power-Mode Control Input. This digital input causes the LDO to change between low-power mode and normal mode when the MSB of LDO_PM[1:0] is set. See the *LDO Power Mode (PMLDO)* section.	digital input
B4	POKLDO	Open-Drain Linear Regulator Power-OK Output. Connect a 100kΩ pullup resistor between POKLDO and a voltage equal to or less than V_{SYS} if this pin is used. Leave unconnected if unused.	digital output
D4	INLDO	Linear Regulator Input. Connect to GND if unused.	power input
D5	LDO	Linear Regulator Output. Bypass to GND with a 2.2µF ceramic capacitor. Leave unconnected if unused.	power output
DUAL-CHANNEL CURRENT SINK			
D2	SNK1	Current Sink Port 1. SNK1 is typically connected to the cathode of an LED and is capable of sinking up to 12.8mA. Connect to GND if unused.	power
D3	SNK2	Current Sink Port 2. SNK2 is typically connected to the cathode of an LED and is capable of sinking up to 12.8mA. Connect to GND if unused.	power
I²C SERIAL INTERFACE			
A5	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
B5	SDA	I²C Serial Interface Data	digital i/o
C4	V_{IO}	I²C Serial Interface Voltage Supply	power input
C5	SCL	I²C Serial Interface Clock	digital input

Simplified Block Diagram



Detailed Description

The MAX77734 is a tiny power-management integrated circuit (PMIC) that integrates the following:

- Instant-on linear-mode lithium-ion/lithium-polymer (Li+) battery charger optimized for small battery cells (see *Detailed Description—Smart Power Selector Charger*)
- NTC thermistor monitor for automatic JEITA-safe-charging (see *Detailed Description—Adjustable Thermistor Temperature Monitors*)
- Analog Multiplexer (MUX) which enables an external ADC to monitor power (see *Detailed Description—Analog Multiplexer*)
- 150mA linear regulator (see *Detailed Description—Linear Regulator*)
- Dual-channel current sinks with individual pattern control (see *Detailed Description—Dual-Channel Current Sink Driver*)

The ICs internal top-level digital logic is described in the *On/Off Controller* section of the data sheet. The IC is fully configurable through I2C (see the *Register Map* and *Detailed Description—I2C Serial Interface*). The active-low nENLDO input can be used to wake-up the LDO using an external on-key. See *Hardware Enable (nENLDO)*.

A low-I_Q (0.2µA typ) factory-ship mode can be entered to isolate the battery node (BATT) from the system (SYS) to prevent slow cell discharge due to a high combined shutdown current of all external SYS loads (see *Factory-Ship Mode State*).

A watchdog timer can be enabled through I2C (or factory-enabled and locked) to provide supervisory reset in the event that serial activity from the host controller suddenly stops (see *Watchdog Timer*).

Additionally, a SYS voltage supervisory function is accomplished by the undervoltage (UVLO), overvoltage (OVLO), and power-on reset (POR) comparators.

On/Off Controller

The IC top-level on/off controller uses a synchronous digital state machine with a 100µs clock. Asynchronous inputs to the state machine can take up to 100µs to take effect due to clock synchronization.

The state machine is drawn in Figure 1 and Figure 2. State transition conditions are listed in Table 1.

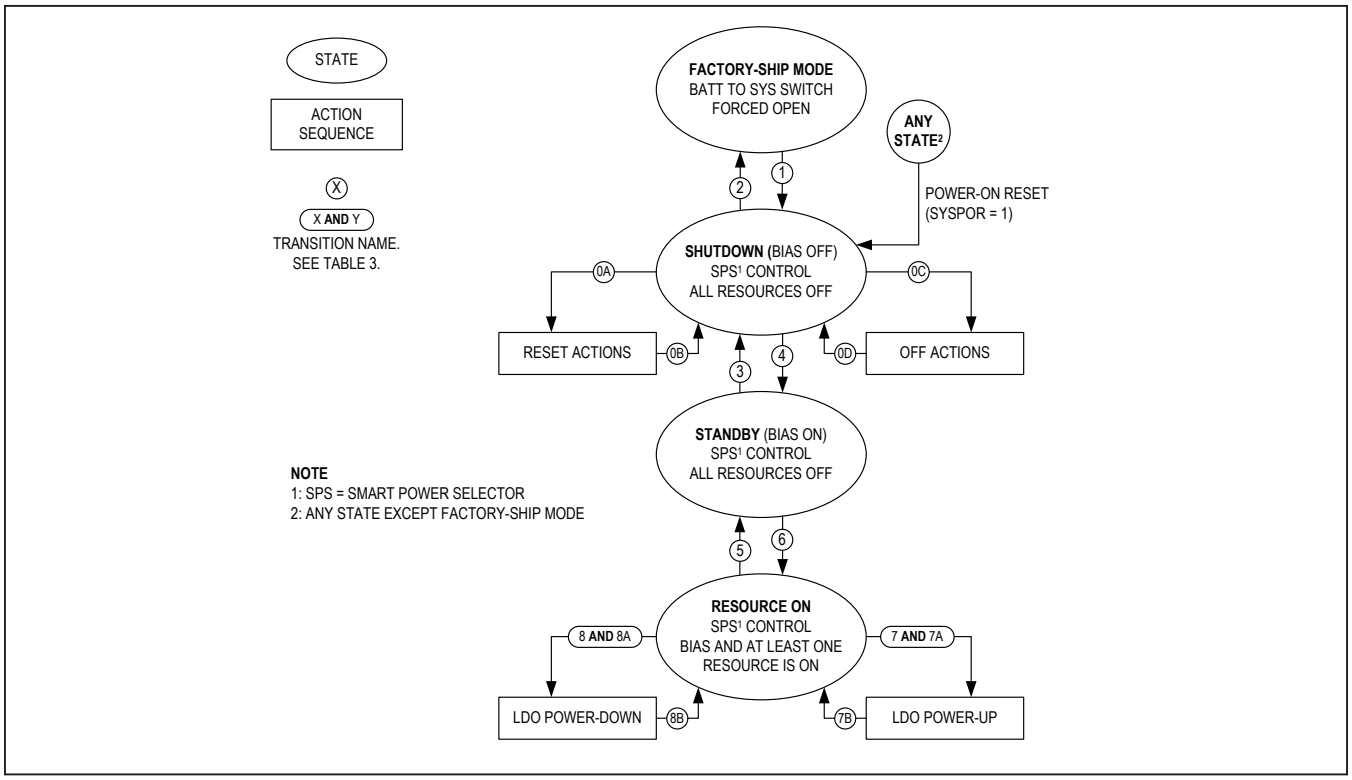


Figure 1. On/Off Controller State Machine