Chipsmall

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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MAX77752   Multichannel Integrated Power Management IC

General Description

The MAX77752 is a highly-integrated power management solution including three step-down converters, a low-dropout linear regulator, two external regulators enable outputs, two dedicated load switch controllers, and an inrush-current limiter which can be configured as a third load switch controller using OTP. The MAX77752 provides a combination of high-performance power management components, high-accuracy monitoring, and a customized top-level controller that results in an efficient, size optimized solution.

The 40-pin, 5mm x 5mm x 0.8mm, 0.4mm pitch TQFN package is ideal for space constrained applications.

Numerous factory programmable options allow the device to be tailored for many variations of the end application.

Applications

- Solid-State Drive Systems
- Handheld Devices
- Gaming Consoles
- Drones
- Automation Systems
- Cameras

Benefits and Features

- Highly Integrated
  - Three Buck Regulators
    - Integrated High-Accuracy Brownout Comparators
  - One Low-Dropout Linear Regulator
    - Low-Input Voltage
  - Two Dedicated Load Switch Controllers
  - One Inrush-Current Limiter, Configurable to be Load Switch 3 Controller Using OTP
  - Two External Regulator Enable Outputs
  - Voltage Monitor for Backup Power Control
- Highly Flexible and Configurable
  - I^2C-Compatible Interface
  - Factory OTP Options Available
  - Flexible Power Sequencer
  - Configurable Sleep-State Control
- Small Size
  - 40-Pin, 5mm x 5mm x 0.8mm, 0.4mm Pitch TQFN
  - 70mm^2 Total Solution Size

Ordering Information appears at end of data sheet.

Simplified Block Diagram
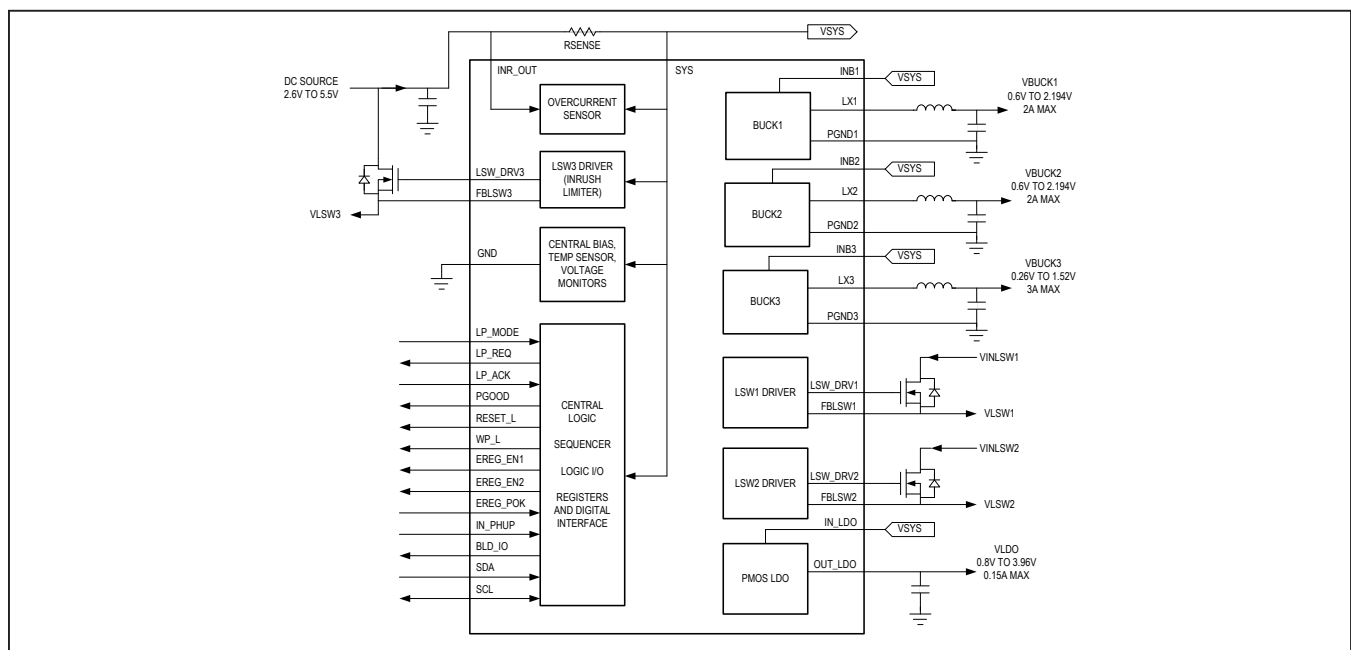
Absolute Maximum Ratings

Top

IN_DRV to GND ....-0.3V to +16.0V

IN_SNS to GND (Note 1) ....-0.3V to +6.0V

INR_OUT to GND..-0.3V to +6.0V

SYS to GND ....-0.3V to +6.0V

IN_PHUP to GND ....-0.3V to +6.0V

RESET_L to GND..................................-0.3V to V_{SYS}+0.3V

LP_REQ to GND ....-0.3V to V_{SYS}+0.3V

LP_ACK to GND....................................-0.3V to V_{SYS}+0.3V

LP_MODE to GND ....-0.3V to V_{SYS}+0.3V

WP_L to GND (Note 2)...................................-0.3V to V_{H_INT}

PGOOD to GND (Note 2)..............................-0.3V to V_{H_INT}

EREG_EN1 to GND (Note 2) ....-0.3V to V_{H_INT}

EREG_EN2 to GND ....-0.3V to 6.0V

EREG_POK to GND ....-0.3V to V_{SYS}+0.3V

BLD_IO to GND (Note 2).................................-0.3V to +6.0V

WP_L Sink Current...35mA

RESET_L Sink Current....................................35mA

PGOOD Sink Current 35mA

EREG_EN1 Sink Current 35mA

EREG_EN2 Sink Current 35mA

LP_REQ Sink Current 35mA

DGND to GND...-0.3V to +0.3V

LDO

IN_LDO to GND...-0.3V to +6.0V

OUT_LDO to GND..............................-0.3V to V_{IN_LDO}+0.3V

Buck

INB1, INB2, INB3 to SYS ....-0.3V to +0.3V

INB1 to PGND1 ....-0.3V to +6.0V

INB2 to PGND2 ....-0.3V to +6.0V

INB3 to PGND3 ....-0.3V to +6.0V

LX1 to PGND1 (Note 3)......................... -0.3V to V_{INB1}+0.3V

LX2 to PGND2 (Note 3)......................... -0.3V to V_{INB2}+0.3V

LX3 to PGND3 (Note 3)......................... -0.3V to V_{INB3}+0.3V

LX1, LX2 RMS Current per pin (T_J = +110°C)
(RMS current per pin (T_J = +110°C)) 1.7A

LX3 RMS Current per pin (T_J = +110°C)
(RMS current per pin (T_J = +110°C)) 3.0A

FBB1, FBB2, FBB3 to GND ....-0.3V to V_{SYS}+0.3V

PGND1, PGND2, PGND3 to GND ....-0.3V to +0.3V

I²C

SDA, SCL to GND .... -0.3V to $V_{IN\_VIO\_I2C}$+0.3V

SDA Sink Current 35mA

Load Switch

LSW_DRV1 to GND ....-0.3V to +16.0V

LSW_DRV2 to GND ....-0.3V to +16.0V

FBLSW1 to GND ....-0.3V to V_{SYS}+0.3V

FBLSW2 to GND ....-0.3V to V_{SYS}+0.3V

Continuous Power Dissipation (Multilayer Board)
T_A = +70°C, derate 35.70mW/°C
above +70°C... mW to 2857.1mW

Operating Temperature Range.......................... -40°C to +85°C

Junction Temperature..+150°C

Storage Temperature Range........................... -40°C to +150°C

Soldering Temperature (reflow)......................................+260°C

Note 1: IN_SNS voltage ramp rates greater than 2.8V/µs trigger the internal ESD device and should be avoided. The ESD device recovers if exposed to an excessive ramp rate.

Note 2: V_{H_INT} is the maximum voltage of V_{SYS} and V_{IN_PHUP}.

Note 3: The specified voltage limitation is for steady state conditions. Dead times of a few nano seconds exist during the dynamic BUCK regulator transitions from inductor charging to inductor discharging and vice versa. These dead times allow internal clamping diodes to PGNDx and INBx to forward bias (Vf~1V). When the LXx waveform is observed on a high-bandwidth oscilloscope (≥100MHz), the LXx transition edges are commonly seen with 1.5V spikes. These spikes are due to (1) the internal clamping diode forward voltage and (2) the high rate of current change through the current loop's inductance (V = L x di/dt). Designs must follow the recommended printed circuit board (PCB) layout in order to minimize this current loop's inductance.

Package Information

TQFN

PACKAGE CODE	T4055+1C
Outline Number	**21-0140**
Land Pattern Number	**90-0016**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics—Global Resources

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
OFF State Quiescent Current	I_{QSYS_OFF}	$V_{SYSUVLO} < V_{SYS} < V_{SYS\_RESET}$ (rising), OTP_INT_PU = 1, all regulators are disabled. This includes any central bias currents disabled (EREG_EN1 pulled to V_{SYS})		86	135	µA
DEVSLP State Quiescent Current	I_{QSYS_DEVSLP}	V_{SYS} = 3.3V, $V_{SYS} > V_{SYS\_RESET}$, OTP_INT_PU = 0, PMIC in DEVSLP State, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		70	125	µA
		V_{SYS} = 5V, $V_{SYS} > V_{SYS\_RESET}$, OTP_INT_PU = 0, PMIC in DEVSLP state, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		90	155	
Buck Quiescent Supply Current	I_{QSYS_BUCK}	V_{SYS} = 5V, $V_{SYS} > V_{SYS\_RESET}$, all bucks enabled in normal-power mode and skip mode		233	420	µA

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS AND REFERENCE CURRENT GENERATOR						
Operating Voltage Range	V_{SYS}		2.6		5.5	V
Quiescent Supply Current	I_{QCBRG}	V_{SYS} > $V_{SYSUVLO}$ (rising)		25		µA
Shutdown Supply Current		V_{SYS} < $V_{SYSUVLO}$ (falling)		0.1		µA
Bias Enable time	t_{BIASOK}			100		µs
POR COMPARATOR (INTERNAL)						
Quiescent Supply Current	I_{QSYS_POR}			1		µA
POR Undervoltage-Lockout Threshold	V_{POR}	V_{SYS} falling		1.33		V
POR Threshold Hysteresis	V_{HYS_POR}	V_{SYS} rising		160		mV
Response Time		100mV overdrive		300		µs
POR to UVLO Delay	$t_{PORUVLO}$	V_{SYS} rising across POR (1V to 2V)		100		µs
		V_{SYS} falling across POR		50		
SYS UNDERVOLTAGE-LOCKOUT COMPARATOR						
Quiescent Supply Current	I_{QSYS_UVLO}			1		µA
SYS Undervoltage-Lockout Threshold	$V_{SYSUVLO}$	V_{SYS} falling	2.00	2.10	2.25	V
SYS Undervoltage-Lockout Hysteresis	V_{INUVLO_HYS}			400		mV
SYS Undervoltage-Lockout Response Time	$t_{SYSUVLO}$	100mV overdrive, falling edge		150		µs
SYS RESET COMPARATOR						
Quiescent Supply Current	I_{QSYS_RESET}			3		µA
Reset Falling Threshold Range	V_{SYS_RESET}	Programmed by SYSRST[3:0]	2650		4150	mV
Reset Threshold Step Size				100		mV
Reset Threshold Hysteresis Range	$V_{SYSRESET\_HYS}$	Programmed by SYSRSTHYS[1:0]	150		300	mV
Reset Threshold Hysteresis Step Size				50		mV
Reset Comparator Response Time	$t_{SYSRESET}$			5		µs
Reset Comparator Accuracy		SYSRSTTH[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF	-2.5		+2.5	%

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS BROWNOUT COMPARATOR						
Brownout Falling Threshold Range	V_{SYS_BO}	Programmed by SYSBOTH[3:0]	2800		4300	mV
Brownout Threshold Step Size				100		mV
Brownout Threshold Hysteresis Range	$V_{SYS\_BO\_HYS}$	Programmed by SYSBOHYS[1:0]	150		300	mV
Brownout Threshold Hysteresis Step Size				50		mV
Brownout Comparator Response Time	t_{SYSBO}	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/μs		1.04		μs
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/μs		1.14		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/μs		1.30		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/μs		1.68		
Brownout Comparator Response Time (DEVSLP)	t_{SYSBO}	PMIC in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/μs		3.53		μs
Quiescent Supply Current	I_{QSYS_BO}	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state		13.4		μA
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state		10.4		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state		7.4		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state		4.4		
Quiescent Supply Current (DEVSLP)	I_{QSYS_BO}	PMIC in DEVSLP state		1.3		μA
Brownout Comparator Accuracy		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is not in DEVSLP state	-2.5		+2.5	%
Brownout Comparator Accuracy (DEVSLP)		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is in DEVSLP state	-2.5		+2.5	%
Brownout Timer Period	t_{BO}	T_BO_EN = 1		100		ms

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Clock Frequency	CLK32K	V_{SYS} = 5V		31.5		kHz
Oscillator Tolerance		V_{SYS} = 3.3V	-10		+10	%
		V_{SYS} = 5V	-10		+10	
WP_L OUTPUT (OPEN DRAIN)						
WP_L Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
WP_L Open Leakage Current		V_{SYS} = V_{WP_L} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{WP_L} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
WP_L Falling Edge Time		C_{WP_L} = 25pF, V_{WP_L} = 1.8V ≥ 0		25		ns
WP_L Output Deassert Delay Time	t_{WPDLY}	WP_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		µs
		WP_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		WP_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		WP_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
WP_L Output Assert Delay Time				0		µs
WP_L Pullup Resistance	$R_{PU\_WP\_L}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
RESET_L OUTPUT (OPEN DRAIN)						
RESET_L Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
RESET_L Open Leakage Current		V_{SYS} = V_{RESET_L} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{RESET_L} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
RESET_L Falling Edge Time		C_{RESET_L} = 25pF, V_{RESET_L} falling from 1.8V ≥ 0		25		ns

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET_L Output Deassert Delay Time	t_{RSTDLY}	RST_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		µs
		RST_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		RST_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		RST_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
RESET_L Output Assert Delay Time				0		µs
RESET_L Pullup Resistance	$R_{PU\_RESET\_L}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
PGOOD OUTPUT (OPEN DRAIN)						
PGOOD Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
PGOOD Open Leakage Current		V_{SYS} = V_{PGOOD} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{PGOOD} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
PGOOD Falling Edge Time		C_{PGOOD} = 25pF, V_{PGOOD} = 1.8V ≥ 0		25		ns
PGOOD Output Assert Delay Time	$t_{PGOODDLY}$	PG_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		31.5		µs
		PG_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		PG_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		PG_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
PGOOD Output Deassert Delay Time				0		µs
PGOOD Pullup Resistance	R_{PU_PGOOD}	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LP_MODE INPUT						
LP_MODE I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
LP_MODE Input-Low Voltage	V_{IL}				0.4	V
LP_MODE Input-High Voltage	V_{IH}		1.4			V
LP_MODE Input Hysteresis	V_{HYS}			50		mV
LP_MODE Input Leakage Current		V_{SYS} = V_{IN_VIO} = 5.5V, V_{LP_MODE} = 0V and 5.5V, T_A = +25°C		0.001	1	µA
		V_{SYS} = V_{IN_VIO} = 5.5V, V_{LP_MODE} = 0V and 5.5V, T_A = +85°C		0.01		
LP_MODE Debounce	t_{LPMD_DBNC}	Debounce applies to rising and falling edge. Does not account for oscillator tolerance (Note 4)		95	127	µs
LP_MODE I/O Pad Undervoltage Lockout	$V_{SYSUVLO}$	V_{SYS} falling		2.1		V
LP_MODE Mask Deassertion Timer	t_{LPMD_MSK}		16	20	25	ms
LP_ACK INPUT						
I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Hysteresis	V_{HYS}			50		mV
Input Leakage Current		V_{SYS} = 5.5V, V_{LP_ACK} = 0V and 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = 5.5V, V_{LP_ACK} = 0V and 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
LP_ACK Pullup Resistance	$R_{PU\_LP\_ACK}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LP_REQ OUTPUT (OPEN DRAIN)						
LP_REQ Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
LP_REQ Open Leakage Current		V_{SYS} = V_{LP_REQ} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	μA
		V_{SYS} = V_{LP_REQ} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
LP_REQ Falling Edge Time		C_{LP_REQ} = 25pF, V_{LP_REQ} = 1.8V ≥ 0		25		ns
LP_REQ Delay	t_{LPREQ_LOW}	LP_REQ_T_EN = 0, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		31.75		μs
		LP_REQ_T_EN = 1, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		20		ms
LP_REQ Pullup Resistance	$R_{PU\_LP\_REQ}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_ENx OUTPUT (OPEN DRAIN)						
EREG_EN1 Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
EREG_EN2 Output-Voltage Low	V_{OL}	I_{SINK} = 10mA			0.4	V
EREG_ENx Open Leakage Current		V_{SYS} = V_{EREG_ENx} = 5.5V, T_A = +25°C, OTP_INT_PU[$\overline{0}$] = 0b0		0.001	1	μA
		V_{SYS} = V_{EREG_ENx} = 5.5V, T_A = +85°C, OTP_INT_PU[$\overline{0}$] = 0b0		0.01		
EREG_ENx Falling Edge Time		C_{EREG_ENx} = 25pF, V_{EREG_ENx} = 1.8V ≥ 0		25		ns
EREG_EN1 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to V_{H_INT}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_EN2 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_POK INPUT						
I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Hysteresis	V_{HYS}			50		mV

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		V_{SYS} = 5.5V, V_{EREG_POK} = 0V and 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = 5.5V, V_{EREG_POK} = 0V and 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
EREG_POK Pullup Resistance	$R_{PU\_EREG\_POK}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
THERMAL MONITORS						
Quiescent Supply Current	I_{QTM}			1.5		µA
Shutdown Supply Current				0.1		µA
Thermal Overload	T_{JOVLD}	T_J rising, 15°C hysteresis		165		°C
Response Time		5°C overdrive		10		µs
FLEXIBLE POWER SEQUENCER						
Power-Up Sequence Enable Delay	t_{FPSDON}	Measured from internal FPSxEN = 1 to start of sequence (based on a 31.5kHz clock)		63.492		µs
Power-Down Sequence Enable Delay	$t_{FPSDOFF}$	Measured from internal FPSxEN = 0 to start of sequence (based on a 31.5kHz clock)		95.240		µs
Flexible Power Sequencer Event Period	t_{FPS_PU}, t_{FPS_PD}	MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b000		31		µs
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b001		63		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b010		127		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b011		253		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b100		508		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b101		984		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b110		1936		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b111		3904		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Sequence Delay	t_{PD_DLY}	PD_DLY[1:0] = 0b00		0		ms
		PD_DLY[1:0] = 0b01		1.0		
		PD_DLY[1:0] = 0b10		1.5		
		PD_DLY[1:0] = 0b11		2.0		
BLD_IO						
Maximum Bleed Time	t_{BLEED_MAX}			20	22	ms
Minimum Bleed Time	t_{BLEED_MIN}			31.5		µs
Bleed Threshold		BLD_IO falling		90	100	mV
Bleed Resistance	R_{BLEED}	BLD_IO = 0.3V		20	27	Ω
BLD_IO Input Leakage Current		V_{SYS} = 5.5V, V_{BLD_IO} = 0V and 5.5V, T_A = +85°C		0.01		µA
		V_{SYS} = 5.5V, V_{BLD_IO} = 0V and 5.5V, T_A = +25°C		0.001	1	
ON/OFF CONTROLLER						
Hiccup Counter Limit	HICCUP_CNT_LIM			7		counts
IN_PHUP						
Operating Voltage Range	V_{IN_PHUP}		2.4		5.5	V
IN_PHUP Supply Current	I_{IN_PHUP}	V_{SYS} = V_{IN_PHUP} = 5.5V, T_A = +25°C		5.0		µA

Note 4: The LP_MODE debounce period has a variation due to the variability associated with quantizing an asynchronous input signal. Additionally, while measuring the period from a valid LP_MODE edge to a subsequent event, such as LP_REQ assertion, there is one more clock cycle (CLK32K) of delay observed in a real system.

Electrical Characteristics—Inrush Control

(V_{IN_SNS} = 5.0V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{IN}			2.1		5.5	V
IN Undervoltage-Lockout Threshold	V_{INUVLO}	V_{IN} rising			2.3	2.55	V
IN Undervoltage-Lockout Hysteresis	V_{INUVLO_HYS}				200		mV
IN Undervoltage-Lockout Response Time	t_{INUVLO}	V_{IN} rising (V_{IN} = V_{INUVLO} + 100mV)			39		µs
IN Overvoltage-Lockout Threshold	V_{INOVLO}	V_{IN} rising		5.70	5.87	6.10	V
IN Overvoltage-Lockout Hysteresis	V_{INOVLO_HYS}				80		mV
IN Overvoltage-Lockout Response Time	t_{INOVLO}	V_{IN} rising (V_{IN} = V_{INOVLO} + 50mV)			8		µs
Leakage	$I_{LKG\_VIN\_DRV}$	V_{IN} = 5.5V, V_{IN_DRV} = 0V and 11V, T_A = +25°C			0.001	1	µA
		V_{IN} = 5.5V, V_{IN_DRV} = 0V and 11V , T_A = +85°C			0.01		
Supply Current (Soft-Start)	$I_{Q\_IN\_SS}$	V_{IN_DRV}-VINR_OUT < V_{IN_SNS} (soft-start state), OTP_GDRV_FREQ = 0b111 (800kHz), V_{IN_SNS} = 3.3V			85		µA
		V_{IN_DRV}-VINR_OUT < V_{IN_SNS} (soft-start state), OTP_GDRV_FREQ = 0b111 (800kHz), V_{IN_SNS} = 5V			138		
Supply Current (Steady-State)	I_{IN}	V_{IN_DRV}-VINR_OUT = V_{IN_SNS} (steady state), t_{SS_DONE} expired, f_{GDRV} = 12.5kHz, V_{IN_SNS} = 3.3V			26		µA
		V_{IN_DRV}-VINR_OUT = V_{IN_SNS} (steady state), t_{SS_DONE} expired, f_{GDRV} = 12.5kHz, V_{IN_SNS} = 5V			37		
NMOS SWITCH DRIVER							
Gate Drive ON Voltage	$V_{IN\_DRV\_ON}$	V_{IN} = 5V	Voltage with respect to ground when external MOSFET is being driven to it's fully ON state	8.5		11	V
Gate Drive Current	I_{GDRV_INRUSH}	V_{IN} = 3.3V, 1X gate drive frequency setting		1.8	3.0	4.2	µA
4x Gate Drive Oscillator Frequency	f_{GDRV_4X}	OTP_INR_FREQ[2:0] = 0b111, V_{IN} = 3.3V, V_{IN} = 5V			720		kHz

Electrical Characteristics—Inrush Control (continued)

(V_{IN_SNS} = 5.0V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2x Gate Drive Oscillator Frequency	f_{GDRV_2X}	OTP_INR_FREQ[2:0] = 0b110, V_{IN} = 3.3V, V_{IN} = 5V		360		kHz
1x Gate Drive Oscillator Frequency	f_{GDRV_1X}	OTP_INR_FREQ[2:0] = 0b101 (nominal gate drive strength), V_{IN} = 3.3V, V_{IN} = 5V	120	180	240	kHz
0.5x Gate Drive Oscillator Frequency	$f_{GDRV\_0.5X}$	OTP_INR_FREQ[2:0] = 0b100, V_{IN} = 3.3V, V_{IN} = 5V		90		kHz
0.25x Gate Drive Oscillator Frequency	$f_{GDRV\_0.25X}$	OTP_INR_FREQ[2:0] = 0b011, V_{IN} = 3.3V, V_{IN} = 5V		45		kHz
0.125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.125X}$	OTP_INR_FREQ[2:0] = 0b010, V_{IN} = 3.3V, V_{IN} = 5V	15	23	32	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{GDRV\_0.0625X}$	OTP_INR_FREQ[2:0] = 0b001, V_{IN} = 3.3V, V_{IN} = 5V		11.25		kHz
0.03125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.03125X}$	OTP_INR_FREQ[2:0] = 0b000, V_{IN} = 3.3V, V_{IN} = 5V		5.625		kHz
Gate Drive Discharge Resistance	R_{GDRV_DIS}	Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT}$ = 4V		74		Ω
		Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT}$ = 3.3V		100		
TIMING						
Start-Up Delay	t_{EN_INRUSH}	Time from V_{IN} rising above V_{INUVLO} to the internal charge pump being enabled. Duration is based on the gate drive oscillator frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		128		cycles of f_{GDRV}
Soft-Start Done Time	t_{SS_1}	Duration from MOSFET drive circuit being enabled (subsequent to startup delay) to the point when the IN_SS_DONE (internal signal) is asserted allowing a power-up sequence to occur. Based on default gate drive frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		512		cycles of f_{GDRV}
Gate Drive Idle Time	t_{SS_DONE}	Duration from MOSFET drive circuit being enabled (subsequent to the startup delay) to the point when the gate drive oscillator frequency folds back to the 12.5kHz setting (idle gate drive). Based on default gate drive frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		1024		cycles of f_{GDRV}

Electrical Characteristics—Current Sense Amplifier

(V_{SYS} = 3.3V, C_{LOAD} = 10pF, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT OVERCURRENT						
Input Overcurrent Threshold		2.25A setting, V_{SYS} = 3.3V	-6.5		+6.5	%
CSA Debounce Timer		OTP_CSA_DBNC = 0		100		μs
		OTP_CSA_DBNC = 1		50		
Overcurrent-Sense Comparator Threshold 1	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b00		30		mV
Overcurrent-Sense Comparator Threshold 2	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b01		35		mV
Overcurrent-Sense Comparator Threshold 3	V_{OC_THR}	Overcurrent-limit, CSTH_OPT[1:0] = 0b10		40		mV
Overcurrent-Sense Comparator Threshold 4	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b11		45		mV

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	V_{INBx}		2.6		5.5	V
Shutdown Supply Current	I_{QSHDN_BUCKx}	(Note 5)		0.1		μA
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCKx}$	No switching, no load, (Note 6), V_{SYS} = 3.3V		19	30	μA
		No switching, no load, (Note 6), V_{SYS} = 5V		19	30	
	$I_{Q\_FPWM\_BUCKx}$	FPWM mode (switching at fixed frequency), no load, V_{SYS} = 3.3V		10		mA
		FPWM mode (switching at fixed frequency), no load, V_{SYS} = 5V		10		
	$I_{Q\_SKIP\_LPM\_BUCKx}$	Low-power mode (no switching), no load, (Note 6), V_{SYS} = 3.3V		5	9	μA
		Low-power mode (no switching), no load, (Note 6), V_{SYS} = 5V		5	9	

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V$_{SYS}$ = 3.6V, T$_A$ = -40°C to +85°C, limits are 100% tested at T$_A$ = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V$_{OUT\_BUCKx}$	Programmable in 6.25mV steps with BUCK1VOUT[7:0] and BUCK2VOUT[7:0]	0.600		2.194	V
Output Voltage Accuracy	V$_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, V$_{OUT\_BUCK1}$ = 1.800V	-2		+2	%
	V$_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, V$_{OUT\_BUCK1}$ = 1.800V	-4		+4	
	V$_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, V$_{OUT\_BUCK2}$ = 1.200V	-2		+2	
	V$_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, V$_{OUT\_BUCK2}$ = 1.200V	-4		+4	
OUTPUT CURRENT						
Maximum Output Current	I$_{OUT\_MAX\_NM\_BUCKx}$	RMS, normal mode, L = 1µH	2000			mA
	I$_{OUT\_MAX\_LPM\_BUCKx}$	RMS, low-power mode, L = 1µH		10		
PMOS Peak Current Limit	I$_{LIMP}$	V$_{SYS}$ = 3.6V	2300	2875	4200	mA
		V$_{SYS}$ = 5V	2300	2875	4200	
NMOS Valley Current Limit	I$_{LIMV}$	V$_{SYS}$ = 3.6V		2125		mA
		V$_{SYS}$ = 5V		2125		
NMOS Negative Current Limit	I$_{LIMN}$	V$_{SYS}$ = 3.6V		800		mA
		V$_{SYS}$ = 5V		800		
PERFORMANCE PARAMETERS						
Line Regulation		V$_{SYS}$ = V$_{INBx}$ = 2.6V to 5.5V		0.2		%/V
Load Regulation		Load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response		FPWM mode, V$_{OUT\_BUCKx}$ = default, L = 1µH, C$_{OUT}$ = 12µF effective Δ I$_{OUT}$ = 0.2A–2A, Δt = 3µs		88		mV
		Skip mode, V$_{OUT\_BUCKx}$ = default, L = 1µH, C$_{OUT}$ = 12µF effective Δ I$_{OUT}$ = 10mA to 0.7A, Δt = 3µs,		90		
Switching Frequency	f$_{SW}$	V$_{SYS}$ = 3.3V	1.8	2	2.2	MHz
Dead Time	t$_{DEAD}$	V$_{SYS}$ = 3.3V		2.0		ns
Switching Frequency	f$_{SW}$	V$_{SYS}$ = 5V	1.8	2	2.2	MHz

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Time	t_{DEAD}	V_{SYS} = 5V		2.0		ns
Soft-Start Slew Rate		Fixed for buck 1		6.5		mV/µs
		Fixed for buck 2		17		
Output Voltage Ramp-Up Slew Rate		Fixed for buckx (Notes 5, 8, 9), C_{OUT} = 22µF		40		mV/µs
Output Voltage Ramp-Down Slew Rate		Fixed for buck 1, 2 (Notes 5, 8), C_{OUT} = 22µF, BUCKxFPWMEN = 1 (x = 1, 2), no load		18		mV/µs
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = $V_{INBUCKx}$ = 3.6V, I_{OUT} = 150mA		100	150	mΩ
		V_{SYS} = $V_{INBUCKx}$ = 5V, I_{OUT} = 150mA		100	150	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = $V_{INBUCKx}$ = 3.6V, I_{OUT} = 150mA		60	100	mΩ
		V_{SYS} = $V_{INBUCKx}$ = 5V, I_{OUT} = 150mA		60	100	
NMOS Zero-Crossing Threshold	I_{ZX}	Threshold to determine transition from PWM to SKIP mode		20		mA
Output Voltage Ripple in Skip Mode		V_{OUT_BUCKx} = 1.0V, L = 1µH, C_{OUT} = 12µF effective, no load (Note 5)		40		mV$_{P-P}$
Output Voltage Ripple in PWM Mode		V_{OUT_BUCKx} = 1.0V, L = 1µH, C_{OUT} = 12µF effective, I_{LOAD} = 0.5 x $I_{OUT\_MAX\_BUCKx}$ (Note 5)		5		mV$_{P-P}$
LX Leakage	$I_{L\_LX\_25C}$	V_{LXx} = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	V_{LXx} = 5.5V or 0V, T_A = +85°C (Note 5)		1		
Output Active Discharge Resistance	R_{DISCHG_BUCKx}	Resistance from FBBx to PGNDx, output disabled, (Note 7)		100		Ω
Nominal Output Inductance	L_{NOM}			1.0		µH
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	0mA < I_{OUT} < 2000mA	18			µF
Light Load Efficiency	Eff_{LIGHT}	Low-power mode, I_{OUT} = 0.5mA, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 22µF (Note 5)		75		%

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Typical Load Efficiency	Eff$_{IOUT\_TYP}$	I_{OUT} = 0.25 x $I_{OUT\_MAX\_BUCKx}$, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR$_L$ = 50mΩ, C_{OUT} = 22µF (Note 5)		85		%
Maximum Load Efficiency	EFF$_{IOUT\_MAX}$	I_{OUT} = $I_{OUT\_MAX\_BUCKx}$, V_{OUT} = 1.0V, L = 1µH, DCR$_L$ = 50mΩ, C_{OUT} = 22µF (Note 5)		70		%
Turn-On Delay Time	t$_{ON\_DLY\_BUCKx}$	EN signal to LX switching with bias ON		30		µs
Maximum Duty Cycle		V_{OUT_BUCKx} / V_{IN_BUCKx} expressed as %		90		%
BROWNOUT COMPARATOR						
Output Brownout Threshold	V$_{BO\_BUCKx}$	Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b00		75		%
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b01		80		
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b10		85		
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b11		90.7		
Output Brownout Accuracy		Normal-power mode. V_{OUT_BUCKx} = 1.0V (VOUT_BUCKx[7:0] = 0 x 40)	-4.0		+4.0	%
Output Brownout Threshold (Low-Power Mode)	V$_{BO\_BUCKx}$	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode. V_{OUT_BUCKx} = 1.0V (VOUT_BUCKx[7:0] = 0 x 40)	-4		+4	%
Output Brownout Hysteresis Range	V$_{BO\_HYS\_BUCKx}$	2-bit control over I²C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with BUCKx_BO_HYS[1:0]		5		%
Output Brownout Hysteresis (Low-Power Mode)	V$_{BO\_HYS\_BUCKx\_LPM}$			5		%

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	t_{BO_BUCKx}	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.04		µs
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.68		
		Buck in low-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		µA
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV COMPARATOR						
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 1, referenced to output voltage setting		116.6		%
Output OV Hysteresis		BUCKx_OV_THR = 1		9.1		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 0, referenced to output voltage setting		108.3		%
Output OV Hysteresis		BUCKx_OV_THR = 0		2.8		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCKx\_OV}$	Rising edge, low-power mode		108.3		%
Output OV hysteresis (Low-Power Mode)		Low-power mode		2.8		%
Output Over-Voltage Response Time	t_{OV_BUCKx}	Normal-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 5)		1.68		µs
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Normal-power mode		4.4		µA
Output Over-Voltage Response Time (Low-Power Mode)	t_{OV_BUCKx}	Low-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 5)		3.18		µs
Output Over-Voltage Supply Current (Low-Power Mode)	$I_{Q\_OV\_BUCKx}$	Low-power mode		1.3		µA

Note 5: Design guidance only and is not production tested.
Note 6: Individual buck Iq is not production tested. It is covered by a combined test by turning on all bucks.
Note 7: There is an n-channel MOSFET in series with the output active-discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.
Note 8: The ramp down slew rate when the output voltage is decreased through I^{2}C is a function of the negative current limit and the output capacitance. With no load, forced PWM mode and 22µF output capacitor, the ramp-down slew rate is
dv/dt = i / C = 0.4A / 22µF = 18mV/µs.
Note 9: DVS and soft-start ramp rates can be expected to vary by up to 30%.

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	$V_{INBUCK3}$		2.6		5.5	V
Shutdown Supply Current	I_{QSHDN_BUCK3}	(Note 10)		0.1		µA
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCK3}$	No switching, no load (Note 10)		26	40	µA
	$I_{Q\_FPWM\_BUCK3}$	FPWM mode, no load (Note 10)		10		mA
	$I_{Q\_SKIP\_LPM\_BUCK3}$	Low-power mode (no switching), no load (Note 10)		10	19	µA
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_BUCK3}	I^2C programmable in 10mV Steps (BUCK3VOUT[6:0] = 0x01 to 0x7F)	0.26		1.52	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_BUCK3}$	FPWM mode, normal mode, no load, T_A = +25°C, V_{OUT_BUCK3} = 1.0V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_BUCK3}$	Low-power mode, no load, T_A = +25°C, V_{OUT_BUCK3} = 1.000V	-4		+4	
PERFORMANCE PARAMETERS						
Switching Frequency	f_{SW}	V_{SYS} = 3.3V	1.8	2	2.2	MHz
		V_{SYS} = 5V	1.8	2	2.2	
Line Regulation		$V_{INBUCK3}$ = 2.6V to 5.5V, V_{OUT_BUCK3} = 1.0V		0.2		%/V
Load Regulation		V_{OUT_BUCK3} = 1.0V, (Note 10), load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response (Droop)		Skip mode, V_{OUT} = default, L = 1µH, C_{OUT} = 28µF effective ΔI_{OUT} = 20mA to 500mA, Δt = 0.8µs (Note 10)		45		mV
		Skip mode, V_{OUT} = default, L = 1µH, C_{OUT} = 28µF effective ΔI_{OUT} = 20mA to 3A, Δt = 4.8µs (Note 10)		70		
Soft-Start Slew Rate		BUCK3SSRAMP = 0		2.5		mV/µs
		BUCK3SSRAMP = 1		10		
Output Voltage Ramp-Up/Down Slew Rate (DVS)				10		mV/µs

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = $V_{INBUCK3}$ = 5V, I_{OUT} = 150mA		60	90	mΩ
		V_{SYS} = $V_{INBUCK3}$ = 3.6V, I_{OUT} = 150mA		60	90	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = $V_{INBUCK3}$ = 5V, I_{OUT} = 150mA		35	60	mΩ
		V_{SYS} = $V_{INBUCK3}$ = 3.6V, I_{OUT} = 150mA		35	60	
NMOS Zero-Crossing Threshold	I_{ZX_SKIP}	SKIP mode		20		mA
	I_{ZX_PWM}	PWM mode		20		
Output Voltage Ripple In Skip Mode		V_{OUT_BUCK3} = 1.0V, L = 1µH, C_{OUT} = 28µF effective, no load (Note 10)		15		mV
Output Voltage Ripple In PWM Mode		V_{OUT_BUCK3} = 1.0V, L = 1µH, C_{OUT} = 28µF effective, I_{LOAD} = 0.5 x $I_{OUT\_MAX\_BUCK3}$ (Note 10)		5		mV
LX Leakage	$I_{L\_LX\_25C}$	$V_{LXBUCK1}$ = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	$V_{LXBUCK1}$ = 5.5V or 0V, T_A = +85°C (Note 10)		1		
Output Active Discharge Resistance	R_{DISCHG_BUCK3}	Resistance from FBB3 to PGND3, output disabled		100		Ω
Nominal Output Inductance	L_{NOM}			1.0		µH
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	0mA < I_{OUT} < 3000mA		28		µF
Turn-On Delay Time	$t_{ON\_DLY\_BUCK1}$	EN signal to LX switching with bias ON		200		µs
Light Load Efficiency	Eff_{LIGHT}	Low-power mode, I_{OUT} = 0.5mA, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		75		%
Typical Load Efficiency	Eff_{IOUT_TYP}	I_{OUT} = 0.25 x $I_{OUT\_MAX\_BUCKx}$, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		88		%
Maximum Load Efficiency	EFF_{IOUT_MAX}	I_{OUT} = $I_{OUT\_MAX\_BUCKx}$, V_{OUT} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		77		%

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_BUCK3}$	RMS, normal mode	3000			mA
	$I_{OUT\_MAX\_LPM\_BUCK3}$	RMS, low-power mode		10		
PMOS Peak Current Limit	I_{LIMP}	T_A = -40°C to +85°C, V_{SYS} = 3.6V	3825	4250	4675	mA
NMOS Valley Current Limit	I_{LIMV}			3750		mA
NMOS (Negative) Current Limit	I_{LIMN}			2000		mA
BROWNOUT COMPARATOR						
Output Brownout Threshold	V_{BO_BUCK3}	Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b00		77		%
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b01		81		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b10		85.7		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b11		91		
Output Brownout Accuracy		Normal-power mode. V_{OUT_BUCK3} = 1.0V (VOUT_BUCK3[7:0] = 0x4B)	-4.5		+4.5	%
Output Brownout Threshold (Low-Power Mode)	V_{BO_BUCKx}	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode, V_{OUT_BUCK3} = 1.0V (VOUT_BUCK3[7:0] = 0x4B)	-4		+4	%
Output Brownout Hysteresis Range	$V_{BO\_HYS\_BUCKx}$	2-Bit control over I²C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with BUCKx_BO_HYS[1:0]		5		%
Output Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_BUCKx\_LPM}$			5		%

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	t_{BO_BUCKx}	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.04		µs
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.68		
		Buck in Low-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		µA
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV COMPARATOR						
Output OV Trip Level	$V_{OUTBUCK3\_OV}$	Rising edge, BUCK3_OV_THR = 1		117.1		%
Output OV hysteresis		BUCK3_OV_THR = 1		8.6		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCK3_OV_THR = 0		108.5		%
Output OV Hysteresis		BUCK3_OV_THR = 0		3.9		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCK3\_OV}$	Rising edge, low-power mode		108.3		%
Output OV Hysteresis (Low-Power Mode)		Low-power mode		3.9		%
Output Over-Voltage Response Time	t_{OV_BUCK3}	Buck in normal-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCK3} rising to PGOOD pin falling (Note 10)		1.68		µs
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Buck in normal-power mode		4.4		µA
Output Over-Voltage Response Time (Low-Power Mode)	t_{OV_BUCKx}	Buck in low-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 10)		3.18		µs
Output Over-Voltage Supply current (Low-Power Mode)	$I_{Q\_OV\_BUCK3}$	Buck in low-power mode		1.3		µA

Note 10: Design guidance only and is not production tested.

Electrical Characteristics—Load Switch Driver (LSW1/2)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. x is used to represent multiple instances of similar resources, for this section x = 1, 2 unless specified for e.g., LSWx represents LSW1, LSW2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	$I_{SYS\_LSW\_SS}$	V_{INLSWx} = V_{SYS} = 5V, LSWxDRV_ FREQ=0b111 (800kHz), $C_{OUTLSWx}$ = 20µF		68		µA
Supply Voltage Range	V_{SYS}		2.6		5.5	V
Supply Current	$I_{SYS\_LSW\_SS}$	V_{INLSWx} = V_{SYS} = 3.3V, LSWxDRV_FREQ = 0b111 (1.6MHz), $C_{OUTLSWx}$ = 20µF		43		µA
		V_{INLSWx} = V_{SYS} = 5V, LSWxDRV_FREQ = 0b101 (400kHz), $C_{OUTLSWx}$ = 20µF		20		
Leakage	$I_{LKG\_LSWx\_DRV}$	VSYS = 5.5V, V_{LSWx_DRV} = 0V and 11V, T_A = +25°C		0.001	1	µA
		V_{SYS} = 5.5V, V_{LSWx_DRV} =0 V and 11V, T_A = +85°C		0.01		
NMOS SWITCH DRIVER						
Gate Drive Voltage	V_{LSWx_DRV}	V_{SYS} = 5V	8.5		11	V
Gate Drive Current	I_{LSWx_DRV}	V_{SYS} = 3.3V, 1X gate drive frequency setting (LSWx_DRV_FREQ[2:0] = 0b101), $C_{OUTLSWx}$ = 20µF	1.85	3.7	5.55	µA
4x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_4X}$	LSWxDRV_FREQ[2:0] = 0b111, V_{SYS} = 3.3V, V_{SYS} = 5V		1600		kHz
2x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_2X}$	LSWx_DRV_FREQ[2:0] = 0b110, V_{SYS} = 3.3V, V_{SYS} = 5V		800		kHz
1x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_1X}$	LSWx_DRV_FREQ[2:0] = 0b101 (nominal gate drive strength), V_{SYS} = 3.3V, V_{SYS} = 5V	200	400	600	kHz
0.5x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.5X}$	LSWx_DRV_FREQ[2:0] = 0b100, V_{SYS} = 3.3V, V_{SYS} = 5V		200		kHz
0.25x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.25X}$	LSWx_DRV_FREQ[2:0] = 0b011, V_{SYS} = 3.3V, V_{SYS} = 5V		100		kHz
0.125x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.125X}$	LSWx_DRV_FREQ[2:0] = 0b010, V_{SYS} = 3.3V, V_{SYS} = 5V	25	50	75	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.0625X}$	LSWx_DRV_FREQ[2:0] = 0b001, V_{SYS} = 3.3V, V_{SYS} = 5V		25		kHz