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MAX77756

24V Input, 500mA Buck Regulator with Dual-Input Power MUX

General Description

The MAX77756 is a synchronous 500mA step-down DC-DC converter with integrated dual-input power multiplexer (MUX). The converter operates on an input supply as low as 3.0V and as high as 24V. Default output voltage is factory-programmed to either 1.8V, 3.3V, or 5.0V. Output voltage is further adjustable through external resistors or an I²C serial interface.

The dual-input power MUX selects the higher voltage from two different input sources to power the step-down converter. Control circuitry ensures that only one channel of the MUX is on at a time to prevent cross-conduction between input sources. For single-input applications, the MUX can be bypassed and the step-down converter can be powered directly from the SUP pin.

The MAX77756 is available in a small 2.33mm x 1.42mm (0.7mm max height), 15-bump wafer-level package (WLP). For a similar buck converter without a power MUX, refer to the MAX77596.

Applications

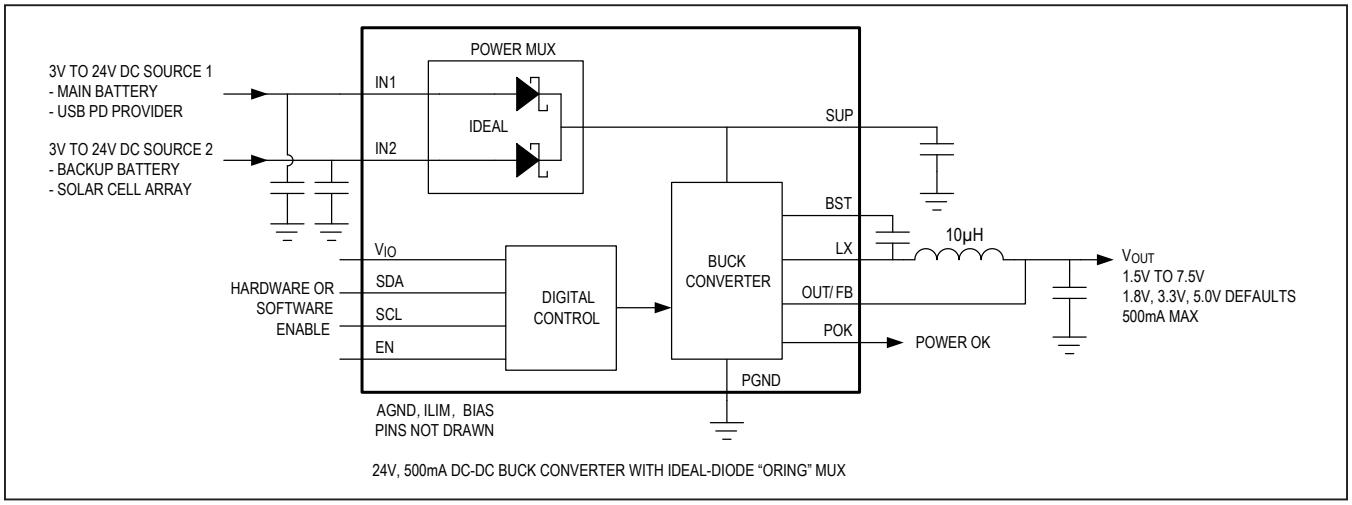
- USB Type-C Power Delivery Accessories and Devices
- Notebook and Tablet Computers
- Home Automation, Low I_Q Smart Hubs
- Battery-Powered Systems, Backup Battery, Uninterruptible Rails

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Wide Input Power Supply
  - 3V to 24V Supply Voltage
  - 500mA (max) Output Current
  - 1.8V, 3.3V, or 5.0V Factory-Set V_{OUT} with Optional I²C Control: 1.5V to 7.5V in 50mV Steps
  - External Feedback Resistor V_{OUT} Option (1V to 99% V_{SUP})
  - Hardware or Software Enable
- Dual-Input Power MUX Replaces Common-Cathode Diode Arrays
  - Automatic Ideal-Diode ORing Voltage Selector
  - 250mΩ MOSFETs Minimize Power Consumption, BOM, and Solution Size
- Low I_Q Enables Always-On Rails
  - 1.5µA Quiescent Current (Only SUP Powered)
  - 19µA Quiescent Current (IN1/IN2 Powered)
  - 88% Peak Efficiency ($12V_{SUP}$, $3.3V_{OUT}$)
- Safe and Easy to Use
  - Short-Circuit Hiccup Mode and Thermal Protection
  - 8ms Soft-Start
  - Software-Enabled Spread Spectrum
  - Pin-Programmable Inductor Peak Current Level
- Small Size
  - 2.33mm x 1.42mm (0.7mm max height) Wafer-Level Package (WLP)
  - 15-Bump, 0.4mm Pitch, 3 x 5 Array

Simplified Block Diagram



24V, 500mA DC-DC BUCK CONVERTER WITH IDEAL-DIODE "ORING" MUX

Absolute Maximum Ratings

IN1, IN2, SUP to PGND .....-0.3V to +26V
BIAS to PGND.....-0.3V to +6V
EN to PGND.....-0.3V to V_{SUP} + 0.3V
BST to LX.....+6V
BST to PGND.....-0.3V to +31V
OUT/FB to PGND.....-0.3V to +12V
POK, ILIM to PGND .....-0.3V to V_{BIAS} + 0.3V
POK, SDA Sink Current 20mA
V_{IO} to PGND .....-0.3V to +6V
SDA, SCL to PGND.....-0.3V to V_{IO} + 0.3V
AGND to PGND.....-0.3V to +0.3V

IN1, IN2 Repetitive Forward Current (T_A = +85°C)
10% Duty Square Wave 4.1A
IN1, IN2 SUP Continuous Current .....1.6A_{RMS}
LX Continuous Current (Note 1).....1.6A_{RMS}
OUT/FB Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
(derate 16.22mW/°C above +70°C) 1298mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Soldering Temperature (reflow).....+260°C

Note 1: LX has internal clamp diodes to PGND and SUP. Applications that forward bias these diodes should not exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

15 WLP

Package Code	W151G2+1
Outline Number	**21-100111**
Land Pattern Number	**90-100052** (Refer to **Application Note 1891)**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	61.65°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{EN} = 12V, V_{IO} = 1.8V, V_{IN1} = V_{IN2} = 0V, configuration registers in reset. Limits are 100% production tested at T_A = +25°C, limits over T_A = -40°C to +85°C are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN CONVERTER							
SUP Voltage Range	V_{SUP}			3		24	V
SUP Undervoltage Lockout	V_{UVLO}	V_{SUP} rising		2.75	2.9	3.0	V
SUP Undervoltage Lockout Hysteresis					300		mV
SUP Shutdown Current	$I_{SUP-SHDN}$	V_{EN} = 0V (buck converter disabled)			0.75	3.0	µA
SUP QUIESCENT CURRENT							
SUP Quiescent Current	I_{SUP-Q}	I_{LOAD} = 0mA, V_{OUT} = 1.8V			6	18	µA
		I_{LOAD} = 0mA, V_{OUT} = 3.3V			1.5	3.0	
		I_{LOAD} = 0mA, V_{OUT} = 5.0V			2.65	5.0	
		I_{LOAD} = 0mA, external feedback version			32	70	
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = 5.5V to 24V, BIAS not internally connected to OUT (Note 1)			5		V
Output Voltage Regulation Range	$V_{OUT-REG}$	Internal feedback version target regulation voltage, adjustable through I²C from 1.5V to 7.5V in 50mV/LSB with V_OUTREG[7:0]		1.5		7.5	V
OUTPUT VOLTAGE ACCURACY							
OUT Voltage Accuracy	V_{OUT}	$V_{OUT-REG}$ = 1.8V, 1.8V factory-default version	V_{SUP} = 12V, I_{OUT} = 250mA, T_A = +25°C	1.78	1.8	1.82	V
			V_{SUP} = 4.5V to 24V, I_{OUT} = 0mA to 500mA, T_A = -40°C to +85°C	1.746	1.8	1.854	
		$V_{OUT-REG}$ = 3.3V, 3.3V factory-default version	V_{SUP} = 12V, I_{OUT} = 250mA, T_A = +25°C	3.27	3.3	3.33	
			V_{SUP} = 4.5V to 24V, I_{OUT} = 0mA to 500mA, T_A = -40°C to +85°C	3.2	3.3	3.4	
		$V_{OUT-REG}$ = 5.0V, 5.0V factory-default version	V_{SUP} = 12V, I_{OUT} = 250mA, T_A = +25°C	4.95	5	5.05	
			V_{SUP} = 6V to 24V, I_{OUT} = 0mA to 500mA, T_A = -40°C to +85°C	4.85	5	5.15	

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, V_{IO} = 1.8V, V_{IN1} = V_{IN2} = 0V, configuration registers in reset. Limits are 100% production tested at T_A = +25°C, limits over T_A = -40°C to +85°C are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB VOLTAGE ACCURACY							
FB Voltage Accuracy	V_{FB}	External feedback version	V_{SUP} = 12V, I_{LOAD} = 250mA, T_A = +25°C	0.99	1	1.01	V
			V_{SUP} = 3.0V to 24V, I_{LOAD} = 0mA to 500mA, T_A = -40°C to +85°C	0.97	1	1.03	
FB Input Current	I_{FB}	V_{FB} = 1V, external feedback version			0.02		µA
OUT/FB Wake-Up Threshold	V_{WAKE}	Standby mode exit threshold, I_{LOAD} = 0mA, expressed as a percentage of $V_{OUT-REG}$			99		%
OUT/FB Load Regulation		0 to 300mA load, FPWM mode (Note 2)			1		%
OUT/FB Line Regulation		V_{SUP} = 4.5V to 24V, V_{OUT} = 3.3V, FPWM mode (Note 2)			0.02		%/V_{SUP}
OUT/FB Soft-Start Ramp Time	t_{SS}	SOFT_ST = 1			4		ms
		SOFT_ST = 0			8		
High-Side MOSFET On-Resistance	R_{ON-HS}	V_{BIAS} = 5V, I_{LX} = 90mA			500	800	mΩ
Low-Side MOSFET On-Resistance	R_{ON-LS}	V_{BIAS} = 5V, I_{LX} = 90mA			500	800	mΩ
High-Side MOSFET Peak Current Limit	$I_{LX-PEAK}$	I_PEAK[1:0] = 0b00			700		mA
		I_PEAK[1:0] = 0b01			800		
		I_PEAK[1:0] = 0b10		800	900	1000	
		I_PEAK[1:0] = 0b11			1000		
Low-Side MOSFET Valley Current Threshold	$I_{LX-VALLEY}$	Output overloaded (V_{OUT} < 25% of $V_{OUT-REG}$), threshold below where on-times are allowed to start			500		mA
High-Side MOSFET Minimum Current Threshold	$I_{LX-PK-MIN}$	Inductor current ramps to at least $I_{LX-PK-MIN}$ while skipping			200		mA
Low-Side MOSFET Zero-Crossing Threshold	I_{ZX}				40		mA
Minimum On-Time (Note 3)	t_{ON-MIN}	V_{OUT} = 3.3V			80		ns
Maximum Duty Cycle	D_{MAX}				99		%
Switching Frequency	f_{SW}	Continuous conduction		0.94	1	1.06	MHz
Spread-Spectrum Frequency Range	Δf_{SW}	Spread-spectrum enabled			±6		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, V_{IO} = 1.8V, V_{IN1} = V_{IN2} = 0V, configuration registers in reset. Limits are 100% production tested at T_A = +25°C, limits over T_A = -40°C to +85°C are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Short Output Voltage Monitor Threshold	$V_{OUT-OVRLD}$			0.25 x $V_{OUT-REG}$		V
Output-Overloaded Retry Timer	t_{RETRY}	Switching stopped because V_{OUT} < 25% of $V_{OUT-REG}$ and 15 consecutive switching cycles ended by current limit, time before converter attempts to soft-start again		15		ms
POWER MULTIPLEXER						
IN1/IN2 Minimum Initial Operating Voltage	V_{IN1}/V_{IN2}	Minimum initial voltage to forward-bias power MUX FET intrinsic body-diode to activate selection logic		V_{UVLO} + 0.7		V
IN1/IN2 QUIESCENT CURRENT						
IN1/IN2 Quiescent Current	I_{IN1-Q}/I_{IN2-Q}	V_{OUT} = 1.8V, V_{IN1} or V_{IN2} = 12V, I_{LOAD} = 0mA		38	100	µA
		V_{OUT} = 3.3V, V_{IN1} or V_{IN2} = 12V, I_{LOAD} = 0mA		18.5	30	
		V_{OUT} = 5.0V, V_{IN1} or V_{IN2} = 12V, I_{LOAD} = 0mA		25	40	
		V_{IN1} or V_{IN2} = 12V, I_{LOAD} = 0mA, external feedback version		42	100	
IN1/IN2 to SUP On-Resistance	R_{ON-IN1}	V_{IN1} = 5.5V, I_{IN1} = 90mA		250	400	mΩ
	R_{ON-IN2}	V_{IN2} = 5.5V, I_{IN2} = 90mA		250	400	
IN1/IN2 Leakage	$I_{IN1-LEAK}$	V_{SUP} = 12V, V_{IN1} = V_{IN2} = 0V, IN1/IN2 to SUP channel is off; Current from IN1		0.003	1	µA
	$I_{IN2-LEAK}$	Current from IN2		0.003	1	
Channel Selection Hysteresis		(Note 4)		400		mV
POWER-OK OUTPUT (POK)						
POK Threshold	$V_{POK-RISING}$	V_{OUT} rising, expressed as a percentage of $V_{OUT-REG}$	90	92	94	%
	$V_{POK-FALLING}$	V_{OUT} falling, expressed as a percentage of $V_{OUT-REG}$	88	90	92	
POK Debounce Timer	t_{POK-DB}			12		µs
POK Leakage Current	I_{POK}	POK = high (high impedance), T_A = +25°C			1	µA
POK Low Voltage	V_{POK}	POK = low, sinking 1mA			0.4	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, V_{IO} = 1.8V, V_{IN1} = V_{IN2} = 0V, configuration registers in reset. Limits are 100% production tested at T_A = +25°C, limits over T_A = -40°C to +85°C are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUT (EN)						
EN Logic-High Threshold	V_{EN_HI}		1.4			V
EN Logic-Low Threshold	V_{EN_LO}				0.4	V
EN Leakage Current	I_{EN}	V_{EN} = V_{SUP} = 12V		0.1		µA
HIGH-SIDE CURRENT LIMIT INPUT (ILIM)						
ILIM Logic-High Threshold	V_{ILIM_HI}		1.4			V
ILIM Logic-Low Threshold	V_{ILIM_LO}				0.4	V
SERIAL INTERFACE/I/O STAGE						
V_{IO} Voltage Range	V_{IO}		1.7		5.5	V
V_{IO} Valid Logic Threshold			1.7			V
V_{IO} Bias Current		T_A = +25°C	-1	0	+1	µA
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 5.5V, V_{SCL} = V_{SDA} = 0V or 5.5V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance		(Note 5)		10		pF
Input Filter Suppressed Spike Maximum Pulse Width	t_{SP}	(Note 5)		50		ns
SERIAL INTERFACE/TIMING						
Clock Frequency	f_{SCL}				1	MHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		260			ns

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, V_{IO} = 1.8V, V_{IN1} = V_{IN2} = 0V, configuration registers in reset. Limits are 100% production tested at T_A = +25°C, limits over T_A = -40°C to +85°C are guaranteed by design and characterization, unless otherwise noted.)

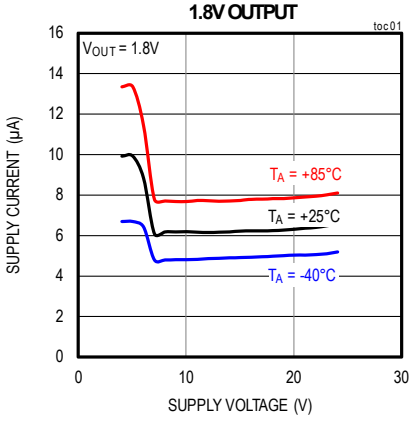
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period	t_{LOW}		500			ns
SCL High Period	t_{HIGH}		260			ns
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
SDA Fall Time	t_F	Time measured between V_{IO} and V_{OL} (Note 5)			120	ns
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	Junction temperature rising		+165		°C
Thermal Shutdown Hysteresis				+15		°C

Note 1: See the *BIAS Regulator* section.
Note 2: Forced PWM (FPWM) is an internal test mode.
Note 3: Output voltage regulation is always maintained. The device skips pulses when the duty cycle needed to regulate the output violates the minimum on-time.
Note 4: Off channel must be half of this value higher than the on channel for switch to happen.
Note 5: Design guidance only. Not production tested.

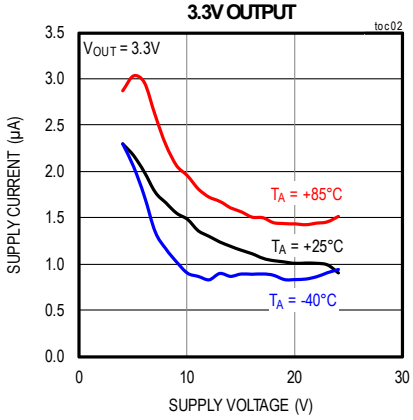
Typical Operating Characteristics

(V_{INx} = V_{EN} = 12V, T_A = +25°C, internal feedback version, unless otherwise noted.)

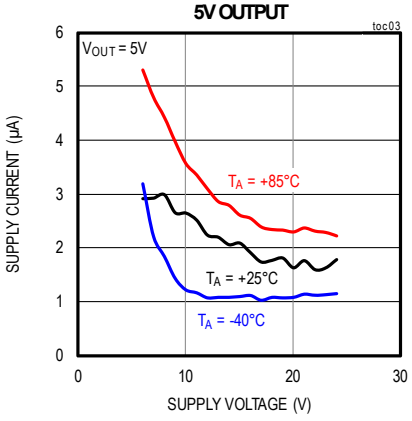
SUP QUIESCENT CURRENT vs. VOLTAGE 1.8V OUTPUT



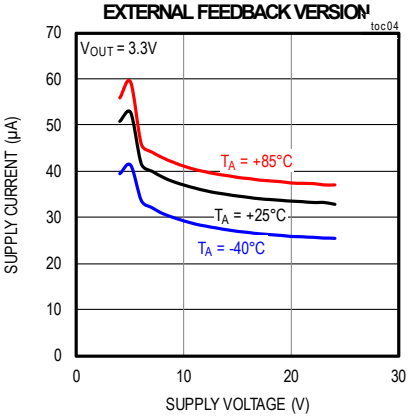
SUP QUIESCENT CURRENT vs.VOLTAGE 3.3V OUTPUT



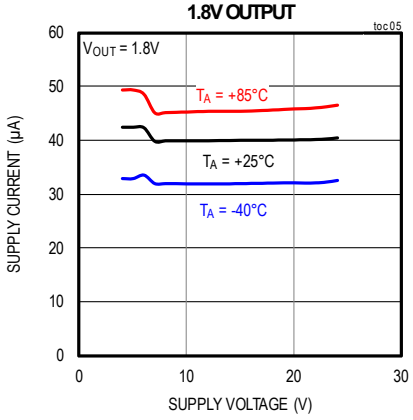
SUP QUIESCENT CURRENT vs. VOLTAGE 5V OUTPUT



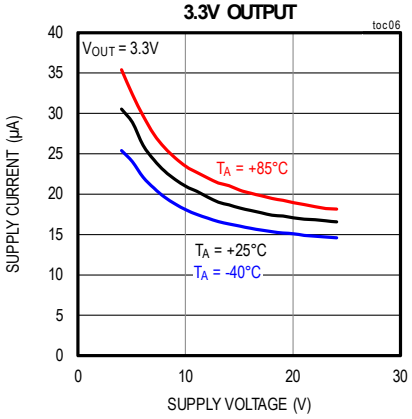
SUP QUIESCENT CURRENT vs.VOLTAGE EXTERNAL FEEDBACK VERSION



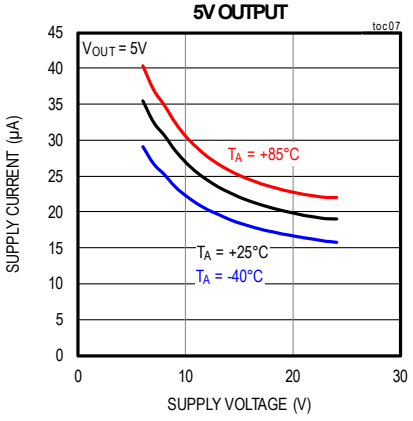
INx QUIESCENT CURRENT vs. VOLTAGE 1.8V OUTPUT



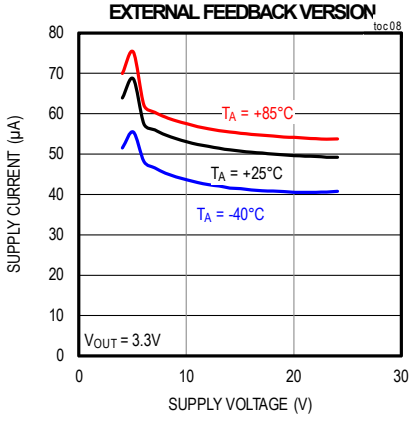
INx QUIESCENT CURRENT vs. VOLTAGE 3.3V OUTPUT



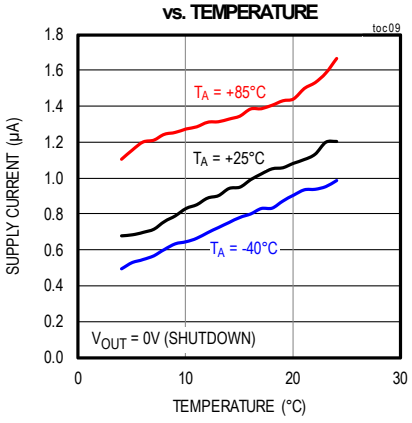
INx QUIESCENT CURRENT vs. VOLTAGE 5V OUTPUT



INx QUIESCENT CURRENT vs. VOLTAGE EXTERNAL FEEDBACK VERSION

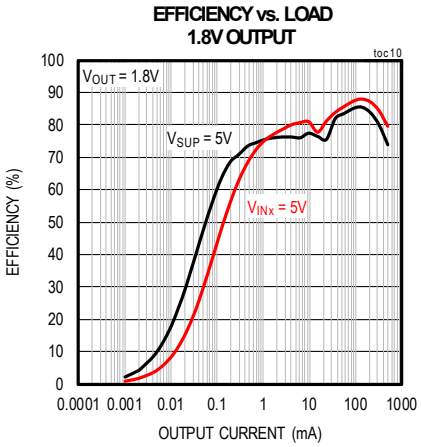


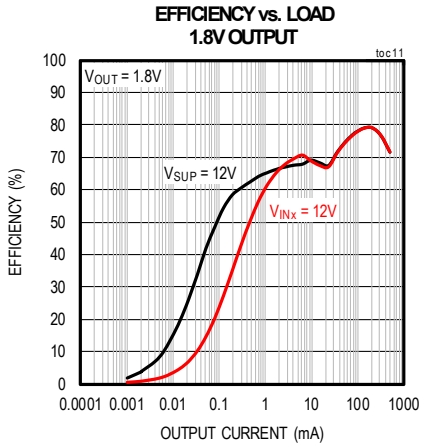
SHUTDOWN CURRENT vs. TEMPERATURE

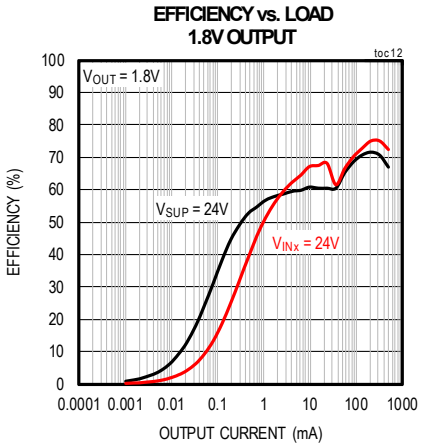


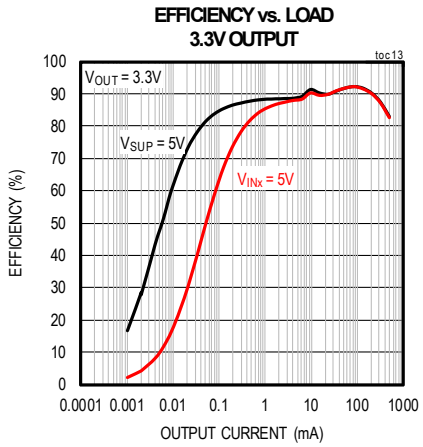
Typical Operating Characteristics (continued)

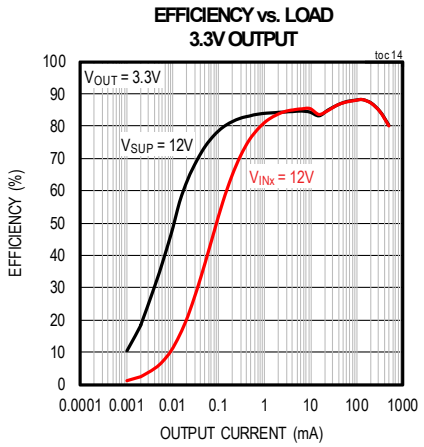
(V_{INx} = V_{EN} = 12V, T_A = +25°C, internal feedback version, unless otherwise noted.)

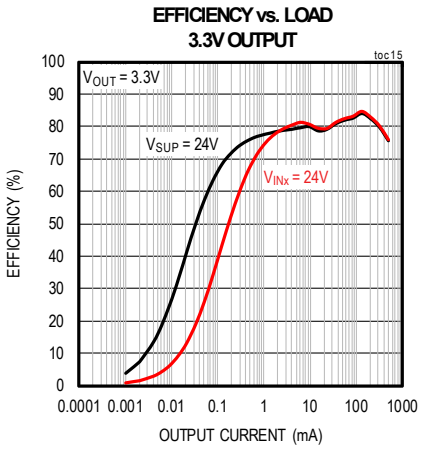


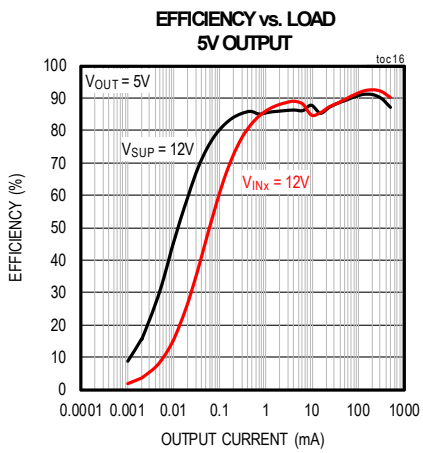


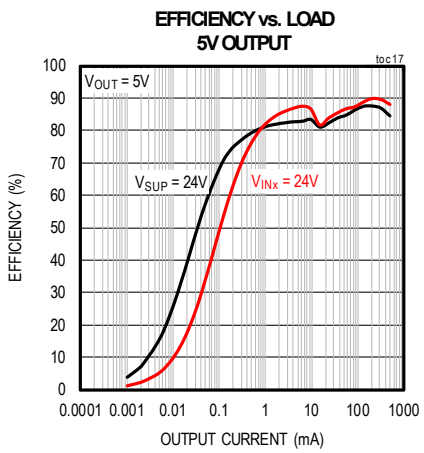


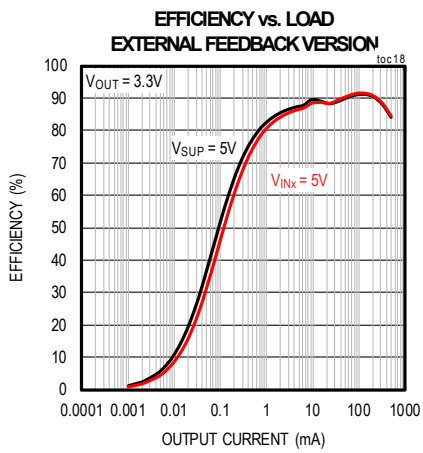








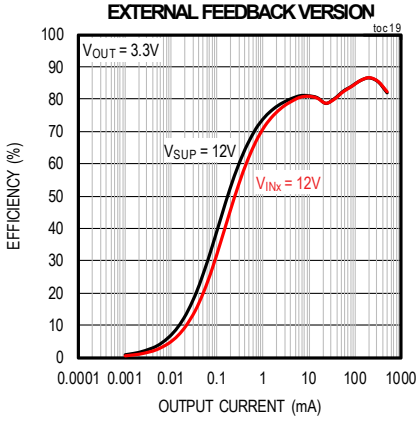




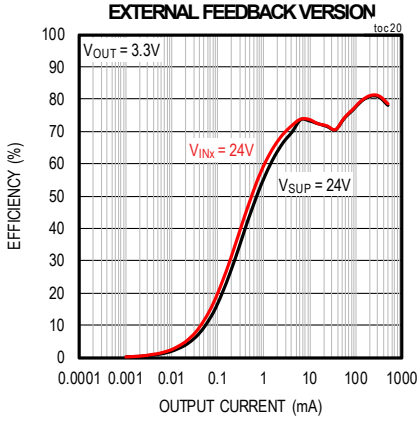
Typical Operating Characteristics (continued)

(V_{INx} = V_{EN} = 12V, T_A = +25°C, internal feedback version, unless otherwise noted.)

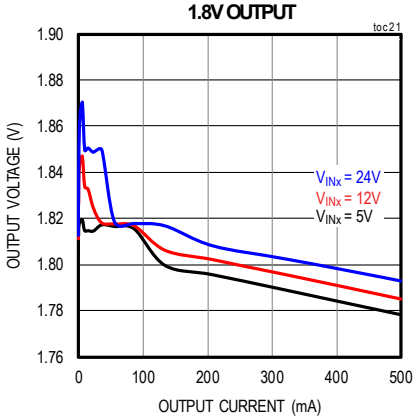
EFFICIENCY vs. LOAD
EXTERNAL FEEDBACK VERSION



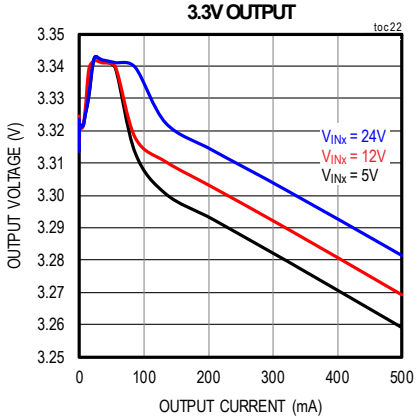
EFFICIENCY vs. LOAD
EXTERNAL FEEDBACK VERSION



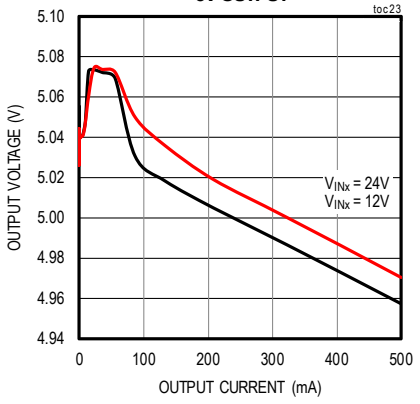
LOAD REGULATION
1.8V OUTPUT



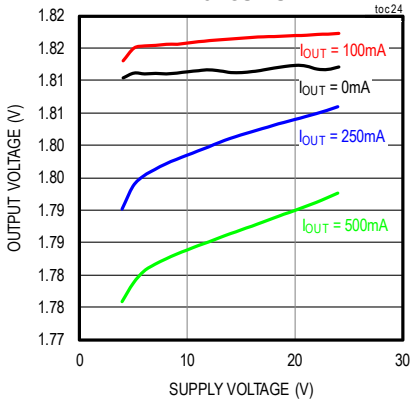
LOAD REGULATION
3.3V OUTPUT



LOAD REGULATION
5V OUTPUT



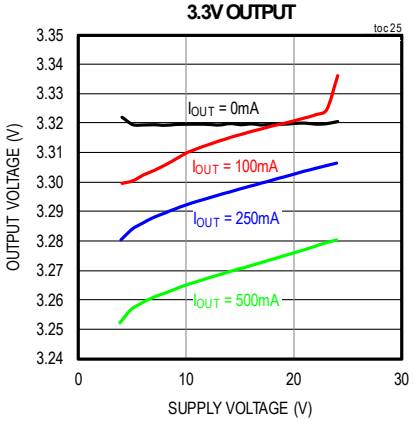
LINE REGULATION
1.8V OUTPUT



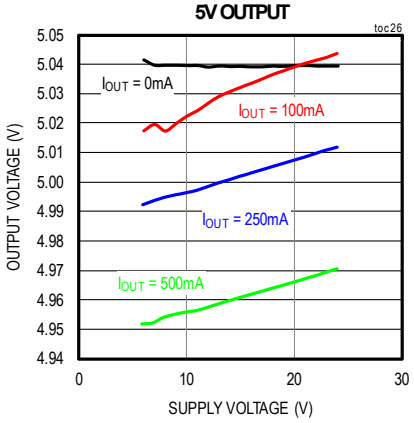
Typical Operating Characteristics (continued)

(V_{INx} = V_{EN} = 12V, T_A = +25°C, internal feedback version, unless otherwise noted.)

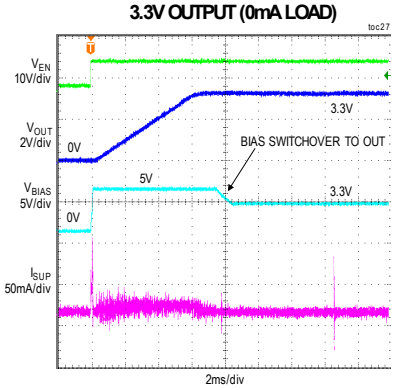
LINE REGULATION
3.3V OUTPUT



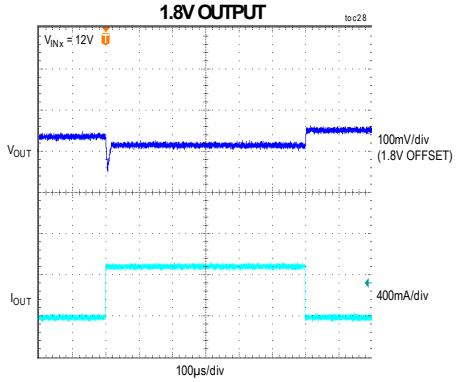
LINE REGULATION
5V OUTPUT



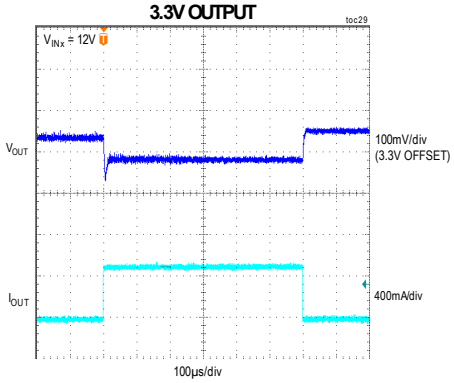
STARTUP WAVEFORM
3.3V OUTPUT (0mA LOAD)



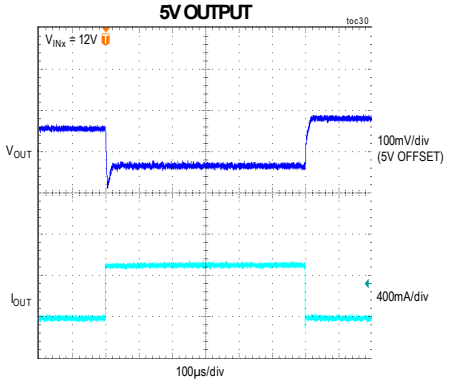
LOAD TRANSIENT RESPONSE
1.8V OUTPUT



LOAD TRANSIENT RESPONSE
3.3V OUTPUT



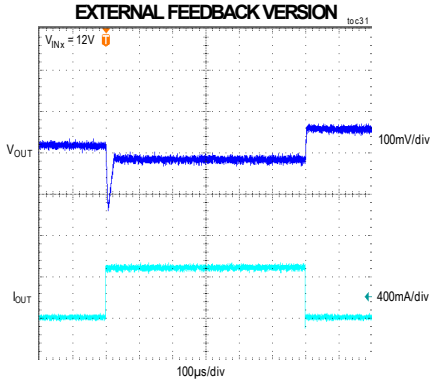
LOAD TRANSIENT RESPONSE
5V OUTPUT



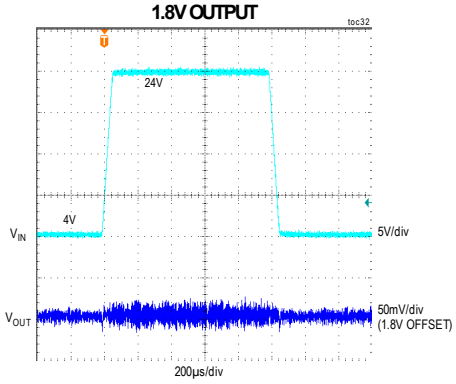
Typical Operating Characteristics (continued)

(V_{INx} = V_{EN} = 12V, T_A = +25°C, internal feedback version, unless otherwise noted.)

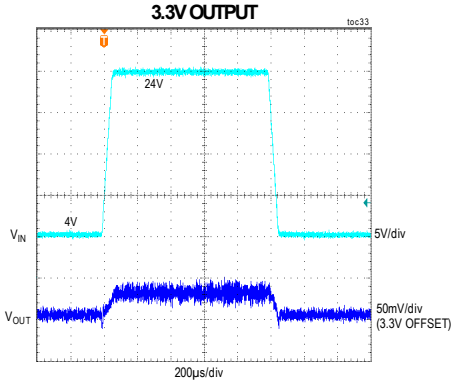
LOAD TRANSIENT RESPONSE
EXTERNAL FEEDBACK VERSION



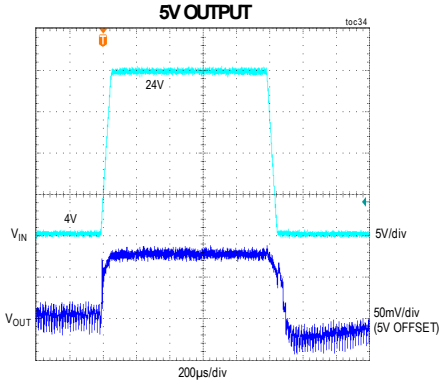
LINE TRANSIENT RESPONSE
1.8V OUTPUT



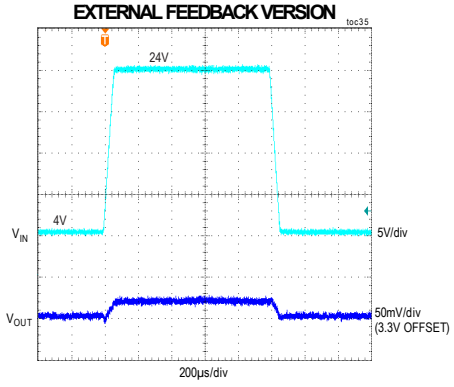
LINE TRANSIENT RESPONSE
3.3V OUTPUT



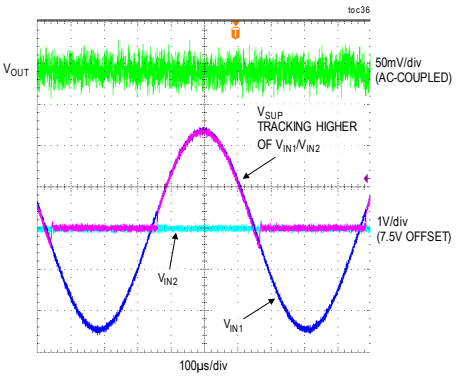
LINE TRANSIENT RESPONSE
5V OUTPUT



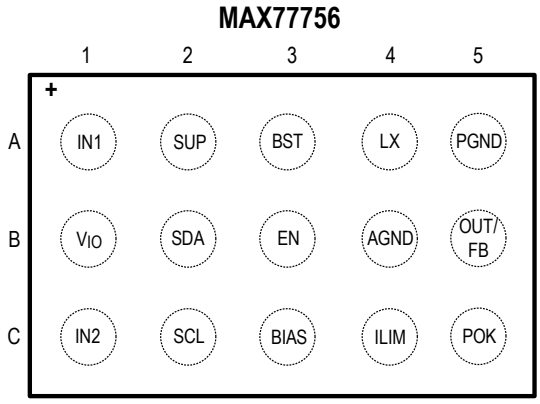
LINE TRANSIENT RESPONSE
EXTERNAL FEEDBACK VERSION



IN1/IN2 SWITCHOVER



Bump Configuration



15 WLP

TOP VIEW (BUMP SIDE DOWN)

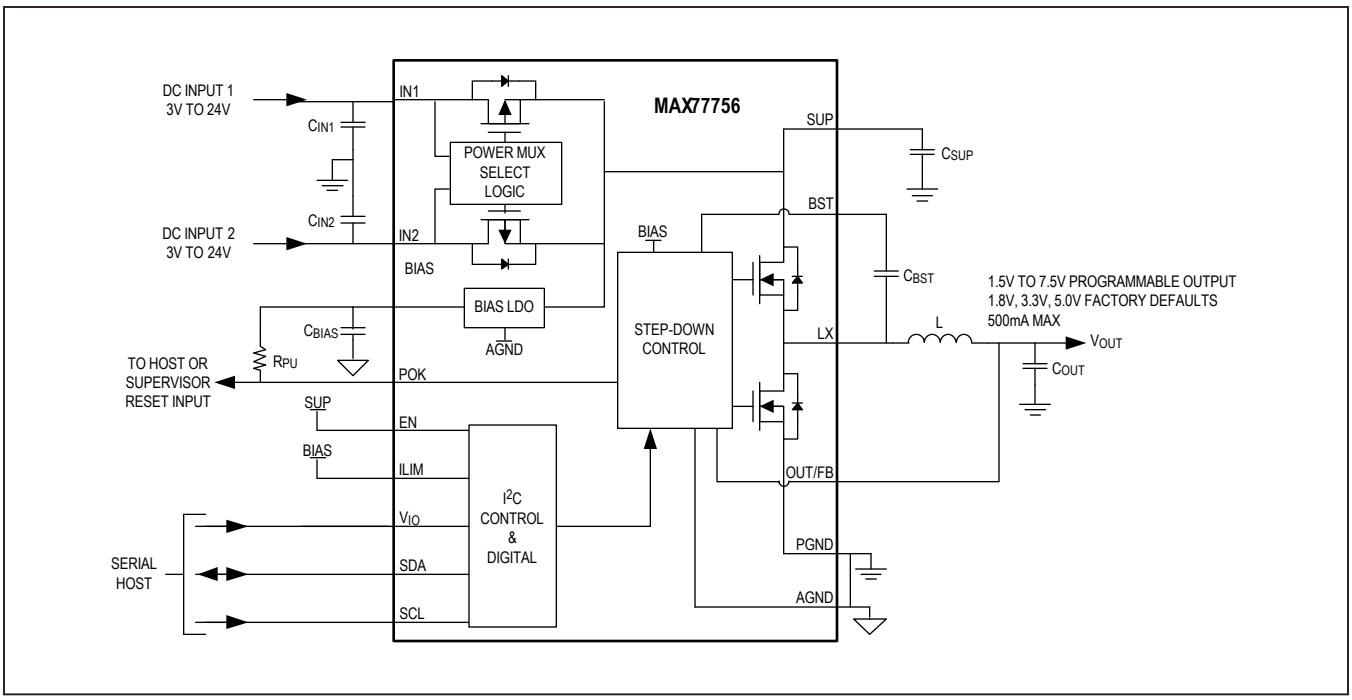
Bump Description

BUMP	NAME	FUNCTION
A1	IN1	Power MUX Input 1. IN1 and IN2 have equal priority to the power selector. Selection logic is only active when the IC is enabled through the EN pin or EN_BIT. A diode always exists between IN1 and SUP. Connect to PGND to force PFET between IN1 and SUP off.
C1	IN2	Power MUX Input 2. IN1 and IN2 have equal priority to the power selector. Selection logic is only active when the IC is enabled through the EN pin or EN_BIT. A diode always exists between IN2 and SUP. Connect to PGND to force PFET between IN2 and SUP off.
A3	BST	High-Side FET Driver Supply. Connect a 0.1µF ceramic capacitor between BST and LX.
A2	SUP	Power MUX Output and Buck Supply Input. Bypass with a 1µF ceramic capacitor to PGND as close as possible to the IC. If using IN1/IN2 to power the IC, do not prebias the SUP capacitor or connect SUP to external loads. If using SUP to power the IC, connect IN1 and IN2 to PGND.
A4	LX	Switching Node. LX is high impedance when the converter is disabled.
A5	PGND	Power Ground. Connect to AGND on the PCB. Return the SUP and OUT bypass capacitors to PGND.
B4	AGND	Quiet Ground. Connect to PGND on the PCB. Return the BIAS bypass capacitor to AGND.
C5	POK	Open-Drain Power OK Output. An external pullup resistor is required.
C3	BIAS	Low-Voltage Internal IC Supply. Bypass to AGND with a 1µF ceramic capacitor. Do not load this pin externally.
B5	OUT/FB	**Internal Feedback Versions (MAX77756A/B/C)**: Output Voltage Sense Input. Connect a 10µH inductor between OUT and LX. Bypass OUT to PGND with a minimum 22µF ceramic capacitor. **External Feedback Version (MAX77756D)**: Feedback Input. Connect a resistor voltage divider between the converter's output and AGND to set the output voltage. Connect a 5.6pF feed-forward capacitor between the converter's output and FB. Do not route FB close to sources of EMI or noise.

Bump Description (continued)

BUMP	NAME	FUNCTION
B3	EN	Enable Input. Enables both the step-down converter and the power MUX. EN is compatible with the SUP voltage domain. Drive EN to PGND to disable the device. Drive EN above V_{EN_HI} to enable the device. If using I^2C to control the buck, the enable bit (EN_BIT) interacts with the EN pin. See the *Enable Control* section.
B1	V_{IO}	I^2C Serial Interface Voltage Supply. Connect to PGND if not used.
C2	SCL	I^2C Serial Interface Clock. This pin requires a pullup resistor to V_{IO}. Connect to PGND if not used.
B2	SDA	I^2C Serial Interface Data. This pin requires a pullup resistor to V_{IO}. Connect to PGND if not used.
C4	ILIM	LX Peak Current Limit Setting Input. Connect to PGND to set $I_{LX-PEAK}$ to 700mA. Connect to BIAS to set $I_{LX-PEAK}$ to 1000mA. I^2C writes to control $I_{LX-PEAK}$ are only accepted while ILIM is logic-low. See the *Peak Inductor Current Limit (ILIM)* section for details.

Functional Diagram



Detailed Description

The MAX77756 is a small 500mA step-down DC-DC converter with integrated dual-input power multiplexer (MUX). The step-down (buck) converter uses synchronous rectification and internal current-mode compensation. The buck operates on a supply voltage from 3V to 24V. Output voltage is configurable through I2C (1.5V to 7.5V in 50mV steps) or external feedback resistors (1V to 99% of V_{SUP}). Factory-default voltage options of 1.8V, 3.3V, and 5.0V are available (see the *Ordering Information* table). Switching frequency in continuous conduction is 1MHz. The buck utilizes an ultra-low quiescent current mode (1.5µA typ for 3.3V_{OUT}) that maintains a very high efficiency at light loads.

The integrated dual-input power MUX automatically selects the higher of two different voltage sources to power the buck converter. The MUX reduces power dissipation versus common-cathode Schottky arrays by using switches (MOSFETs) instead of diodes. The output of the power MUX is the input to the buck (SUP). Single power source applications should bypass the power MUX and power SUP directly.

Dual-Input Power MUX

The device integrates a 24V power multiplexer (MUX) with two inputs (IN1 and IN2) and one output (SUP). SUP is the supply input for the buck. The input channels consist of P-type MOSFETs. IN1 and IN2 are the individual FET drains and SUP is the common FET source. An intrinsic body-diode is always present in both FETs.

The MUX connects the higher of V_{IN1} or V_{IN2} to SUP to power the buck. Only the higher voltage input channel is on. The lower voltage input channel is off. The MUX logic is only active while the buck converter is enabled. Both channels are off when the buck is disabled.

The selection logic has switchover hysteresis to avoid chattering. The off channel must be 200mV higher than the on channel to cause a switchover. Switchover is automatic and can happen any time while the buck is enabled. Equal priority is given to each input. Neither channel is prioritized over the other.

When powering IN1 or IN2, do not connect anything to SUP besides a decoupling capacitor. To use the buck without the power MUX, connect IN1 and IN2 to PGND and power SUP directly.

Buck Regulator Control Scheme

The step-down converter uses a PWM peak current-mode control scheme with a load-line architecture. Peak current-mode control provides precise control of the inductor current on a cycle-by-cycle basis and inherent compensation for input voltage variation.

On-times (MOSFET Q1 on) are started by a fixed-frequency clock and terminated by a PWM comparator. See Figure 1. When an on-time ends (starting an off-time) current conducts through the low-side MOSFET (Q2 on). Shoot-through current from SUP to PGND is avoided by introducing a brief period of dead time between switching events when neither MOSFET is on. Inductor current conducts through Q2's intrinsic body diode during dead time.

The PWM comparator regulates V_{OUT} by controlling duty cycle. The negative input of the PWM comparator is a voltage proportional to the actual output voltage error. The positive input is the sum of the current-sense signal through MOSFET Q1 and a slope-compensation ramp. The PWM comparator ends an on-time when the error voltage becomes less than the slope-compensated current-sense signal. On-times begin again due to a fixed-frequency clock pulse. The controller's compensation components and current-sense circuits are integrated. This reduces the risk of routing sensitive control signals on the PCB.

A load-line architecture is present in the controller design. The output voltage is positioned slightly above nominal regulation at no load and slightly below nominal regulation at full load. As the output load changes, a small but controlled amount of load regulation (load line) error occurs on the output voltage. This voltage positioning architecture allows the output voltage to respond to sudden load transients in a critically damped manner, and effectively reduces the amount of output capacitance needed when compared to classical integrating controllers. See the *Typical Operating Characteristics* section for information about the converter's typical voltage regulation behavior versus load.

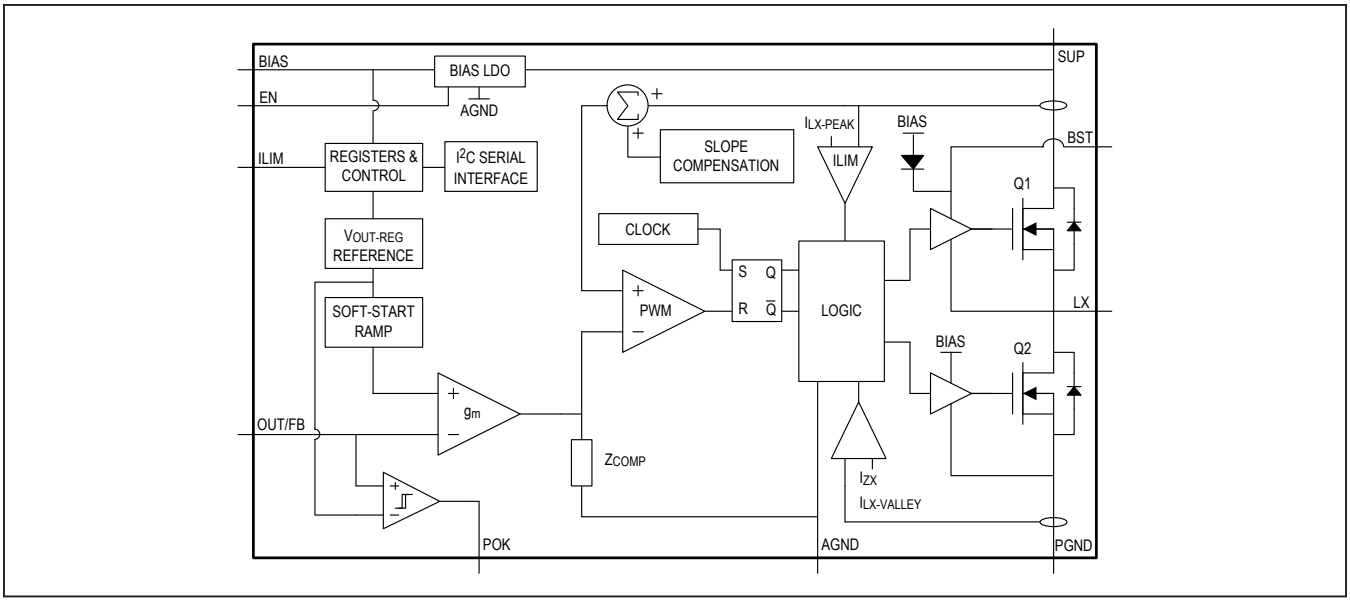


Figure 1. Buck Control Scheme Diagram

SKIP Mode Operation

The buck converter permanently operates in SKIP mode with the added ability to transition into a lower power mode called standby. SKIP mode causes discontinuous inductor current at light loads by forcing the low-side MOSFET (Q2) off if inductor current falls below I_{ZX} (40mA typ) during an off-time. This prevents inductor current from sourcing back to the input (SUP) and enables high efficiency by reducing the total number of switching cycles required to regulate the output voltage.

If the output voltage is within regulation and the load is very light then the converter automatically transitions to standby mode. In this mode, the LX node is high impedance and the converter's internal circuit blocks are deactivated to reduce I_Q consumption. A single, low-power comparator remains on to monitor the output voltage during standby. When V_{OUT} drops below V_{WAKE} (99% of $V_{OUT-REG}$ typ), the converter reactivates and starts switching again.

Enable Control

Raise the EN pin voltage above V_{EN_HI} (or tie to SUP) to enable the IC. To disable, bring EN pin voltage to PGND.

When using I^2C to control the MAX77756, the EN pin interacts with the enable bit (EN_BIT). The logical relationship between the EN pin and EN_BIT is by default an OR. The EN_CTRL bit can be used to switch this relationship to a logical AND. See Table 1.

The reset state (default state) of EN_BIT and EN_CTRL is 0. This means that the default relationship between EN pin and EN_BIT is a logical OR.

Table 1. Enable Control Truth Table

EN_CTRL (BIT)	EN (PIN)	EN_BIT (BIT)	REGULATOR OUTPUT
0 (logical OR)	0	0	OFF
	0	1	ON
	1	0	ON
	1	1	ON
1 (logical AND)	0	0	OFF
	0	1	OFF
	1	0	OFF
	1	1	ON

BIAS Regulator

An integrated 5V (V_{BIAS}) linear regulator provides power to internal circuit blocks. This regulator is used during startup for all versions of the MAX77756. For internal feedback versions (no external programming resistors) where $V_{OUT-REG}$ is programmed between (and including) 3.3V and 5.0V, the BIAS regulator is deactivated and the BIAS node is internally connected to OUT after the output voltage is within regulation. Switching BIAS to OUT utilizes the buck converter's efficiency to power its own internal circuit blocks (as opposed to a linear regulator) and improves the IC's power efficiency. For the external feedback version of the MAX77756, the BIAS regulator is permanently active. Do not load BIAS externally for any MAX77756 version.

The BIAS regulator is on whenever the EN pin is high or V_{IO} voltage is valid (regardless of whether the buck regulator is on or off). Connect a 1µF ceramic capacitor from BIAS and GND.

Soft-Start

The device has an internal soft-start timer (t_{SS}) that controls the ramp time of V_{OUT} as the converter is starting. The soft-start feature limits inrush current during startup. SOFT_ST programs t_{SS} to 8ms or 4ms. The default value is 8ms. The converter soft-starts every time the IC is enabled, exits a UVLO condition, and/or retries from an overcurrent or overtemperature condition.

Power-OK (POK) Output

The device features an open-drain POK output to monitor the output voltage. POK requires an external pullup resistor. POK goes high (high-impedance) after the regulator output increases above 92% ($V_{POK-RISING}$) of the nominal regulated voltage ($V_{OUT-REG}$). POK goes low when the regulator output drops to below 90% ($V_{POK-FALLING}$) of $V_{OUT-REG}$.

Peak Inductor Current Limit (ILIM)

The buck converter's high-side MOSFET peak current limit ($I_{LX-PEAK}$) is register or pin programmable. Applications can use $I_{LX-PEAK}$ programmability to ensure that the converter never exceeds the saturation current rating of the inductor on the PCB.

Connect ILIM to PGND to set $I_{LX-PEAK}$ to 700mA. While ILIM is logic-low, the bits in I_PEAK[1:0] can be changed through I^2C to program $I_{LX-PEAK}$ from 700mA to 1000mA in 100mA steps. The value of $I_{LX-PEAK}$ returns to 700mA (I_PEAK[1:0] = 0b00) if the configuration registers reset.

Connect ILIM to a voltage above V_{ILIM_HI} to program $I_{LX-PEAK}$ to 1000mA. While ILIM is high, $I_{LX-PEAK}$ is fixed at 1000mA and the I_PEAK[1:0] bitfield is ignored.

Short-Circiut Hiccup Mode and Thermal Protection

The device has fault protection designed to protect itself from abnormal conditions. If the output is overloaded, cycle-by-cycle current limit prevents inductor current from increasing beyond $I_{LX-PEAK}$.

The buck stops switching if V_{OUT} falls to less than 25% of programmed $V_{OUT-REG}$ and 15 consecutive on-times are ended by current limit. After switching stops, the buck waits for t_{RETRY} (15ms typ) before attempting to soft-start again (hiccup mode). While V_{OUT} is less than 25% of target, the converter prevents new on-times if the inductor current has not fallen below $I_{LX-VALLEY}$ (500mA typ). This prevents inductor current from increasing uncontrollably due to the short-circuited output.

Spread-Spectrum Option

Enable spread-spectrum operation by setting the S_SPECT bit to 1. When enabled, the switching frequency is varied ±6% centered on 1MHz. The modulation signal is a triangle wave with a period of 256µs.

Register Reset Condition

The device's internal configuration registers reset to their default values if V_{SUP} falls below the UVLO falling threshold ($V_{SUP-UVLO}$ minus UVLO hysteresis, 2.6V typ) or if the voltage on the V_{IO} pin becomes invalid (< 1.7V). Connect V_{IO} to PGND to ensure that configuration registers remain in factory-configured reset. Contact the factory to request a version of the IC that does not reset registers when V_{IO} becomes invalid.

Serial Interface

Overview

The MAX77756 features a revision 3.0 I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77756 acts as a slave-only devices where it relies on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported. I^2C is an open-drain bus, and therefore, SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals. For additional information on I^2C, refer the I^2C bus specification and users manual UM10204 that is readily available and free on the internet.

Features

- I2C Revision 3-compatible serial communications channel
- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)
- Does not utilize I2C clock stretching

I2C System Configuration

The I2C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I2C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The MAX77756 I2C-compatible interface operates as a slave on the I2C bus with transmit and receive capabilities.

I2C Interface Power

The IC's I2C interface derives its power from V_{IO}. Typically, a power input such as V_{IO} requires a local 0.1µF ceramic bypass capacitor to ground. However, in highly-integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to PGND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 5.5V. Cycling V_{IO} resets the I2C registers.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I2C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I2C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 3.

A START condition from the master signals the beginning of a transmission to the MAX77756. The master terminates transmission by issuing a not acknowledge (nA) followed by a STOP condition. See the *I2C Acknowledge Bit* section for information on not acknowledge. The STOP

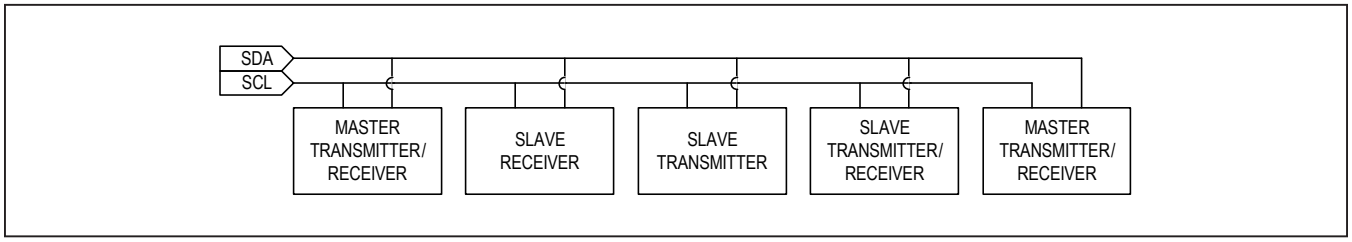


Figure 2. I2C System Configuration

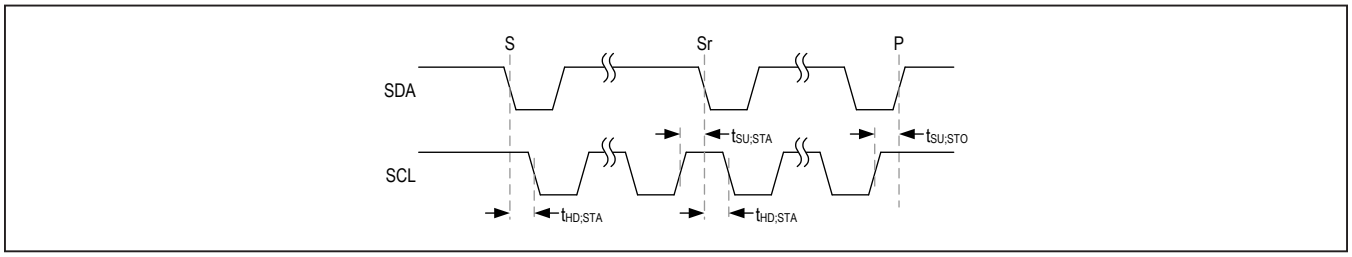


Figure 3. I2C Start and Stop Conditions

condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the IC disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

I²C Acknowledge Bit

Both the I²C bus master and the MAX77756 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 4. To generate a not acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

The MAX77756 issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

I²C Slave Address

The I²C controller implements 7-bit slave addressing in Table 2. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 5.

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

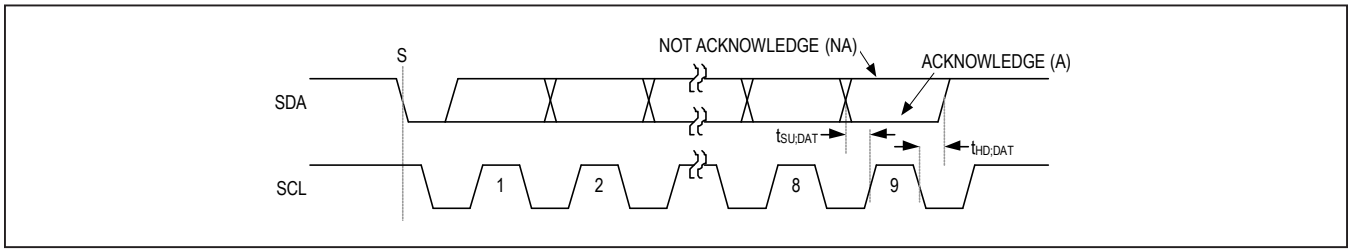


Figure 4. Acknowledge Bit

Table 2. I²C Slave Address Options

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
0x1E, 0b 001 1110	0x3C, 0b 0011 1100	0x3D, 0b 0011 1101

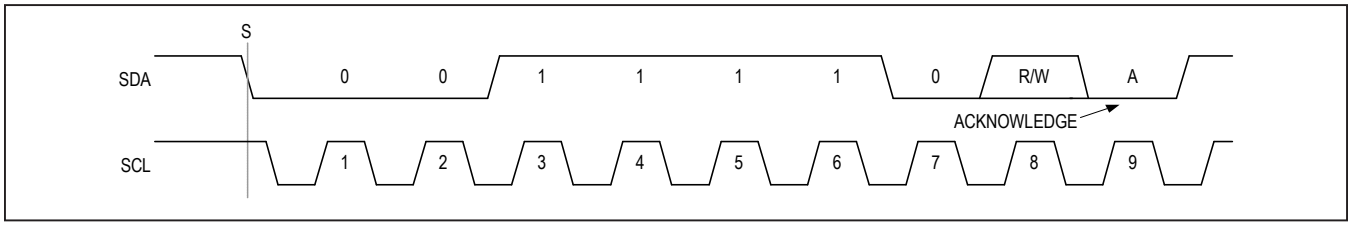


Figure 5. Slave Address Example

I²C Communication Speed

The MAX77756 is compatible with all 4 communication speed ranges as defined by the Revision 3 I²C specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C Revision 3.0 specification (UM10204) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, lower value pullup resistors dissipate more power.

Operating in high-speed mode requires some special considerations. The major considerations with respect to the IC:

- The I²C bus master use current source pullups to shorten the signal rise.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the faster bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the IC input filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I²C Communication Protocols* section.

I²C Communication Protocols

The IC supports both writing and reading from its registers.

Writing to a Single Register

Figure 6 shows the protocol for the I²C master device to write one byte of data to the MAX77756. This protocol is the same as the SMBus specification's write byte protocol. The write byte protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.

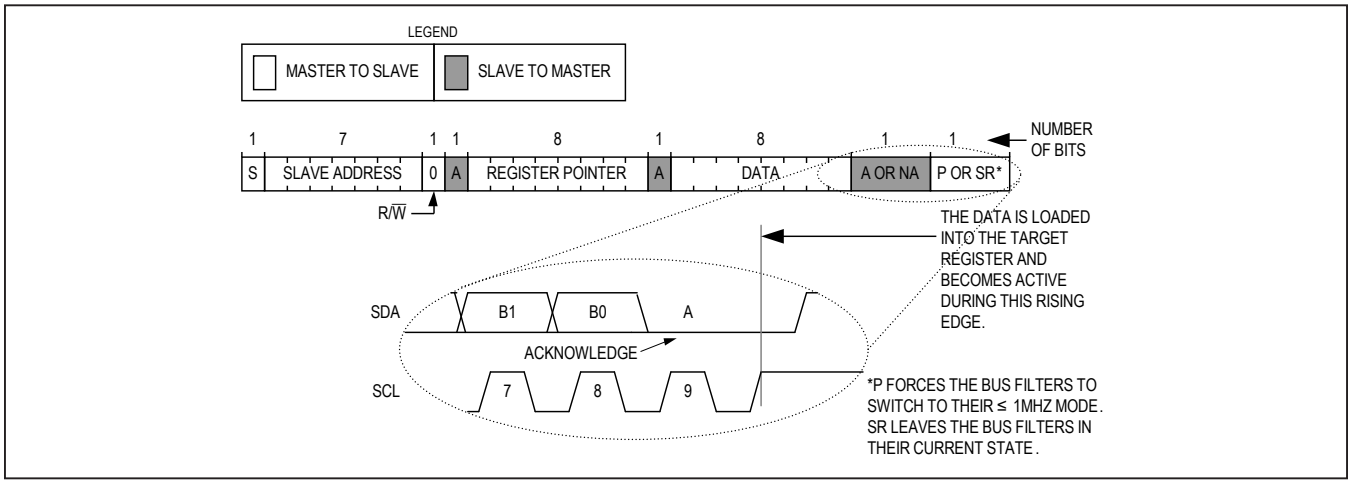


Figure 6. Writing to a Single Register with the Write Byte Protocol

8) The slave acknowledges or does not acknowledge the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Writing Multiple Bytes to Sequential Registers

Figure 7 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start.The writing to sequential registers protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
10) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

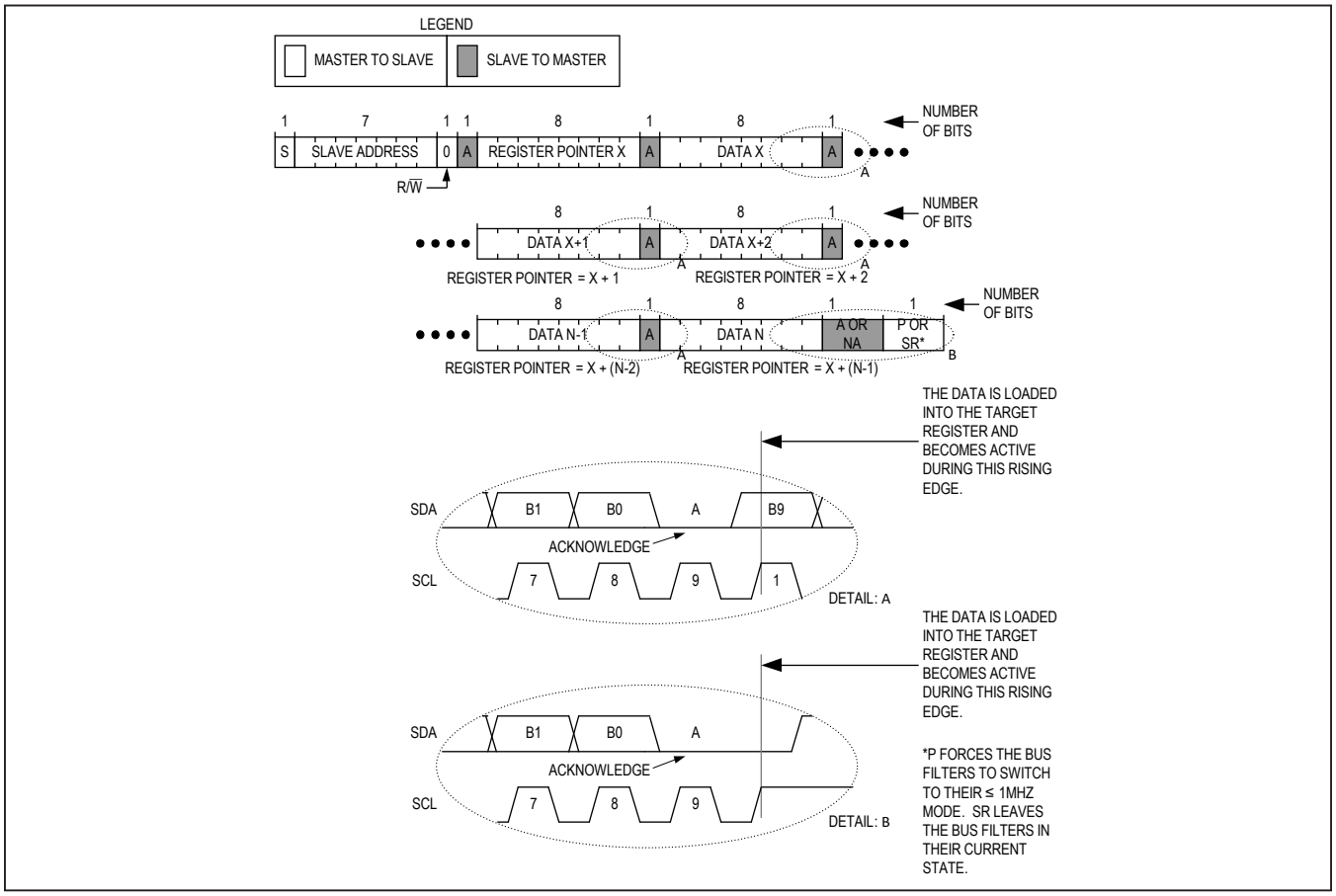


Figure 7. Writing to Sequential Registers X to N

Reading from a Single Register

Figure 8 shows the protocol for the I2C master device to read one byte of data to the MAX77756. This protocol is the same as the SMBus specification's read byte protocol. The read byte protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10) The master issues a not acknowledge (nA).
11) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the IC receives a stop, it does not modify its register pointer.

Reading from Sequential Registers

Figure 9 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.The continuous read from sequential registers protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.

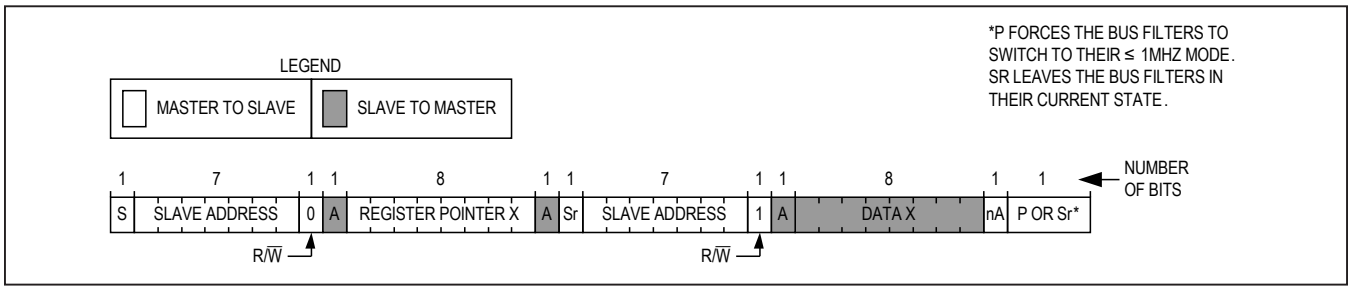


Figure 8. Reading from a Single Register with the Read Byte Protocol

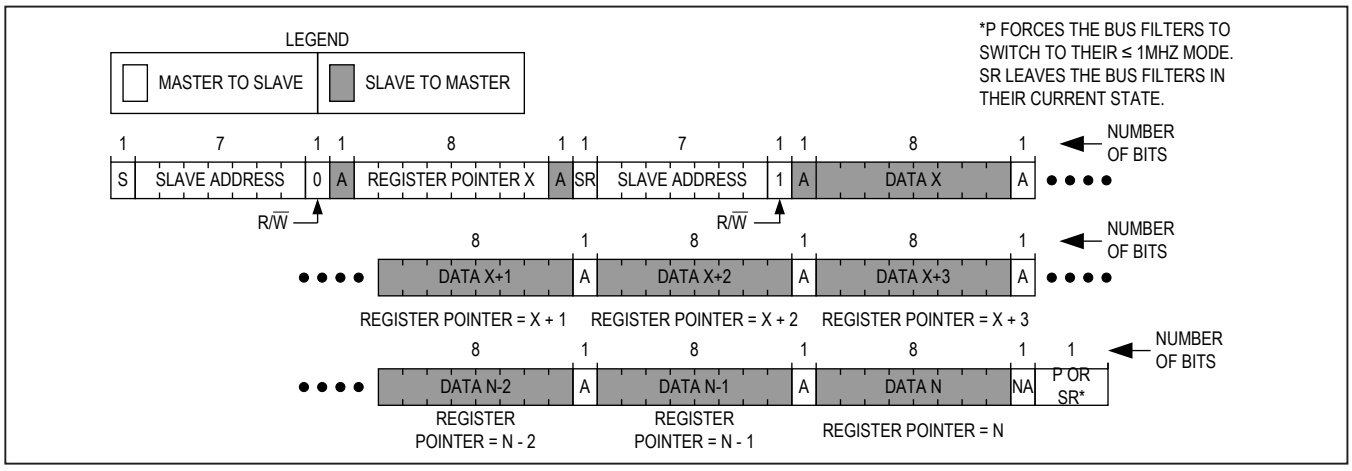


Figure 9. Reading Continuously from Sequential Registers X to N

4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/W = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10) The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the IC receives a stop it does not modify its register pointer.

Engaging High-Speed (HS) Mode for Operation Up to 3.4MHz

Figure 10 shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed up to 3.4MHz.The procedure to engage HS mode protocol is as follows:

- Begin the protocol while operating at a bus speed of 1MHz or lower.
- The master sends a start command (S).
- The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
- The addressed slave issues a not acknowledge (nA).
- The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a stop (P) is issued. Use repeated start (Sr) to continue operations in high speed mode.

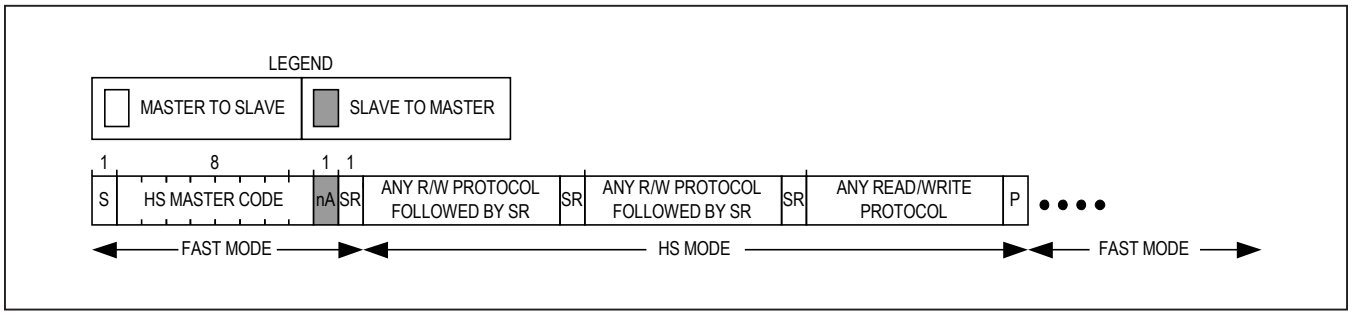


Figure 10. Engaging HS Mode

Register Map

MAX77756

ADDRESS	NAME	MSB							LSB
Configuration Registers									
0x00	CONFIG_A[7:0]	S_SPECT	SOFT_ST	I_PEAK[1:0]		RSVD	RSVD	EN_CTRL	EN_BIT
0x01	CONFIG_B[7:0]	V_OUTREG[7:0]							

CONFIG_A (0x00)

BIT	7	6	5	4	3	2	1	0
Field	S_SPECT	SOFT_ST	I_PEAK[1:0]		RSVD	RSVD	EN_CTRL	EN_BIT
Reset	0	0	00		OTP	0	0	0
Access Type	Write, Read	Write, Read	Write, Read		Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
S_SPECT	7	Spread-spectrum modulation enable control.	0 = Spread-spectrum modulation off 1 = Spread-spectrum modulation on
SOFT_ST	6	Soft-start control. Sets the regulator's startup ramp time (t_{SS}).	0 = 8ms 1 = 4ms
I_PEAK	5:4	High-side DMOS peak current limit threshold control. Sets peak LX current ($I_{LX-PEAK}$) only while the ILIM pin is low. See *Peak Inductor Current Limit (ILIM)* for details.	00 = 700mA 01 = 800mA 10 = 900mA 11 = 1000mA
RSVD	3	Factory-set control bit. Writes are ignored.	N/A
RSVD	2	Reserved control bit. Write to 0.	N/A
EN_CTRL	1	Enable logic control bit. Determines the logical relationship between the EN_BIT (enable bit) and EN (enable pin).	0 = Logical OR relationship 1 = Logical AND relationship
EN_BIT	0	Regulator enable bit.	0 = Disabled 1 = Enabled

CONFIG_B (0x01)

BIT	7	6	5	4	3	2	1	0
Field	V_OUTREG[7:0]							
Reset	0x06 / 0x24 / 0x46 (See *Ordering Information*)							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_OUTREG	7:0	Output Voltage Control. Programmable in 50mV per LSB from 0x00 (1.5V) to 0x78 (7.5V). Restrict writes to this register between 0x00 and 0x78. Do not program this register with codes outside this range. This register is a don't care for the external feedback version (MAX77756D).	0x00 = 1.5V 0x01 = 1.55V 0x02 = 1.6V . . 0x24 = 3.3V . . 0x46 = 5.0V . . 0x78 = 7.5V

Applications Information

IN1/IN2/SUP Capacitor Selection

For dual-input applications, connect separate voltage supplies to IN1 and IN2 and bypass IN1 (C_{IN1}) and IN2 (C_{IN2}) to PGND with 2.2µF ceramic capacitors. Bypass SUP to PGND with a 1µF ceramic capacitor (C_{SUP}). The C_{SUP} capacitor adds with the C_{IN1}/C_{IN2} capacitor to decouple the input of the buck. Larger values of C_{SUP} improve decoupling, but increase inrush current from IN1 or IN2 to SUP when a power source is connected. Limit IN1/IN2 inrush current to 4.1A. See the *Absolute Maximum Ratings* section for more information.

For single input applications that do not utilize IN1 and IN2, choose C_{SUP} to be a 2.2µF nominal capacitor that maintains a 1µF effective capacitance at its working voltage. Larger values improve the decoupling for the buck regulator, but increase inrush current from the voltage supply when connected. Connect IN1 and IN2 to PGND to force the power MUX selection logic off for applications that require no selector.

C_{IN1}/C_{IN2} plus C_{SUP} reduces the current peaks drawn from the input power source during buck operation and reduces switching noise in the system. The ESR/ESL of C_{SUP} and its series PCB traces should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Choose the $C_{IN1}/C_{IN2}/C_{SUP}$ capacitor voltage rating to be greater than the expected input voltage of the system. For systems using the full input voltage range (24V max) of the MAX77756, choose capacitors rated to 25V or greater.

All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Output Capacitor Selection

Choose the output bypass capacitance (C_{OUT}) to be 22µF. Larger values of C_{OUT} improve load transient performance, but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple in continuous conduction mode.